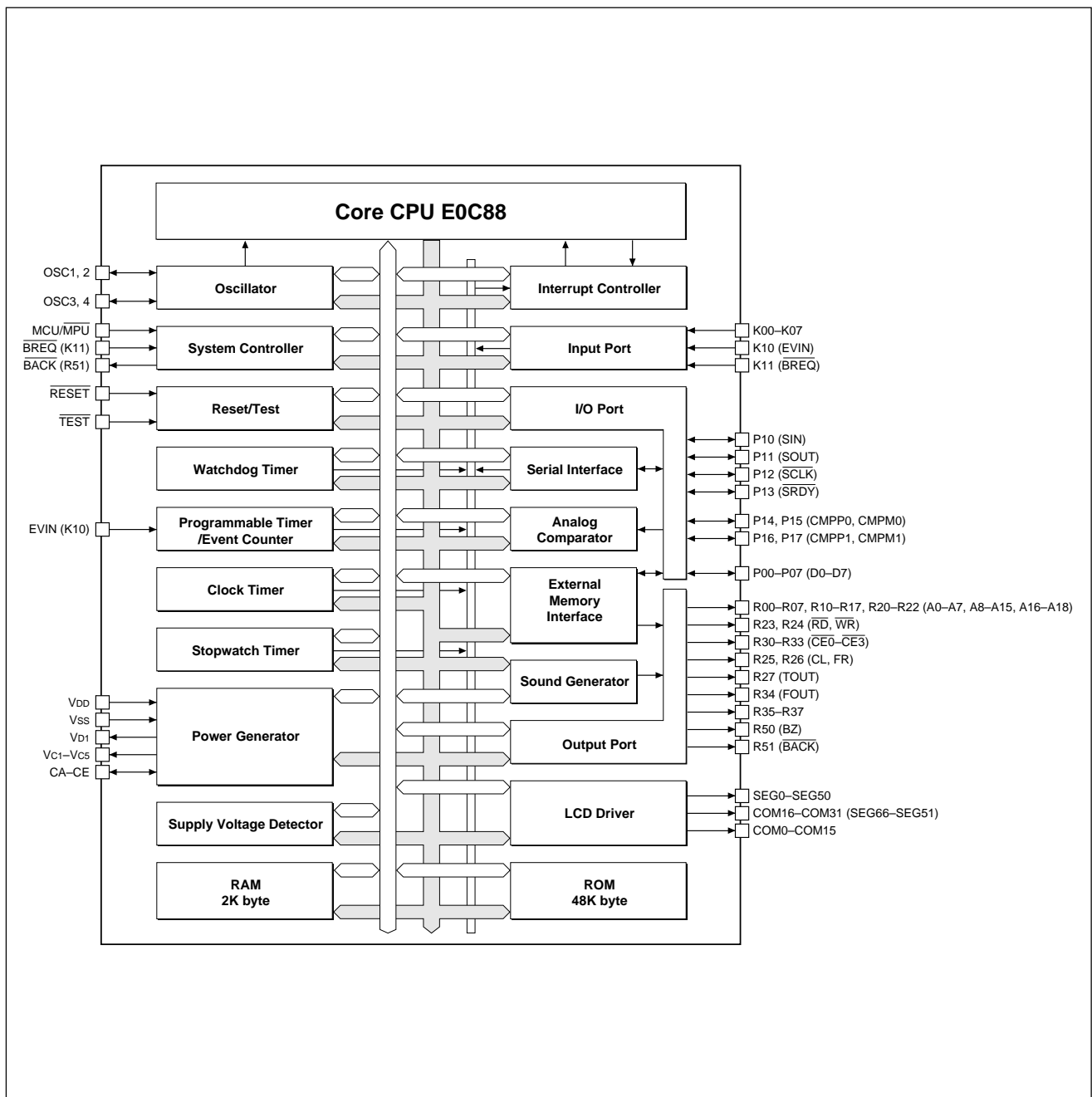




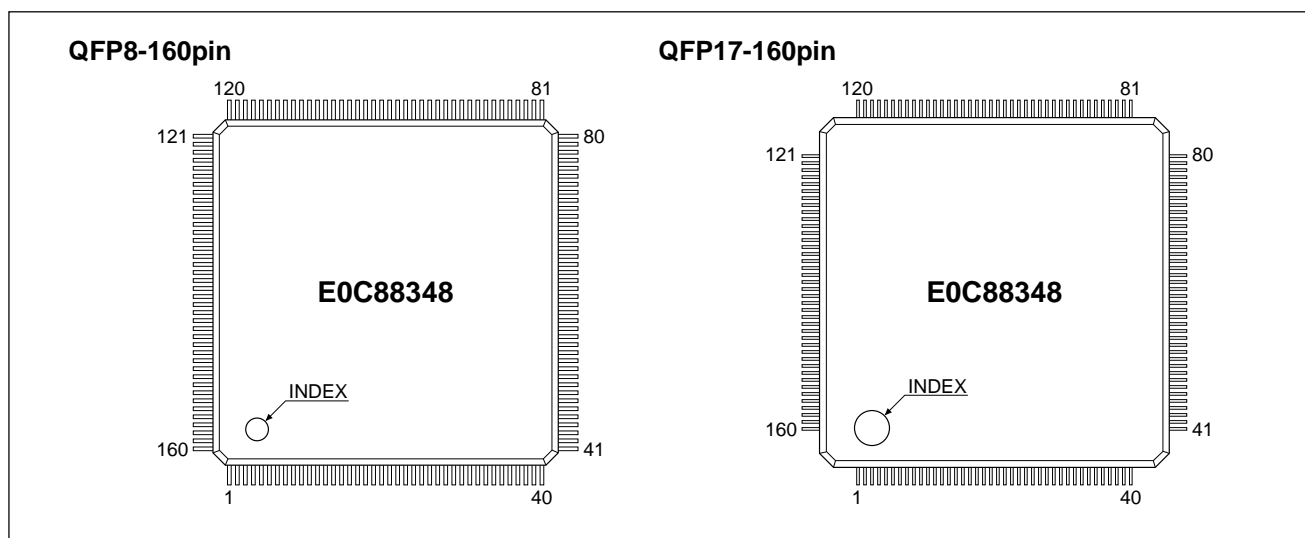
# E0C88348

- Interrupt ..... External : 2 systems (SCI, K inputs)  
Internal : 4 systems (W/D, PTM/EV, TMB, SW)
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... SLEEP mode 200nA (3V) (Low power mode)  
HALT mode 1.0μA (32.768kHz/3V) (Low power mode)  
RUN mode 8.0μA (32.768kHz/3V) (Low power mode)  
1.8mA (4.2MHz/3V) (Normal mode)
- Package ..... QFP8-160pin (plastic), QFP17-160pin (plastic)

## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG18	41	COM24/SEG58	81	OSC1	121	R11/A9
2	SEG19	42	COM23/SEG59	82	OSC2	122	R12/A10
3	SEG20	43	COM22/SEG60	83	TEST	123	R13/A11
4	SEG21	44	COM21/SEG61	84	RESET	124	R14/A12
5	SEG22	45	COM20/SEG62	85	MCU/MPU	125	R15/A13
6	SEG23	46	COM19/SEG63	86	K11/BREQ	126	R16/A14
7	SEG24	47	COM18/SEG64	87	K10/EVIN	127	R17/A15
8	SEG25	48	COM17/SEG65	88	K07	128	R20/A16
9	SEG26	49	COM16/SEG66	89	K06	129	R21/A17
10	SEG27	50	COM15	90	K05	130	R22/A18
11	SEG28	51	COM14	91	K04	131	R23/RD
12	SEG29	52	COM13	92	K03	132	R24/WR
13	SEG30	53	COM12	93	K02	133	R25/CL
14	SEG31	54	COM11	94	K01	134	R26/FR
15	SEG32	55	COM10	95	K00	135	R27/TOUT
16	SEG33	56	COM9	96	P17/CMPM1	136	R30/CE0
17	SEG34	57	COM8	97	P16/CMPP1	137	R31/CE1
18	SEG35	58	COM7	98	P15/CMPM0	138	R32/CE2
19	SEG36	59	COM6	99	P14/CMPP0	139	R33/CE3
20	SEG37	60	COM5	100	P13/SRDY	140	R34/FOUT
21	SEG38	61	COM4	101	P12/SCLK	141	R50/BZ
22	SEG39	62	COM3	102	P11/SOUT	142	R51/BACK
23	SEG40	63	COM2	103	P10/SIN	143	SEG0
24	SEG41	64	COM1	104	P07/D7	144	SEG1
25	SEG42	65	COM0	105	P06/D6	145	SEG2
26	SEG43	66	CE	106	P05/D5	146	SEG3
27	SEG44	67	CD	107	P04/D4	147	SEG4
28	SEG45	68	CC	108	P03/D3	148	SEG5
29	SEG46	69	CB	109	P02/D2	149	SEG6
30	SEG47	70	CA	110	P01/D1	150	SEG7
31	SEG48	71	Vc5	111	P00/D0	151	SEG8
32	SEG49	72	Vc4	112	R00/A0	152	SEG9
33	SEG50	73	Vc3	113	R01/A1	153	SEG10
34	COM31/SEG51	74	Vc2	114	R02/A2	154	SEG11
35	COM30/SEG52	75	Vc1	115	R03/A3	155	SEG12
36	COM29/SEG53	76	OSC3	116	R04/A4	156	SEG13
37	COM28/SEG54	77	OSC4	117	R05/A5	157	SEG14
38	COM27/SEG55	78	Vd1	118	R06/A6	158	SEG15
39	COM26/SEG56	79	VdD	119	R07/A7	159	SEG16
40	COM25/SEG57	80	Vss	120	R10/A8	160	SEG17

## ■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V <sub>DD</sub>	79	–	Power supply (+) terminal
V <sub>SS</sub>	80	–	Power supply (GND) terminal
V <sub>D1</sub>	78	–	Regulated voltage output terminal for oscillators
V <sub>C1</sub> –V <sub>C5</sub>	75–71	O	LCD drive voltage output terminals
CA–CE	70–66	–	Booster capacitor connection terminals for LCD
OSC1	81	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input with mask option)
OSC2	82	O	OSC1 oscillation output terminal
OSC3	76	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input with mask option)
OSC4	77	O	OSC3 oscillation output terminal
MCU/MPU	85	I	Terminal for setting MCU or MPU modes
K00–K07	95–88	I	Input terminals (K00–K07)
K10/EVIN	87	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
K11/BREQ	86	I	Input terminal (K11) or bus request signal input terminal (BREQ)
R00–R07/A0–A7	112–119	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	120–127	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	128–130	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/RD	131	O	Output terminal (R23) or read signal output terminal (RD)
R24/WR	132	O	Output terminal (R24) or write signal output terminal (WR)
R25/CL	133	O	Output terminal (R25) or LCD synchronous signal output terminal (CL)
R26/FR	134	O	Output terminal (R26) or LCD frame signal output terminal (FR)
R27/TOUT	135	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R30–R33/CE0–CE3	136–139	O	Output terminals (R30–R33) or chip enable output terminals (CE0–CE3)
R34/FOUT	140	O	Output terminal (R34) or clock output terminal (FOUT)
R35–R37 *2		O	Output terminals (R35–R37)
R50/BZ	141	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/BACK	142	O	Output terminal (R51) or bus acknowledge signal output terminal (BACK)
P00–P07/D0–D7	111–104	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	103	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	102	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/SCLK	101	I/O	I/O terminal (P12) or serial I/F clock I/O terminal (SCLK)
P13/SRDY	100	I/O	I/O terminal (P13) or serial I/F ready signal output terminal (SRDY)
P14/CMPP0	99	I/O	I/O terminal (P14) or comparator 0 non-inverted input terminal
P15/CMPM0	98	I/O	I/O terminal (P15) or comparator 0 inverted input terminal
P16/CMPP1	97	I/O	I/O terminal (P16) or comparator 1 non-inverted input terminal
P17/CMPM1	96	I/O	I/O terminal (P17) or comparator 1 inverted input terminal
COM0–COM15	65–50	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	49–34	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG50	143–160, 1–33	O	LCD segment output terminals
RESET	84	I	Initial reset input terminal
TEST *1	83	I	Test input terminal

\*1 TEST is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V<sub>DD</sub>.

\*2 R35–R37 terminals can be used only when chip is being shipped.

## ■ ELECTRICAL CHARACTERISTICS

### ● Absolute Maximum Ratings

(V<sub>SS</sub> = 0V)

Item	Symbol	Condition	Value	Unit	Note
Power voltage	V <sub>DD</sub>		-0.3 to +7.0	V	
Liquid crystal power voltage	V <sub>C5</sub>		-0.3 to +7.0	V	
Input voltage	V <sub>I</sub>		-0.3 to V <sub>DD</sub> + 0.3	V	
Output voltage	V <sub>O</sub>		-0.3 to V <sub>DD</sub> + 0.3	V	1
High level output current	I <sub>OH</sub>	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I <sub>OL</sub>	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P <sub>D</sub>		200	mW	2
Operating temperature	T <sub>opr</sub>		-40 to +85	°C	
Storage temperature	T <sub>stg</sub>		-65 to +150	°C	

Note) 1 Case that to Nch open drain output by the mask option is included.

2 In case of plastic package.

### ● Recommended Operating Conditions

(V<sub>SS</sub> = 0V, T<sub>a</sub> = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V <sub>DD</sub>		2.4		5.5	V	
Operating power voltage (Low power mode)	V <sub>DD</sub>		1.8		3.5	V	
Operating power voltage (High speed mode)	V <sub>DD</sub>		3.5		5.5	V	
Operating frequency (Normal mode)	f <sub>OSC1</sub> f <sub>OSC3</sub>	V <sub>DD</sub> = 2.4 to 5.5V	30	32.768	50	kHz	3
			0.03		4.2	MHz	3
Operating frequency (Low power mode)	f <sub>OSC1</sub>	V <sub>DD</sub> = 1.8 to 3.5V	30	32.768	50	kHz	3
Operating frequency (High speed mode)	f <sub>OSC1</sub> f <sub>OSC3</sub>	V <sub>DD</sub> = 3.5 to 5.5V	30	32.768	50	kHz	3
			0.03		8.2	MHz	3
Liquid crystal power voltage	V <sub>C5</sub>	V <sub>C5</sub> ≥ V <sub>C4</sub> ≥ V <sub>C3</sub> ≥ V <sub>C2</sub> ≥ V <sub>C1</sub> ≥ V <sub>SS</sub>			6.0	V	4
Capacitor between V <sub>D1</sub> and V <sub>SS</sub>	C1			0.1		μF	
Capacitor between V <sub>C1</sub> and V <sub>SS</sub>	C2			0.1		μF	5
Capacitor between V <sub>C2</sub> and V <sub>SS</sub>	C3			0.1		μF	5
Capacitor between V <sub>C3</sub> and V <sub>SS</sub>	C4			0.1		μF	5
Capacitor between V <sub>C4</sub> and V <sub>SS</sub>	C5			0.1		μF	5
Capacitor between V <sub>C5</sub> and V <sub>SS</sub>	C6			0.1		μF	5
Capacitor between CA and CB	C7			0.1		μF	5
Capacitor between CA and CC	C8			0.1		μF	5
Capacitor between CD and CE	C9			0.1		μF	5
Resistor between V <sub>C1</sub> and V <sub>SS</sub>	R1			100		kΩ	6

Note) 3 When an external clock is input from the OSC1 terminal by the mask option, do not connect anything to the OSC2 terminal, and when an external clock is input from the OSC3 terminal, do not connect to the OSC4 terminal.

4 When external power supply is selected by the mask option.

5 When LCD drive power is not used, the capacitor is not necessary. In this case, do not connect anything to V<sub>C1</sub> to V<sub>C5</sub> and CA to CE terminals.

6 It is necessary when the panel load is large and for 1/32 duty driving. The resistance value should be decided by connecting it to the actual panel to be used.

## ● DC Characteristics

(Unless otherwise specified:  $V_{DD} = 1.8$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	$V_{IH1}$	Kxx, Pxx, MCU/MPU	$0.8V_{DD}$		$V_{DD}$	V	
Low level input voltage (1)	$V_{IL1}$	Kxx, Pxx, MCU/MPU	0		$0.2V_{DD}$	V	
High level input voltage (2) (Normal mode)	$V_{IH2}$	OSC1, OSC3	1.6		$V_{DD}$	V	7
High level input voltage (2) (Low power mode)	$V_{IH2}$	OSC1	1.0		$V_{DD}$	V	7
High level input voltage (2) (High speed mode)	$V_{IH2}$	OSC1, OSC3	2.4		$V_{DD}$	V	7
Low level input voltage (2) (Normal mode)	$V_{IL2}$	OSC1, OSC3	0		0.6	V	7
Low level input voltage (2) (Low power mode)	$V_{IL2}$	OSC1	0		0.3	V	7
Low level input voltage (2) (High speed mode)	$V_{IL2}$	OSC1, OSC3	0		0.9	V	7
High level schmitt input voltage	$V_{T+}$	RESET	$0.5V_{DD}$		$0.9V_{DD}$	V	
Low level schmitt input voltage	$V_{T-}$	RESET	$0.1V_{DD}$		$0.5V_{DD}$	V	
High level output current	$I_{OH}$	Pxx, Rxx, $V_{OH} = 0.9V_{DD}$			-0.5	mA	
Low level output current	$I_{OL}$	Pxx, Rxx, $V_{OL} = 0.1V_{DD}$	0.5			mA	
Input leak current	$I_{LI}$	Kxx, Pxx, RESET, MCU/MPU	-1		1	$\mu A$	
Output leak current	$I_{LO}$	Pxx, Rxx	-1		1	$\mu A$	
Input pull-up resistance	$R_{IN}$	Kxx, Pxx, RESET, MCU/MPU	100		500	k $\Omega$	8
Input terminal capacitance	$C_{IN}$	Kxx, Pxx, $V_{IN} = 0V$ , $f = 1MHz$ , $T_a = 25^{\circ}C$			15	pF	
Segment/Common output current	ISEGH	SEGxx, COMxx, $V_{SEGH} = V_{C5} - 0.1V$			-5	$\mu A$	
	ISEGL	SEGxx, COMxx, $V_{SEGL} = 0.1V$	5			$\mu A$	

Note) 7 When external clock is selected by mask option.

8 When addition of pull-up resistor is selected by mask option.

## ● SVD Circuit

(Unless otherwise specified:  $V_{DD} = 1.8$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = 25^{\circ}C$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	$V_{SVD}$	Level 1 → Level 0		1.82		V	9
		Level 2 → Level 1		2.00		V	9
		Level 3 → Level 2		2.18		V	9
		Level 4 → Level 3		2.36		V	10
		Level 5 → Level 4	Typ×0.92	2.54	Typ×1.08	V	10
		Level 6 → Level 5		2.72		V	10
		Level 7 → Level 6		2.90		V	11
		Level 8 → Level 7		3.08		V	11
		Level 9 → Level 8		3.26		V	11
		Level 10 → Level 9		3.45		V	12
		Level 11 → Level 10		3.65		V	12
		Level 12 → Level 11	Typ×0.88	3.85	Typ×1.12	V	12
		Level 13 → Level 12		4.05		V	12
		Level 14 → Level 13		4.25		V	12
		Level 15 → Level 14		4.50		V	12

Note) 9 Low power operating mode only.

10 Low power operating mode or Normal operating mode only.

11 Normal operating mode only.

12 Normal operating mode or High speed operating mode only.

## ● Analog Comparator Circuit

(Unless otherwise specified:  $V_{DD} = 1.8$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	VCMIP	Non-inverted input (CMPP)	0.7		$V_{DD} - 0.7$	V	13
	VCMIM	Inverted input (CMPM)	0.7		$V_{DD} - 0.7$	V	13
Analog comparator offset voltage	VCMOF	VCMIP = $0.7V$ to $V_{DD} - 0.7V$ VCMIM = $0.7V$ to $V_{DD} - 0.7V$			20	mV	13
Analog comparator stability time	t <sub>CMP1</sub>				1	mS	14
Analog comparator response time	t <sub>CMP2</sub>	VCMIP = $0.7V$ to $V_{DD} - 0.7V$			2	mS	13
		VCMIM = $0.7V$ to $V_{DD} - 0.7V$					15
		VCMIP = $V_{CMIM} \pm 0.025V$					

Note) 13 When "without pull-up resistor" (comparator input terminal) is selected by mask option.

14 Stability time is the time from turning the circuit ON until the circuit is stabilized.

15 Response time is the time that the output result responds to the input signal.

## ● Current Consumption

(Unless otherwise specified:  $V_{DD}$  = Within the operating voltage in each operating mode,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,

OSC1 = 32.768kHz crystal oscillation,  $C_G = 25pF$ , OSC3 = External clock input, Non heavy load protection mode, C1-C9 = 0.1 $\mu F$ , No panel load)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Power current (Normal mode)	I <sub>DD1</sub>	In SLEEP status *1		0.3	1	$\mu A$		
	I <sub>DD2</sub>	In HALT status *2		2	5	$\mu A$		
	I <sub>DD3</sub>	CPU is in operating (32.768kHz) *3		14	18	$\mu A$		
	I <sub>DD4</sub>	CPU is in operating (1MHz) *4		0.45	0.60	mA		
	I <sub>HVL</sub>	In heavy load protection mode			25	50	$\mu A$	16
Power current (Low power mode)	I <sub>DD1</sub>	In SLEEP status *1		0.2	1	$\mu A$		
	I <sub>DD2</sub>	In HALT status *2		1	5	$\mu A$		
	I <sub>DD3</sub>	CPU is in operating (32.768kHz) *3		8	12	$\mu A$		
	I <sub>HVL</sub>	In heavy load protection mode			15	30	$\mu A$	16
	Power current (High speed mode)	I <sub>DD1</sub>	In SLEEP status *1		1	3	$\mu A$	
I <sub>DD2</sub>		In HALT status *2		5	10	$\mu A$		
I <sub>DD3</sub>		CPU is in operating (32.768kHz) *3		24	30	$\mu A$		
I <sub>DD4</sub>		CPU is in operating (1MHz) *4		0.70	1.00	mA		
I <sub>HVL</sub>		In heavy load protection mode			35	70	$\mu A$	16
LCD drive circuit current	I <sub>LCDN</sub>			2.5	5	$\mu A$		
	I <sub>LCDH</sub>	In heavy load protection mode			15	30	$\mu A$	16
SVD circuit current	I <sub>SVDN</sub>	$V_{DD} = 3.0V$		30	60	$\mu A$	17	
	I <sub>SVDH</sub>	In heavy load protection mode			25	75	$\mu A$	16
Analog comparator circuit current	I <sub>CMP1</sub>	CMPXDT = "1"			40	100	$\mu A$	
	I <sub>CMP2</sub>	CMPXDT = "0"			4	10	$\mu A$	
OSC1 CR oscillation current	I <sub>CR1</sub>			20	50	$\mu A$	18	

\*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status

\*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status

\*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768kHz, Clock timer: Operating, Others: Stop status

\*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 1MHz, Clock timer: Operating, Others: Stop status

Note) 16 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).

17 The value in x V can be found by the following expression:

$I_{SVDN} (V_{DD} = x V) = (x \times 20) - 30$  (Typ. value),  $I_{SVDN} (V_{DD} = x V) = (x \times 30) - 30$  (Max. value)

18 When OSC1 CR oscillation circuit is selected by the mask option.

# E0C88348

## ● LCD Driver

(Unless otherwise specified:  $V_{DD} = V_{C2}$  (LCX = FH) +0.1 to 5.5V,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $C1-C9 = 0.1\mu F$ )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
LCD drive voltage	Vc1	*1	0.18Vc5		0.22Vc5	V		
	Vc2	*2	0.39Vc5		0.43Vc5	V		
	Vc3	*3	0.59Vc5		0.63Vc5	V		
	Vc4	*4	0.80Vc5		0.84Vc5	V		
	Vc5 TYPE A (4.5V)	*5	LCX = 0H	Typ×0.94	3.89	Typ×1.06	V	
			LCX = 1H		3.96		V	
			LCX = 2H		4.04		V	
			LCX = 3H		4.11		V	
			LCX = 4H		4.18		V	
			LCX = 5H		4.26		V	
			LCX = 6H		4.34		V	
			LCX = 7H		4.42		V	
			LCX = 8H		4.50		V	
			LCX = 9H		4.58		V	
			LCX = AH		4.66		V	
			LCX = BH		4.74		V	
			LCX = CH		4.82		V	
			LCX = DH		4.90		V	
			LCX = EH		4.99		V	
			LCX = FH		5.08		V	
	Vc5 TYPE B (5.5V)	*5	LCX = 0H	Typ×0.94	4.73	Typ×1.06	V	
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
LCX = 7H			5.40		V			
LCX = 8H			5.50		V			
LCX = 9H			5.60		V			
LCX = AH			5.70		V			
LCX = BH	5.81	V						
LCX = CH	5.93	V						
LCX = DH	6.05	V						
LCX = EH	6.17	V						
LCX = FH	6.29	V						

\*1 Connects 1MΩ load resistor between Vss and Vc1.

\*2 Connects 1MΩ load resistor between Vss and Vc2.

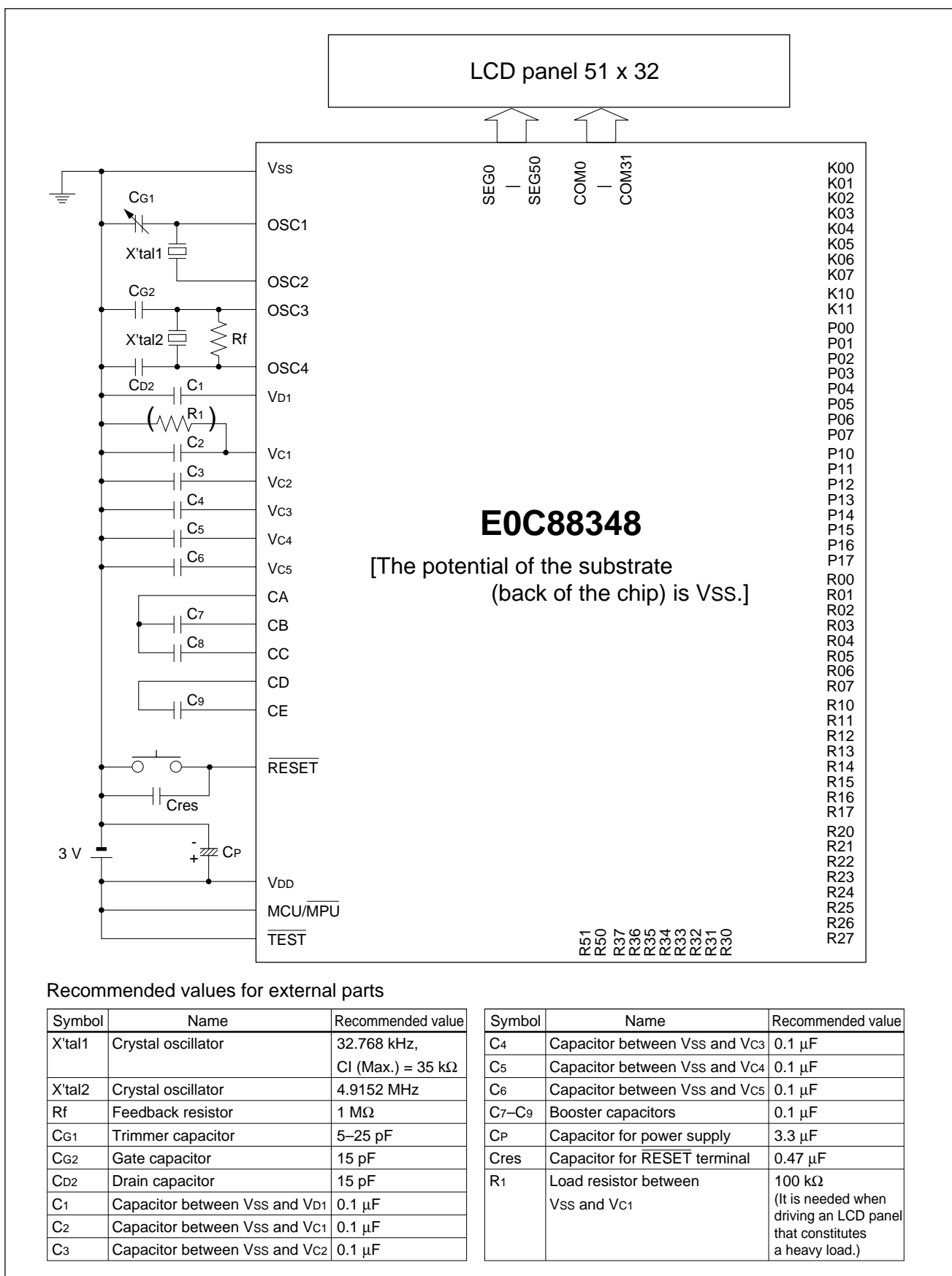
\*3 Connects 1MΩ load resistor between Vss and Vc3.

\*4 Connects 1MΩ load resistor between Vss and Vc4.

\*5 Connects 1MΩ load resistor between Vss and Vc5.

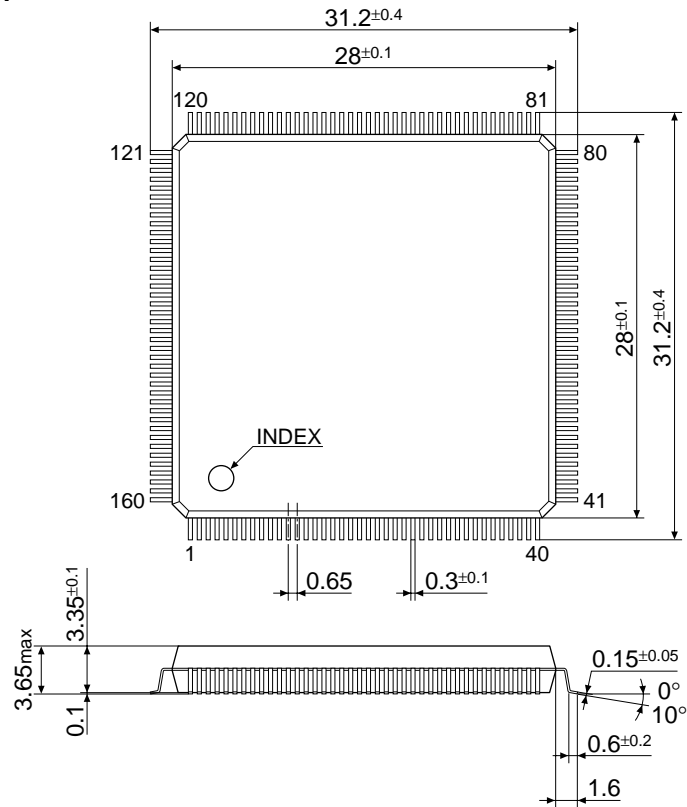


## ■ BASIC EXTERNAL CONNECTION DIAGRAM

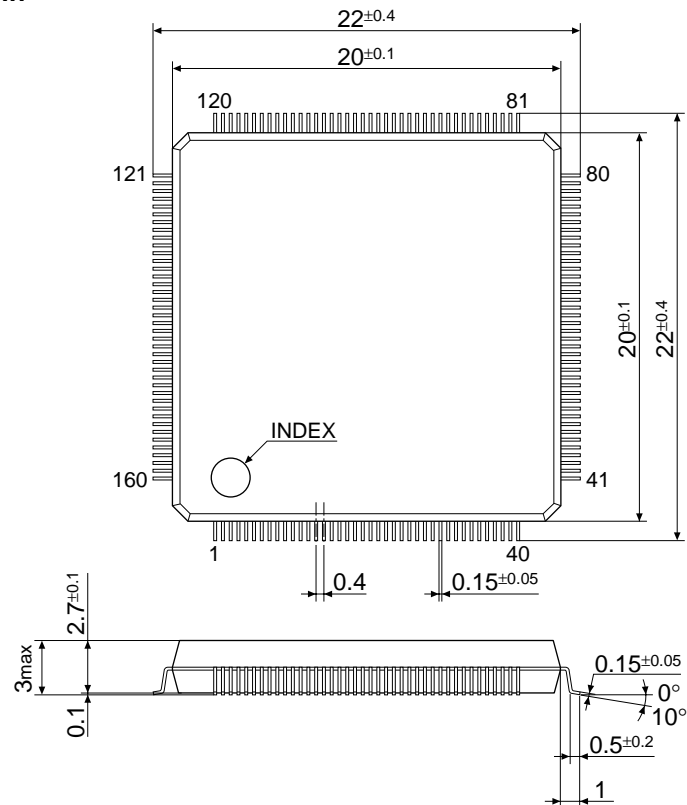


## ■ PACKAGE DIMENSIONS

Plastic QFP8-160pin

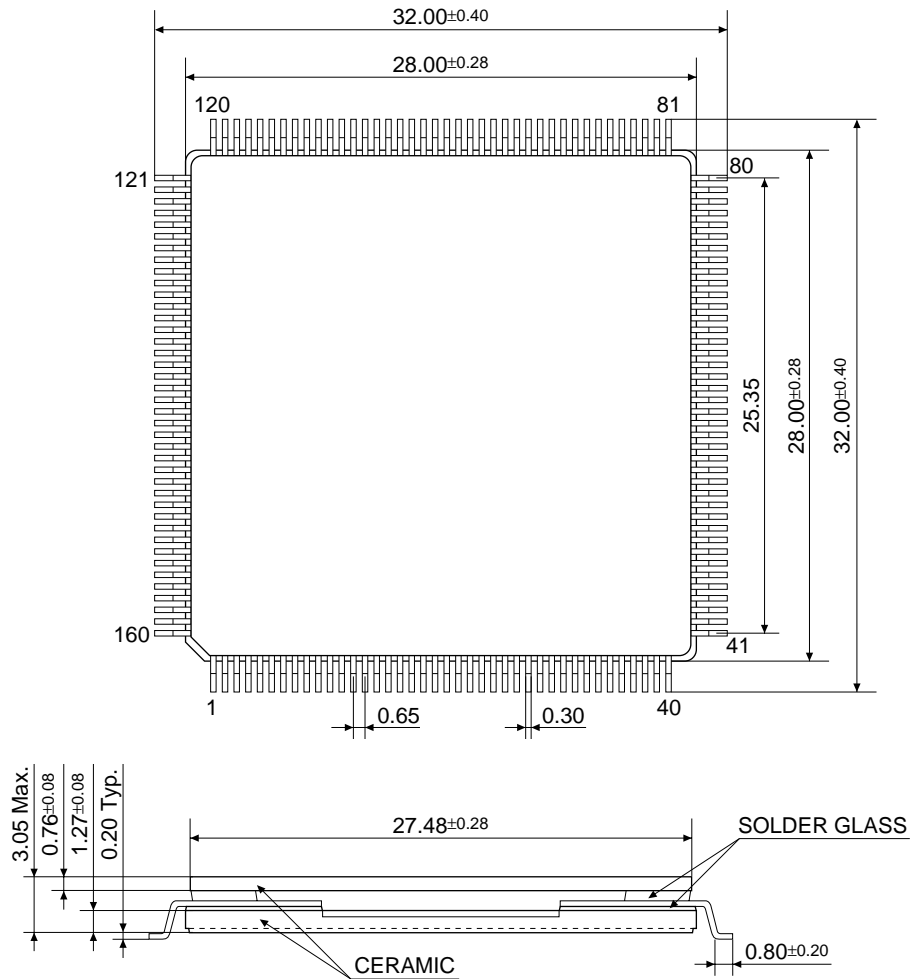


Plastic QFP17-160pin



Unit: mm

Ceramic QFP8-160pin



Unit: mm

# E0C88348

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