EPSON

E0C88349

8-bit Single Chip Microcomputer

Preliminary

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (1.8V to 5.5V)
- High Speed Operation in Low Voltage (0.48µsec/3.0V)
- A/D Converter

■ DESCRIPTION

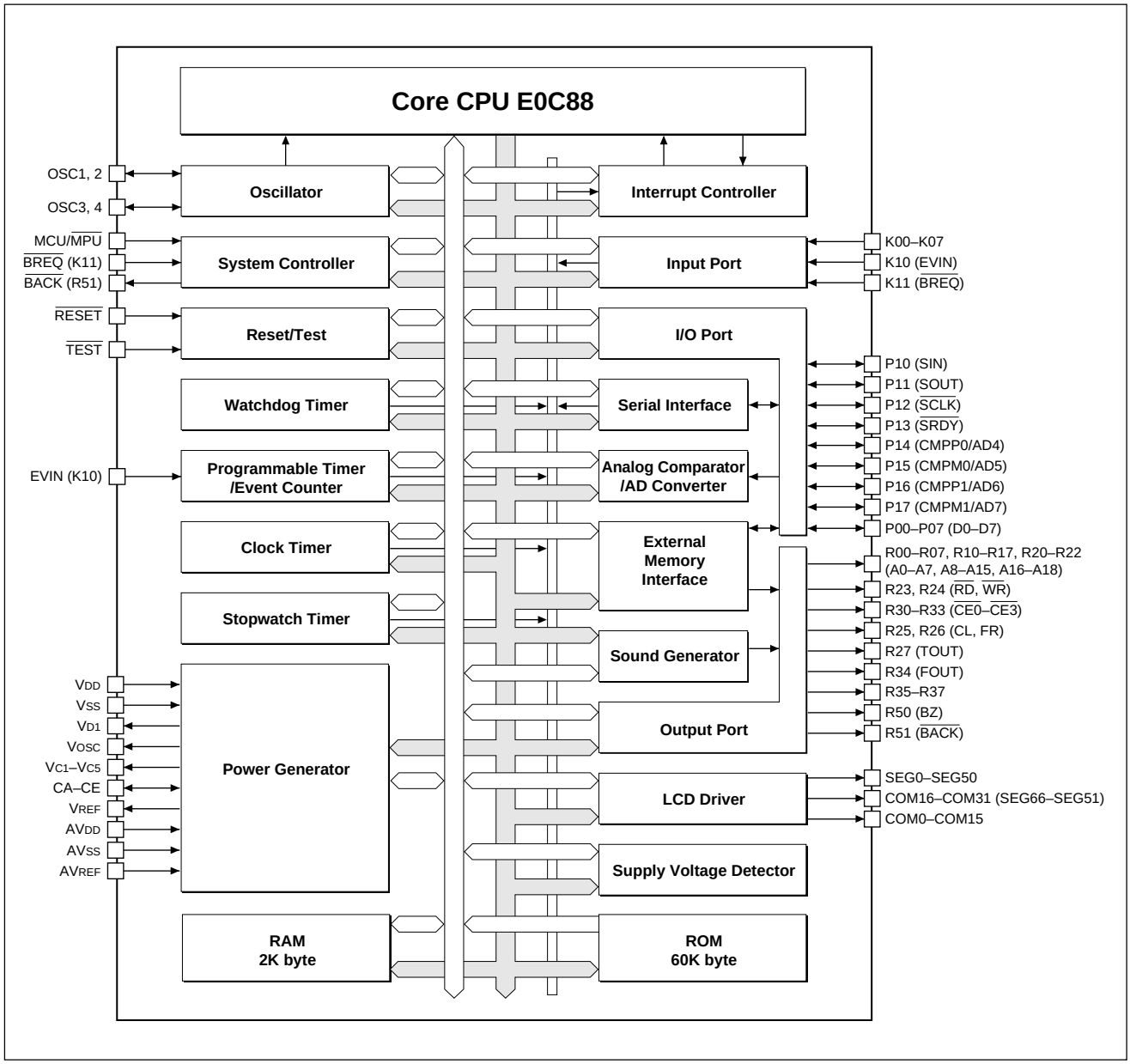
The E0C88349 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, I/O, serial interface, dot-matrix LCD driver, timer, event counter and A/D converter. The E0C88349 fully operable over a wide range of voltages, and can perform high speed operations even at low voltage and low current consumption, it is suitable for portable systems that need to be driven with a battery.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- OSC1 oscillation circuit ..... 32.768kHz (Typ.) crystal/CR oscillation circuit
- OSC3 oscillation circuit ..... 8.2MHz (Max.) crystal/ceramic/CR oscillation circuit
- Instruction set ..... 608 types (usable for multiplication and division instructions)
- Instruction execution time ..... 0.244 µsec/8.2MHz (for 2-clock instructions)
- ROM ..... 48K bytes
- RAM ..... 2K-byte RAM
  3,216-bit display memory
- Bus line ..... Address bus : 19 bits (shared with output ports)
  Data bus : 8 bits (shared with I/O ports)
  $\overline{CE}$ signal : 4 bits (shared with output ports)
  $\overline{WR}$ signal : 1 bit (shared with output port)
  $\overline{RD}$ signal : 1 bit (shared with output port)
- Input port ..... 10 bits (usable for EVIN and $\overline{BREQ}$ signal inputs)
- Output port ..... 9 bits (usable for buzzer, LCD control, FOUT, TOUT and $\overline{BACK}$ signal outputs)
- I/O port ..... 8 bits (usable for serial I/O and analog comparator/AD inputs)
- Serial interface ..... 1 ch. (8-bit clock synchronous or asynchronous system)
- Timer ..... Programmable timer (8 bits) : 2 ch. (usable as a 1-ch. 16-bit timer)
  Clock timer (8 bits) : 1 ch.
  Stopwatch timer (8 bits) : 1 ch.
- LCD driver ..... Dot-matrix type (supports 5 × 8 or 5 × 5 dot font)
  51 segments × 32 commons, 67 segments × 16 or 8 commons
  LCD power supply circuit built-in (boostor type, 5 potentials)
- Sound generator ..... Envelope and volume control functions built-in
- Watchdog timer ..... Built-in
- Analog comparator ..... 2 ch. (not available if A/D converter is used)
- A/D converter ..... 4 ch., 10-bit resolution, maximum error = ±3LSB
  (not available if analog comparator is used)
- Supply voltage detection (SVD) circuit ... 16-level detection

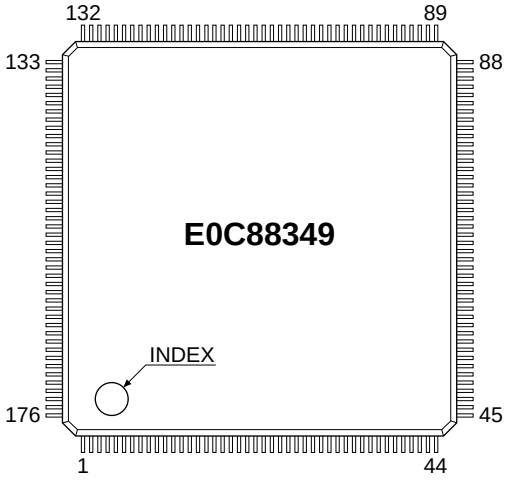
- External interrupt ..... Input port interrupt : 2 systems (3 types)
- Internal interrupt ..... Timer interrupt : 3 systems (9 types)
  Serial interface interrupt : 1 system (3 types)
  A/D converter interrupt : 1 system (1 type)
- Power supply voltage ..... Normal mode : 2.4V to 5.5V (Max. 4.2MHz) V_{D1} = 2.2V
  Low-power mode : 1.8V to 3.5V (Max. 50kHz) V_{D1} = 1.3V
  High-speed mode : 3.5V to 5.5V (Max. 8.2MHz) V_{D1} = 3.3V
- Current consumption ..... SLEEP mode 0.3µA
  HALT mode : 1.5µA (Typ., normal mode)
  Run (32kHz) : 9µA (Typ., normal mode)
  Run (4MHz) : 1.1mA (Typ., normal mode)
- Package ..... QFP18-176pin (plastic) or chip

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP18-176pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG2	45	SEG46	89	OSC1	133	R11/A9
2	SEG3	46	SEG47	90	OSC2	134	R12/A10
3	SEG4	47	SEG48	91	$\overline{\text{TEST}}$	135	R13/A11
4	SEG5	48	SEG49	92	$\overline{\text{RESET}}$	136	R14/A12
5	SEG6	49	SEG50	93	MCU/$\overline{\text{MPU}}$	137	R15/A13
6	SEG7	50	COM31/SEG51	94	K11/$\overline{\text{BREQ}}$	138	R16/A14
7	SEG8	51	COM30/SEG52	95	K10/EVIN	139	R17/A15
8	SEG9	52	COM29/SEG53	96	K07	140	R20/A16
9	SEG10	53	COM28/SEG54	97	K06	141	R21/A17
10	SEG11	54	COM27/SEG55	98	K05	142	R22/A18
11	SEG12	55	COM26/SEG56	99	K04	143	R23/$\overline{\text{RD}}$
12	SEG13	56	COM25/SEG57	100	K03	144	R24/$\overline{\text{WR}}$
13	SEG14	57	COM24/SEG58	101	K02	145	R25/CL
14	SEG15	58	COM23/SEG59	102	K01	146	R26/FR
15	SEG16	59	COM22/SEG60	103	K00	147	R27/TOUT
16	SEG17	60	COM21/SEG61	104	P17/CMPM1/AD7	148	R30/$\overline{\text{CE0}}$
17	SEG18	61	COM20/SEG62	105	P16/CMPP1/AD6	149	R31/$\overline{\text{CE1}}$
18	SEG19	62	COM19/SEG63	106	P15/CMPM0/AD5	150	R32/$\overline{\text{CE2}}$
19	SEG20	63	COM18/SEG64	107	P14/CMPP0/AD4	151	R33/$\overline{\text{CE3}}$
20	SEG21	64	COM17/SEG65	108	P13/$\overline{\text{SRDY}}$	152	R34/FOUT
21	SEG22	65	COM16/SEG66	109	P12/$\overline{\text{SCLK}}$	153	R35
22	SEG23	66	N.C.	110	P11/SOUT	154	R36
23	SEG24	67	N.C.	111	P10/SIN	155	R37
24	SEG25	68	N.C.	112	AV_{DD}	156	V_{SS}
25	SEG26	69	N.C.	113	AV_{SS}	157	R50/$\overline{\text{BZ}}$
26	SEG27	70	N.C.	114	AV_{REF}	158	R51/$\overline{\text{BACK}}$
27	SEG28	71	N.C.	115	V_{DD}	159	COM0
28	SEG29	72	V_{REF}	116	P07/D7	160	COM1
29	SEG30	73	CE	117	P06/D6	161	COM2
30	SEG31	74	CD	118	P05/D5	162	COM3
31	SEG32	75	CC	119	P04/D4	163	COM4
32	SEG33	76	CB	120	P03/D3	164	COM5
33	SEG34	77	CA	121	P02/D2	165	COM6
34	SEG35	78	V_{C5}	122	P01/D1	166	COM7
35	SEG36	79	V_{C4}	123	P00/D0	167	COM8
36	SEG37	80	V_{C3}	124	R00/A0	168	COM9
37	SEG38	81	V_{C2}	125	R01/A1	169	COM10
38	SEG39	82	V_{C1}	126	R02/A2	170	COM11
39	SEG40	83	OSC3	127	R03/A3	171	COM12
40	SEG41	84	OSC4	128	R04/A4	172	COM13
41	SEG42	85	V_{D1}	129	R05/A5	173	COM14
42	SEG43	86	V_{DD}	130	R06/A6	174	COM15
43	SEG44	87	V_{SS}	131	R07/A7	175	SEG0
44	SEG45	88	V_{OSC}	132	R10/A8	176	SEG1

N.C.: No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	86, 115	–	Power supply (+) terminal
V_{SS}	87, 156	–	Power supply (GND) terminal
V_{D1}	85	–	Internal logic system voltage regulator output terminal
V_{OSC}	88	–	Oscillation system voltage regulator output terminal
V_{C1}–V_{C5}	82–78	–	LCD drive voltage output terminals
CA–CE	77–73	–	Booster capacitor connection terminals for LCD
V_{REF}	72	O	LCD power test terminal
OSC1	89	I	OSC1 oscillation input terminal (Crystal, CR or external clock input can be selected by mask option)
OSC2	90	O	OSC1 oscillation output terminal
OSC3	83	I	OSC3 oscillation input terminal (Crystal, Ceramic, CR or external clock input can be selected by mask option)
OSC4	84	O	OSC3 oscillation output terminal
MCU/$\overline{MPU}$	93	I	MCU or MPU mode setting terminal
K00–K07	103–96	I	Input terminals (K00–K07)
K10/EVIN	95	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
K11/$\overline{BREQ}$	94	I	Input terminal (K11) or bus request signal input terminal ($\overline{BREQ}$)
R00–R07/A0–A7	124–131	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	132–139	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	140–142	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/$\overline{RD}$	143	O	Output terminal (R23) or read signal output terminal ($\overline{RD}$)
R24/$\overline{WR}$	144	O	Output terminal (R24) or write signal output terminal ($\overline{WR}$)
R25/CL	145	O	Output terminal (R25) or LCD synchronous signal output terminal (CL)
R26/FR	146	O	Output terminal (R26) or LCD frame signal output terminal (FR)
R27/TOUT	147	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R30–R33/$\overline{CE0}$–$\overline{CE3}$	148–151	O	Output terminals (R30–R33) or chip enable output terminals ($\overline{CE0}$–$\overline{CE3}$)
R34/FOUT	152	O	Output terminal (R34) or clock output terminal (FOUT)
R35–R37	153–155	O	Output terminals (R35–R37)
R50/BZ	157	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{BACK}$	158	O	Output terminal (R51) or bus acknowledge signal output terminal ($\overline{BACK}$)
P00–P07/D0–D7	123–116	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	111	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	110	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{SCLK}$	109	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{SCLK}$)
P13/$\overline{SRDY}$	108	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{SRDY}$)
P14/CMPP0/AD4	107	I/O	I/O terminal (P14), analog comparator 0 non-inverted input terminal or A/D converter input terminal
P15/CMPM0/AD5	106	I/O	I/O terminal (P15), analog comparator 0 inverted input terminal or A/D converter input terminal
P16/CMPP1/AD6	105	I/O	I/O terminal (P16), analog comparator 1 non-inverted input terminal or A/D converter input terminal
P17/CMPM1/AD7	104	I/O	I/O terminal (P17), analog comparator 1 inverted input terminal or A/D converter input terminal
COM0–COM15	159–174	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	65–50	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 duty is selected)
SEG0–SEG50	175–176, 1–49	O	LCD segment output terminals
$\overline{RESET}$	92	I	Initial reset input terminal
$\overline{TEST}$	91	I	Test input terminal
AV_{DD}	112	–	Analog system power supply (+) terminal
AV_{SS}	113	–	Analog system power supply (–) terminal
AV_{REF}	114	–	Analog system reference voltage terminal

■ MASK OPTION

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. External Clock
☐ 3. CR
☐ 4. Crystal (with Gate Capacity)

The specification of the OSC1 oscillation circuit can be selected from among four types: "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" and "External clock input".

2 OSC3 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. Ceramic
☐ 3. CR
☐ 4. External Clock

The specification of the OSC3 oscillation circuit can be selected from among four types: "Crystal oscillation", "Ceramic oscillation", "CR oscillation" and "External clock input".

3 MULTIPLE KEY ENTRY RESET

• Combination ☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

Selects whether the reset function when several keys are pressed simultaneously is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected.

4 MPU MODE INITIAL SET

☐ 1. 512K (MAX)
☐ 2. 512K (MIN)
☐ 3. 64K

The initial bus mode for MPU mode can be selected from among three types: "Extended 512K maximum mode", "Extended 512K minimum mode" and "Extended 64K mode".

5 SVD RESET

☐ 1. Not Use
☐ 2. Use

Selects whether the SVD reset function when the supply voltage drops is used or not.

6 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K04	☐ 1. With Resistor	☐ 2. Gate Direct
• K05	☐ 1. With Resistor	☐ 2. Gate Direct
• K06	☐ 1. With Resistor	☐ 2. Gate Direct
• K07	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• MCU/$\overline{\text{MPU}}$	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{RESET}}$	☐ 1. With Resistor	☐ 2. Gate Direct

Selects whether the pull-up resistor for the input port terminal is used or not. It is possible to select for each bit of the input ports.
Furthermore, pull-up option is also provided for the MCU/$\overline{\text{MPU}}$ and $\overline{\text{RESET}}$ terminals.

7 I/O PORT PULL UP RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P04	☐ 1. With Resistor	☐ 2. Gate Direct
• P05	☐ 1. With Resistor	☐ 2. Gate Direct
• P06	☐ 1. With Resistor	☐ 2. Gate Direct
• P07	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P14	☐ 1. With Resistor	☐ 2. Gate Direct
• P15	☐ 1. With Resistor	☐ 2. Gate Direct
• P16	☐ 1. With Resistor	☐ 2. Gate Direct
• P17	☐ 1. With Resistor	☐ 2. Gate Direct

Selects whether the pull-up resistor for the I/O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the I/O ports.
Since P10 to P13 are shared with the serial interface I/O terminals, the selected P10 and P12 terminal configuration is applied to the serial input (SIN) terminal and serial clock input terminal ($\overline{\text{SCLK}}$ in clock synchronous mode) when the serial interface is used.

8 OUTPUT PORT SPECIFICATION

- R00 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R01 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R02 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R03 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R04 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R05 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R06 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R07 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R10 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R11 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R12 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R13 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R14 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R15 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R16 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain
- R17 ..... ☐ 1. Complementary ☐ 2. Nch Open Drain

The output specification of the output ports R00–R07 and R10–R17 can be selected from complementary output and Nch open drain output in 1-bit units.

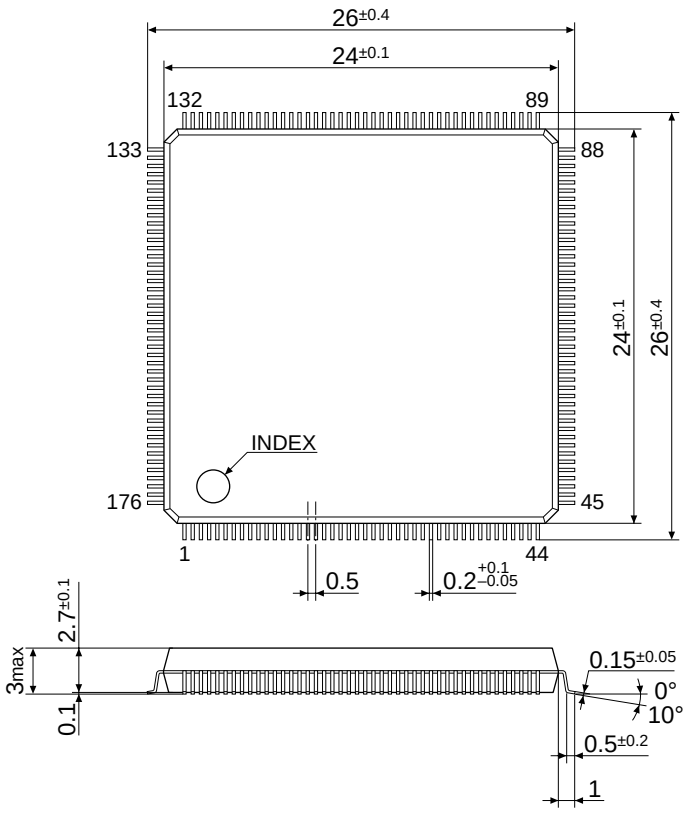
9 LCD POWER SUPPLY

☐ 1. Internal Power Supply
☐ 2. External Power Supply

Either the internal power supply (V_{C1} to V_{C5} are generated by the internal LCD system voltage circuit and voltage booster) or an external power supply can be selected as the LCD system power source.

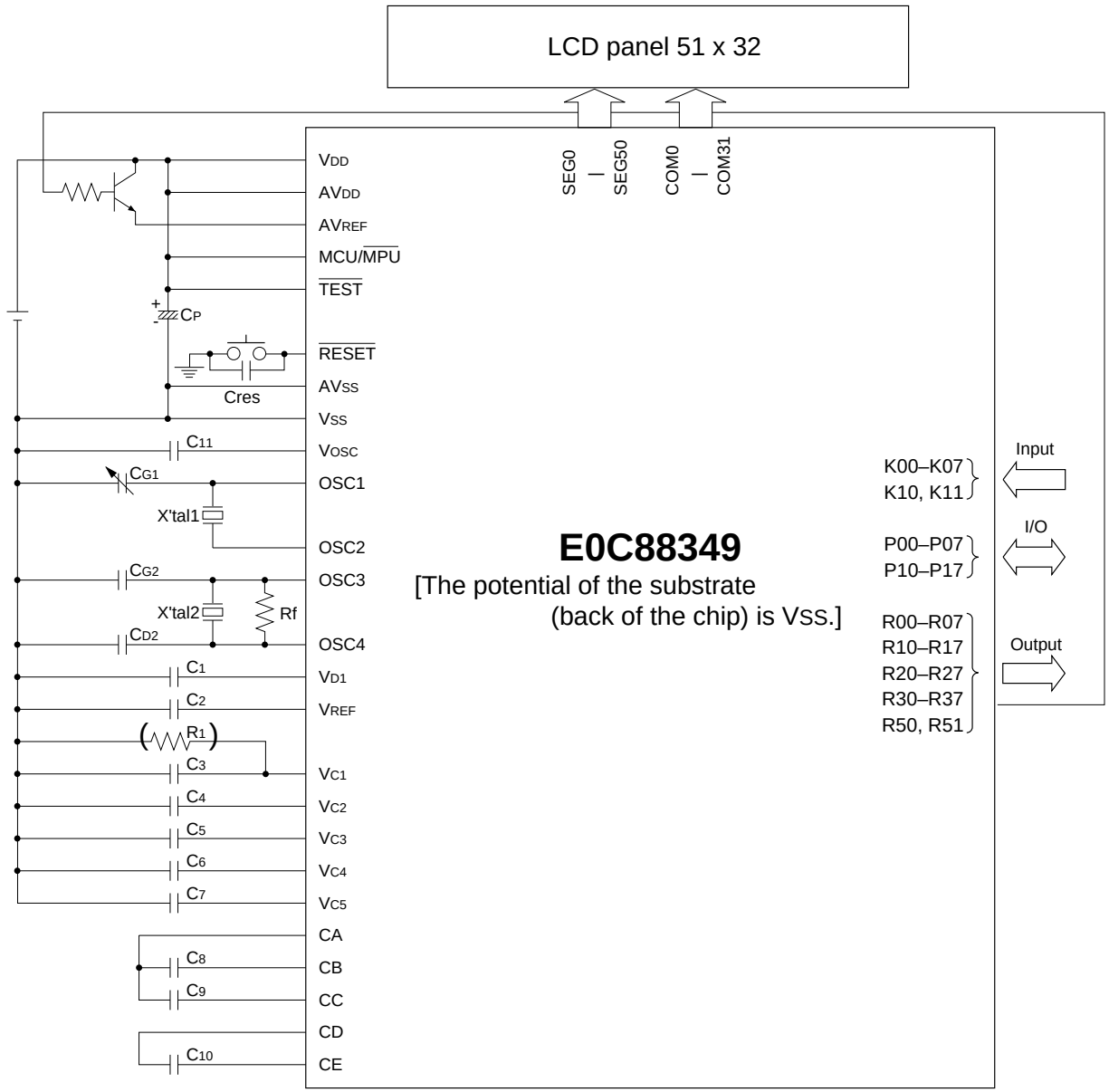
■ PACKAGE DIMENSIONS

Plastic QFP18-176pin



Unit: mm

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
X'tal2	Crystal oscillator	4.9152 MHz
Rf	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15–30 pF
C_{D2}	Drain capacitor	15–30 pF
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{REF}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C2}	0.1 µF

Symbol	Name	Recommended value
C_5	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_7	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_{8}–C_{10}	Booster capacitors	0.1 µF
C_{11}	Capacitor between V_{SS} and V_{OSC}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF
R_1	Load resistor between V_{SS} and V_{C1}	100 kΩ (It is needed when driving an LCD panel that constitutes a heavy load.)

∗ The connection diagram shown above is an example of when mask option settings are as follows:
OSC1: Crystal oscillation, OSC3: Crystal oscillation, LCD power source: Internal power supply,
$\overline{\text{RESET}}$ terminal: With pull-up resistor

Note: The above table is simply an example, and is not guaranteed to work.

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

■ EPSON Electronic Devices Website
http://www.epson.co.jp/device/

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