EPSON

E0C88365

8-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Original Architecture Core CPU
- High Speed Operation in Low Voltage (2.5MHz/2.2V)
- Dot Matrix LCD Driver (18com × 80seg)
- Serial Interface

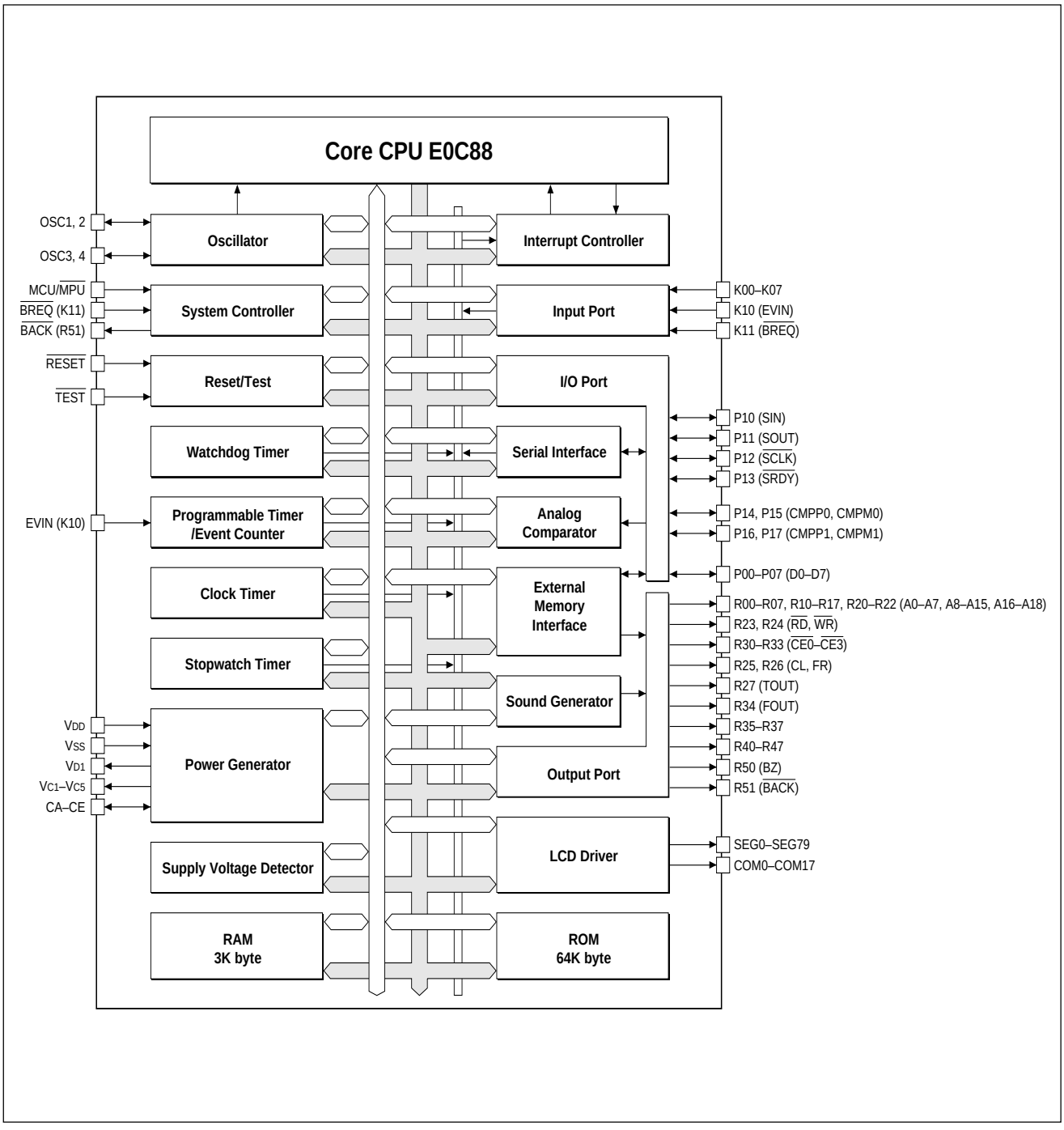
■ DESCRIPTION

The E0C88365 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU E0C88, ROM, RAM, dot matrix LCD driver, serial interface and other circuits. The E0C88365 features a high speed operation with a low voltage, and is most suitable for various application equipment such as pagers and electronic organizers.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Twin clock ..... OSC1: 32.768kHz (Typ.) or 153.6kHz (Max.) OSC3: 2.5MHz (Max.)
- Special instruction set ..... 608 types (Multiplicatin/Division)
- Instruction execution time ..... 0.8µsec (Min.)
- ROM capacity ..... 64K × 8 bits
- RAM capacity ..... 3K × 8 bits (Work) 4,608 bits (Display)
- Addressing ..... 512K-byte (19 bits)
  - Address bus : 19-bit ROM addressing, 19-bit RAM addressing
  - Data bus : 8 bits
  - $\overline{CE}$ signal : 4 bits
  - $\overline{WR}$ signal : 1 bit
  - $\overline{RD}$ signal : 1 bit
  - (Address bus, Data bus, $\overline{CE}$, $\overline{WR}$, $\overline{RD}$ can be used as general purpose I/O ports)
- I/O port ..... Input only : 10 bits ($\overline{BREQ}$ and EVIN are available by software)
  - Output only : 17 bits (BZ, FOUT, TOUT and $\overline{BACK}$ are available by software)
  - Bidirectional I/O : 8 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN and SOUT are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software)
- LCD driver ..... Dot matrix 18 commons × 80 segments
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  - (16-bit 1 channel timer is available)
  - Time base counter : 1 channel
  - Stopwatch timer : 1 channel
- Sound generator ..... 8 levels, with envelope, volume adjustment and 1 shot functions
- Watchdog timer ..... Generates NMI
- Supply voltage detection (SVD) circuit .. 16 levels
- Analog comparator ..... 2 channels built-in (Bidirectional I/O port is used as the input port)
- Interrupt ..... External : 2 systems (3 types)
  - Internal : 3 systems (9 types)
  - Serial I/F : 1 system (3 types)
- Supply voltage ..... 2.2V to 5.5V (Max. 2.5MHz)
- Current consumption ..... SLEEP mode 300nA (3V)
  - HALT mode 2.0µA (32.768kHz/3V)
  - RUN mode 14.0µA (32.768kHz/3V)
  - 1.5mA (2.5MHz/3V)
- Package ..... Die form (188 pads)

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin name	Pin No.	In/out	Function
V_{DD}	93	–	Power supply (+) terminal
V_{SS}	94, 126, 151	–	Power supply (GND) terminal
V_{D1}	92	–	Regulated voltage output terminal for oscillators
V_{C1}–V_{C5}	89–85	O	LCD drive voltage output terminals
CA–CE	84–80	–	Booster capacitor connection terminals for LCD
OSC1	95	I	OSC1 oscillation input terminal (select crystal oscillation/external clock input with mask option)
OSC2	96	O	OSC1 oscillation output terminal
OSC3	90	I	OSC3 oscillation input terminal
OSC4	91	O	OSC3 oscillation output terminal
MCU/$\overline{\text{MPU}}$	99	I	Terminal for setting MCU or $\overline{\text{MPU}}$ modes
K00–K07	109–102	I	Input port (K00–K07) terminal
K10/EVIN	101	I	Input port (K10) terminal or event counter external clock (EVIN) input terminal
K11/$\overline{\text{BREQ}}$	100	I	Input port (K11) terminal or bus request signal ($\overline{\text{BREQ}}$) input terminal
R00–R07/A0–A7	127–134	O	Output port (R00–R07) terminals or address bus (A0–A7)
R10–R17/A8–A15	135–142	O	Output port (R10–R17) terminals or address bus (A8–A15)
R20–R22/A16–A18	143–145	O	Output port (R20–R22) terminals or address bus (A16–A18)
R23/$\overline{\text{RD}}$	146	O	Output port (R23) terminal or read signal ($\overline{\text{RD}}$) output terminal
R24/$\overline{\text{WR}}$	147	O	Output port (R24) terminal or write signal ($\overline{\text{WR}}$) output terminal
R25/CL	148	O	Output port (R25) terminal or LCD synchronous signal (CL) output terminal
R26/FR	149	O	Output port (R26) terminal or LCD frame signal (FR) output terminal
R27/TOUT	150	O	Output port (R27) terminal or programmable timer underflow signal (TOUT) output terminal
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	152–155	O	Output port (R30–R33) terminals or chip enable ($\overline{\text{CE0}}$–$\overline{\text{CE3}}$) output terminals
R34/FOUT	156	O	Output port (R34) terminal or clock (FOUT) output terminal
R35–R37	157–159	O	Output port (R35–R37) terminal
R40–R47	160–167	O	Output port (R40–R47) terminal
R50/BZ	168	O	Output port (R50) terminal or buzzer (BZ) output terminal
R51/$\overline{\text{BACK}}$	169	O	Output port (R51) terminal or bus acknowledge signal ($\overline{\text{BACK}}$) output terminal
P00–P07/D0–D7	125–118	I/O	I/O port (P00–P07) terminals or data bus (D0–D7)
P10/SIN	117	I/O	I/O port (P10) terminal or serial I/F data input (SIN) terminal
P11/SOUT	116	I/O	I/O port (P11) terminal or serial I/F data output (SOUT) terminal
P12/$\overline{\text{SCLK}}$	115	I/O	I/O port (P12) terminal or serial I/F clock ($\overline{\text{SCLK}}$) I/O terminal
P13/$\overline{\text{SRDY}}$	114	I/O	I/O port (P13) terminal or serial I/F ready signal ($\overline{\text{SRDY}}$) output terminal
P14/CMPP0	113	I/O	I/O port (P14) terminal or comparator 0 non-inverted input terminal
P15/CMPM0	112	I/O	I/O port (P15) terminal or comparator 0 inverted input terminal
P16/CMPP1	111	I/O	I/O port (P16) terminal or comparator 1 non-inverted input terminal
P17/CMPM1	110	I/O	I/O port (P17) terminal or comparator 1 inverted input terminal
COM0–COM17	79–62	O	LCD common output terminals
SEG0–SEG79	170–188, 1–61	O	LCD segment output terminals
$\overline{\text{RESET}}$	98	I	Initial reset input terminal
$\overline{\text{TEST}}$ ∗1	97	I	Test input terminal

∗1 $\overline{\text{TEST}}$ is the terminal used for outgoing inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}	–	-0.3 to +7.0	V	–
Liquid crystal power voltage	V_{C5}	–	-0.3 to +7.0	V	–
Input voltage	V_I	–	-0.3 to V_{DD} + 0.3	V	–
Output voltage	V_O	–	-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	–
		Total of all terminals	-20	mA	–
Low level output current	I_{OL}	1 terminal	5	mA	–
		Total of all terminals	20	mA	–
Operating temperature	Topr	–	-40 to +85	°C	–
Storage temperature	Tstg	–	-65 to +150	°C	–

Note) 1 Case that to Nch open drain output by the mask option is included.

● Recommended Operating Conditions

(V_{SS} = 0 V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage	V_{DD}	–	2.2	–	5.5	V	–
Operating frequency	f_{OSC1}	V_{DD} = 2.2 to 5.5 V	30	–	155	kHz	2
	f_{OSC3}		0.03	–	2.5	MHz	–
Capacitor between V_{D1} and V_{SS}	C1	–	–	0.1	–	µF	–
Capacitor between V_{C1} and V_{SS}	C2	–	–	0.1	–	µF	–
Capacitor between V_{C2} and V_{SS}	C3	–	–	0.1	–	µF	–
Capacitor between V_{C3} and V_{SS}	C4	–	–	0.1	–	µF	–
Capacitor between V_{C4} and V_{SS}	C5	–	–	0.1	–	µF	–
Capacitor between V_{C5} and V_{SS}	C6	–	–	0.1	–	µF	–
Capacitor between CA and CB	C7	–	–	0.1	–	µF	–
Capacitor between CA and CC	C8	–	–	0.1	–	µF	–
Capacitor between CD and CE	C9	–	–	0.1	–	µF	–
Resistor between V_{C1} and V_{SS}	R1	–	–	100	–	kΩ	3

Note) 2 When an external clock is input from the OSC1 terminal by the mask option, do not connect anything to the OSC2 terminal.
3 It is necessary when a large panel is used. The resistance value should be decided by connecting it to the actual panel to be used.

● DC Characteristics

(Unless otherwise specified: V_{DD} = 2.2 to 5.5V, V_{SS} = 0V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx, MCU/$\overline{MPU}$	0.8V_{DD}	–	V_{DD}	V	–
Low level input voltage (1)	V_{IL1}	Kxx, Pxx, MCU/$\overline{MPU}$	0	–	0.2V_{DD}	V	–
High level input voltage (2)	V_{IH2}	OSC1	1.6	–	V_{DD}	V	4
Low level input voltage (2)	V_{IL2}	OSC1	0	–	0.6	V	4
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}	–	0.9V_{DD}	V	–
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}	–	0.5V_{DD}	V	–
High level output current (1)	I_{OH1}	P1x, Rxx, V_{OH} = 0.9 V_{DD}	–	–	-0.5	mA	–
Low level output current (1)	I_{OL1}	P1x, Rxx, V_{OL} = 0.1 V_{DD}	0.5	–	–	mA	–
High level output current (2)	I_{OH2}	P0x	–	–	-0.1	mA	–
Low level output current (2)	I_{OL2}	P0x	0.1	–	–	mA	–
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	-1	–	1	µA	–
Output leak current	I_{LO}	Pxx, Rxx	-1	–	1	µA	–
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$, MCU/$\overline{MPU}$	100	–	500	kΩ	5
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0 V, f = 1 MHz, Ta = 25°C	–	–	15	pF	–
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V	–	–	-5	µA	–
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V	5	–	–	µA	–

Note) 4 When external clock is selected by mask option.
5 When addition of pull-up resistor is selected by mask option.

● LCD Circuit

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number). Therefore, these should be evaluated by connecting to the actual panel to be used. Moreover, if the display is uneven with a large panel load, connect a resistor (R_1) between the V_{SS} and V_{C1} terminal.

(Unless otherwise specified: $V_{DD} = V_{C2}$ (LCX = FH) + 0.3 to 5.5V, V_{SS} = 0V, Ta = 25°C, C1–C9 = 0.1µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	*1		0.18V_{C5}	–	0.22V_{C5}	V	–
	V_{C2}	*2		0.39V_{C5}	–	0.43V_{C5}	V	–
	V_{C3}	*3		0.59V_{C5}	–	0.63V_{C5}	V	–
	V_{C4}	*4		0.80V_{C5}	–	0.84V_{C5}	V	–
	V_{C5}	*5	LCX = 0H	Typ×0.94	3.89	Typ×1.06	V	–
			LCX = 1H		3.96		V	–
			LCX = 2H		4.04		V	–
			LCX = 3H		4.11		V	–
			LCX = 4H		4.18		V	–
			LCX = 5H		4.26		V	–
			LCX = 6H		4.34		V	–
			LCX = 7H		4.42		V	–
			LCX = 8H		4.50		V	–
			LCX = 9H		4.58		V	–
			LCX = AH		4.66		V	–
			LCX = BH		4.74		V	–
			LCX = CH		4.82		V	–
			LCX = DH		4.90		V	–
			LCX = EH		4.99		V	–
			LCX = FH		5.08		V	–

*1 Connects 1 MΩ load resistor between V_{SS} and V_{C1}. (without panel load)
*2 Connects 1 MΩ load resistor between V_{SS} and V_{C2}. (without panel load)
*3 Connects 1 MΩ load resistor between V_{SS} and V_{C3}. (without panel load)
*4 Connects 1 MΩ load resistor between V_{SS} and V_{C4}. (without panel load)
*5 Connects 1 MΩ load resistor between V_{SS} and V_{C5}. (without panel load)

● SVD Circuit

(Unless otherwise specified: V_{DD} = 2.2 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	–
		Level 2 → Level 1		2.00		V	–
		Level 3 → Level 2		2.18		V	–
		Level 4 → Level 3		2.36		V	–
		Level 5 → Level 4		2.54		V	–
		Level 6 → Level 5		2.72		V	–
		Level 7 → Level 6		2.90		V	–
		Level 8 → Level 7		3.08		V	–
		Level 9 → Level 8		3.26		V	–
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	–
		Level 11 → Level 10		3.65		V	–
		Level 12 → Level 11		3.85		V	–
		Level 13 → Level 12		4.05		V	–
		Level 14 → Level 13		4.25		V	–
		Level 15 → Level 14		4.50		V	–

● Analog Comparator Circuit

(Unless otherwise specified: V_{DD} = 2.2 to 5.5V, V_{SS} = 0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	V_{CMIP}	Non-inverted input (CMPP)	0.7	–	V_{DD}-0.7	V	6
	V_{CMIM}	Inverted input (CMPM)	0.7	–	V_{DD}-0.7	V	6
Analog comparator offset voltage	V_{CMOF}	V_{CMIP} = 0.7 V to V_{DD} - 0.7 V V_{CMIM} = 0.7 V to V_{DD} - 0.7 V	–	–	20	mV	6
Analog comparator stability time	t_{CMP1}		–	–	1	mS	7
Analog comparator response time	t_{CMP2}	V_{CMIP} = 0.7 V to V_{DD} - 0.7 V V_{CMIM} = 0.7 V to V_{DD} - 0.7 V V_{CMIP} = V_{CMIM} ± 0.025 V	–	–	2	mS	6 8

Note) 6 When "without pull-up resistor" (comparator input terminal) is selected by mask option
7 Stability time is the time from turning the circuit ON until the circuit is stabilized.
8 Response time is the time that the output result responds to the input signal.

● Current Consumption

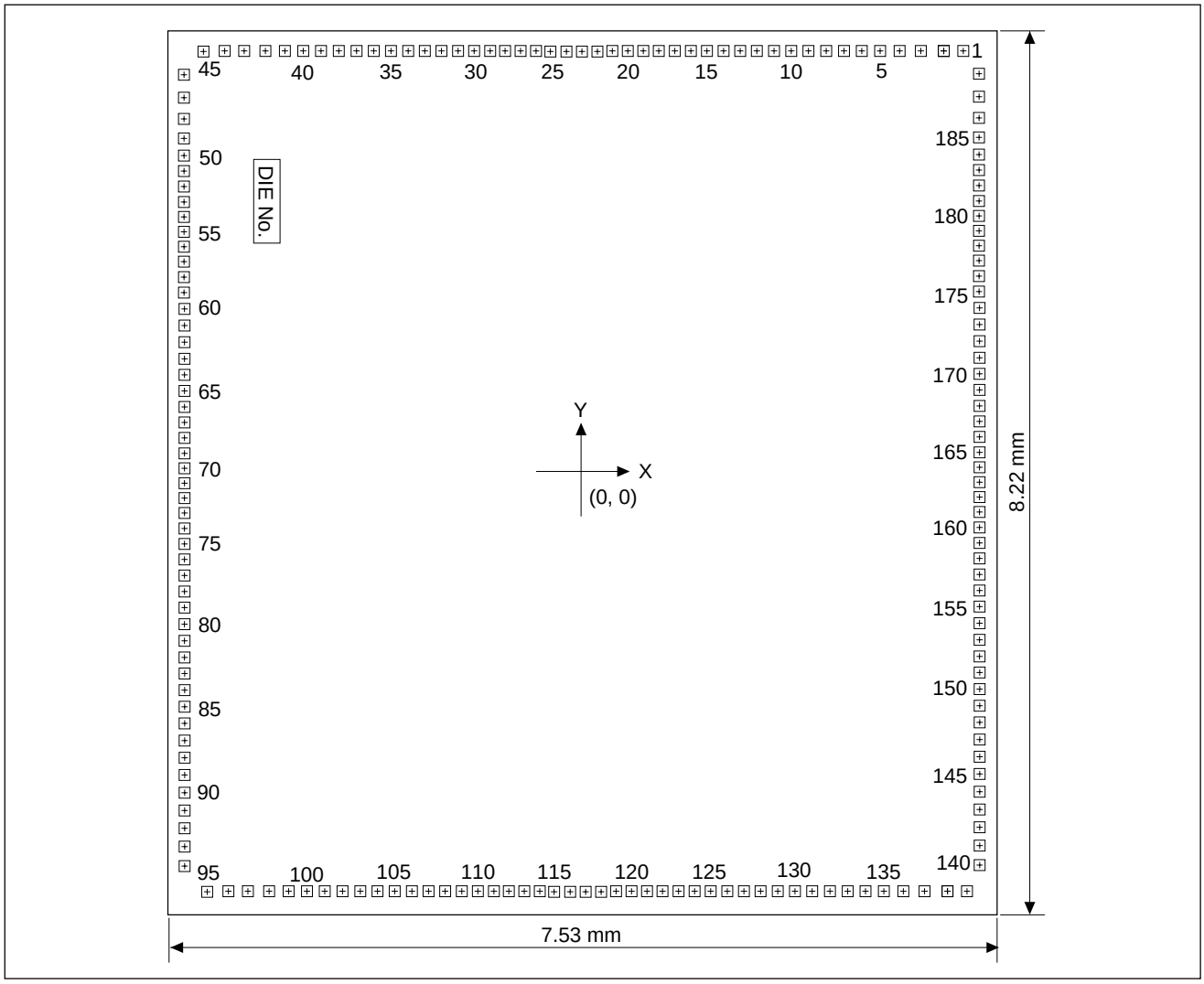
(Unless otherwise specified: V_{DD} = 2.2 to 5.5V, V_{SS} = 0V, Ta = 25°C, OSC1 = 153.6kHz crystal oscillation, C_{G1} = 20pF, OSC3 = CR oscillation, Non heavy load protection mode, C1–C9 = 0.1µF, No panel load)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current	I_{DD1}	In SLEEP status *1	–	0.3	1	µA	–
	I_{DD2}	In HALT status (153.6 kHz) *2	–	10	25	µA	–
	I_{DD3}	CPU is in operating (153.6 kHz) *3	–	70	90	µA	–
	I_{DD4}	CPU is in operating (2.5 MHz) *4	–	1.5	2	mA	–
	I_{HVL}	In heavy load protection mode	–	25	50	µA	9
LCD drive circuit current	I_{LCDN}	–	–	2.5	5	µA	–
	I_{LCDH}	In heavy load protection mode	–	15	30	µA	9
SVD circuit current	I_{SVDN}	V_{DD} = 3.0 V	–	30	60	µA	10
	I_{SVDH}	In heavy load protection mode	–	25	75	µA	9
Analog comparator circuit current	I_{CMP1}	CMPXDT = "1"	–	40	100	µA	–
	I_{CMP2}	CMPXDT = "0"	–	4	10	µA	–

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 153.6 kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 2.5 MHz, Clock timer: Operating, Others: Stop status

Note) 9 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
10 The value in x V can be found by the following expression: I_{SVDN} (V_{DD} = x V) = (x × 20) - 30 (Typ. value), I_{SVDN} (V_{DD} = x V) = (x × 30) - 30 (Max. value)

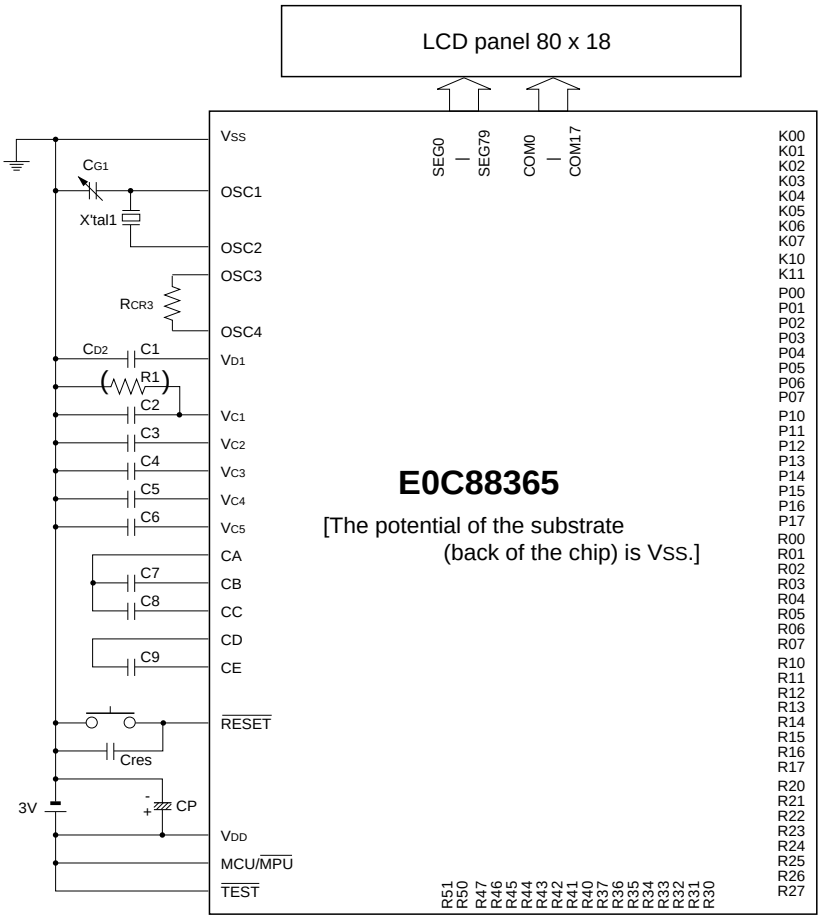
■ DIAGRAM OF PAD LAYOUT



■ PAD COORDINATES

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	SEG19	3.450	3.968	48	SEG66	-3.624	3.400	95	OSC1	-3.450	-3.968	142	R17	3.624	-3.400
2	SEG20	3.240	3.968	49	SEG67	-3.624	3.210	96	OSC2	-3.240	-3.968	143	R20	3.624	-3.210
3	SEG21	3.040	3.968	50	SEG68	-3.624	3.020	97	$\overline{\text{TEST}}$	-3.040	-3.968	144	R21	3.624	-3.020
4	SEG22	2.850	3.968	51	SEG69	-3.624	2.830	98	$\overline{\text{RESET}}$	-2.850	-3.968	145	R22	3.624	-2.830
5	SEG23	2.660	3.968	52	SEG70	-3.624	2.660	99	$\overline{\text{MPU}}$	-2.660	-3.968	146	R23	3.624	-2.660
6	SEG24	2.490	3.968	53	SEG71	-3.624	2.490	100	K11	-2.490	-3.968	147	R24	3.624	-2.490
7	SEG25	2.320	3.968	54	SEG72	-3.624	2.320	101	K10	-2.320	-3.968	148	R25	3.624	-2.320
8	SEG26	2.150	3.968	55	SEG73	-3.624	2.150	102	K07	-2.150	-3.968	149	R26	3.624	-2.150
9	SEG27	2.000	3.968	56	SEG74	-3.624	2.000	103	K06	-2.000	-3.968	150	R27	3.624	-2.000
10	SEG28	1.850	3.968	57	SEG75	-3.624	1.850	104	K05	-1.850	-3.968	151	V_{SS}	3.624	-1.850
11	SEG29	1.700	3.968	58	SEG76	-3.624	1.700	105	K04	-1.700	-3.968	152	R30	3.624	-1.700
12	SEG30	1.550	3.968	59	SEG77	-3.624	1.550	106	K03	-1.550	-3.968	153	R31	3.624	-1.550
13	SEG31	1.400	3.968	60	SEG78	-3.624	1.400	107	K02	-1.400	-3.968	154	R32	3.624	-1.400
14	SEG32	1.260	3.968	61	SEG79	-3.624	1.260	108	K01	-1.260	-3.968	155	R33	3.624	-1.260
15	SEG33	1.120	3.968	62	COM17	-3.624	1.120	109	K00	-1.120	-3.968	156	R34	3.624	-1.120
16	SEG34	0.980	3.968	63	COM16	-3.624	0.980	110	P17	-0.980	-3.968	157	R35	3.624	-0.980
17	SEG35	0.840	3.968	64	COM15	-3.624	0.840	111	P16	-0.840	-3.968	158	R36	3.624	-0.840
18	SEG36	0.700	3.968	65	COM14	-3.624	0.700	112	P15	-0.700	-3.968	159	R37	3.624	-0.700
19	SEG37	0.560	3.968	66	COM13	-3.624	0.560	113	P14	-0.560	-3.968	160	R40	3.624	-0.560
20	SEG38	0.420	3.968	67	COM12	-3.624	0.420	114	P13	-0.420	-3.968	161	R41	3.624	-0.420
21	SEG39	0.280	3.968	68	COM11	-3.624	0.280	115	P12	-0.280	-3.968	162	R42	3.624	-0.280
22	SEG40	0.140	3.968	69	COM10	-3.624	0.140	116	P11	-0.140	-3.968	163	R43	3.624	-0.140
23	SEG41	0.000	3.968	70	COM9	-3.624	0.000	117	P10	0.000	-3.968	164	R44	3.624	0.000
24	SEG42	-0.140	3.968	71	COM8	-3.624	-0.140	118	P07	0.140	-3.968	165	R45	3.624	0.140
25	SEG43	-0.280	3.968	72	COM7	-3.624	-0.280	119	P06	0.280	-3.968	166	R46	3.624	0.280
26	SEG44	-0.420	3.968	73	COM6	-3.624	-0.420	120	P05	0.420	-3.968	167	R47	3.624	0.420
27	SEG45	-0.560	3.968	74	COM5	-3.624	-0.560	121	P04	0.560	-3.968	168	R50	3.624	0.560
28	SEG46	-0.700	3.968	75	COM4	-3.624	-0.700	122	P03	0.700	-3.968	169	R51	3.624	0.700
29	SEG47	-0.840	3.968	76	COM3	-3.624	-0.840	123	P02	0.840	-3.968	170	SEG0	3.624	0.840
30	SEG48	-0.980	3.968	77	COM2	-3.624	-0.980	124	P01	0.980	-3.968	171	SEG1	3.624	0.980
31	SEG49	-1.120	3.968	78	COM1	-3.624	-1.120	125	P00	1.120	-3.968	172	SEG2	3.624	1.120
32	SEG50	-1.260	3.968	79	COM0	-3.624	-1.260	126	V_{SS}	1.260	-3.968	173	SEG3	3.624	1.260
33	SEG51	-1.400	3.968	80	CE	-3.624	-1.400	127	R00	1.400	-3.968	174	SEG4	3.624	1.400
34	SEG52	-1.550	3.968	81	CD	-3.624	-1.550	128	R01	1.550	-3.968	175	SEG5	3.624	1.550
35	SEG53	-1.700	3.968	82	CC	-3.624	-1.700	129	R02	1.700	-3.968	176	SEG6	3.624	1.700
36	SEG54	-1.850	3.968	83	CB	-3.624	-1.850	130	R03	1.850	-3.968	177	SEG7	3.624	1.850
37	SEG55	-2.000	3.968	84	CA	-3.624	-2.000	131	R04	2.000	-3.968	178	SEG8	3.624	2.000
38	SEG56	-2.150	3.968	85	V_{C5}	-3.624	-2.150	132	R05	2.150	-3.968	179	SEG9	3.624	2.150
39	SEG57	-2.320	3.968	86	V_{C4}	-3.624	-2.320	133	R06	2.320	-3.968	180	SEG10	3.624	2.320
40	SEG58	-2.490	3.968	87	V_{C3}	-3.624	-2.490	134	R07	2.490	-3.968	181	SEG11	3.624	2.490
41	SEG59	-2.660	3.968	88	V_{C2}	-3.624	-2.660	135	R10	2.660	-3.968	182	SEG12	3.624	2.660
42	SEG60	-2.850	3.968	89	V_{C1}	-3.624	-2.830	136	R11	2.850	-3.968	183	SEG13	3.624	2.830
43	SEG61	-3.040	3.968	90	OSC3	-3.624	-3.020	137	R12	3.040	-3.968	184	SEG14	3.624	3.020
44	SEG62	-3.240	3.968	91	OSC4	-3.624	-3.210	138	R13	3.240	-3.968	185	SEG15	3.624	3.210
45	SEG63	-3.450	3.968	92	V_{D1}	-3.624	-3.400	139	R14	3.450	-3.968	186	SEG16	3.624	3.400
46	SEG64	-3.624	3.810	93	V_{DD}	-3.624	-3.600	140	R15	3.624	-3.810	187	SEG17	3.624	3.600
47	SEG65	-3.624	3.600	94	V_{SS}	-3.624	-3.810	141	R16	3.624	-3.600	188	SEG18	3.624	3.810

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
R_{CR3}	Feedback resistor	50 kΩ *1
C_{G1}	Trimmer capacitor	5–25 pF *2
C1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C7–C9	Booster capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF
R1	Load resistor between V_{SS} and V_{C1}	100 kΩ (It is needed when driving an LCD panel that constitutes a heavy load.)

∗1 The CR oscillation frequency changes depending on conditions such as board pattern and elements used. 50 kΩ is only for reference, so select the resistance according to the evaluation using the actual product.

∗2 C_{G1} = 5–20 pF (including board capacitance) when f_{OSC1} is 153.6 kHz.

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