EPSON

E0C88409

8-bit Single Chip Microcomputer

- Original Architecture Core CPU
- Low Voltage Operation (1.8V min.)
- High Speed Operation (0.48µsec/3.0V)
- Built-in LCD Controller
- Built-in Touch Panel Controller
- Built-in 10bit A/D Converter

■ DESCRIPTION

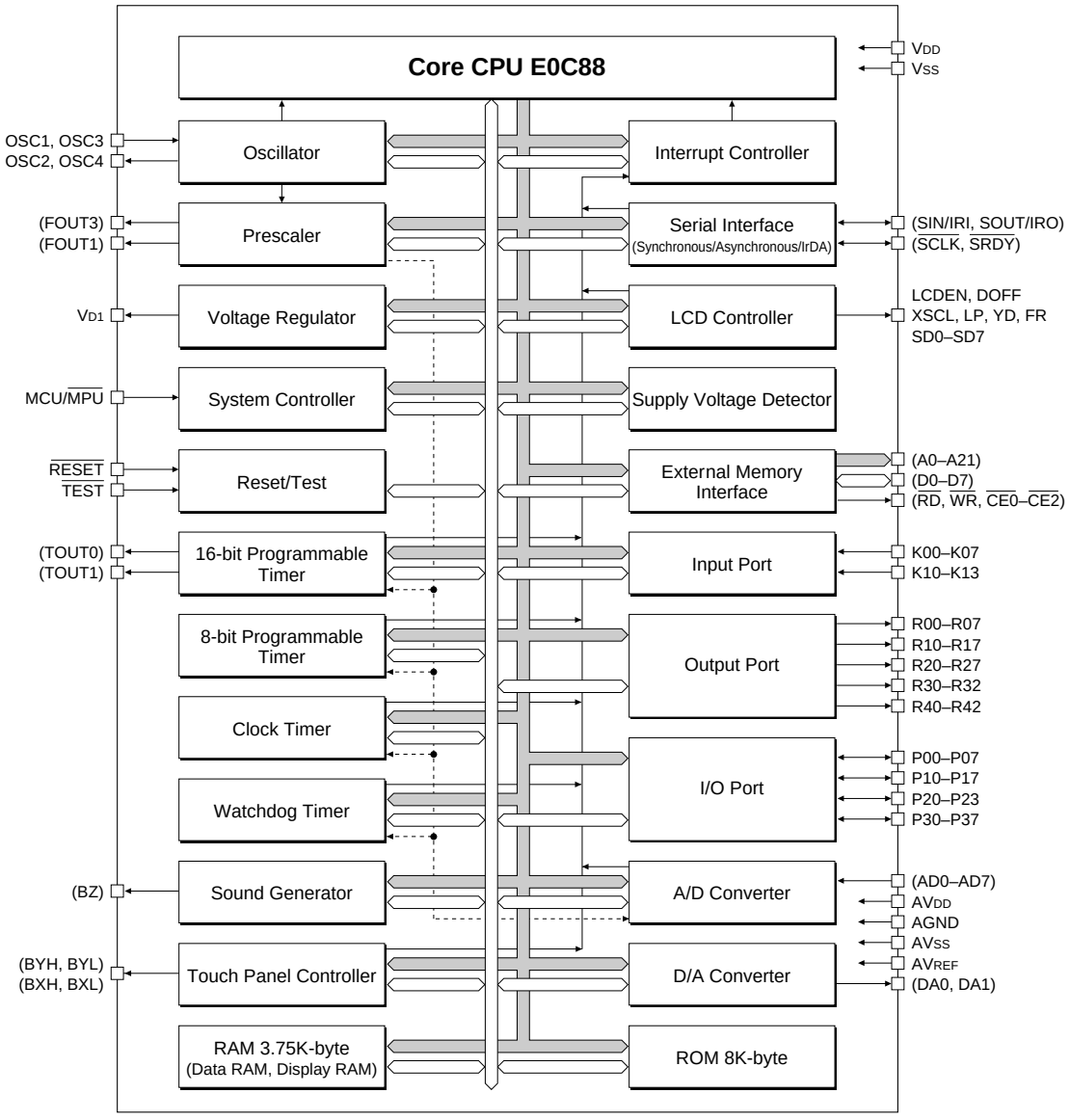
The E0C88409 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, LCD controller, Display RAM, A/D converter and touch key controller. So that the E0C88409 can drive mid size LCD panel (for example, 160 × 100 dots), with A/D touch key. The LCD controller supports 4 gray scale display. The E0C88409 also has A/D converter and touch panel controller, so that it is easy to detect coordinates on touch panel. The E0C88409 is suitable for organizer and educational computer with mid size display and touch panel.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Clock ..... Twin clock system Low-speed clock: 32.768kHz
  High-speed clock: 4.4MHz (2.6V) / 8.8MHz (4.5V)
- Instruction execution time ..... 0.24µsec (Min.)
- Multiplication and division instructions included
- ROM capacity ..... 8K × 8 bits
- RAM capacity ..... 3.75K × 8 bits (Can be chosen as data RAM or display RAM by option swich)
- Addressing ..... 4M-byte (22 bits)
  Address bus: 22-bit ROM addressing, 22-bit RAM addressing
  (Can be used as general output ports when the address bus is not used.)
  Data bus : 8 bits
  (Can be used as general I/O ports when the data bus is not used.)
  $\overline{CE}$ signal : 3 bits
  $\overline{WR}$ signal : 1 bit
  $\overline{RD}$ signal : 1 bit
  (Can be used as general output ports when the control signals are not used.)
- I/O port ..... Input only : 12 bits (EXCL0 or EXCL1 is available by software)
  Output only : 30 bits (BZ, FOUT and TOUT are available by software)
  Bidirectional I/O : 26 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN and SOUT are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software, available for IrDA protocol)
- LCD controller ..... Dot-matrix type (size programmable) controller built-in
  LCD function can be implemented with external segment driver (SED1606 or SED1570) common driver (SED1635)
- A/D converter ..... 10 bits × 8 channels
- D/A converter ..... 8 bits × 2 channels
- Touch panel controller ..... Built-in
- Supply voltage detection (SVD) circuit .... 3 levels (1.9, 2.8, 3.4V) can be detected
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  8-bit programmable for SIO baud rate generator
  Time base counter : 1 channel (Include 60 seconds)

- Watchdog timer ..... Generates NMI
- Sound generator ..... 8 levels, with envelope, volume adjustment and 1 shot functions
- Interrupt ..... External : 2 systems
  Internal : 4 systems
- Supply voltage ..... 1.8V to 5.5V
- Current consumption ..... SLEEP mode 500nA (3V)
  HALT mode 3µA (32.768kHz/3V)
  RUN mode 15µA (32.768kHz/3V)
  2mA (8.2MHz/3.5V)
- Package ..... Die form or QFP15-100pin

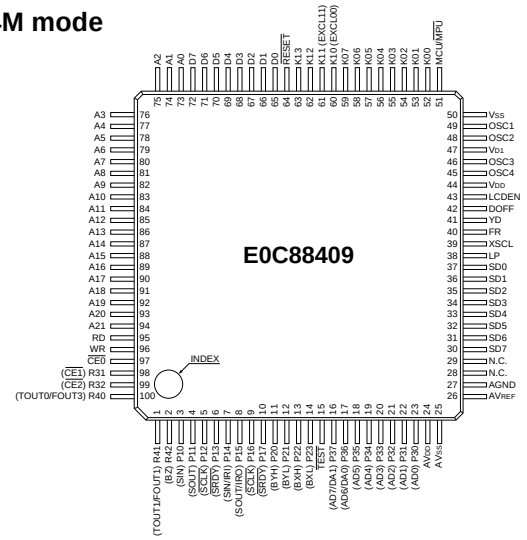
■ BLOCK DIAGRAM



* The terminals that are shown in ( ) are shared with Pxx or Rxx terminals.

■ PIN CONFIGURATION

• Pin layout for expanded 4M mode (for multi-chip system)



■ PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
V_{DD}	44	–	Power supply (+) pin
V_{SS}	50	–	Power supply (GND) pin
V_{D1}	47	O	Voltage regulator output pin
AV_{DD}	24	–	Power supply (+) pin for analog circuit system
AGND	27	–	GND pin for analog circuit system
AV_{SS}	25	–	Power supply (GND) pin for analog circuit system
AV_{REF}	26	I	Reference voltage input pin for analog circuit system
OSC1	49	I	OSC1 oscillation input pin (32 kHz crystal, CR oscillation, external clock input)
OSC2	48	O	OSC1 oscillation output pin
OSC3	46	I	OSC3 oscillation input pin (crystal/ceramic, CR oscillation, external clock input)
OSC4	45	O	OSC3 oscillation output pin
MCU/$\overline{MPU}$	51	I	MCU/MPU mode stting pin
K00~K07	52~59	I	Input port pin
K10 (EXCL00)	60	I	Input port pin or external clock input pin for event counter (Timer 0)
K11 (EXCL01)	61	I	Input port pin or external clock input pin for event counter (Timer 1)
K12~K13	62~63	I	Input port pin
A00~A21	73~94	O	Address bus
$\overline{RD}$	95	O	Read signal output pin
$\overline{WR}$	96	O	Write signal output pin
$\overline{CE0}$	97	O	Chip enable signal output pin
$\overline{CE1}$ (R31)	98	O	Chip enable signal output pin or output port pin
$\overline{CE2}$ (R32)	99	O	Chip enable signal output pin or output port pin
R40 (TOUT0/FOUT3)	100	O	Output port pin or TOUT0/FOUT3 clock output pin
R41 (TOUT1/FOUT1)	1	O	Output port pin or TOUT1/FOUT1 clock output pin
R42 (BZ)	2	O	Output port pin or buzzer signal output pin
D0~D7	65~72	I/O	Data bus
P10 (SIN)	3	I/O	I/O port pin or serial I/F data input pin
P11 (SOUT)	4	I/O	I/O port pin or serial I/F data output pin
P12 ($\overline{SCLK}$)	5	I/O	I/O port pin or serial I/F clock input/output pin
P13 ($\overline{SRDY}$)	6	I/O	I/O port pin or serial I/F ready signal output pin
P14 (SIN/IRI)	7	I/O	I/O port pin, serial I/F data input or IR receiver input pin
P15 (SOUT/IRO)	8	I/O	I/O port pin, serial I/F data output or IR transmitter output pin
P16 ($\overline{SCLK}$)	9	I/O	I/O port pin or serial I/F clock input/output pin
P17 ($\overline{SRDY}$)	10	I/O	I/O port pin or serial I/F ready signal output pin
P20 (BYH)	11	I/O	I/O port pin or touch panel controller BYH signal output pin
P21 (BYL)	12	I/O	I/O port pin or touch panel controller BYL signal output pin
P22 (BXH)	13	I/O	I/O port pin or touch panel controller BXH signal output pin
P23 (BXL)	14	I/O	I/O port pin or touch panel controller BXL signal output pin
P30~P35 (AD0~AD5)	23~18	I/O	I/O port pin or A/D converter analog signal input pin
P36, P37 (AD6/DA0, AD7/DA1)	17,16	I/O	I/O port pin, A/D converter analog signal input pin or D/A converter analog signal output pin
LCDEN	43	O	LCD controller enable signal output pin
DOFF	42	O	LCD controller forced blank signal output pin
YD	41	O	LCD controller scan start pulse output pin
FR	40	O	LCD controller frame signal output pin
XSCL	39	O	LCD controller shift clock output pin
LP	38	O	LCD controller latch pulse output pin
SD0~SD7	37~30	O	LCD controller data output pin
$\overline{RESET}$	64	I	Initial reset input pin
$\overline{TEST}$	15	I	Test input pin*1

*1 $\overline{TEST}$ is the terminal used for factory inspection of the IC. For normal operation, be sure to connect the $\overline{TEST}$ terminal to V_{DD}.

(Note) The pin configuration is different from that of single-chip mode or expanded 64K mode. Please refer to the technical manual before designing the system.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0 V)

Rating	Symbol	Condition	Value	Unit	Note
Supply voltage	V_{DD}		-0.3 to +7.0	V	
Analog supply voltage	AV_{DD}		-0.3 to +7.0	V	
Reference supply voltage	AV_{REF}		-0.3 to AV_{DD}+0.3	V	
Input voltage	V_I		-0.3 to V_{DD}+0.3	V	
Output voltage	V_O		-0.3 to V_{DD}+0.3	V	
High-level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low-level output current	I_{OL}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Operating temperature	Topr		-20 to +70	°C	
Storage temperature	Tstg		-65 to +150	°C	
Permissible disspation	P_D	Ta=25°C	200	mW	1

Note) 1. In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=0 V)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}		1.8		5.5	V	
Analog supply voltage	AV_{DD}	AV_{DD}≥2.7 V	V_{DD}-0.05		V_{DD}+0.05	V	
Clock frequency	f_{OSC1}	V_{DD}=1.8 to 5.5 V	30.000	32.768	50.000	kHz	1
	f_{OSC3}	V_{DD}=1.8 to 5.5 V	0.03		1.1	MHz	1
		V_{DD}=2.6 to 5.5 V	0.03		4.4	MHz	1
		V_{DD}=3.5 to 5.5 V	0.03		6.6	MHz	1
		V_{DD}=4.5 to 5.5 V	0.03		8.8	MHz	1
Operating temperature	Topr		-20		+70	°C	
Capacitor between V_{SS} and V_{D1}	C_1			0.1		µF	

Note) 1. When an external clock is input from the OSC1 terminal by setting the mask option, do not connect anything to the OSC2 terminal. When an external clock is input from the OSC3 terminal, do not connect anything to the OSC4 terminal.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=-20 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High-level input voltage	V_{IH1}	Pxx, MCU/$\overline{MPU}$, Kxx	0.8V_{DD}		V_{DD}	V	
Low-level input voltage	V_{IL1}	Pxx, MCU/$\overline{MPU}$, Kxx	0		0.2V_{DD}	V	
High-level input voltage	V_{IH2}	OSC1, OSC3, V_{D1} = 1.6V	1.3		V_{DD}	V	1,3
		OSC1, OSC3, V_{D1} = 2.4V	1.8		V_{DD}	V	1,4
		OSC1, OSC3, V_{D1} = 3.2V	2.4		V_{DD}	V	1,5
		OSC1, OSC3, V_{D1} = 4.2V	3.2		V_{DD}	V	1,6
Low-level input voltage	V_{IL2}	OSC1, OSC3, V_{D1} = 1.6V	0		0.3	V	1,3
		OSC1, OSC3, V_{D1} = 2.4V	0		0.6	V	1,4
		OSC1, OSC3, V_{D1} = 3.2V	0		0.8	V	1,5
		OSC1, OSC3, V_{D1} = 4.2V	0		1.0	V	1,6
High-level schmitt trigger input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low-level schmitt trigger input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
Schmitt trigger hysteresis voltage	V_{HS}	$\overline{RESET}$, $V_{HS}=V_{T+}-V_{T-}$	0.2			V	
High-level output current	I_{OH}	Pxx, Rxx, $V_{OH}=V_{DD}$-0.2 V	-0.5			mA	7
Low-level output current	I_{OL}	Pxx, Rxx, V_{OL}=0.2 V			0.5	mA	7
Input leak current	I_{LI1}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	-1		1	µA	
Input leak current	I_{LI2}	OSC1, OSC3	-1		1	µA	1
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, MCU/$\overline{MPU}$, $\overline{RESET}$	100		500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN}=0 V, ϕ=1 MHz, Ta=25°C			15	pF	

Note) 1. When external clock is selected by mask option.
2. When pull-up resistor is added by mask option.
3. Low-power mode (VD1C1 = "0", VD1C0 = "1")
4. Normal mode (VD1C1 = "0", VD1C0 = "0")
5. High-speed mode 1 (VD1C1 = "1", VD1C0 = "0")
6. High-speed mode 2 (VD1C1 = "1", VD1C0 = "1")
7. Characteristics when only one terminal is driven. If two or more terminals are driven simultaneously, the characteristics had happen to reduced because the V_{OH} and V_{OL} voltages drop due to the parasitic resistance on the power line in the IC.

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=1.8 to 5.5 V, V_{SS}=0 V, Ta=25°C, OSC1=32.768 kHz crystal oscillation, OSC3=external clock input)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	SVD1="1", SVD0=X	3.05	3.4	3.75	V	
		SVD1="0", SVD0="1"	2.55	2.8	3.05	V	
		SVD1="0", SVD0="0"	1.7	1.9	2.1	V	
SVD circuit response time	t_{SVD}				100	µs	
Power current	I_{DD1}	In SLEEP status		0.45	1.0	µA	1
Low-power mode	I_{DD2}	In HALT status		1.8	5.0	µA	2
VD1C1="0", VD1C0="1"	I_{DD3}	CPU is in operating (32.768 kHz)		9.0	20.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.3	0.5	mA	4
Power current	I_{DD1}	In SLEEP status		0.55	1.5	µA	1
Normal mode	I_{DD2}	In HALT status		3.0	7.0	µA	2
VD1C1="0", VD1C0="0"	I_{DD3}	CPU is in operating (32.768 kHz)		14.0	25.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.45	0.7	mA	4
Power current	I_{DD1}	In SLEEP status		0.65	2.0	µA	1
High-speed mode 1	I_{DD2}	In HALT status		5.0	12.0	µA	2
VD1C1="1", VD1C0="0"	I_{DD3}	CPU is in operating (32.768 kHz)		21.0	35.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.65	1.0	mA	4
Power current	I_{DD1}	In SLEEP status		0.75	3.0	µA	1
High-speed mode 2	I_{DD2}	In HALT status		9.0	20.0	µA	2
VD1C1="1", VD1C0="1"	I_{DD3}	CPU is in operating (32.768 kHz)		32.0	50.0	µA	3
	I_{DD4}	CPU is in operating (1 MHz)		0.9	1.4	mA	4
SVD circuit current	I_{SVDN}	V_{DD}=5.0 V		7	15	µA	5
OSC1 CR oscillation current	I_{CR1}	R_{CR}=1.5MΩ, normal mode		20	50	µA	6

Note) 1. OSC1: Stop OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Stop SVD: Off Others: Stop
2. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: Off Others: Stop
3. OSC1: On OSC3: Stop CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
4. OSC1: On OSC3: On CPU, ROM, RAM: Run Clock Timer: Run SVD: Off Others: Stop
5. OSC1: On OSC3: Stop CPU, ROM, RAM: Stop Clock Timer: Run SVD: On Others: Stop
6. When the OSC1 CR oscillation circuit is selected by mask option.

● D/A Converter Characteristics

(Unless otherwise specified: V_{DD}=AV_{DD}=AV_{REF}=5.0 V, V_{SS}=AV_{SS}=AGND=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=1.0 MHz, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
D/A conversion speed	t_{DA}	V_{DD}=AV_{DD}=AV_{REF}=V_{D1}=5.5 V Load capacitance=parasitic capacitance only	–	–	10	µs	
		V_{DD}=AV_{DD}=AV_{REF}=V_{D1}=5.5 V Load capacitance=100 pF+parasitic capacitance	–	–	30	µs	
Integral linearity error	E_{IDA}	V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=3.0 V, I_L=1 µA, Ta=-20 to 70°C	-2.0	–	+2.0	LSB	1
		V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=5.0 V, I_L=1 µA, Ta=-20 to 70°C	-2.0	–	+2.0	LSB	1
Differential linearity error	E_{dDA}	V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=3.0 V, I_L=1 µA, Ta=-20 to 70°C	-1.5	–	+1.5	LSB	2
		V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=5.0 V, I_L=1 µA, Ta=-20 to 70°C	-1.5	–	+1.5	LSB	2
Total error	E_{tDA}	V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=3.0V, I_L=1µA, Ta=-20 to 70°C	-2.5	–	+2.5	LSB	3
		V_{DD}=AV_{DD}=V_{D1}=AV_{REF}=5.0V, I_L=1µA, Ta=-20 to 70°C	-2.5	–	+2.5	LSB	3
D/A converter current consumption	I_{DA}	V_{DD}=AV_{DD}=AV_{REF}=3.0V, Ta=25°C, 55H output Reference resistor current not included	–	0.35	1	mA	
		V_{DD}=AV_{DD}=AV_{REF}=5.5V, Ta=25°C, 55H output Reference resistor current not included	–	0.7	2	mA	

∗ Integral linearity error: E_{IDA} = difference between the real conversion characteristic and the end point line
∗ Differential linearity error: E_{dDA} = difference between the real step width and the ideal step width
∗ Total error: E_{tDA} = max(Ezs, Efs, Eabs)
Eabs = deviation from the ideal line (including quantization error)
Ezs = deviation from the ideal value at zero point (zero-scale error)
Efs = deviation from the ideal value at the full scale point (full-scale error)

Note) 1. ±2.5 LSB when chip is used.
2. ±2.0 LSB when chip is used.
3. ±3.0 LSB when chip is used.

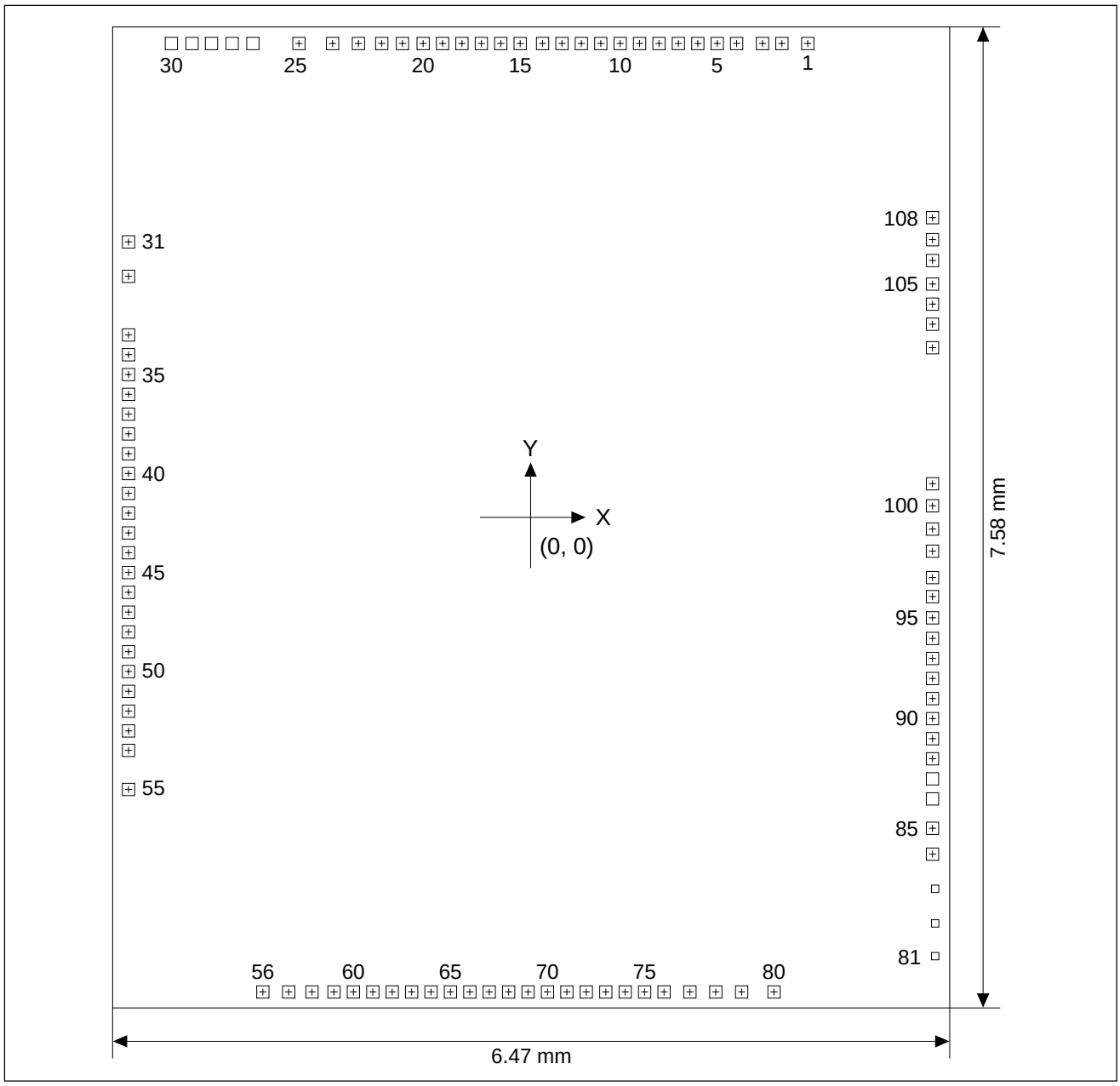
● A/D Converter Characteristics

(Unless otherwise specified: V_{DD}=AV_{DD}=AV_{REF}=5.0 V, V_{SS}=AV_{SS}=AGND=0 V, f_{OSC1}=32.768 kHz, f_{OSC3}=4.0 MHz, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Zero-scale error	Ezs	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5V, AV_{SS}=0V, ADCLK=2MHz, Ta=25°C	-3.0	–	+3.0	LSB	
Full-scale error	Efs		-3.0	–	+3.0	LSB	
Non-linearity error	El		-3.0	–	+3.0	LSB	
Total error	Et		-3.5	–	+3.5	LSB	
A/D converter current consumption	I_{AD}	V_{DD}=AV_{DD}=AV_{REF}=3.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included	–	0.50	1.00	mA	
		V_{DD}=AV_{DD}=AV_{REF}=5.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included	–	1.80	3.50	mA	
Input clock frequency	f	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5 V, Ta=25°C	–	2	4	MHz	

∗ Zero-scale error: Ezs = deviation from the ideal value at zero point
∗ Full-scale error: Efs = deviation from the ideal value at the full scale point
∗ Non-linearity error: El = deviation of the real conversion curve from the end point line
∗ Total error: Et = max(Ezs, Efs, Eabs), Eabs = deviation from the ideal line (including quantization error)

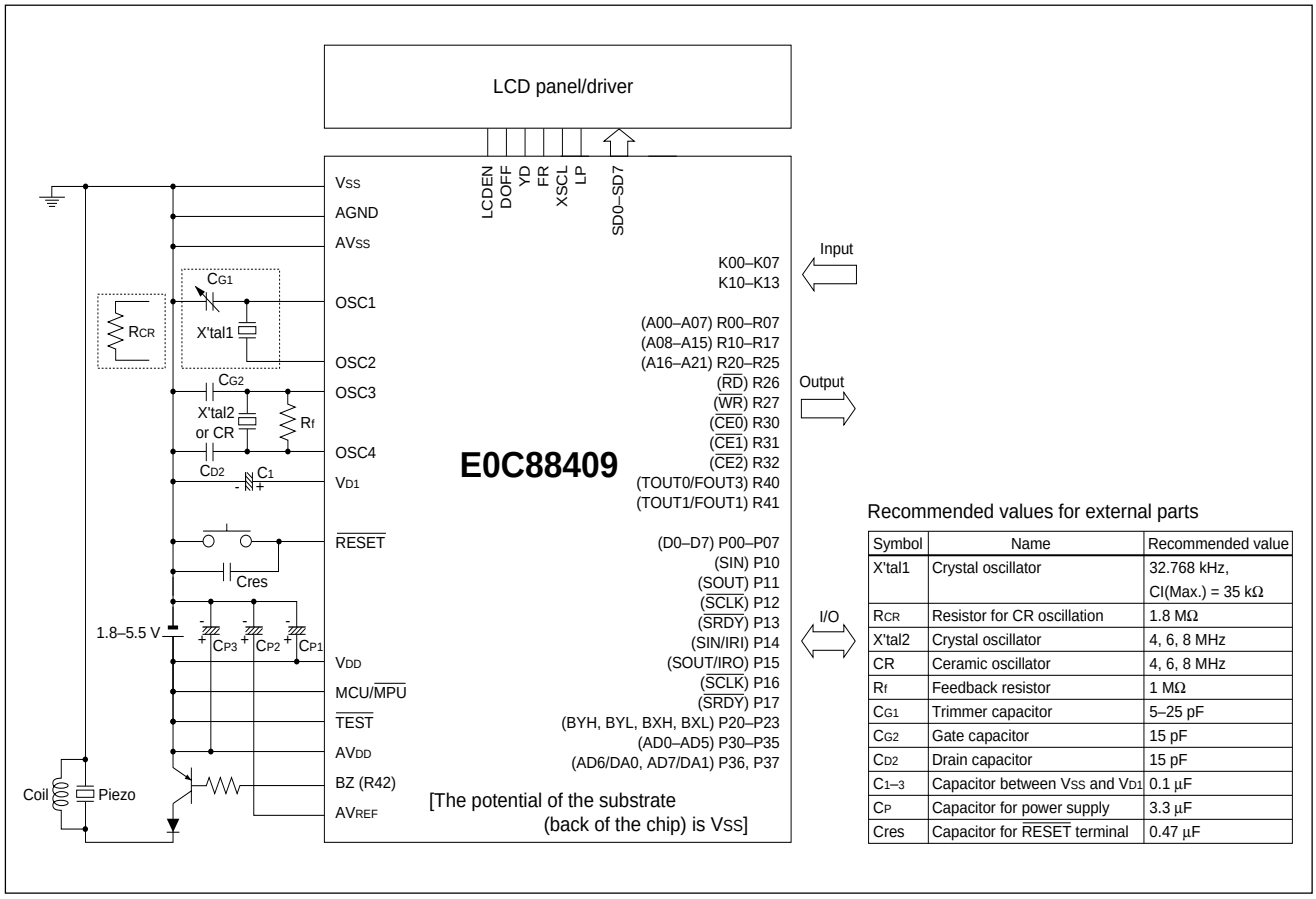
■ DIAGRAM OF PAD LAYOUT



■ PAD COORDINATES

No.	Pad name	X	Y	No.	Pad name	X	Y
1	MCU/$\overline{\text{MPU}}$	2,143	3,664	55	R40/TOUT0/FOUT3	-3,107	-2,100
2	K00	1,943	3,664	56	R41/TOUT1/FOUT1	-2,069	-3,665
3	K01	1,793	3,664	57	R42/BZ	-1,869	-3,665
4	K02	1,593	3,664	58	P10/SIN	-1,689	-3,665
5	K03	1,443	3,664	59	P11/SOUT	-1,519	-3,665
6	K04	1,293	3,664	60	P12/$\overline{\text{SCLK}}$	-1,369	-3,665
7	K05	1,143	3,664	61	P13/$\overline{\text{SRDY}}$	-1,219	-3,665
8	K06	993	3,664	62	P14/SIN/IRI	-1,069	-3,665
9	K07	843	3,664	63	P15/SOUT/IRO	-919	-3,665
10	K10/EXCL00	693	3,664	64	P16/$\overline{\text{SCLK}}$	-769	-3,665
11	K11/EXCL11	543	3,664	65	P17/$\overline{\text{SRDY}}$	-619	-3,665
12	K12	393	3,664	66	P20/BYH	-469	-3,665
13	K13	243	3,664	67	P21/BYL	-319	-3,665
14	$\overline{\text{RESET}}$	93	3,664	68	P22/BXH	-169	-3,665
15	P00/D0	-80	3,664	69	P23/BXL	-19	-3,665
16	P01/D1	-230	3,664	70	$\overline{\text{TEST}}$	131	-3,665
17	P02/D2	-380	3,664	71	P37/AD7/DA1	281	-3,665
18	P03/D3	-530	3,664	72	P36/AD6/DA0	431	-3,665
19	P04/D4	-680	3,664	73	P35/AD5	582	-3,665
20	P05/D5	-830	3,664	74	P34/AD4	732	-3,665
21	P06/D6	-990	3,664	75	P33/AD3	882	-3,665
22	P07/D7	-1,150	3,664	76	P32/AD2	1,032	-3,665
23	R00/A0	-1,330	3,664	77	P31/AD1	1,232	-3,665
24	R01/A1	-1,530	3,664	78	P30/AD0	1,432	-3,665
25	R02/A2	-1,790	3,664	79	AV_{DD}	1,632	-3,665
26	N.C.	-2,146	3,664	80	AV_{SS}	1,882	-3,665
27	N.C.	-2,306	3,664	81	N.C.	3,127	-3,390
28	N.C.	-2,466	3,664	82	N.C.	3,127	-3,137
29	N.C.	-2,616	3,664	83	N.C.	3,127	-2,870
30	N.C.	-2,776	3,664	84	AV_{REF}	3,107	-2,600
31	R03/A3	-3,107	2,131	85	AGND	3,107	-2,400
32	R04/A4	-3,107	1,865	86	N.C.	3,107	-2,173
33	R05/A5	-3,107	1,412	87	N.C.	3,107	-2,018
34	R06/A6	-3,107	1,259	88	SD7	3,107	-1,863
35	R07/A7	-3,107	1,106	89	SD6	3,107	-1,708
36	R10/A8	-3,107	953	90	SD5	3,107	-1,553
37	R11/A9	-3,107	800	91	SD4	3,107	-1,398
38	R12/A10	-3,107	647	92	SD3	3,107	-1,243
39	R13/A11	-3,107	494	93	SD2	3,107	-1,088
40	R14/A12	-3,107	341	94	SD1	3,107	-933
41	R15/A13	-3,107	188	95	SD0	3,107	-774
42	R16/A14	-3,107	35	96	LP	3,107	-610
43	R17/A15	-3,107	-118	97	XSCL	3,107	-463
44	R20/A16	-3,107	-271	98	FR	3,107	-259
45	R21/A17	-3,107	-424	99	YD	3,107	-88
46	R22/A18	-3,107	-577	100	DOFF	3,107	92
47	R23/A19	-3,107	-730	101	LCDEN	3,107	262
48	R24/A20	-3,107	-883	102	V_{DD}	3,107	1,313
49	R25/A21	-3,107	-1,036	103	OSC4	3,107	1,495
50	R26/$\overline{\text{RD}}$	-3,107	-1,189	104	OSC3	3,107	1,650
51	R27/$\overline{\text{WR}}$	-3,107	-1,342	105	V_{D1}	3,107	1,805
52	R30/$\overline{\text{CE0}}$	-3,107	-1,495	106	OSC2	3,107	1,987
53	R31/$\overline{\text{CE1}}$	-3,107	-1,648	107	OSC1	3,107	2,148
54	R32/$\overline{\text{CE2}}$	-3,107	-1,798	108	V_{SS}	3,107	2,318

■ BASIC EXTERNAL CONNECTION DIAGRAM



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.) = 35 kΩ
R_{CR}	Resistor for CR oscillation	1.8 MΩ
X'tal2	Crystal oscillator	4, 6, 8 MHz
CR	Ceramic oscillator	4, 6, 8 MHz
R_f	Feedback resistor	1 MΩ
C_{G1}	Trimmer capacitor	5–25 pF
C_{G2}	Gate capacitor	15 pF
C_{D2}	Drain capacitor	15 pF
$C_{1–3}$	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION
IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : 042-587-5814 FAX : 042-587-5110

ENERGY SAVING EPSON