EPSON

E0C88832

8-bit Single Chip Microcomputer

Low Voltage Operation Products

- Original Architecture Core CPU
- Low Current Consumption
- Wide-range Operating Voltage (1.8V to 5.5V)
- High Speed Operation in Low Voltage (0.48µsec/3.0V)

■ DESCRIPTION

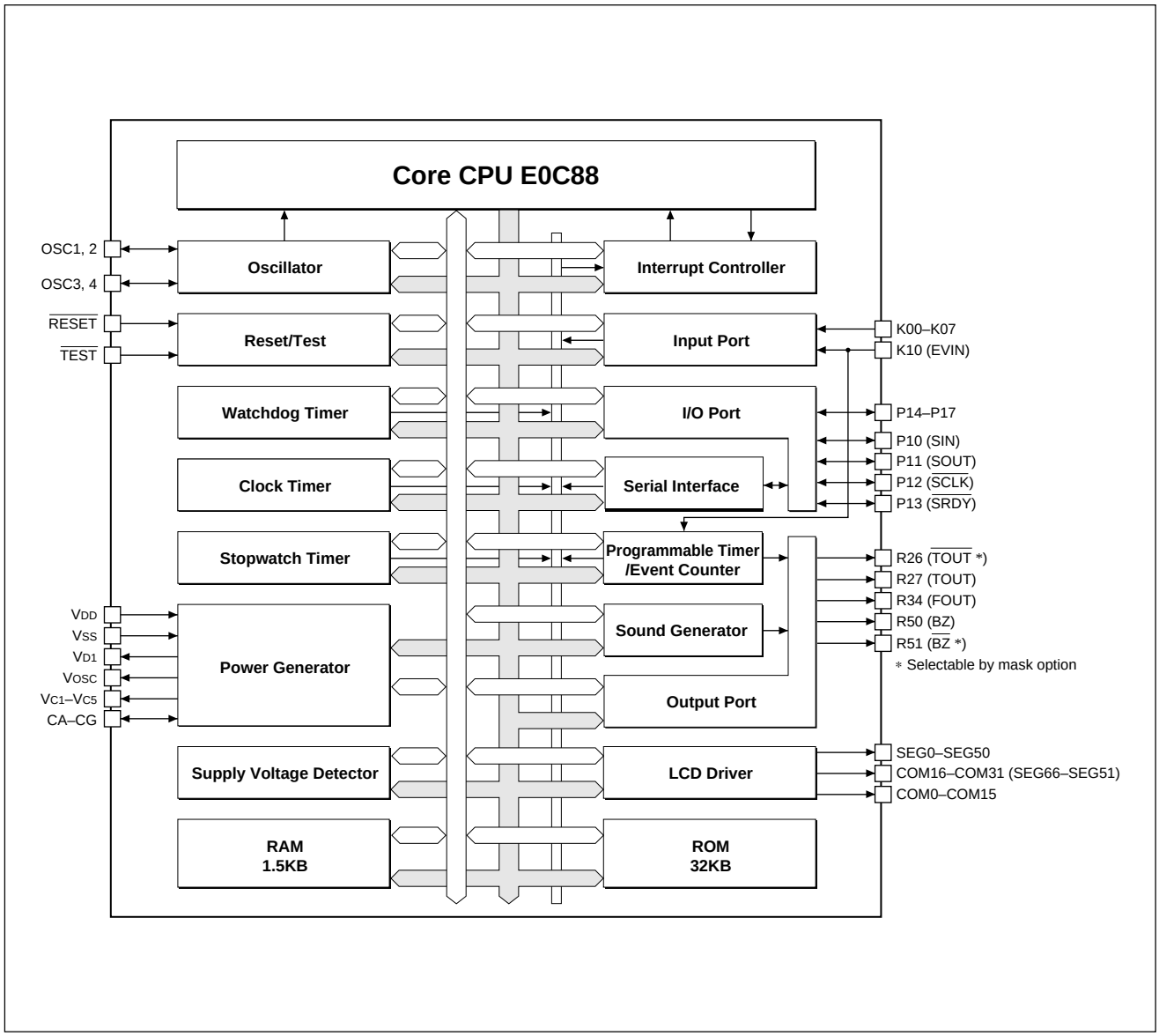
The E0C88832 is a CMOS 8-bit microcomputer composed of a CMOS 8-bit core CPU, ROM, RAM, I/O, serial interface, dot-matrix LCD driver, timer and event counter. The E0C88832 fully operable over a wide range of voltages, and can perform high speed operations even at low voltage and low current consumption, it is suitable for portable systems that need to be driven with a battery.

■ FEATURES

- CMOS LSI 8-bit parallel processing
- Twin clock ..... OSC1 : 32.768kHz (Typ.)
  OSC3 : 8.2MHz (Max.)
- Instruction execution time ..... 0.244µsec (Min.)
- Multiplication and division instructions included
- ROM capacity 32K-byte
- RAM capacity ..... 1.5K-byte (RAM)
  3,216 (Display RAM)
- I/O port ..... Input only : 9 bits (EVIN is available by software)
  Output only : 5 bits (BZ, $\overline{BZ}$, TOUT, $\overline{TOUT}$ and FOUT are available by software)
  Bidirectional I/O : 8 bits ($\overline{SRDY}$, $\overline{SCLK}$, SIN and SOUT are available by software)
- Serial interface ..... 1 channel (Clock synchronous or Asynchronous can be selected by software)
- Power supply circuit to drive liquid crystals .. Built-in (booster type, 5 potentials)
- LCD driver ..... Dot-matrix type (5 × 8 or 5 × 5)
  51 segments × 32 commons (1/5 bias)
  67 segments × 16 commons (1/5 bias)
  67 segments × 8 commons (1/5 bias)
- Timer ..... 8-bit programmable timer/event counter : 2 channels
  (16-bit 1 channel timer is available)
  Clock timer (8 bits) : 1 channel
  Stopwatch timer (8 bits) : 1 channel
- Sound generator ..... Envelope function, equipped with volume control
- Watchdog timer ..... Built-in
- Supply voltage detection (SVD) circuit .... 16 levels can be detected
- Interrupt ..... External : Input interrupt 2 systems (3 types)
  Internal : Timer interrupt 3 systems (9 types)
  : Serial I/F interrupt 1 system (3 types)

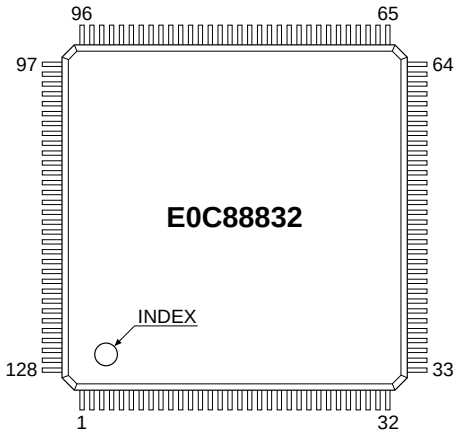
- Supply voltage ..... Normal mode : 2.4V to 5.5V (Max. 4.2MHz)
  Low power mode : 1.8V to 3.5V (Max. 80kHz)
  High speed mode : 3.5V to 5.5V (Max. 8.2MHz)
- Current consumption ..... SLEEP mode 0.3µA (Normal mode)
  HALT mode 2µA (32.768kHz/Normal mode)
  RUN mode 10µA (32.768kHz/Normal mode)
  1.3mA (4.9152MHz/Normal mode)
- Package ..... QFP8-128pin (plastic), QFP15-128pin (plastic)

■ BLOCK DIAGRAM

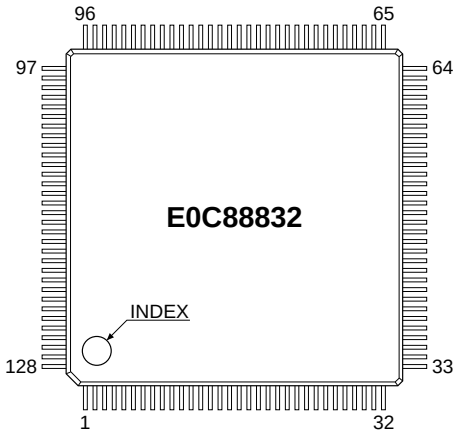


■ PIN CONFIGURATION

QFP8-128pin



QFP15-128pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	COM19/SEG63	33	OSC3	65	N.C.	97	SEG31
2	COM18/SEG64	34	OSC4	66	SEG0	98	SEG32
3	COM17/SEG65	35	V_{OSC}	67	SEG1	99	SEG33
4	COM16/SEG66	36	V_{D1}	68	SEG2	100	SEG34
5	COM15	37	V_{DD}	69	SEG3	101	SEG35
6	COM14	38	V_{SS}	70	SEG4	102	SEG36
7	COM13	39	OSC1	71	SEG5	103	SEG37
8	COM12	40	OSC2	72	SEG6	104	SEG38
9	COM11	41	$\overline{TEST}$	73	SEG7	105	SEG39
10	COM10	42	$\overline{RESET}$	74	SEG8	106	SEG40
11	COM9	43	K10/EVIN	75	SEG9	107	SEG41
12	COM8	44	K07	76	SEG10	108	SEG42
13	COM7	45	K06	77	SEG11	109	SEG43
14	COM6	46	K05	78	SEG12	110	SEG44
15	COM5	47	K04	79	SEG13	111	SEG45
16	COM4	48	K03	80	SEG14	112	SEG46
17	COM3	49	K02	81	SEG15	113	SEG47
18	COM2	50	K01	82	SEG16	114	SEG48
19	COM1	51	K00	83	SEG17	115	SEG49
20	COM0	52	P17	84	SEG18	116	SEG50
21	CG	53	P16	85	SEG19	117	COM31/SEG51
22	CF	54	P15	86	SEG20	118	COM30/SEG52
23	CE	55	P14	87	SEG21	119	COM29/SEG53
24	CD	56	P13/$\overline{SRDY}$	88	SEG22	120	COM28/SEG54
25	CC	57	P12/$\overline{SCLK}$	89	SEG23	121	COM27/SEG55
26	CB	58	P11/SOUT	90	SEG24	122	COM26/SEG56
27	CA	59	P10/SIN	91	SEG25	123	COM25/SEG57
28	V_{C5}	60	R26/$\overline{TOUT}$	92	SEG26	124	COM24/SEG58
29	V_{C4}	61	R27/TOUT	93	SEG27	125	COM23/SEG59
30	V_{C3}	62	R34/FOUT	94	SEG28	126	COM22/SEG60
31	V_{C2}	63	R50/BZ	95	SEG29	127	COM21/SEG61
32	V_{C1}	64	R51/$\overline{BZ}$	96	SEG30	128	COM20/SEG62

N.C.: No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	37	–	Power supply (+) terminal
V_{SS}	38	–	Power supply (GND) terminal
V_{D1}	36	–	Regulated voltage for internal circuit
V_{OSC}	35	–	Regulated voltage for OSC1 oscillation circuit
V_{C1}–V_{C5}	32–28	O	LCD drive voltage output terminals
CA–CG	27–21	–	Booster capacitor connection terminals for LCD
OSC1	39	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input with mask option)
OSC2	40	O	OSC1 oscillation output terminal
OSC3	33	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input with mask option)
OSC4	34	O	OSC3 oscillation output terminal
K00–K07	51–44	I	Input terminals (K00–K07)
K10/EVIN	43	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
R26/$\overline{\text{TOUT}}$	60	O	Output terminal (R26) or programmable timer underflow signal inverted output terminal ($\overline{\text{TOUT}}$) (selectable by mask option)
R27/TOUT	61	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R34/FOUT	62	O	Output terminal (R34) or clock output terminal (FOUT)
R50/BZ	63	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BZ}}$	64	O	Output terminal (R51) or buzzer inverted output terminal ($\overline{\text{BZ}}$) (selectable by mask option)
P10/SIN	59	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	58	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	57	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	56	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14–P17	55–52	I/O	I/O terminals (P14–P17)
COM0–COM15	20–5	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	4–1, 128–117	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG50	66–116	O	LCD segment output terminals
$\overline{\text{RESET}}$	42	I	Initial reset input terminal
$\overline{\text{TEST}}$ *1	41	I	Test input terminal

*1 $\overline{\text{TEST}}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Condition	Value	Unit	Note
Power voltage	V_{DD}		-0.3 ~ +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 ~ +7.0	V	
Input voltage	V_I		-0.3 ~ V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 ~ V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 ~ +85	°C	
Storage temperature	Tstg		-65 ~ +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

● Recommended Operating Conditions

(V_{SS}=0V, Ta=-40 to 85°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		3.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Operating frequency	f_{OSC1}	V_{DD} = 2.4 to 5.5V	30.000	32.768	80.000	kHz	1
(Normal mode)	f_{OSC3}		0.03		4.2	MHz	1
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 3.5V	30.000	32.768	80.000	kHz	1
Operating frequency	f_{OSC1}	V_{DD} = 3.5 to 5.5V	30.000	32.768	80.000	kHz	1
(High speed mode)	f_{OSC3}		0.03		8.2	MHz	1
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	2
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3
Capacitor between CF and CG	C_{10}			0.1		µF	3

Note) 1 When an external clock is input from the OSC1 terminal by the mask option, leave the OSC2 terminal open, and when an external clock is input from the OSC3 terminal, leave the OSC4 terminal open.
2 When external power supply is selected by the mask option.
3 When LCD drive power is not used, the capacitor is not necessary. In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC1, OSC3	1.6		V_{DD}	V	1
High level input voltage (2) (Low power mode)	V_{IH2}	OSC1	1.0		V_{DD}	V	1
High level input voltage (2) (High speed mode)	V_{IH2}	OSC1, OSC3	2.4		V_{DD}	V	1
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC1, OSC3	0		0.6	V	1
Low level input voltage (2) (Low power mode)	V_{IL2}	OSC1	0		0.3	V	1
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC1, OSC3	0		0.9	V	1
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	100	300	500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx, V_{IN} = 0V, f = 1MHz, Ta = 25°C		7	15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

Note) 1 When external clock is selected by mask option.
2 When pull-up resistor is added by mask option.

● SVD Circuit

(Unless otherwise specified: V_{DD}=1.8~5.5V, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	1
		Level 2 → Level 1		2.00		V	1
		Level 3 → Level 2		2.18		V	1
		Level 4 → Level 3		2.36		V	2
		Level 5 → Level 4		2.54		V	2
		Level 6 → Level 5		2.72		V	2
		Level 7 → Level 6		2.90		V	3
		Level 8 → Level 7		3.08		V	3
		Level 9 → Level 8		3.26		V	3
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	4
		Level 11 → Level 10		3.65		V	4
		Level 12 → Level 11		3.85		V	4
		Level 13 → Level 12		4.05		V	4
		Level 14 → Level 13		4.25		V	4
		Level 15 → Level 14		4.50		V	4

$V_{SVD\ (Level\ 0)} < V_{SVD\ (Level\ 1)} < V_{SVD\ (Level\ 2)} < V_{SVD\ (Level\ 3)} < V_{SVD\ (Level\ 4)} < V_{SVD\ (Level\ 5)} < V_{SVD\ (Level\ 6)} < V_{SVD\ (Level\ 7)}$
$< V_{SVD\ (Level\ 8)} < V_{SVD\ (Level\ 9)} < V_{SVD\ (Level\ 10)} < V_{SVD\ (Level\ 11)} < V_{SVD\ (Level\ 12)} < V_{SVD\ (Level\ 13)} < V_{SVD\ (Level\ 14)} < V_{SVD\ (Level\ 15)}$

Note) 1 Low power operating mode only
2 Low power operating mode or Normal operating mode only
3 Normal operating mode only
4 Normal operating mode or High speed operating mode only

● Current Consumption

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, OSC1=32.768kHz crystal oscillation, C_G=25pF, OSC3=Crystal/ceramic oscillation, Non heavy load protection mode, C_1 to C_{10}=0.1µF, No panel load)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.3	1	µA	
	I_{DD2}	In HALT status *2		2	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		10	15	µA	
	I_{DD4}	CPU is in operating (4MHz) *4		1.3	1.9	mA	
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.2	1	µA	
	I_{DD2}	In HALT status *2		1	5	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		5	10	µA	
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		5	10	µA	
	I_{DD3}	CPU is in operating (32.768kHz) *3		20	27	µA	
	I_{DD4}	CPU is in operating (8MHz) *5		4.5	6.4	mA	
LCD drive circuit current	I_{LCDN}			2.5	5	µA	1
	I_{LCDH}	In heavy load protection mode		23	30	µA	2
SVD circuit current	I_{SVDN}	V_{DD} = 3.0V		30	60	µA	3
OSC1 CR oscillation current	I_{CR1}	R_{CR1} = 1MΩ		20	60	µA	4

*1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
*2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status
*3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status
*4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 4 MHz, Clock timer: Operating, Others: Stop status
*5 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Operating in 8 MHz, Clock timer: Operating, Others: Stop status

Note) 1 The LCD drive circuit current varies according to the display patterns.
2 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
3 The value in ***x*** V can be found by the following expression: I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 20) - 30 (Typ. value), I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 30) - 30 (Max. value)
4 When OSC1 CR oscillation circuit is selected by the mask option.

● LCD Driver

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number, display pattern). Therefore, these should be evaluated by connecting to the actual panel to be used.

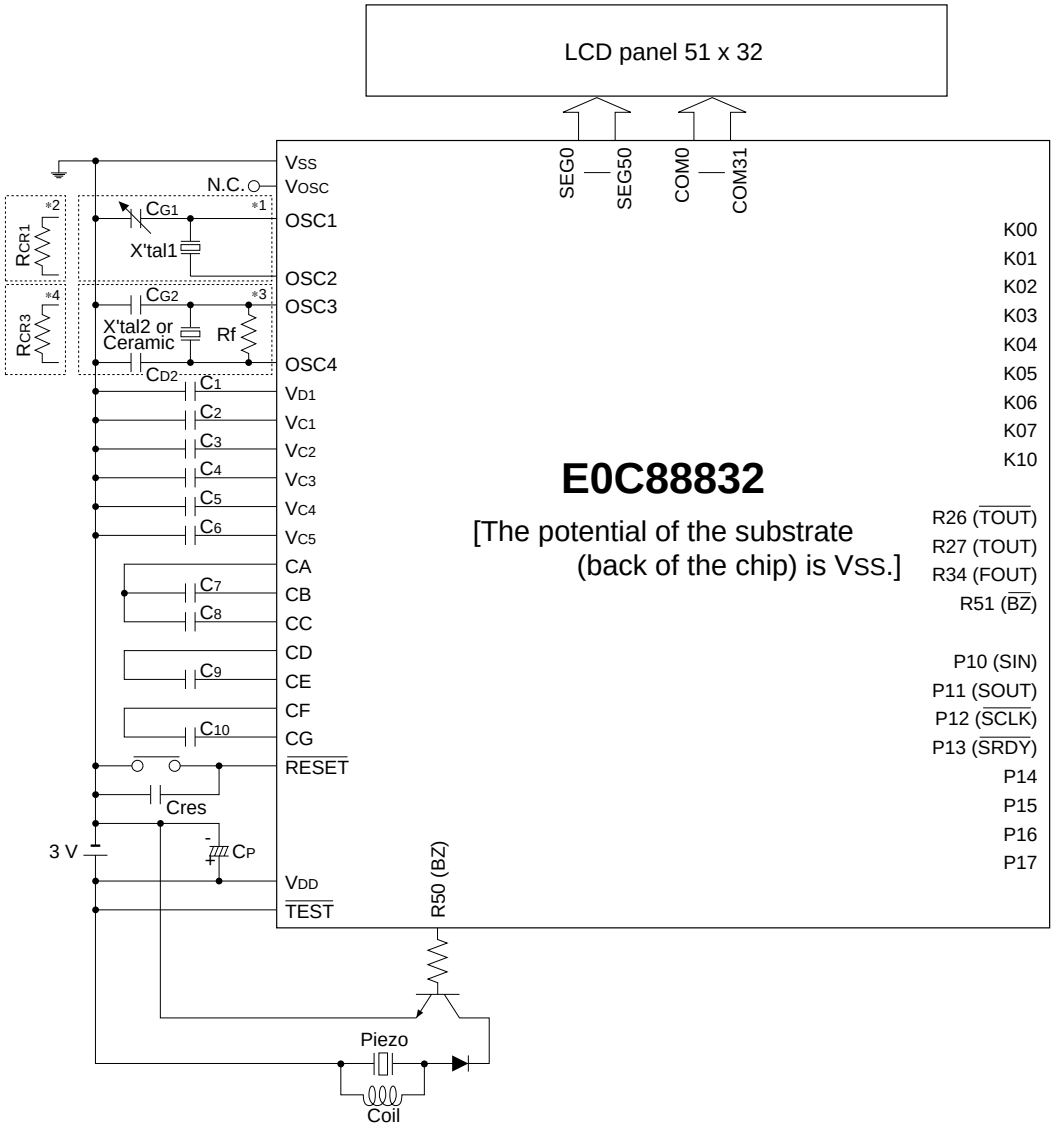
(Unless otherwise specified: V_{DD}=V_{C2} (LCX=FH)+0.1 to 5.5V, V_{SS}=0V, Ta=25°C, C_1 to C_{10}=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C2}	When 1MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.412V_{C5}		V	
	V_{C5} TYPE A (4.5V)	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		3.52		V	1
			LCX = 1H		3.64		V	
			LCX = 2H		3.76		V	
			LCX = 3H		3.88		V	
			LCX = 4H		4.00		V	
			LCX = 5H		4.12		V	
			LCX = 6H	Typ×0.94	4.24	Typ×1.06	V	
			LCX = 7H		4.37		V	
			LCX = 8H		4.51		V	
			LCX = 9H		4.63		V	
			LCX = AH		4.75		V	
			LCX = BH		4.87		V	
			LCX = CH		5.00		V	
			LCX = DH		5.12		V	
			LCX = EH		5.24		V	
			LCX = FH		5.36		V	
	V_{C5} TYPE B (5.5V)	When 1MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H		4.20		V	1
			LCX = 1H		4.34		V	
			LCX = 2H		4.49		V	
			LCX = 3H		4.63		V	
			LCX = 4H		4.78		V	
			LCX = 5H		4.92		V	
			LCX = 6H	Typ×0.94	5.07	Typ×1.06	V	
			LCX = 7H		5.21		V	
			LCX = 8H		5.36		V	
			LCX = 9H		5.50		V	
			LCX = AH		5.65		V	
			LCX = BH		5.80		V	
			LCX = CH		5.94		V	
			LCX = DH		6.09		V	
			LCX = EH		6.23		V	
			LCX = FH		6.38		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

■ BASIC EXTERNAL CONNECTION DIAGRAM

● **When piezoelectric buzzer is driven with single terminal**



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI (Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–25 pF
R_{CR1}	Resistor for CR oscillation	1 MΩ
X'tal2	Crystal oscillator	4.9152 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal osciilation)
		30 pF (Ceramic osciilation)
C_{D2}	Drain capacitor	15 pF (Crystal osciilation)
		30 pF (Ceramic osciilation)

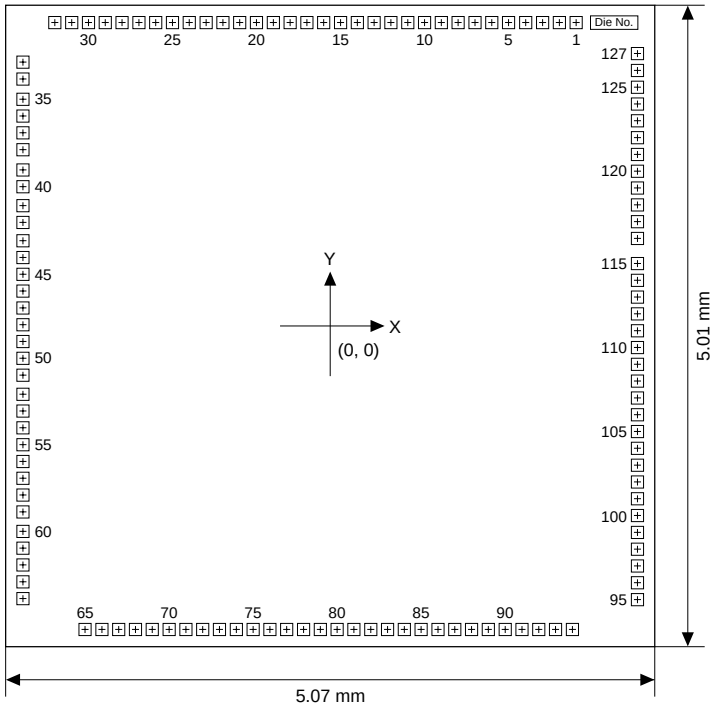
Symbol	Name	Recommended value
R_{CR3}	Resistor for CR oscillation	20 kΩ
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_{10}	Booster/reducer capacitors	0.1 µF
C_P	Capacitor for power supply	3.3 µF
Cres	Capacitor for $\overline{RESET}$ terminal	0.47 µF

∗ The connection diagram shown above is an example of when mask option settings are as follows:
LCD power source: Internal power supply, $\overline{RESET}$ terminal: With pull-up resistor,
R51 specification: General-purpose output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal/Ceramic oscillation, ∗4 OSC3 = CR oscillation

Note: The above table is simply an example, and is not guaranteed to work.

■ DIAGRAM OF PAD LAYOUT



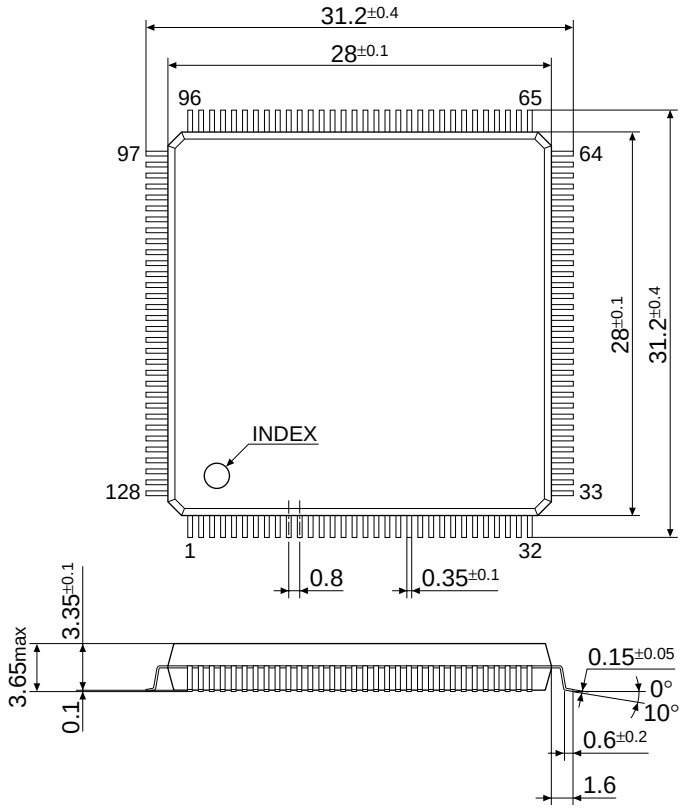
Chip thickness: 0.4 mm
Pad opening: 95 µm

■ PAD COORDINATES

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	COM19/SEG63	1,921	2,370	33	OSC3	-2,400	2,061	65	SEG0	-1,915	-2,370	97	SEG32	2,400	-1,874
2	COM18/SEG64	1,790	2,370	34	OSC4	-2,400	1,929	66	SEG1	-1,783	-2,370	98	SEG33	2,400	-1,743
3	COM17/SEG65	1,659	2,370	35	V_{OSC}	-2,400	1,771	67	SEG2	-1,652	-2,370	99	SEG34	2,400	-1,612
4	COM16/SEG66	1,527	2,370	36	V_{D1}	-2,400	1,640	68	SEG3	-1,521	-2,370	100	SEG35	2,400	-1,480
5	COM15	1,393	2,370	37	V_{DD}	-2,400	1,509	69	SEG4	-1,390	-2,370	101	SEG36	2,400	-1,349
6	COM14	1,262	2,370	38	V_{SS}	-2,400	1,377	70	SEG5	-1,258	-2,370	102	SEG37	2,400	-1,218
7	COM13	1,131	2,370	39	OSC1	-2,400	1,219	71	SEG6	-1,127	-2,370	103	SEG38	2,400	-1,087
8	COM12	999	2,370	40	OSC2	-2,400	1,088	72	SEG7	-996	-2,370	104	SEG39	2,400	-955
9	COM11	868	2,370	41	$\overline{TEST}$	-2,400	940	73	SEG8	-865	-2,370	105	SEG40	2,400	-824
10	COM10	737	2,370	42	$\overline{RESET}$	-2,400	809	74	SEG9	-733	-2,370	106	SEG41	2,400	-693
11	COM9	606	2,370	43	K10/EVIN	-2,400	666	75	SEG10	-602	-2,370	107	SEG42	2,400	-562
12	COM8	474	2,370	44	K07	-2,400	535	76	SEG11	-471	-2,370	108	SEG43	2,400	-430
13	COM7	343	2,370	45	K06	-2,400	404	77	SEG12	-340	-2,370	109	SEG44	2,400	-299
14	COM6	212	2,370	46	K05	-2,400	273	78	SEG13	-208	-2,370	110	SEG45	2,400	-168
15	COM5	81	2,370	47	K04	-2,400	141	79	SEG14	-77	-2,370	111	SEG46	2,400	-37
16	COM4	-51	2,370	48	K03	-2,400	10	80	SEG15	54	-2,370	112	SEG47	2,400	95
17	COM3	-182	2,370	49	K02	-2,400	-121	81	SEG16	185	-2,370	113	SEG48	2,400	226
18	COM2	-313	2,370	50	K01	-2,400	-252	82	SEG17	317	-2,370	114	SEG49	2,400	357
19	COM1	-444	2,370	51	K00	-2,400	-384	83	SEG18	448	-2,370	115	SEG50	2,400	488
20	COM0	-576	2,370	52	P17	-2,400	-533	84	SEG19	579	-2,370	116	COM31/SEG51	2,400	684
21	CG	-707	2,370	53	P16	-2,400	-664	85	SEG20	710	-2,370	117	COM30/SEG52	2,400	815
22	CF	-838	2,370	54	P15	-2,400	-795	86	SEG21	842	-2,370	118	COM29/SEG53	2,400	946
23	CE	-969	2,370	55	P14	-2,400	-927	87	SEG22	973	-2,370	119	COM28/SEG54	2,400	1,078
24	CD	-1,101	2,370	56	P13/$\overline{SRDY}$	-2,400	-1,058	88	SEG23	1,104	-2,370	120	COM27/SEG55	2,400	1,209
25	CC	-1,232	2,370	57	P12/$\overline{SCLK}$	-2,400	-1,189	89	SEG24	1,235	-2,370	121	COM26/SEG56	2,400	1,340
26	CB	-1,363	2,370	58	P11/SOUT	-2,400	-1,320	90	SEG25	1,367	-2,370	122	COM25/SEG57	2,400	1,471
27	CA	-1,494	2,370	59	P10/SIN	-2,400	-1,452	91	SEG26	1,498	-2,370	123	COM24/SEG58	2,400	1,603
28	V_{C5}	-1,626	2,370	60	R26/$\overline{TOUT}$	-2,400	-1,604	92	SEG27	1,629	-2,370	124	COM23/SEG59	2,400	1,734
29	V_{C4}	-1,757	2,370	61	R27/TOUT	-2,400	-1,735	93	SEG28	1,760	-2,370	125	COM22/SEG60	2,400	1,865
30	V_{C3}	-1,888	2,370	62	R34/FOUT	-2,400	-1,866	94	SEG29	1,892	-2,370	126	COM21/SEG61	2,400	1,996
31	V_{C2}	-2,019	2,370	63	R50/BZ	-2,400	-1,998	95	SEG30	2,400	-2,137	127	COM20/SEG62	2,400	2,128
32	V_{C1}	-2,151	2,370	64	R51/$\overline{BZ}$	-2,400	-2,129	96	SEG31	2,400	-2,005	–			

■ PACKAGE DIMENSIONS

Plastic QFP8-128pin



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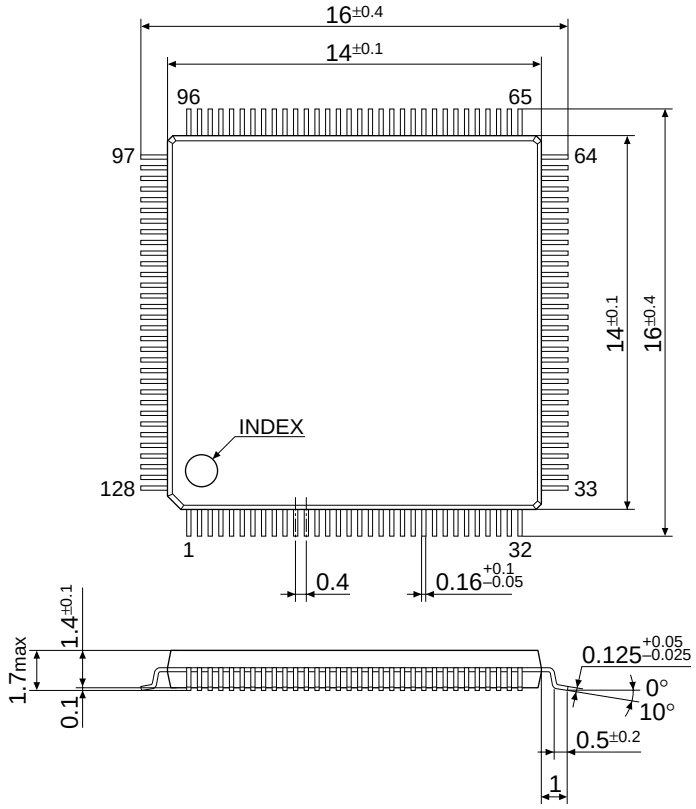
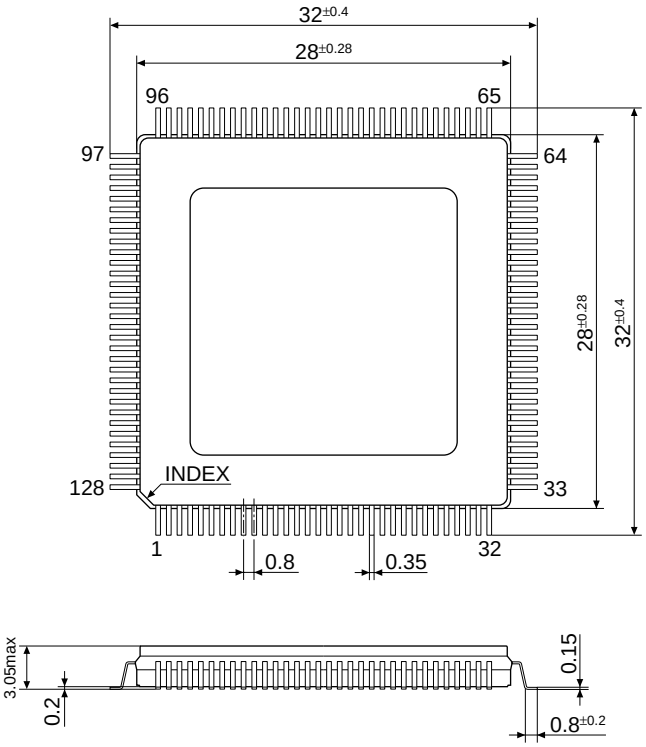


Unit: mm

Ceramic QFP8-128pin



Unit: mm

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