MF1380-01

EPSON

CMOS 8-BIT SINGLE CHIP MICROCOMPUTER

E0C88816 TECHNICAL MANUAL

E0C88816 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

Contents

1 INTRODUCTION

The E0C88816 microcomputer features the E0C88 (MODEL 3) CMOS 8-bit core CPU along with a 116K bytes of ROM, an 8K bytes of RAM, three different timers, a serial interface with optional asynchronization or clock synchronization, a melody generator and an A / D converter.

The E0C88816 has large capacity of ROM and RAM and fully operable over a wide range of voltages. Furthermore, it can perform high speed operations even at low voltage. Like all the equipment in the E0C Family, these microcomputers have low power consumption.

1.1 Features

Table 1.1.1 lists the features of the E0C88816.

Table 1.1.1 Main features

Core CPU	E0C88 (MODEL3) CMOS 8-bit core CPU
OSC1 Oscillation circuit	Crystal oscillation circuit/CR oscillation circuit/external clock input 32.768 kHz (Typ.)
OSC3 Oscillation circuit	Crystal oscillation circuit/ceramic oscillation circuit/CR oscillation circuit/external clock input 8.2 MHz (Max.)
Instruction set	608 types (usable for multiplication and division instructions)
Min. instruction execution time	0.244 µsec/8.2 MHz (2 clock)
Internal ROM capacity	116K bytes
Internal RAM capacity	8K bytes/RAM, 4224 bits/display memory, 512 bytes/melody RAM
Input port	9 bits (1 bit can be set for event counter external clock input)
Output port	7 bits (can be set for BZ, $\overline{BZ}$, TOUT, $\overline{TOUT}$ and FOUT output)
I/O port	16 bits (P10–P13 and P14–P17 can be set for serial I/F input/output and A/D converter input, respectively)
Serial interface	1ch (Optional clock synchronous system or asynchronous system)
Timer	Programmable timer (8 bits): 2ch (1ch can be set as a an event counter or 2ch as a 16 bits programmable timer for 1ch) Clock timer (8 bits): 1ch Stopwatch timer (8 bits): 1ch
LCD driver	Dot matrix type (supports 5 × 8 and 5 × 5 fonts) 72 segments × 32 common (1/5 bias) 88 segments × 16 common (1/5 or 1/4 bias) 88 segments × 8 common (1/5 or 1/4 bias) LCD drive power supply circuit built-in (booster/reducer type, 5 potentials/4 potentials)
Sound generator	Envelope function, equipped with volume control
Watchdog timer	Built-in
Supply voltage detection (SVD) circuit	Can detect up to 16 different voltage levels
Melody generator	1 sound source (scale: 3 octaves, note: 8 types, tempo: 16 types) Note and scale data are stored into the melody RAM (allows the CPU to read and write)
A/D converter	Successive-approximation type, resolution: 10 bits, input: 4ch (shared with P14–P17)
Interrupt	External interrupt: Input interrupt 2 systems (3 types) Internal interrupt: Timer interrupt 3 systems (9 types) Serial interface interrupt 1 system (3 types) Melody interrupt 1 system (1 type) A/D converter interrupt 1 system (1 type)
Supply voltage	Normal mode: 2.4 V–5.5 V (Max. 4.2 MHz) Low power mode: 1.8 V–5.5 V (Max. 80 kHz) High speed mode: 3.5 V–5.5 V (Max. 8.2 MHz)
Current consumption	SLEEP mode: 0.45 µA (Typ./normal mode) HALT mode (32.768 kHz): 1.5 µA (Typ./normal mode) During running (32.768 kHz): 7 µA (Typ./normal mode) During running (4 MHz): 0.9 mA (Typ./normal mode)
Supply form	QFP18-176pin or chip

1.2 Block Diagram

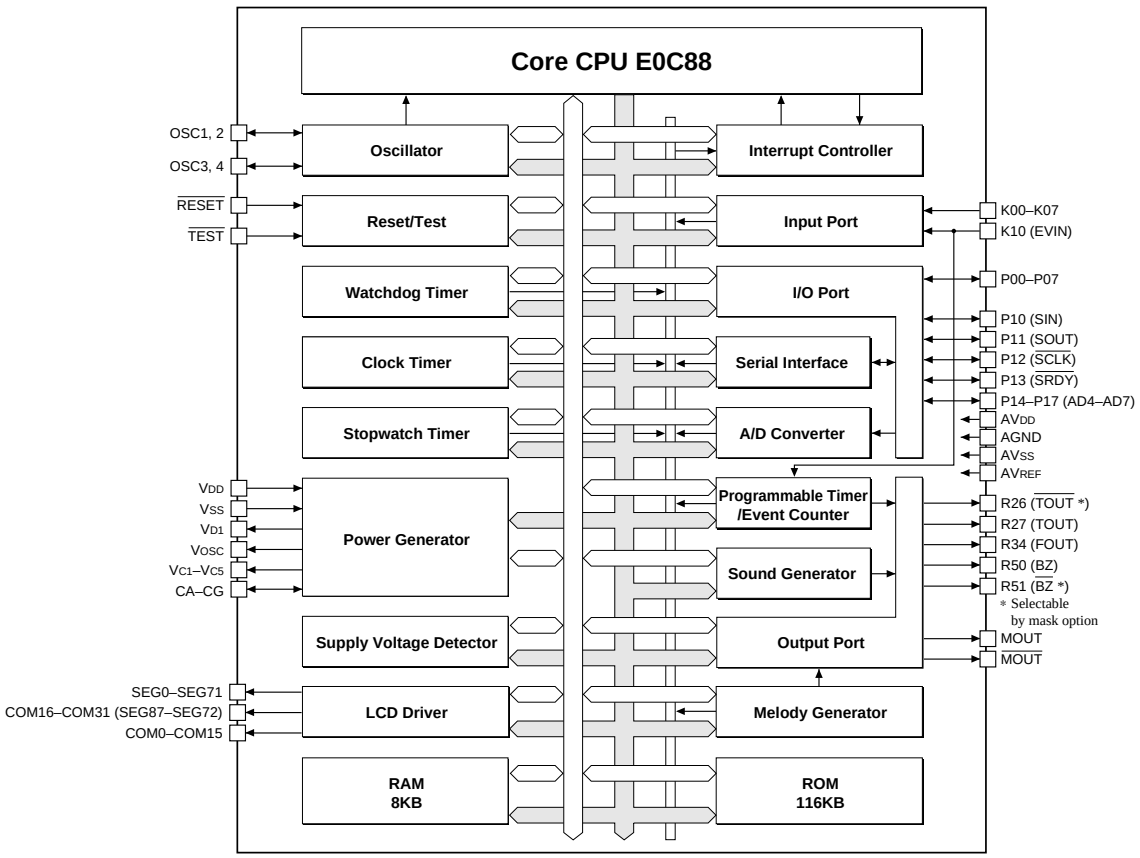
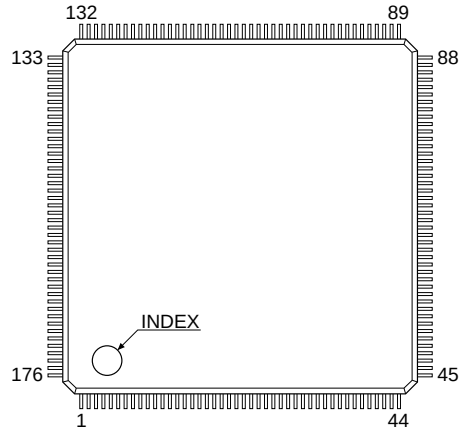


Fig. 1.2.1 E0C88816 block diagram

1.3 Pin Layout Diagram

QFP18-176pin



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	45	N.C.	89	N.C.	133	N.C.
2	N.C.	46	SEG56	90	N.C.	134	N.C.
3	SEG16	47	SEG57	91	V_{C3}	135	P01
4	SEG17	48	SEG58	92	V_{C2}	136	P00
5	SEG18	49	SEG59	93	V_{C1}	137	MOUT
6	SEG19	50	SEG60	94	OSC3	138	$\overline{\text{MOUT}}$
7	SEG20	51	SEG61	95	OSC4	139	R26/$\overline{\text{TOUT}}$
8	SEG21	52	SEG62	96	V_{D1}	140	R27/TOUT
9	SEG22	53	SEG63	97	V_{DD}	141	R34/FOUT
10	SEG23	54	SEG64	98	V_{SS}	142	R50/BZ
11	SEG24	55	SEG65	99	V_{OSC}	143	R51/$\overline{\text{BZ}}$
12	SEG25	56	SEG66	100	OSC1	144	COM0
13	SEG26	57	SEG67	101	OSC2	145	COM1
14	SEG27	58	SEG68	102	$\overline{\text{TEST}}$	146	COM2
15	SEG28	59	SEG69	103	$\overline{\text{RESET}}$	147	COM3
16	SEG29	60	SEG70	104	K10/EVIN	148	COM4
17	SEG30	61	SEG71	105	K07	149	COM5
18	SEG31	62	COM31/SEG72	106	K06	150	COM6
19	SEG32	63	COM30/SEG73	107	K05	151	COM7
20	SEG33	64	COM29/SEG74	108	K04	152	COM8
21	SEG34	65	COM28/SEG75	109	K03	153	COM9
22	SEG35	66	COM27/SEG76	110	K02	154	COM10
23	SEG36	67	COM26/SEG77	111	K01	155	COM11
24	SEG37	68	COM25/SEG78	112	K00	156	COM12
25	SEG38	69	COM24/SEG79	113	P17/AD7	157	COM13
26	SEG39	70	COM23/SEG80	114	P16/AD6	158	COM14
27	SEG40	71	COM22/SEG81	115	P15/AD5	159	COM15
28	SEG41	72	COM21/SEG82	116	P14/AD4	160	SEG0
29	SEG42	73	COM20/SEG83	117	P13/$\overline{\text{SRDY}}$	161	SEG1
30	SEG43	74	COM19/SEG84	118	P12/$\overline{\text{SCLK}}$	162	SEG2
31	SEG44	75	COM18/SEG85	119	P11/SOUT	163	SEG3
32	SEG45	76	COM17/SEG86	120	P10/SIN	164	SEG4
33	SEG46	77	COM16/SEG87	121	AV_{DD}	165	SEG5
34	SEG47	78	CG	122	AGND	166	SEG6
35	SEG48	79	CF	123	AV_{SS}	167	SEG7
36	SEG49	80	CE	124	AV_{REF}	168	SEG8
37	SEG50	81	CD	125	P07	169	SEG9
38	SEG51	82	CC	126	P06	170	SEG10
39	SEG52	83	CB	127	P05	171	SEG11
40	SEG53	84	CA	128	P04	172	SEG12
41	SEG54	85	V_{C5}	129	P03	173	SEG13
42	SEG55	86	V_{C4}	130	P02	174	SEG14
43	N.C.	87	N.C.	131	N.C.	175	SEG15
44	N.C.	88	N.C.	132	N.C.	176	N.C.

N.C.: No Connection

Fig. 1.3.1 E0C88816 pin layout

Table 1.3.1 E0C88816 pin description

Pin name	Pin No.	In/out	Function
V_{DD}	97	–	Power supply (+) terminal
V_{SS}	98	–	Power supply (GND) terminal
V_{D1}	96	–	Regulated voltage for internal circuit
V_{OSC}	99	–	Regulated voltage for OSC1 oscillation circuit
V_{C1}–V_{C5}	93–91, 86, 85	O	LCD drive voltage output terminals
CA–CG	84–78	–	Voltage boost/reduce-capacitor connection terminals for LCD
OSC1	100	I	OSC1 oscillation input terminal (select crystal oscillation/CR oscillation/external clock input by mask option)
OSC2	101	O	OSC1 oscillation output terminal
OSC3	94	I	OSC3 oscillation input terminal (select crystal/ceramic/CR oscillation/external clock input by mask option)
OSC4	95	O	OSC3 oscillation output terminal
K00–K07	112–105	I	Input terminals (K00–K07)
K10/EVIN	104	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
R26/$\overline{\text{TOUT}}$	139	O	Output terminal (R26) or programmable timer underflow signal inverted output terminal ($\overline{\text{TOUT}}$) (selectable by mask option)
R27/TOUT	140	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R34/FOUT	141	O	Output terminal (R34) or clock output terminal (FOUT)
R50/BZ	142	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BZ}}$	143	O	Output terminal (R51) or buzzer inverted output terminal ($\overline{\text{BZ}}$) (selectable by mask option)
P00–P07	136, 135, 130–125	I/O	I/O terminals (P00–P07)
P10/SIN	120	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	119	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	118	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	117	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/AD4	116	I/O	I/O terminal (P14) or A/D converter input terminal (AD4)
P15/AD5	115	I/O	I/O terminal (P15) or A/D converter input terminal (AD5)
P16/AD6	114	I/O	I/O terminal (P16) or A/D converter input terminal (AD6)
P17/AD7	113	I/O	I/O terminal (P17) or A/D converter input terminal (AD7)
MOUT	137	O	Melody output terminal
$\overline{\text{MOUT}}$	138	O	Melody inverted output terminal
COM0–COM15	144–159	O	LCD common output terminals
COM16–COM31 /SEG87–SEG72	77–62	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 or 1/8 duty is selected)
SEG0–SEG71	160–175, 3–42, 46–61	O	LCD segment output terminals
$\overline{\text{RESET}}$	103	I	Initial reset input terminal
$\overline{\text{TEST}}$ *1	102	I	Test input terminal
AV_{DD}	121	–	Analog system power supply (+) terminal
AV_{SS}	123	–	Analog system power supply (–) terminal
AGND	122	–	Analog system ground terminal
AV_{REF}	124	I	Analog system reference voltage input terminal

*1 $\overline{\text{TEST}}$ is the terminal used for shipping inspection of the IC. For normal operation be sure it is connected to V_{DD}.

1.4 Mask Option

Mask options shown below are provided for the E0C88816. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of the E0C88816, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "E0C88 Family Development Tool Manual" for details on the winfog.

Option list

The following options can be set for the E0C88816 and ICE88R/ICE88UR. Multiple specifications are available in each option item as indicated in the Option List. Select the specifications that meet the target system and check the appropriate box.
The option selection is done interactively on the screen during winfog execution, using this option list as reference.

PRC88816 option list

A OSC1 SYSTEM CLOCK

☐ 1. Internal Clock (32.768 kHz)
☐ 2. User Clock

B OSC3 SYSTEM CLOCK

☐ 1. Internal Clock (4.9152 MHz)
☐ 2. User Clock

E0C88816 mask option list

1 OSC1 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. External Clock
☐ 3. CR
☐ 4. Crystal (with Gate Capacity)

2 OSC3 SYSTEM CLOCK

☐ 1. Crystal
☐ 2. Ceramic
☐ 3. CR
☐ 4. External Clock

3 MULTIPLE KEY ENTRY RESET

• Combination ... ☐ 1. Not Use
☐ 2. Use K00, K01
☐ 3. Use K00, K01, K02
☐ 4. Use K00, K01, K02, K03

4 SVD RESET

☐ 1. Not Use
☐ 2. Use

5 INPUT PORT PULL UP RESISTOR

• K00	☐ 1. With Resistor	☐ 2. Gate Direct
• K01	☐ 1. With Resistor	☐ 2. Gate Direct
• K02	☐ 1. With Resistor	☐ 2. Gate Direct
• K03	☐ 1. With Resistor	☐ 2. Gate Direct
• K04	☐ 1. With Resistor	☐ 2. Gate Direct
• K05	☐ 1. With Resistor	☐ 2. Gate Direct
• K06	☐ 1. With Resistor	☐ 2. Gate Direct
• K07	☐ 1. With Resistor	☐ 2. Gate Direct
• K10	☐ 1. With Resistor	☐ 2. Gate Direct
• $\overline{\text{RESET}}$	☐ 1. With Resistor	☐ 2. Gate Direct

6 I/O PORT PULL UP RESISTOR

• P00	☐ 1. With Resistor	☐ 2. Gate Direct
• P01	☐ 1. With Resistor	☐ 2. Gate Direct
• P02	☐ 1. With Resistor	☐ 2. Gate Direct
• P03	☐ 1. With Resistor	☐ 2. Gate Direct
• P04	☐ 1. With Resistor	☐ 2. Gate Direct
• P05	☐ 1. With Resistor	☐ 2. Gate Direct
• P06	☐ 1. With Resistor	☐ 2. Gate Direct
• P07	☐ 1. With Resistor	☐ 2. Gate Direct
• P10	☐ 1. With Resistor	☐ 2. Gate Direct
• P11	☐ 1. With Resistor	☐ 2. Gate Direct
• P12	☐ 1. With Resistor	☐ 2. Gate Direct
• P13	☐ 1. With Resistor	☐ 2. Gate Direct
• P14	☐ 1. With Resistor	☐ 2. Gate Direct
• P15	☐ 1. With Resistor	☐ 2. Gate Direct
• P16	☐ 1. With Resistor	☐ 2. Gate Direct
• P17	☐ 1. With Resistor	☐ 2. Gate Direct

7 LCD DRIVE DUTY

☐ 1. 1/32 & 1/16 Duty
☐ 2. 1/8 Duty

8 LCD POWER SUPPLY

☐ 1. Internal TYPE A (V_{C2} Standard, 1/5 Bias, 4.5 V)
☐ 2. External
☐ 3. Internal TYPE B (V_{C2} Standard, 1/5 Bias, 5.5 V)
☐ 4. Internal TYPE C (V_{C2} Standard, 1/4 Bias, 4.5 V)
☐ 5. Internal TYPE D (V_{C1} Standard, 1/4 Bias, 4.5 V)

9 $\overline{BZ}$ OUTPUT (R51)

☐ 1. Use
☐ 2. Not Use

10 $\overline{TOUT}$ OUTPUT (R26)

☐ 1. Use
☐ 2. Not Use

11 CPU MODE

☐ 1. Maximum Mode
☐ 2. Minimum Mode

12 MODE DURING BUZZER OUTPUT

☐ 1. Normal Mode
☐ 2. Heavy Load Protection Mode

13 MODE DURING MELODY OUTPUT

☐ 1. Normal Mode
☐ 2. Heavy Load Protection Mode

Outline of mask options

(1) OSC1 oscillation circuit

The specification of the OSC1 oscillation circuit can be selected from among four types: "Crystal oscillation", "CR oscillation", "Crystal oscillation (gate capacitor built-in)" and "External clock input". Refer to Section 5.3.3, "OSC1 oscillation circuit", for details.

(2) OSC3 oscillation circuit

The specification of the OSC3 oscillation circuit can be selected from among four types: "Crystal oscillation", "Ceramic oscillation", "CR oscillation" and "External clock input". Refer to Section 5.3.4, "OSC3 oscillation circuit", for details.

(3) Multiple key entry reset (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input ports (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 4.1.2, "Simultaneous LOW level input at input port terminals K00–K03", for details.

(4) Initial reset by SVD circuit

The SVD circuit has a function that generates an initial reset signal when the supply voltage drops to level 0 or less. The mask option is used to select whether this function is used or not. Refer to Section 5.14, "Supply Voltage Detection (SVD) Circuit", for details.

(5) Input port/$\overline{\text{RESET}}$ terminal pull-up resistor

This mask option can select whether the pull-up resistor for the input port terminal is used or not. It is possible to select for each bit of the input ports. Refer to Section 5.4, "Input Ports (K ports)", for details.
Furthermore, a pull-up option is also provided for the $\overline{\text{RESET}}$ terminal.

(6) I/O port pull-up resistor

This mask option can select whether the pull-up resistor for the I/O port terminal (it works during input mode) is used or not. It is possible to select for each bit of the I/O ports. Refer to Section 5.6, "I/O Ports (P ports)", for details.

Since P10 to P13 are shared with the serial interface I/O terminals, the selected P10 and P12 terminal configuration is applied to the serial input (SIN) terminal and serial clock input terminal ($\overline{\text{SCLK}}$ in clock synchronous mode) when the serial interface is used. Refer to Section 5.7, "Serial Interface", for details.

(7) LCD drive duty

The drive duty for the built-in LCD driver can be selected whether it will be 1/32 and 1/16 software-switched or fixed at 1/8. Refer to Section 5.11, "LCD Controller", for details.

(8) LCD power supply

Either the internal power supply or an external power supply can be selected as the LCD system power source. Furthermore, when using the internal power supply, the LCD drive voltage can be set for a 4.5 V panel or a 5.5 V panel and the drive bias to 1/5 or 1/4. Refer to Section 5.11, "LCD Controller", for details.

(9) $\overline{\text{BZ}}$ output (R51 port specification)

The R51 port can be configured as a general purpose output port or as the $\overline{\text{BZ}}$ output port ($\overline{\text{BZ}}$ inverted output). Refer to Section 5.5, "Output Ports (R ports)" for details.

(10) $\overline{\text{TOUT}}$ output (R26 port specification)

The R26 port can be configured as a general purpose output port or as the $\overline{\text{TOUT}}$ output port ($\overline{\text{TOUT}}$ inverted output). Refer to Section 5.5, "Output Ports (R ports)" for details.

(11) CPU mode

The CPU mode of the E0C88 core can select either maximum mode or minimum mode (fixed after selection).
In the maximum mode, since the E0C88816 saves the program counter (PC), system condition flag (SC) and code bank register (CB) values into the stack when an interrupt is generated, the program sequence is able to return to the previous bank if the interrupt handler routines change banks without saving.

(12) Heavy load protection mode during buzzer output

This option allows selection whether the heavy load protection mode is set or not when the buzzer (BZ) signal is output.
When direct driving a piezoelectric buzzer, select Normal mode to reduce current consumption. When using an external bipolar transistor, select Heavy load protection mode. Refer to Section 2.3, "Heavy Load Protection Mode", for details.

(13) Heavy load protection mode during melody output

This option allows selection whether the heavy load protection mode is set or not when the melody (MOUT) signal is output.
When direct driving a piezoelectric buzzer, select Normal mode to reduce current consumption. When using an external bipolar transistor, select Heavy load protection mode. Refer to Section 2.3, "Heavy Load Protection Mode", for details.

2 POWER SUPPLY

In this section, we will explain the operating voltage and the configuration of the internal power supply circuit of the E0C88816.

2.1 Operating Voltage

The E0C88816 operating power voltage is as follows:

Normal mode:	2.4 V to 5.5 V
Low power mode:	1.8 V to 5.5 V
High speed mode:	3.5 V to 5.5 V

If supply voltage drops below level 0 (see Chapter 7, "ELECTRICAL CHARACTERISTICS"), the system is automatically reset by a supply voltage detection (SVD) circuit described in the latter. This function can be selected by mask option.

2.2 Internal Power Supply Circuit

The E0C88816 incorporates the power supply circuit shown in Figure 2.2.1. When voltage within the range described above is supplied to V_{DD} (+) and V_{SS} (GND), all the voltages needed for the internal circuit are generated internally in the IC.

Roughly speaking, the power supply circuit is divided into three sections.

The internal logic voltage regulator generates the operating voltage <V_{D1}> for driving the internal logic circuits and the OSC3 oscillation circuit.

The V_{D1} voltage can be selected from the following three types: 1.3 V for low-power mode, 2.2 V for normal mode and 3.3 V for high-speed mode.
It should be selected by a program to switch according to the supply voltage and oscillation frequency.
See Section 5.3, "Oscillation Circuits and Operating Mode", for the switching of operating mode.

The oscillation system voltage regulator generates the operating voltage <V_{OSC}> for the OSC1 oscillation circuit.

The LCD system power supply circuit generates the LCD drive voltages <V_{C1}> to <V_{C5}>. In 1/5 bias mode, V_{C1} is generated by halving V_{C2} output from the LCD system voltage regulator and V_{C3} to V_{C5} are generated by boosting V_{C2}. These five voltages can be supplied from outside the IC by mask option.
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the voltage values.
In the E0C88816, the LCD drive voltage is supplied to the built-in LCD driver which drives the LCD panel connected to the SEG and COM terminals.

Note: Do not use the voltages output from the internal power supply circuit for driving external circuits.

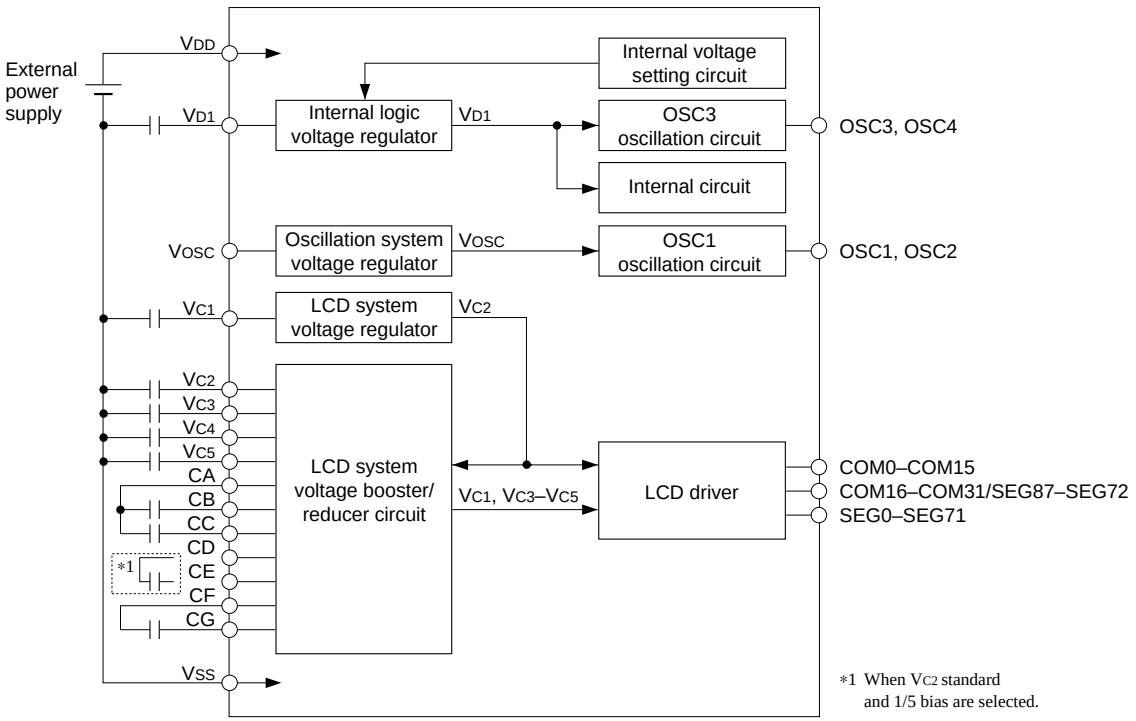


Fig. 2.2.1 Configuration of power supply circuit (V_{C2} standard, 1/4 bias)

2.3 Heavy Load Protection Mode

The E0C88816 has a heavy load protection function for stable operation even when the supply voltage fluctuates by driving a heavy load. The heavy load protection mode becomes valid when the peripheral circuits are in the following status:

(1) When the OSC3 oscillation circuit is ON
(OSCC = "1" and not in SLEEP)

(2) When the buzzer output is ON
(BZON = "1" or BZSHT = "1")

(3) When the melody output is ON
(MBUSY = "1")

The conditions (2) and (3) can be selected by mask option.

Heavy load protection mode
during buzzer output
☐ Normal mode
☐ Heavy load protection mode

Heavy load protection mode
during melody output
☐ Normal mode
☐ Heavy load protection mode

When direct driving a piezoelectric buzzer with the buzzer (BZ, $\overline{BZ}$) or melody signal (MOUT, $\overline{MOUT}$), select Normal mode to reduce current consumption. When driving an external bipolar transistor with the BZ or MOUT signal, select Heavy load protection mode.
When using the melody output terminal (MOUT, $\overline{MOUT}$) for buzzer output, select the same option for both the buzzer and melody outputs.

For details of the OSC3 oscillation circuit, buzzer output and melody output, refer to "5.3 Oscillation Circuits and Operating Mode", "5.12 Sound Generator" and "5.13 Melody Generator", respectively.

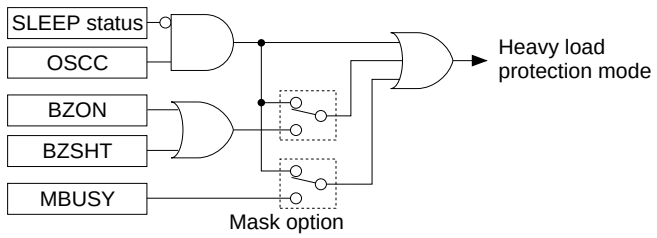


Fig. 2.3.1 Configuration of heavy load protection mode control circuit

3 CPU AND MEMORY CONFIGURATION

In this section, we will explain the CPU and memory configuration.

3.1 CPU

The E0C88816 utilize the E0C88 8-bit core CPU whose resistor configuration, command set, etc. are virtually identical to other units in the family of processors incorporating the E0C88.

See the "E0C88 Core CPU Manual" for the E0C88.

The E0C88816 supports Model 3/minimum mode of the E0C88 CPU which allows accessing of the internal memory mapped within the physical space from 000000H to 01FFFFH.

3.2 Internal Memory

The E0C88816 is equipped with internal ROM and RAM as shown in Figure 3.2.1.

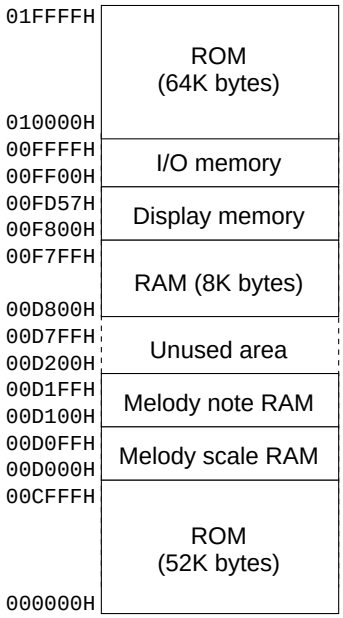


Fig. 3.2.1 Internal memory map

3.2.1 ROM

The internal ROM capacity is shown below.

Capacity: 116K bytes
Address: 000000H to 00CFFFH
010000H to 01FFFFH

3.2.2 RAM

The internal ROM capacity is shown below.

Capacity: 8K bytes
Address: 00D800H to 00F7FFH

3.2.3 I/O memory

A memory mapped I/O method is employed in the E0C88816 for interfacing with internal peripheral circuit. Peripheral circuit control bits and data register are arranged in data memory space. Control and data exchange are conducted via normal memory access. The I/O memory is arranged from address 00FF00H to address 00FFFFH. See Section 5.1, "I/O Memory Map", for details of the I/O memory.

3.2.4 Display memory

The E0C88816 is equipped with an internal display memory which stores a display data for LCD driver.
The display memory is arranged from address 00F800H to address 00FD57H (including the unused area). See Section 5.11, "LCD Controller", for details of the display memory.

3.3 Exception Processing Vectors

Address 000000H to address 000027H in the program area of the E0C88816 is assigned as exception processing vectors. Furthermore, from address 00002AH to address 0000FFH, software interrupt vectors are assignable to any two bytes which begin with an even address.
Table 3.3.1 lists the vector addresses and the exception processing factors to which they correspond.

Table 3.3.1 Vector addresses and exception processing factors

Vector address	Exception processing factor	Priority
000000H	Reset	High
000002H	Zero division	↑
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	
000024H	A/D conversion complete interrupt	↓
000026H	Melody play complete interrupt	Low
000028H	System reserved (cannot be used)	No priority rating
00002AH : 0000FEH	Software interrupt	

For each vector address and the address after it, the start address of the exception processing routine is written into the subordinate and super ordinate sequence. When an exception processing factor is generated, the exception processing routine is executed starting from the recorded address.

When multiple exception processing factors are generated at the same time, execution starts with the highest priority item.
The priority sequence shown in Table 3.3.1 assumes that the interrupt priority levels are all the same. The interrupt priority levels can be set by software in each system. (See Section 5.16, "Interrupt and Standby Status".)

Note: For exception processing other than reset, SC (system condition flag) and PC (program counter) are evacuated to the stack and branches to the exception processing routines. Consequently, when returning to the main routine from exception processing routines, please use the RETE instruction.

See the "E0C88 Core CPU Manual" for information on CPU operations when an exception processing factor is generated.

3.4 CC (Customized Condition Flag)

The E0C88816 does not use the customized condition flag (CC) in the core CPU. Accordingly, it cannot be used as a branching condition for the conditional branching instruction (JRS, CARS).

4 INITIAL RESET

Initial reset in the E0C88816 is required in order to initialize circuits. This chapter describes initial reset factors and the initial settings for internal registers.

4.1 Initial Reset Factors

There are three initial reset factors for the E0C88816 as shown below.

(1) $\overline{\text{RESET}}$ terminal
(2) Simultaneous LOW level input at input port terminals K00–K03
(3) Supply voltage detection (SVD) circuit

Figure 4.1.1 shows the configuration of the initial reset circuit.

The CPU and peripheral circuits are initialized by means of initial reset factors. When the factor is canceled, the CPU commences reset exception processing. (See "E0C88 Core CPU Manual".)

When this occurs, reset exception processing vectors, Bank 0, 000000H–000001H from program memory are read out and the program (initialization routine) which begins at the readout address is executed.

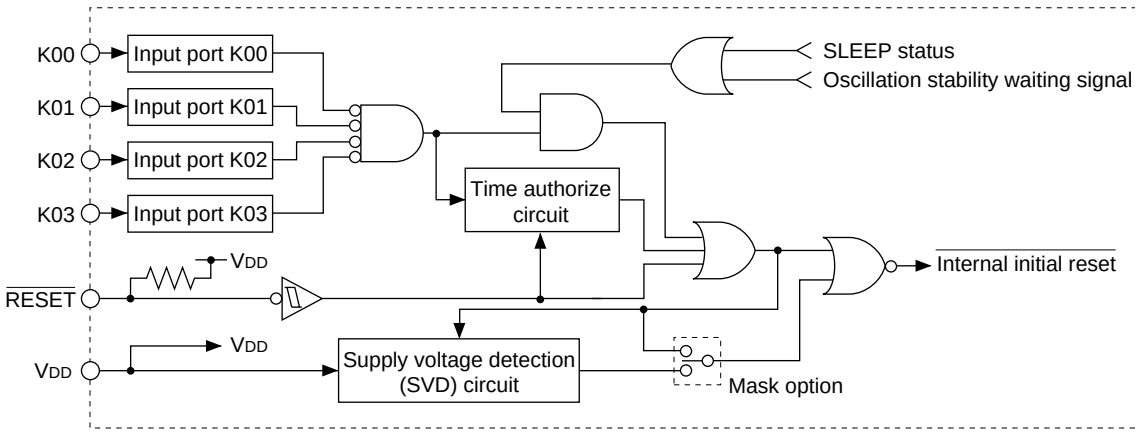


Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 $\overline{\text{RESET}}$ terminal

Initial reset can be done by executed externally inputting a LOW level to the $\overline{\text{RESET}}$ terminal.
Be sure to maintain the $\overline{\text{RESET}}$ terminal at LOW level for the regulation time after the power on to assure the initial reset.
In addition, be sure to use the $\overline{\text{RESET}}$ terminal for the first initial reset after the power is turned on.
The $\overline{\text{RESET}}$ terminal is equipped with a pull-up resistor. You can select whether or not to use by mask option.

$\overline{\text{RESET}}$ terminal pull-up resistors
$\overline{\text{RESET}}$ ..... ☐ With resistor ☐ Gate direct

4.1.2 Simultaneous LOW level input at input port terminals K00–K03

Another way of executing initial reset externally is to input a LOW level simultaneously to the input ports (K00–K03) selected by mask option.
Since there is a built-in time authorize circuit, be sure to maintain the designated input port terminal at LOW level for two seconds (when the oscillation frequency f_{OSC1} = 32.768 kHz) or more to perform the initial reset by means of this function.
However, the time authorize circuit is bypassed during the SLEEP (standby) status and oscillation stabilization waiting period, and initial reset is executed immediately after the simultaneous LOW level input to the designated input ports.
The combination of input ports (K00–K03) that can be selected by mask option are as follows:

Multiple key entry reset
☐ Not use
☐ K00 & K01
☐ K00 & K01 & K02
☐ K00 & K01 & K02 & K03

For instance, if mask option "K00 & K01 & K02 & K03" is selected, initial reset will take place when the input level at input ports K00–K03 is simultaneously LOW.

When using this function, make sure that the designated input ports do not simultaneously switch to LOW level while the system is in normal operation.

4.1.3 Supply voltage detection (SVD) circuit

When the SVD circuit detects that supply voltage has dropped below level 0 four successive times (see Chapter 7, "ELECTRICAL CHARACTERISTICS"), it outputs an initial reset signal until the supply voltage has been restored to level 2.
You can select whether or not to use the initial reset according to the SVD circuit by mask option. If you use it, the supply voltage must be at least level 2 for the first sampling of the SVD circuit, when the power is turned on. At this time, if the power voltage level is less than level 2, the initial reset status will not be canceled and instead the SVD circuit will continue sampling until the supply voltage reaches level 2 or more.
For more information, see "5.14 Supply Voltage Detection (SVD) Circuit" in this Manual.

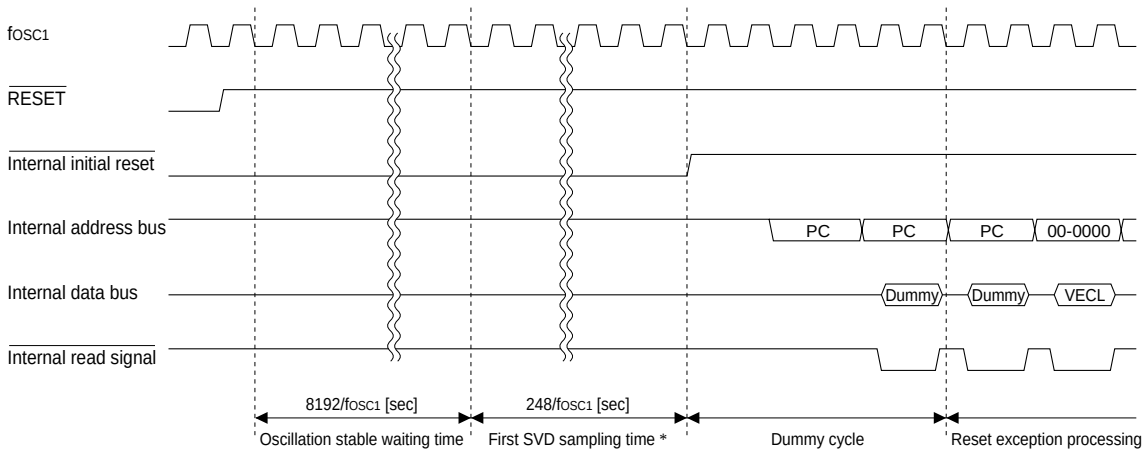
4.1.4 Initial reset sequence

After cancellation of the LOW level input to the $\overline{\text{RESET}}$ terminal, when the power is turned on, the start-up of the CPU is held back until the oscillation stabilization waiting time (8,192 / f_{OSC1} sec.) has elapsed. When the initial reset by the SVD circuit has been used, an initial sampling time (248 / f_{OSC1} sec.) is added as additional waiting time.
Figure 4.1.4.1 shows the operating sequence following initial reset release.

Also, when using the initial reset by simultaneous LOW level input into the input port, you should be careful of the following points.

(1) During SLEEP status, since the time authorization circuit is bypassed, an initial reset is triggered immediately after a LOW level simultaneous input value. In this case, the CPU starts after waiting the oscillation stabilization time and the SVD circuit initial sampling time (when used with the mask option), following cancellation of the LOW level simultaneous input.

(2) Other than during SLEEP status, an initial reset will be triggered 1–2 seconds after a LOW level simultaneous input. In this case, since a reset differential pulse (64 / f_{OSC1} sec.) is generated within the E0C88816, the CPU will start even if the LOW level simultaneous input status is not canceled.



** When the initial reset by the SVD circuit with the mask option has been used, this cycle is inserted as the waiting time.*

Fig. 4.1.4.1 Initial reset sequence

4.2 Initial Settings After Initial Reset

The CPU internal registers are initialized as follows during initial reset.

Table 4.2.1 Initial settings

Register name	Code	Bit length	Setting value
Data register A	A	8	Undefined
Data register B	B	8	Undefined
Index (data) register L	L	8	Undefined
Index (data) register H	H	8	Undefined
Index register IX	IX	16	Undefined
Index register IY	IY	16	Undefined
Program counter	PC	16	Undefined*
Stack pointer	SP	16	Undefined
Base register	BR	8	Undefined
Zero flag	Z	1	0
Carry flag	C	1	0
Overflow flag	V	1	0
Negative flag	N	1	0
Decimal flag	D	1	0
Unpack flag	U	1	0
Interrupt flag 0	I0	1	1
Interrupt flag 1	I1	1	1
New code bank register	NB	8	01H
Code bank register	CB	8	Undefined*
Expand page register	EP	8	00H
Expand page register for IX	XP	8	00H
Expand page register for IY	YP	8	00H

* Reset exception processing loads the preset values stored in 0 bank, 000000H–000001H into the PC. At the same time, 01H of the NB initial value is loaded into CB.

Initialize the registers which are not initialized at initial reset using software.

Since the internal RAM and display memory are not initialized at initial reset, be sure to initialize using software.

The respectively stipulated initializations are done for internal peripheral circuits. If necessary, the initialization should be done using software.
For initial value at initial reset, see the sections on the I/O memory map and peripheral circuit descriptions in the following chapter of this Manual.

4.3 Programming Note

All the interrupts including $\overline{\text{NMI}}$ are masked until any value is written to both addresses "00FF00H" and "00FF01H".
In the E0C88816, it is not necessary to change the contents of these addresses because they are general-purpose registers, note, however, to be sure to write any data in the initial routine to cancel interrupt masks.

5 PERIPHERAL CIRCUITS AND THEIR OPERATION

The peripheral circuits of the E0C88816 is interfaced with the CPU by means of the memory mapped I/O method. For this reason, just as with other memory access operations, peripheral circuits can be controlled by manipulating I/O memory. Below is a description of the operation and control method for each individual peripheral circuit.

5.1 I/O Memory Map

Table 5.1.1(a) I/O Memory map (00FF00H–00FF10H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF00	D7	BSMD1	General-purpose register	1	0	0	R/W	Reserved register
	D6	BSMD0	General-purpose register			0	R/W	
	D5	CEMD1	General-purpose register			1	R/W	
	D4	CEMD0	General-purpose register			1	R/W	
	D3	CE3	General-purpose register			0	R/W	
	D2	CE2	General-purpose register			0	R/W	
	D1	CE1	General-purpose register			0	R/W	
	D0	CE0	General-purpose register			0	R/W	
00FF01	D7	SPP7	General-purpose register	1	0	0	R/W	Reserved register
	D6	SPP6	General-purpose register			0	R/W	
	D5	SPP5	General-purpose register			0	R/W	
	D4	SPP4	General-purpose register			0	R/W	
	D3	SPP3	General-purpose register			0	R/W	
	D2	SPP2	General-purpose register			0	R/W	
	D1	SPP1	General-purpose register			0	R/W	
	D0	SPP0	General-purpose register			0	R/W	
00FF02	D7	EBR	General-purpose register	1	0	0	R/W	Reserved register
	D6	WT2	General-purpose register			0	R/W	
	D5	WT1	General-purpose register			0	R/W	
	D4	WT0	General-purpose register			0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection VDC1 VDC0 Operating mode 1 × High speed (V_{D1}=3.3V) 0 1 Low power (V_{D1}=1.3V) 0 0 Normal (V_{D1}=2.2V)			0	R/W	
	D0	VDC0				0	R/W	
00FF10	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	General-purpose register	1	0	0	R/W	Reserved register
	D3	LCFRM	General-purpose register			0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	General-purpose register	1	0	0	R/W	Reserved register

*1 When 1/8 duty has been selected by mask option, setting of this register becomes invalid.

Table 5.1.1(b) I/O Memory map (00FF11H–00FF22H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	
00FF12	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	SVDSP	SVD auto-sampling control	On	Off	0	R/W	These registers are reset to "0" when SLP instruction is executed.
	D4	SVDON	SVD continuous sampling control/status R	Busy	Ready	1→0*1	R/W	
			W	On	Off	0		
	D3	SVD3	SVD detection level SVD3 SVD2 SVD1 SVD0 Detection level 1 1 1 1 Level 15 1 1 1 0 Level 14 : : : : : 0 0 0 0 Level 0			X	R	*2
	D2	SVD2				X	R	
	D1	SVD1				X	R	
	D0	SVD0				X	R	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 Priority level PK11 PK10 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	

*1 After initial reset, this status is set "1" until conclusion of hardware first sampling.
*2 Initial values are set according to the supply voltage detected at first sampling by hardware.
Until conclusion of first sampling, SVD0–SVD3 data are undefined.

Table 5.1.1(c) I/O Memory map (00FF23H–00FF2CH)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	
00FF28	D7	PADC1	A/D converter interrupt priority register	PADC1 PMDY1 / PADC0 PMDY0 / Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D6	PADC0				0	R/W	
	D5	PMDY1	Melody interrupt priority register			0	R/W	
	D4	PMDY0				0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EMDY	Melody interrupt enable register			0	R/W	
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag (R)	Generated	Not generated	0	R/W	
	D6	FMDY	Melody interrupt factor flag (W)	Reset	No operation	0	R/W	
	D5	–	–	–	–	–		Constantly "0" when being read
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		

Table 5.1.1(d) I/O Memory map (00FF30H–00FF34H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE16	8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF31	D7	EVCNT	Timer 0 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL	Timer 0 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 0 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL	Timer 0 pulse polarity selection: Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
			Timer 0 pulse polarity selection: In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection			0	R/W	
	D3	PSC00	PSC01 PSC00 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT0	Timer 0 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control	Run	Stop	0	R/W	
00FF32	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection			0	R/W	
	D3	PSC10	PSC11 PSC10 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT1	Timer 1 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control	Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6			1	R/W	
	D5	RLD05	Timer 0 reload data D5			1	R/W	
	D4	RLD04	Timer 0 reload data D4			1	R/W	
	D3	RLD03	Timer 0 reload data D3			1	R/W	
	D2	RLD02	Timer 0 reload data D2			1	R/W	
	D1	RLD01	Timer 0 reload data D1			1	R/W	
	D0	RLD00	Timer 0 reload data D0 (LSB)			1	R/W	
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6			1	R/W	
	D5	RLD15	Timer 1 reload data D5			1	R/W	
	D4	RLD14	Timer 1 reload data D4			1	R/W	
	D3	RLD13	Timer 1 reload data D3			1	R/W	
	D2	RLD12	Timer 1 reload data D2			1	R/W	
	D1	RLD11	Timer 1 reload data D1			1	R/W	
	D0	RLD10	Timer 1 reload data D0 (LSB)			1	R/W	

Table 5.1.1(e) I/O Memory map (00FF35H–00FF43H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6			1	R	
	D5	PTD05	Timer 0 counter data D5			1	R	
	D4	PTD04	Timer 0 counter data D4			1	R	
	D3	PTD03	Timer 0 counter data D3			1	R	
	D2	PTD02	Timer 0 counter data D2			1	R	
	D1	PTD01	Timer 0 counter data D1			1	R	
	D0	PTD00	Timer 0 counter data D0 (LSB)			1	R	
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6			1	R	
	D5	PTD15	Timer 1 counter data D5			1	R	
	D4	PTD14	Timer 1 counter data D4			1	R	
	D3	PTD13	Timer 1 counter data D3			1	R	
	D2	PTD12	Timer 1 counter data D2			1	R	
	D1	PTD11	Timer 1 counter data D1			1	R	
	D0	PTD10	Timer 1 counter data D0 (LSB)			1	R	
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when being read
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data			0	R	
	D6	SWD6				0	R	
	D5	SWD5	BCD (1/10 sec)			0	R	
	D4	SWD4				0	R	
	D3	SWD3	Stopwatch timer data			0	R	
	D2	SWD2				0	R	
	D1	SWD1	BCD (1/100 sec)			0	R	
	D0	SWD0				0	R	

Table 5.1.1(f) I/O Memory map (00FF44H–00FF47H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF44	D7	–	–	–	–	–		Constantry "0" when
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	
00FF45	D7	–	–	–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection			0	R/W	
	D5	DUTY1	DUTY2–1 (2 1 0) / Buzzer frequency (Hz): 4096.0 / 2048.0 — 3276.8 / 1638.4 — 2730.7 / 1365.3 — 2340.6 / 1170.3 0 0 0: 8/16 — 8/20 — 12/24 — 12/28 0 0 1: 7/16 — 7/20 — 11/24 — 11/28 0 1 0: 6/16 — 6/20 — 10/24 — 10/28 0 1 1: 5/16 — 5/20 — 9/24 — 9/28			0	R/W	
	D4	DUTY0	1 0 0: 4/16 — 4/20 — 8/24 — 8/28 1 0 1: 3/16 — 3/20 — 7/24 — 7/28 1 1 0: 2/16 — 2/20 — 6/24 — 6/28 1 1 1: 1/16 — 1/20 — 5/24 — 5/28			0	R/W	
	D3	–	–	–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection			0	R/W	
	D1	BZFQ1	BZFQ2 BZFQ1 BZFQ0 — Frequency (Hz) 0 0 0: 4096.0 0 0 1: 3276.8 0 1 0: 2730.7 0 1 1: 2340.6 1 0 0: 2048.0 1 0 1: 1638.4 1 1 0: 1365.3 1 1 1: 1170.3			0	R/W	
	D0	BZFQ0				0	R/W	
00FF46	D7	MCAD7	Note/scale RAM address D7 (MSB)			0	R/W	ADC7
	D6	MCAD6	Note/scale RAM address D6			0	R/W	ADC6
	D5	MCAD5	Note/scale RAM address D5			0	R/W	ADC5
	D4	MCAD4	Note/scale RAM address D4			0	R/W	ADC4
	D3	MCAD3	Note/scale RAM address D3			0	R/W	ADC3
	D2	MCAD2	Note/scale RAM address D2			0	R/W	ADC2
	D1	MCAD1	Note/scale RAM address D1			0	R/W	ADC1
	D0	MCAD0	Note/scale RAM address D0 (LSB)			0	R/W	ADC0
00FF47	D7	MTT3	Tempo selection register			0	R/W	TT3
	D6	MTT2	MTT3 MTT2 MTT1 MTT0 — Tempo 1 1 1 1: 480 1 1 1 0: 240 1 1 0 1: 160 1 1 0 0: 120 1 0 1 1: 96 1 0 1 0: 80 1 0 0 1: 68.6			0	R/W	TT2
	D5	MTT1	1 0 0 0: 60 0 1 1 1: 53.3 0 1 1 0: 48 0 1 0 1: 43.6 0 1 0 0: 40			0	R/W	TT1
	D4	MTT0	0 0 1 1: 36.9 0 0 1 0: 34.3 0 0 0 1: 32 0 0 0 0: 30			0	R/W	TT0
	D3	MLEV	Play mode selection	One shot	Level hold	0	R/W	
	D2	MOSEL	Output selection	MOUT	BZ priority	0	R/W	MOUTSEL
	D1	MBUSY	Melody play status	Busy	Ready	0	R	
	D0	MTC	Melody output control	Play	Stop	0	R/W	MT

*1 Reset to "0" during one-shot output.

Table 5.1.1(g) I/O Memory map (00FF48H–00FF51H)

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF48	D7	–	–		–	–	–		"0" when being read
	D6	EPR	Parity enable register		With parity	Non parity	0	R/W	Only for asynchronous mode
	D5	PMD	Parity mode selection		Odd	Even	0	R/W	
	D4	SCS1	Clock source selection SCS1 SCS0 Clock source 1 1 Programmable timer				0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS0	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16				0	R/W	
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 Asynchronous 8-bit				0	R/W	
	D1	SMD0	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master				0	R/W	
	D0	ESIF	Serial I/F enable register		Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–		–	–	–		"0" when being read
	D6	FER	Framing error flag	R	Error	No error	0	R/W	Only for asynchronous mode
				W	Reset (0)	No operation			
	D5	PER	Parity error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D4	OER	Overrun error flag	R	Error	No error	0	R/W	
				W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D2	RXEN	Receive enable		Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status	R	Run	Stop	0	R/W	
				W	Trigger	No operation			
	D0	TXEN	Transmit enable		Enable	Disable	0	R/W	
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)		High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6				X	R/W	
	D5	TRXD5	Transmit/Receive data D5				X	R/W	
	D4	TRXD4	Transmit/Receive data D4				X	R/W	
	D3	TRXD3	Transmit/Receive data D3				X	R/W	
	D2	TRXD2	Transmit/Receive data D2				X	R/W	
	D1	TRXD1	Transmit/Receive data D1				X	R/W	
	D0	TRXD0	Transmit/Receive data D0 (LSB)				X	R/W	
00FF50	D7	SIK07	K07 interrupt selection register		Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register				0	R/W	
	D5	SIK05	K05 interrupt selection register				0	R/W	
	D4	SIK04	K04 interrupt selection register				0	R/W	
	D3	SIK03	K03 interrupt selection register				0	R/W	
	D2	SIK02	K02 interrupt selection register				0	R/W	
	D1	SIK01	K01 interrupt selection register				0	R/W	
	D0	SIK00	K00 interrupt selection register				0	R/W	
00FF51	D7	–	–		–	–	–		Constantly "0" when being read
	D6	–	–		–	–	–		
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		
	D2	–	–		–	–	–		
	D1	SIK11	General-purpose register		1	0	0	R/W	Reserved register
	D0	SIK10	K10 interrupt selection register		Enable	Disable	0	R/W	

Table 5.1.1(h) I/O Memory map (00FF52H–00FF61H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FF53	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	General-purpose register	1	0	1	R/W	Reserved register
	D0	KCP10	K10 input comparison register	Falling edge	Rising edge	1	R/W	
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data			–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FF55	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	_		
	D4	–	–	–	–	_		
	D3	–	–	–	–	_		
	D2	–	–	–	–	_		
	D1	–	–	–	–	–		"1" when being read
	D0	K10D	K10 input port data	High level	Low level	–	R	
00FF60	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register			0	R/W	
	D5	IOC05	P05 I/O control register			0	R/W	
	D4	IOC04	P04 I/O control register			0	R/W	
	D3	IOC03	P03 I/O control register			0	R/W	
	D2	IOC02	P02 I/O control register			0	R/W	
	D1	IOC01	P01 I/O control register			0	R/W	
	D0	IOC00	P00 I/O control register			0	R/W	
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	

Table 5.1.1(i) I/O Memory map (00FF62H–00FF75H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF62	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data			1	R/W	
	D5	P05D	P05 I/O port data			1	R/W	
	D4	P04D	P04 I/O port data			1	R/W	
	D3	P03D	P03 I/O port data			1	R/W	
	D2	P02D	P02 I/O port data			1	R/W	
	D1	P01D	P01 I/O port data			1	R/W	
	D0	P00D	P00 I/O port data			1	R/W	
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data			1	R/W	
	D5	P15D	P15 I/O port data			1	R/W	
	D4	P14D	P14 I/O port data			1	R/W	
	D3	P13D	P13 I/O port data			1	R/W	
	D2	P12D	P12 I/O port data			1	R/W	
	D1	P11D	P11 I/O port data			1	R/W	
	D0	P10D	P10 I/O port data			1	R/W	
00FF70	D7	HZR51	R51 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR50	R50 high impedance control			0	R/W	
	D5	HZR4H	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR4L	General-purpose register			0	R/W	
	D3	HZR1H	General-purpose register			0	R/W	
	D2	HZR1L	General-purpose register			0	R/W	
	D1	HZR0H	General-purpose register			0	R/W	
	D0	HZR0L	General-purpose register			0	R/W	
00FF71	D7	HZR27	R27 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR26	R26 high impedance control			0	R/W	
	D5	HZR25	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR24	General-purpose register			0	R/W	
	D3	HZR23	General-purpose register			0	R/W	
	D2	HZR22	General-purpose register			0	R/W	
	D1	HZR21	General-purpose register			0	R/W	
	D0	HZR20	General-purpose register			0	R/W	
00FF72	D7	HZR37	General-purpose register	1	0	0	R/W	Reserved register
	D6	HZR36	General-purpose register			0	R/W	
	D5	HZR35	General-purpose register			0	R/W	
	D4	HZR34	R34 high impedance control	Hi-Z	Output	0	R/W	
	D3	HZR33	General-purpose register	1	0	0	R/W	Reserved register
	D2	HZR32	General-purpose register			0	R/W	
	D1	HZR31	General-purpose register			0	R/W	
	D0	HZR30	General-purpose register			0	R/W	
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data			1 *1	R/W	
	D5	R25D	General-purpose register	1	0	1	R/W	Reserved register
	D4	R24D	General-purpose register			1	R/W	
	D3	R23D	General-purpose register			1	R/W	
	D2	R22D	General-purpose register			1	R/W	
	D1	R21D	General-purpose register			1	R/W	
	D0	R20D	General-purpose register			1	R/W	

*1 "0" when $\overline{\text{TOUT}}$ output is selected by mask option.

Table 5.1.1(j) I/O Memory map (00FF76H–00FF82H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF76	D7	R37D	General-purpose register	1	0	1	R/W	Reserved register
	D6	R36D	General-purpose register			1	R/W	
	D5	R35D	General-purpose register			1	R/W	
	D4	R34D	R34 output port data	High	Low	1	R/W	
	D3	R33D	General-purpose register	1	0	1	R/W	Reserved register
	D2	R32D	General-purpose register			1	R/W	
	D1	R31D	General-purpose register			1	R/W	
	D0	R30D	General-purpose register			1	R/W	
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data			0	R/W	
00FF80	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PRAD	A/D converter clock control	On	Off	0	R/W	
	D2	PSAD2	A/D converter division ratio			0	R/W	
	D1	PSAD1	PSAD2 PSAD1 PSAD0 Division ratio 1 1 1 f_{OSC1} / 1 1 1 0 f_{OSC3} / 64 1 0 1 f_{OSC3} / 32 1 0 0 f_{OSC3} / 16 0 1 1 f_{OSC3} / 8 0 1 0 f_{OSC3} / 4 0 0 1 f_{OSC3} / 2 0 0 0 f_{OSC3} / 1			0	R/W	
	D0	PSAD0				0	R/W	
00FF81	D7	PAD7	P17 A/D converter input control	A/D converter input	I/O port	0	R/W	
	D6	PAD6	P16 A/D converter input control			0	R/W	
	D5	PAD5	P15 A/D converter input control			0	R/W	
	D4	PAD4	P14 A/D converter input control			0	R/W	
	D3	–	–	–	–	–		Constantly "0" when being read
	D2	–	–	–	–	–		
	D1	–	–	–	–	–		
	D0	–	–	–	–	–		
00FF82	D7	ADRUN	A/D conversion start control register	Start	Invalid	0	W	Constantry "0" when being read
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	
	D4	–	–	–	–	–	–	
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	CHS1	Analog input channel selection			0	R/W	
	D0	CHS0	CHS1 CHS0 Input channel 1 1 AD7 1 0 AD6 0 1 AD5 0 0 AD4			0	R/W	

Table 5.1.1(k) I/O Memory map (00FF83H–00FF84H)

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF83	D7	ADDR9	A/D conversion result D9 (MSB)			–	R	
	D6	ADDR8	A/D conversion result D8			–	R	
	D5	ADDR7	A/D conversion result D7			–	R	
	D4	ADDR6	A/D conversion result D6			–	R	
	D3	ADDR5	A/D conversion result D5			–	R	
	D2	ADDR4	A/D conversion result D4			–	R	
	D1	ADDR3	A/D conversion result D3			–	R	
	D0	ADDR2	A/D conversion result D2			–	R	
00FF84	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	ADDR1	A/D conversion result D1			–	R	
	D0	ADDR0	A/D conversion result D0 (LSB)			–	R	

5.2 Watchdog Timer

5.2.1 Configuration of watchdog timer

The E0C88816 is equipped with a watchdog timer driven by OSC1 as source oscillation. The watchdog timer must be reset periodically in software, and if reset of more than 3–4 seconds (when f_{OSC1} = 32.768 kHz) does not take place, a non-maskable interrupt signal is generated and output to the CPU.

Figure 5.2.1.1 is a block diagram of the watchdog timer.

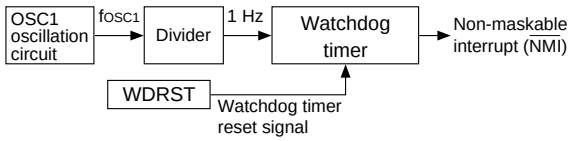


Fig. 5.2.1.1 Block diagram of watchdog timer

By running watchdog timer reset during the main routine of the program, it is possible to detect program runaway as if watchdog timer processing had not been applied. Normally, this routine is integrated at points that are regularly being processed.

The watchdog timer continues to operate during HALT and when a HALT state is continuous for longer than 3–4 seconds, the CPU shifts to exception processing.
During SLEEP, the watchdog timer is stopped.

5.2.2 Interrupt function

In cases where the watchdog timer is not periodically reset in software, the watchdog timer outputs an interrupt signal to the CPU's $\overline{NMI}$ (level 4) input. Unmaskable and taking priority over other interrupts, this interrupt triggers the generation of exception processing. See the "E0C88 Core CPU Manual" for more details on $\overline{NMI}$ exception processing.
This exception processing vector is set at 000004H.

5.2.3 I/O memory for watchdog timer

Table 5.2.3.1 shows the control bits for the watchdog timer.

WDRST: 00FF40H•D2

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" to WDRST, the watchdog timer is reset, after which it is immediately restarted.
Writing "0" will mean no operation.
Since WDRST is for writing only, it is constantly set to "0" during readout.

5.2.4 Programming notes

(1) The watchdog timer must reset within 3-second cycles by software.

(2) Do not execute the SLP instruction for 2 msec after a $\overline{NMI}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

Table 5.2.3.1 Watchdog timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
			FOUT2 FOUT1 FOUT0 Frequency					
			0 0 0 f_{OSC1} / 1					
	D5	FOUT1	0 0 1 f_{OSC1} / 2			0	R/W	
			0 1 0 f_{OSC1} / 4					
			0 1 1 f_{OSC1} / 8					
			1 0 0 f_{OSC3} / 1					
	D4	FOUT0	1 0 1 f_{OSC3} / 2			0	R/W	
			1 1 0 f_{OSC3} / 4					
			1 1 1 f_{OSC3} / 8					
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	

5.3 Oscillation Circuits and Operating Mode

5.3.1 Configuration of oscillation circuits

The E0C88816 is twin clock system with two internal oscillation circuits (OSC1 and OSC3). The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) main clock and the OSC3 oscillation circuit generates the sub-clock when the CPU and some peripheral circuits (output port, serial interface and programmable timer) are in high speed operation. Figure 5.3.1.1 shows the configuration of the oscillation circuit.

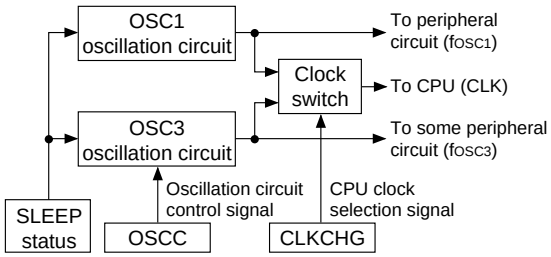


Fig. 5.3.1.1 Configuration of oscillation circuits

At initial reset, the OSC1 oscillation circuit is selected for the CPU operating clock and the OSC3 oscillation circuit is in a stopped state. ON / OFF switching of the OSC3 oscillation circuit and switching of the system clock between OSC1 and OSC3 are controlled in software. The OSC3 circuit is utilized when high speed operation of the CPU and some peripheral circuits become necessary. Otherwise, OSC1 should be used to generate the operating clock and the OSC3 circuit placed in a stopped state in order to reduce current consumption.

5.3.2 Mask option

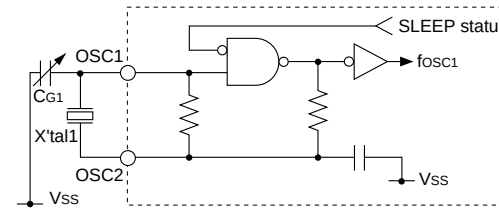
OSC1 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ External clock input
- ☐ CR oscillation circuit
- ☐ Crystal oscillation circuit (gate capacitor built-in)

OSC3 oscillation circuit
- ☐ Crystal oscillation circuit
- ☐ Ceramic oscillation circuit
- ☐ CR oscillation circuit
- ☐ External clock input

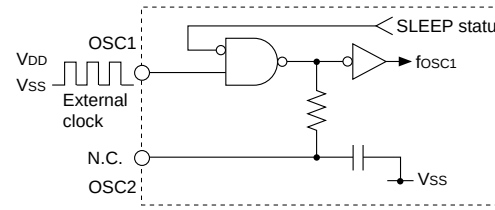
In terms of the oscillation circuit types for OSC1, either crystal oscillation, CR oscillation, crystal oscillation (gate capacitor built-in) or external clock input can be selected with the mask option.
In terms of oscillation circuit types for OSC3, either crystal oscillation, ceramic oscillation, CR oscillation or external clock input can be selected with the mask option, in the same way as OSC1.

5.3.3 OSC1 oscillation circuit

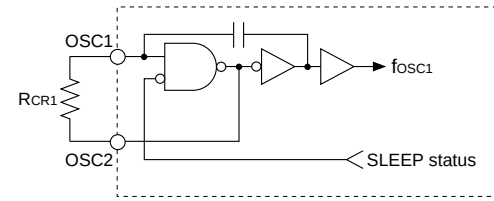
The OSC1 oscillation circuit generates the 32.768 kHz (Typ.) system clock which is utilized during low speed operation (low power mode) of the CPU and peripheral circuits. Furthermore, even when OSC3 is utilized as the system clock, OSC1 continues to generate the source clock for the clock timer and stopwatch timer.
This oscillation circuit stops when the SLP instruction is executed. However, in case the SVD circuit is runninging at this time, oscillation is stopped in synchronization with the completion of sampling.
In terms of the oscillation circuit types, either crystal oscillation, CR oscillation, crystal oscillation (gate capacitor built-in) or external clock input can be selected with the mask option.
Figure 5.3.3.1 shows the configuration of the OSC1 oscillation circuit.



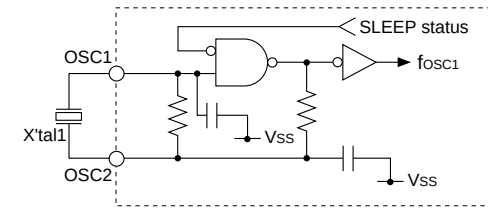
(1) Crystal oscillation circuit



(2) External clock input



(3) CR oscillation circuit



(4) Crystal oscillation circuit (gate capacitor built-in)

Fig. 5.3.3.1 OSC1 oscillation circuit

When crystal oscillation is selected, a crystal oscillation circuit can be easily formed by connecting a crystal oscillator X'tal1 (Typ. 32.768 kHz) between the OSC1 and OSC2 terminals along with a trimmer capacitor C_{G1} (5–30 pF) between the OSC1 terminal and V_{SS}.
In addition, the gate capacitor C_{G1} (15 pF) can be built into the circuit by the mask option.
When CR oscillation is selected, connect a resistor (R_{CR1}) between the OSC1 and OSC2 terminals.
When external input is selected, release the OSC2 terminal and input the rectangular wave clock into the OSC1 terminal.

5.3.4 OSC3 oscillation circuit

The OSC3 oscillation circuit generates the system clock when the CPU and some peripheral circuits (output port, serial interface and programmable timer) are in high speed operation.
This oscillation circuit stops when the SLP instruction is executed, or the OSCC register is set to "0".
In terms of oscillation circuit types, any one of crystal oscillation, ceramic oscillation, CR oscillation or external clock input can be selected with the mask option. Figure 5.3.4.1 shows the configuration of the OSC3 oscillation circuit.

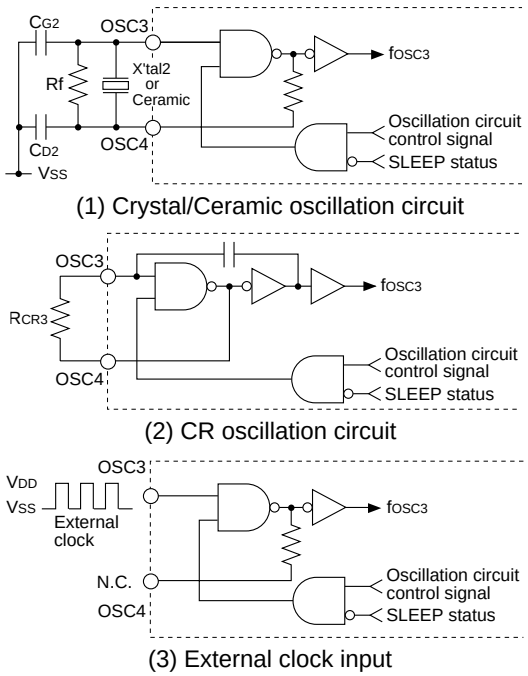


Fig. 5.3.4.1 OSC3 oscillation circuit

When crystal or ceramic oscillation circuit is selected, the crystal or ceramic oscillation circuit are formed by connecting either a crystal oscillator (X'tal2) or a combination of ceramic oscillator (Ceramic) and feedback resistor (Rf) between OSC3 and OSC4 terminals and connecting two capacitors (C_{G2}, C_{D2}) between the OSC3 terminal and V_{SS}, and between the OSC4 terminal and V_{SS}, respectively.

When CR oscillation is selected, the CR oscillation circuit is formed merely by connecting a resistor (R_{CR3}) between OSC3 and OSC4 terminals.
When external input is selected, release the OSC4 terminal and input the rectangular wave clock into the OSC3 terminal.

5.3.5 Operating mode

You can select three types of operating modes using software, to obtain a stable operation and good characteristics (operating frequency and current consumption) over a broad operation voltage. Here below are indicated the features of the respective modes.

- **Normal mode (V_{DD} = 2.4 V–5.5 V)**
  This mode is set following the initial reset. It permits the OSC3 oscillation circuit (Max. 4.2 MHz) to be used and also permits relative low power operation.
- **Low power mode (V_{DD} = 1.8 V–5.5 V)**
  This is a lower power mode than the normal mode. It makes ultra-low power consumption possible by operation on the OSC1 oscillation circuit, although the OSC3 circuit cannot be used.
- **High speed mode (V_{DD} = 3.5 V–5.5 V)**
  This mode permits higher speed operation than the normal mode. Since the OSC3 oscillation circuit (Max. 8.2 MHz) can be used, you should use this mode, when you require operation at 4.2 MHz or more. However, the current consumption will increase relative to the normal mode.

Using software to switch over among the above three modes to meet your actual usage circumstances will make possible a low power system. For example, you will be able to reduce current consumption by switching over to the normal mode when using the OSC3 as the CPU clock and, conversely, changing over to the low power mode when using the OSC1 as the CPU clock (OSC3 oscillation circuit is OFF).

Note: Do not turn the OSC3 oscillation circuit ON in the low power mode. Do not switch over the operating mode (normal mode ↔ high speed mode) in the OSC3 oscillation circuit ON status, as this will cause faulty operation.
You can not use two modes, the low power mode and the high speed mode on one application, with respect to the operating voltages.
When CR oscillation is selected for the OSC1 oscillation circuit, the operating mode is fixed in the normal mode to stabilize the oscillation frequency. Consequently, settings of the mode setting registers VDC0 and VDC1 become invalid.

5.3.6 Switching the CPU clocks

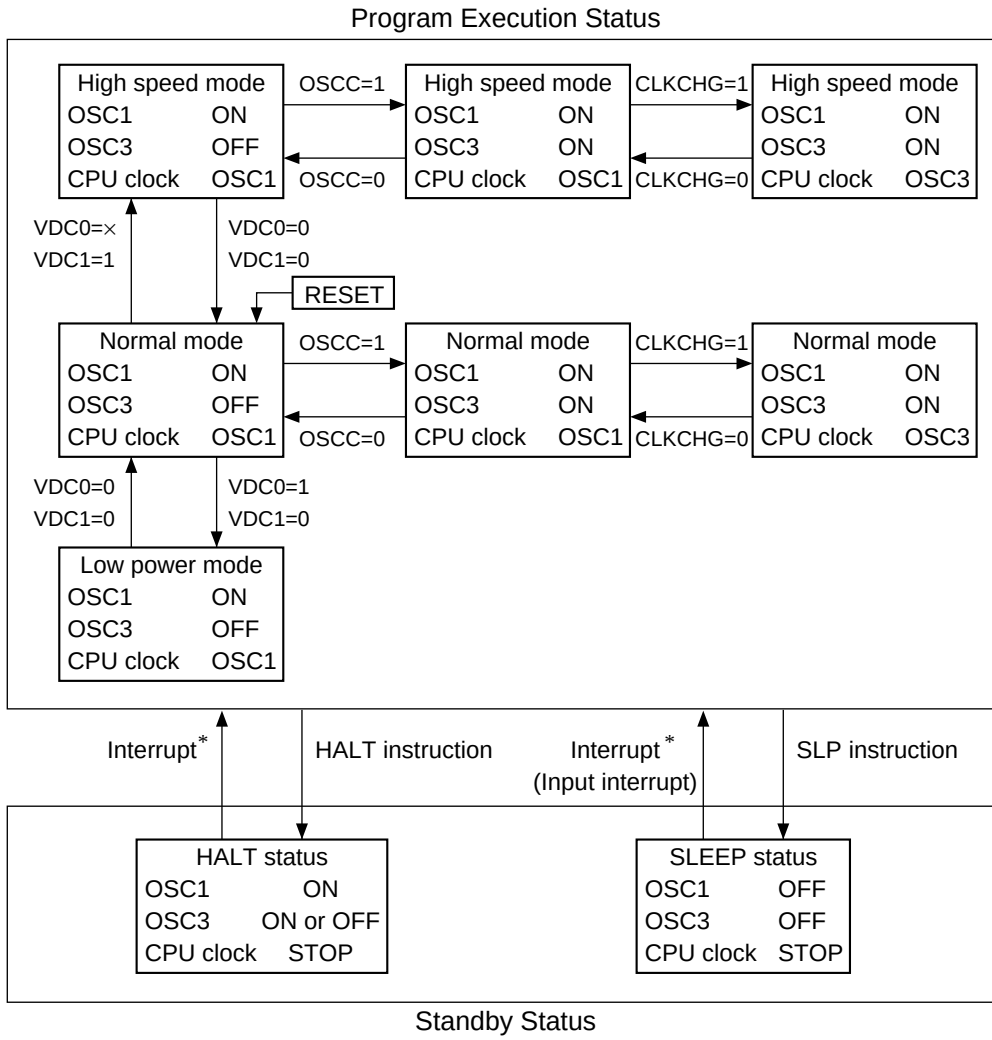
You can use either OSC1 or OSC3 as the system clock for the CPU and you can switch over by means of software.
You can save power by turning the OSC3 oscillation circuit off while the CPU is operating in OSC1. When you must operate on OSC3, you can change to high speed operation by turning the OSC3 oscillation circuit ON and switching over the system clock. In this case, since several msec to several 10 msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON, you should switch over the clock after stabilization time has elapsed. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)

When switching over from the OSC3 to the OSC1, turn the OSC3 oscillation circuit OFF immediately following the clock changeover.

The basic clock switching procedure is as described above, however, you must also combine it with the changeover of the operating mode to permit low current consumption and high speed operation.

Figure 5.3.6.1 indicates the status transition diagram for the operation mode and clock changeover.

Note: When turning ON the OSC3 oscillation circuit after switching the operating mode, you should allow a minimum waiting time of 5 msec.



* The return destination from the standby status becomes the program execution status prior to shifting to the standby status

Fig. 5.3.6.1 Status transition diagram for the operation mode and clock changeover

5.3.7 I/O memory for oscillation circuit

Table 5.3.7.1 shows the control bits for the oscillation circuits and operating modes.

Table 5.3.7.1 Oscillation circuit and operating mode control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF02	D7	EBR	General-purpose register	1	0	0	R/W	Reserved register
	D6	WT2	General-purpose register			0	R/W	
	D5	WT1	General-purpose register			0	R/W	
	D4	WT0	General-purpose register			0	R/W	
	D3	CLKCHG	CPU operating clock switch	OSC3	OSC1	0	R/W	
	D2	OSCC	OSC3 oscillation On/Off control	On	Off	0	R/W	
	D1	VDC1	Operating mode selection			0	R/W	
	D0	VDC0				0	R/W	

VDC1	VDC0	Operating mode
1	×	High speed (V_{D1}=3.3V)
0	1	Low power (V_{D1}=1.3V)
0	0	Normal (V_{D1}=2.2V)

VDC1, VDC0: 00FF02H•D1, D0

Selects the operating mode according to supply voltage and operating frequency.
Table 5.3.7.2 shows the correspondence between register preset values and operating modes.

Table 5.3.7.2 Correspondence between register preset values and operating modes

Operating mode	VDC1	VDC0	V_{D1}	Power voltage	Operating frequency
Normal mode	0	0	2.2 V	2.4–5.5 V	4.2 MHz (Max.)
Low power mode	0	1	1.3 V	1.8–5.5 V	80 kHz (Max.)
High speed mode	1	×	3.3 V	3.5–5.5 V	8.2 MHz (Max.)

* The V_{D1} voltage is the value where V_{SS} has been made the standard (GND).

At initial reset, this register is set to "0" (normal mode).

OSCC: 00FF02H•D2

Controls the ON and OFF settings of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When the CPU and some peripheral circuits (output port, serial interface and programmable timer) are to be operated at high speed, OSCC is to be set to "1". At all other times, it should be set to "0" in order to reduce current consumption.
At initial reset, OSCC is set to "0" (OSC3 oscillation OFF).

CLKCHG: 00FF02H•D3

Selects the operating clock for the CPU.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

When the operating clock for the CPU is switched to OSC3, CLKCHG should be set to "1" and when the clock is switched to OSC1, CLKCHG should be set to "0".
At initial reset, CLKCHG is set to "0" (OSC1 clock).

5.3.8 Programming notes

(1) When the high speed CPU operation is not necessary, you should operate the peripheral circuits according to the setting outline indicate below.

- CPU operating clock
  OSC1
- OSC3 oscillation circuit
  OFF (When the OSC3 clock is not necessary for some peripheral circuits.)
- Operating mode
  Low power mode
  or Normal mode

(2) Do not turn the OSC3 oscillation circuit ON in the low power mode.
Do not switch over the operating mode (normal mode ↔ high speed mode) in the OSC3 oscillation circuit ON status, as this will cause faulty operation.

(3) When turning ON the OSC3 oscillation circuit after switching the operating mode, you should allow a minimum waiting time of 5 msec.

(4) Since several msec to several 10 msec are necessary for the oscillation to stabilize after turning the OSC3 oscillation circuit ON. Consequently, you should switch the CPU operating clock (OSC1 → OSC3) after allowing for a sufficient waiting time once the OSC3 oscillation goes ON. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)

(5) When switching the clock from OSC3 to OSC1, be sure to switch OSC3 oscillation OFF with separate instructions. Using a single instruction to process simultaneously can cause a malfunction of the CPU.

5.4 Input Ports (K ports)

5.4.1 Configuration of input ports

The E0C88816 is equipped with 9 input port bits (K00–K07 and K10) which are usable as general purpose input port terminals with interrupt function.

K10 terminal doubles as the external clock (EVIN) input terminal of the programmable timer (event counter) with input port functions sharing the input signal as is. (See "5.10 Programmable Timer")

Each input port is equipped with a pull-up resistor. The mask option can be used to select either "With resistor" or "Gate direct" for each input port. Figure 5.4.1.1 shows the structure of the input port.

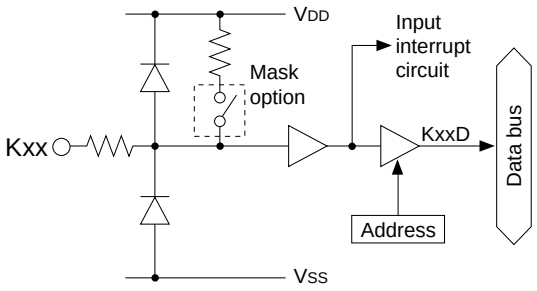


Fig. 5.4.1.1 Structure of input port

Each input port terminal is directly connected via a three-state buffer to the data bus. Furthermore, the input signal state at the instant of input port readout is read in that form as data.

5.4.2 Mask option

Input port pull-up resistors

K00	☐ With resistor	☐ Gate direct
K01	☐ With resistor	☐ Gate direct
K02	☐ With resistor	☐ Gate direct
K03	☐ With resistor	☐ Gate direct
K04	☐ With resistor	☐ Gate direct
K05	☐ With resistor	☐ Gate direct
K06	☐ With resistor	☐ Gate direct
K07	☐ With resistor	☐ Gate direct
K10	☐ With resistor	☐ Gate direct

Input ports K00–K07 and K10 are all equipped with pull-up resistors. The mask option can be used to select 'With resistor' or 'Gate direct' for each port (bit).

The 'With resistor' option is rendered suitable for purposes such as push switch or key matrix input. When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

When 'Gate direct' is selected, the pull-up resistor is detached and the port is rendered suitable for purposes such as slide switch input and interfacing with other LSIs.
In this case, take care that a floating state does not occur in input.

For unused input ports, select the default setting of "With resistor".

5.4.3 Interrupt function and input comparison register

Input port K00–K07 and K10 are all equipped with an interrupt function. These input ports are divided into three groupings: K00–K03 (K0L), K04–K07 (K0H) and K10 (K1). Furthermore, the interrupt generation condition for each series of terminals can be set by software.
When the interrupt generation condition set for each series of terminals is met, the interrupt factor flag FK0L, FK0H or FK1 corresponding to the applicable series is set at "1" and an interrupt is generated.
Interrupt can be prohibited by setting the interrupt enable registers EK0L, EK0H and EK1 for the corresponding interrupt factor flags.
Furthermore, the priority level for input interrupt can be set at the desired level (0–3) using the interrupt priority registers PK00–PK01 and PK10–PK11 corresponding to each of two groups K0x (K00–K07) and K10.
For details on the interrupt control registers for the above and on operations subsequent to interrupt generation, see "5.16 Interrupt and Standby Status".

The exception processing vectors for each interrupt factor are set as follows:

K10 input interrupt:	00000AH
K04–K07 input interrupt:	00000CH
K00–K03 input interrupt:	00000EH

Figure 5.4.3.1 shows the configuration of the input interrupt circuit.

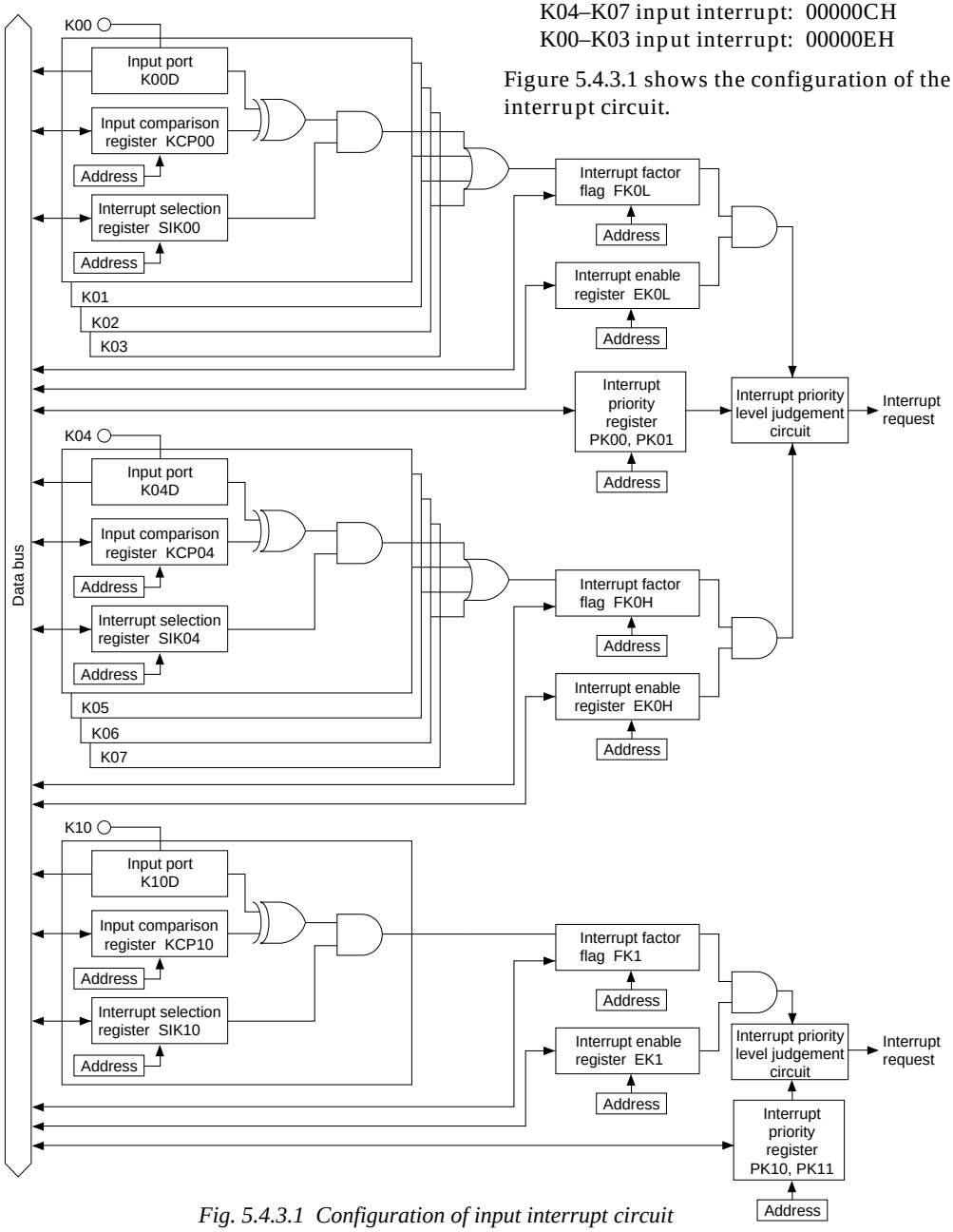


Fig. 5.4.3.1 Configuration of input interrupt circuit

The interrupt selection registers SIK00–SIK03, SIK04–SIK07 and SIK10 and input comparison registers KCP00–KCP03, KCP04–KCP07 and KCP10 for each port are used to set the interrupt generation condition described above.

Input port interrupt can be permitted or prohibited by the setting of the interrupt selection register SIK. In contrast to the interrupt enable register EK which masks the interrupt factor for each series of terminals, the interrupt selection register SIK is masks the bit units.

The input comparison register KCP selects whether the interrupt for each input port will be generated on the rising edge or the falling edge of input.

When the data content of the input terminals in which interrupt has been permitted by the interrupt selection register SIK and the data content of the input comparison register KCP change from a conformity state to a non-conformity state, the interrupt factor flag FK should be set to "1" and an interrupt is generated.

Figure 5.4.3.2 shows an example of interrupt generation in the series of terminals K0L (K00–K03).

Because interrupt has been prohibited for K00 by the interrupt selection register SIK00, with the settings as shown in (2), an interrupt will not be generated.
Since K03 is "0" in the next settings (3) in the figure, the non-conformity between the input terminal data K01–K03 where interrupt is permitted and the data from the input comparison registers KCP01–KCP03 generates an interrupt.
In line with the explanation above, since the change in the contents of input data and input comparison registers KCP from a conformity state to a non-conformity state introduces an interrupt generation condition, switching from one non-conformity state to another, as is the case in (4) in the figure, will not generate an interrupt. Consequently, in order to be able to generate a second interrupt, either the input terminal must be returned to a state where its content is once again in conformity with that of the input comparison register KCP, or the input comparison register KCP must be reset.
Input terminals for which interrupt is prohibited will not influence an interrupt generation condition.

Interrupt is generated in exactly the same way in the other two series of terminals K0H (K04–K07) and K1 (K10).

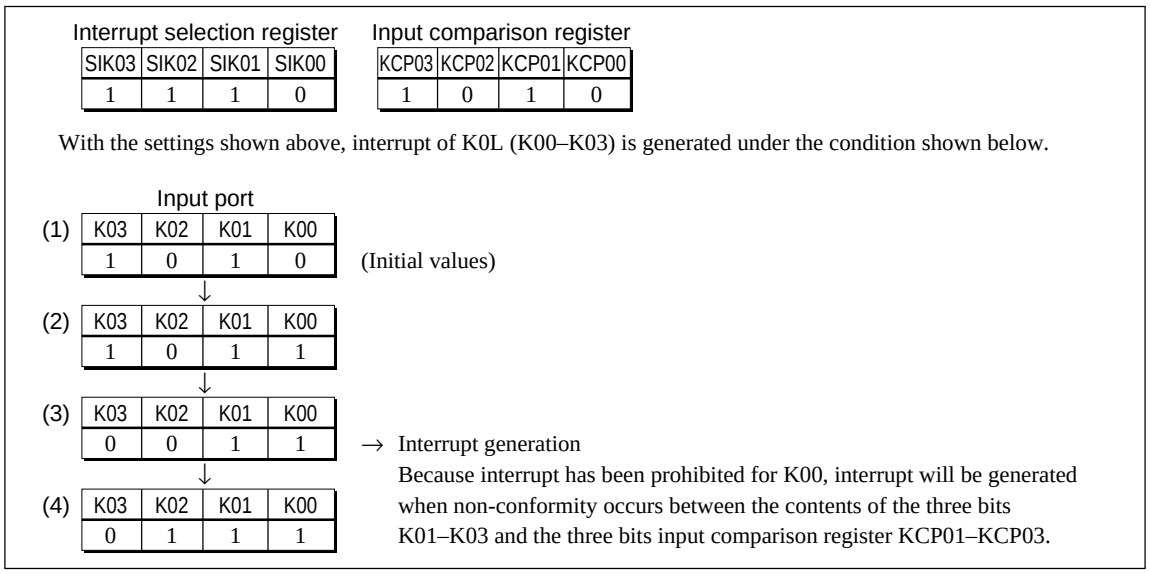


Fig. 5.4.3.2 Interrupt generation example in K0L (K00–K03)

5.4.4 I/O memory for input ports

Table 5.4.4.1 shows the input port control bits.

Table 5.4.4.1(a) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF50	D7	SIK07	K07 interrupt selection register	Interrupt enable	Interrupt disable	0	R/W	
	D6	SIK06	K06 interrupt selection register			0	R/W	
	D5	SIK05	K05 interrupt selection register			0	R/W	
	D4	SIK04	K04 interrupt selection register			0	R/W	
	D3	SIK03	K03 interrupt selection register			0	R/W	
	D2	SIK02	K02 interrupt selection register			0	R/W	
	D1	SIK01	K01 interrupt selection register			0	R/W	
	D0	SIK00	K00 interrupt selection register			0	R/W	
00FF51	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SIK11	General-purpose register	1	0	0	R/W	Reserved register
	D0	SIK10	K10 interrupt selection register	Enable	Disable	0	R/W	
00FF52	D7	KCP07	K07 input comparison register	Interrupt generated at falling edge	Interrupt generated at rising edge	1	R/W	
	D6	KCP06	K06 input comparison register			1	R/W	
	D5	KCP05	K05 input comparison register			1	R/W	
	D4	KCP04	K04 input comparison register			1	R/W	
	D3	KCP03	K03 input comparison register			1	R/W	
	D2	KCP02	K02 input comparison register			1	R/W	
	D1	KCP01	K01 input comparison register			1	R/W	
	D0	KCP00	K00 input comparison register			1	R/W	
00FF53	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	KCP11	General-purpose register	1	0	1	R/W	Reserved register
	D0	KCP10	K10 input comparison register	Falling edge	Rising edge	1	R/W	
00FF54	D7	K07D	K07 input port data	High level input	Low level input	–	R	
	D6	K06D	K06 input port data			–	R	
	D5	K05D	K05 input port data			–	R	
	D4	K04D	K04 input port data			–	R	
	D3	K03D	K03 input port data			–	R	
	D2	K02D	K02 input port data			–	R	
	D1	K01D	K01 input port data			–	R	
	D0	K00D	K00 input port data			–	R	
00FF55	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	_		Constantly "0" when
	D4	–	–	–	–	_		being read
	D3	–	–	–	–	_		
	D2	–	–	–	–	_		
	D1	–	–	–	–	–		"1" when being read
	D0	K10D	K10 input port data	High level	Low level	–	R	

Table 5.4.4.1(b) Input port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 Priority PTM1 PTM0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 Priority PK11 PK10 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

K00D–K07D: 00FF54H
K10D: 00FF55H•D0

Input data of input port terminal Kxx can be read out.

When "1" is read: HIGH level
When "0" is read: LOW level
Writing: Invalid

The terminal voltage of each of the input port K00–K07 and K10 can be directly read out as either a "1" for HIGH (V_{DD}) level or a "0" for LOW (V_{SS}) level. This bit is exclusively for readout and are not usable for write operations.

SIK00–SIK07: 00FF50H
SIK10: 00FF51H•D0

Sets the interrupt generation condition (interrupt permission / prohibition) for input port terminals K00–K07 and K10.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

SIKxx is the interrupt selection register which correspond to the input port Kxx. A "1" setting permits interrupt in that input port and a "0" prohibits it. Changes of state in an input terminal in which interrupt is prohibited, will not influence interrupt generation.
At initial reset, this register is set to "0" (interrupt prohibited).

KCP00–KCP07: 00FF52H
KCP10: 00FF53H•D0

Sets the interrupt generation condition (interrupt generation timing) for input port terminals K00–K07 and K10.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

KCPxx is the input comparison register which correspond to the input port Kxx. Interrupt in those ports which have been set to "1" is generated on the falling edge of the input and in those set to "0" on the rising edge.
At initial reset, this register is set to "1" (falling edge).

PK00, PK01: 00FF20H•D6, D7
PK10, PK11: 00FF21H•D0, D1

Sets the input interrupt priority level. The two bits PK00 and PK01 are the interrupt priority registers corresponding to the interrupts for K00–K07 (K0L and K0H). Corresponding to K10 (K1), the two bits PK10 and PK11 perform the same function.
Table 5.4.4.2 shows the interrupt priority level which can be set by this register.

Table 5.4.4.2 Interrupt priority level settings

PK11 PK01	PK10 PK00	Interrupt priority level
1	1	Level 3 ($\overline{\text{IRQ3}}$)
1	0	Level 2 ($\overline{\text{IRQ2}}$)
0	1	Level 1 ($\overline{\text{IRQ1}}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EK0L, EK0H, EK1: 00FF23H•D3, D4, D5

How interrupt generation to the CPU is permitted or prohibited.

When "1" is written: Interrupt permitted
When "0" is written: Interrupt prohibited
Reading: Valid

The interrupt enable register EK0L corresponds to K00–K03, EK0H to K04–K07, and EK1 to K10. Interrupt is permitted in those series of terminals set to "1" and prohibited in those set to "0".
At initial reset, this register is set to "0" (interrupt prohibited).

FK0L, FK0H, FK1: 00FF25H•D3, D4, D5

Indicates the generation state for an input interrupt.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Reset factor flag
When "0" is written: Invalid

The interrupt factor flag FK0L corresponds to K00–K03, FK0H to K04–K07, and FK1 to K10 and they are set to "1" by the occurrence of an interrupt generation condition.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is all reset to "0".

5.4.5 Programming note

When changing the input terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an input port. In particular, special attention should be paid to key scan for key matrix formation. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

5.5 Output Ports (R ports)

5.5.1 Configuration of output ports

The E0C88816 is equipped with 5 bits of output ports (R26, R27, R34, R50 and R51).
Furthermore, 2 bits of melody output ports MOUT and $\overline{\text{MOUT}}$ are available.
Figure 5.5.1.1 shows the basic structure (excluding special and melody output circuits) of the output ports.
The output specification of each port is fixed at complementary output.

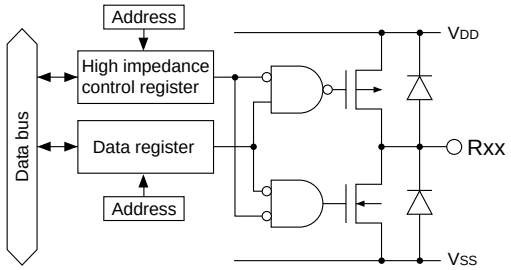


Fig. 5.5.1.1 Structure of output ports

Each output port can be set into high impedance state by software.
Besides normal DC output, the output ports have special output functions. The R27, R34 and R50 functions can be selected by software and the R26 and R51 functions can be selected by mask option.
Figure 5.5.1.2 shows the basic structure of the melody output port. The output specification is fixed at complementary output. This circuit has no high-impedance control function and data register, and is driven by the melody generator directly.

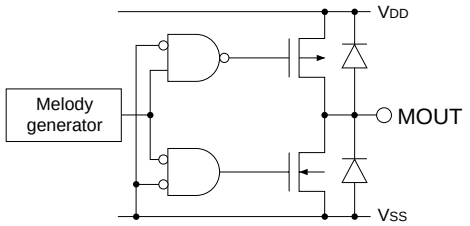


Fig. 5.5.1.2 Structure of melody output port

5.5.2 Mask option

R26 and R51 output port specifications
R26 ..... ☐ DC output ☐ $\overline{\text{TOUT}}$ output
R51 ..... ☐ DC output ☐ $\overline{\text{BZ}}$ output

The mask option allows selection of special outputs for the R26 and R51 output ports as well as the DC output. The R26 port can be set as the $\overline{\text{TOUT}}$ output port (TOUT signal inverted output) and the R51 port can be set as the $\overline{\text{BZ}}$ output port (buzzer signal inverted output).

5.5.3 High impedance control

The output port can be high impedance controlled in software.

A high impedance control register is set for each output port terminal as shown below. Either complementary output and high impedance state can be selected with this register.

HZR26: R26 high impedance control register
HZR27: R27 high impedance control register
HZR34: R34 high impedance control register
HZR50: R50 high impedance control register
HZR51: R51 high impedance control register

When a high impedance control register HZRxx is set to "1", the corresponding output port terminal becomes high impedance state and when set to "0", it becomes complementary output.

5.5.4 DC output

As Figure 5.5.1.1 shows, when "1" is written to the output port data register, the output terminal switches to HIGH (V_{DD}) level and when "0" is written it switches to LOW (V_{SS}) level. When output is in a high impedance state, the data written to the data register is output from the terminal at the instant when output is switched to complementary.

5.5.5 Special output

Besides normal DC output, each output port can also be assigned special output function in software (R27, R34, R50) or mask option (R26, R51) as shown in Table 5.5.5.1.

Table 5.5.5.1 Special output ports

Output port	Special output
R26	$\overline{\text{TOUT}}$ output (mask option)
R27	TOUT output (software selection)
R34	FOUT output (software selection)
R50	BZ output (software selection)
R51	$\overline{\text{BZ}}$ output (mask option)

■ TOUT output (R27), $\overline{\text{TOUT}}$ output (R26)

In order for the E0C88816 to provide clock signal to an external device, the R27 output port terminal can be used to output the TOUT signal (clock output by the programmable timer). Furthermore, the R26 output port terminal can be used to output the $\overline{\text{TOUT}}$ signal (TOUT inverted signal). The configuration of the output ports R26 and R27 is shown in Figure 5.5.5.1.

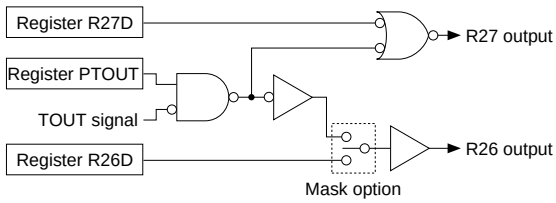


Fig. 5.5.5.1 Configuration of R26 and R27

The output control for the TOUT ($\overline{\text{TOUT}}$) signals is done by the register PTOUT. When you set "1" for the PTOUT, the TOUT ($\overline{\text{TOUT}}$) signal is output from the R27 (R26) output port terminal. When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D.
The data register R26D does not affect the $\overline{\text{TOUT}}$ output.

The TOUT signal is generated from the programmable timer underflow signal by halving the frequency.
With respect to frequency control, see "5.10 Programmable Timer".
Since the TOUT ($\overline{\text{TOUT}}$) signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by setting the register, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.2 shows the output waveform of the TOUT ($\overline{\text{TOUT}}$) signal.

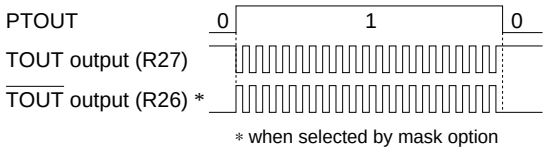


Fig. 5.5.5.2 TOUT ($\overline{\text{TOUT}}$) output waveform

■ FOUT output (R34)

In order for the E0C88816 to provide clock signal to an external device, the FOUT signal (divided clock of oscillation clock f_{OSC1} or f_{OSC3}) can be output from the output port terminal R34.
Figure 5.5.5.3 shows the configuration of output port R34.

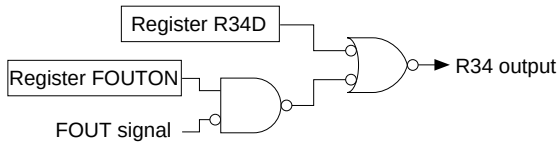


Fig. 5.5.5.3 Configuration of R34

The output control for the FOUT signal is done by the register FOUTON. When you set "1" for the FOUTON, the FOUT signal is output from the output port terminal R34, when "0" is set, the HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R34D.
The frequency of the FOUT signal can be selected in software by setting the registers FOUT0–FOUT2. The frequency is selected any one from among eight settings as shown in Table 5.5.5.2.

Table 5.5.5.2 FOUT frequency setting

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	f_{OSC1} / 1
0	0	1	f_{OSC1} / 2
0	1	0	f_{OSC1} / 4
0	1	1	f_{OSC1} / 8
1	0	0	f_{OSC3} / 1
1	0	1	f_{OSC3} / 2
1	1	0	f_{OSC3} / 4
1	1	1	f_{OSC3} / 8

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

When the FOUT frequency is made "f_{OSC3} / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF state.

Since the FOUT signal is generated asynchronously from the register FOUTON, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.4 shows the output waveform of the FOUT signal.

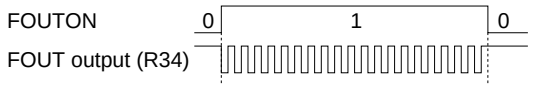


Fig. 5.5.5.4 Output waveform of FOUT signal

■ BZ output (R50), $\overline{BZ}$ output (R51)

In order for the E0C88816 to drive an external buzzer, the BZ signal (sound generator output) can be output from the output port terminal R50. Furthermore, the R51 output port terminal can be used to output the $\overline{BZ}$ signal (BZ inverted signal). The configuration of the output ports R50 and R51 is shown in Figure 5.5.5.5.

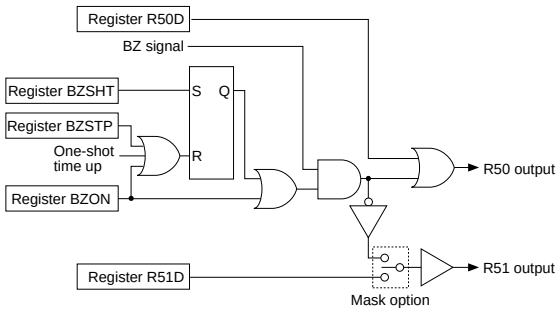


Fig. 5.5.5.5 Configuration of R50 and R51

The output control for the BZ ($\overline{BZ}$) signal is done by the registers BZON, BZSHT and BZSTP. When you set "1" for the BZON or BZSHT, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set for the BZON or "1" is set for the BZSTP, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.

The BZ ($\overline{BZ}$) signal is generated by the sound generator. With respect to control of frequency and envelope, see "5.12 Sound Generator".
Since the BZ ($\overline{BZ}$) signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by setting the registers, a hazard of a 1/2 cycle or less is generated.
Figure 5.5.5.6 shows the output waveform of the BZ ($\overline{BZ}$) signal.

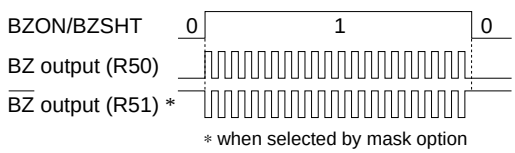


Fig. 5.5.5.6 BZ ($\overline{BZ}$) output waveform

■ MOUT and $\overline{MOUT}$ outputs

MOUT and $\overline{MOUT}$ are the output ports dedicated to direct driving an external piezoelectric buzzer with the melody signal. These ports are fixed at complementary output and cannot be set into high-impedance state. Also data register is not available. At initial reset, the MOUT and $\overline{MOUT}$ terminals go HIGH.
See "5.13 Melody Generator" for melody output.

5.5.6 I/O memory for output ports

Table 5.5.6.1 shows the output port control bits.

Table 5.5.6.1(a) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF70	D7	HZR51	R51 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR50	R50 high impedance control			0	R/W	
	D5	HZR4H	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR4L	General-purpose register			0	R/W	
	D3	HZR1H	General-purpose register			0	R/W	
	D2	HZR1L	General-purpose register			0	R/W	
	D1	HZR0H	General-purpose register			0	R/W	
	D0	HZR0L	General-purpose register			0	R/W	
00FF71	D7	HZR27	R27 high impedance control	Hi-Z	Output	0	R/W	
	D6	HZR26	R26 high impedance control			0	R/W	
	D5	HZR25	General-purpose register	1	0	0	R/W	Reserved register
	D4	HZR24	General-purpose register			0	R/W	
	D3	HZR23	General-purpose register			0	R/W	
	D2	HZR22	General-purpose register			0	R/W	
	D1	HZR21	General-purpose register			0	R/W	
	D0	HZR20	General-purpose register			0	R/W	
00FF72	D7	HZR37	General-purpose register	1	0	0	R/W	Reserved register
	D6	HZR36	General-purpose register			0	R/W	
	D5	HZR35	General-purpose register			0	R/W	
	D4	HZR34	R34 high impedance control	Hi-Z	Output	0	R/W	
	D3	HZR33	General-purpose register	1	0	0	R/W	Reserved register
	D2	HZR32	General-purpose register			0	R/W	
	D1	HZR31	General-purpose register			0	R/W	
	D0	HZR30	General-purpose register			0	R/W	
00FF75	D7	R27D	R27 output port data	High	Low	1	R/W	
	D6	R26D	R26 output port data			1 *1	R/W	
	D5	R25D	General-purpose register	1	0	1	R/W	Reserved register
	D4	R24D	General-purpose register			1	R/W	
	D3	R23D	General-purpose register			1	R/W	
	D2	R22D	General-purpose register			1	R/W	
	D1	R21D	General-purpose register			1	R/W	
	D0	R20D	General-purpose register			1	R/W	
00FF76	D7	R37D	General-purpose register	1	0	1	R/W	Reserved register
	D6	R36D	General-purpose register			1	R/W	
	D5	R35D	General-purpose register			1	R/W	
	D4	R34D	R34 output port data	High	Low	1	R/W	
	D3	R33D	General-purpose register	1	0	1	R/W	Reserved register
	D2	R32D	General-purpose register			1	R/W	
	D1	R31D	General-purpose register			1	R/W	
	D0	R30D	General-purpose register			1	R/W	
00FF78	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	R51D	R51 output port data	High	Low	1	R/W	
	D0	R50D	R50 output port data			0	R/W	

*1 "0" when $\overline{\text{TOUT}}$ output is selected by mask option.

Table 5.5.6.1(b) Output port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	–	–	–	–	–		Constantry "0" when
	D6	–	–	–	–	–		being read
	D5	–	–	–	–	–		
	D4	MODE16	8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	fOSC3	fOSC1	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	fOSC3	fOSC1	0	R/W	
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection			0	R/W	
	D5	FOUT1	FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF44	D7	–	–	–	–	–		Constantry "0" when
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	

*1 Reset to "0" during one-shot output.

■ High impedance control

HZR26: 00FF71H•D6
HZR27: 00FF71H•D7
HZR34: 00FF72H•D4
HZR50: 00FF70H•D6
HZR51: 00FF70H•D7

Sets the output terminals to a high impedance state.

When "1" is written:	High impedance
When "0" is written:	Complementary
Reading:	Valid

HZRxx is the high impedance control register which correspond to the Rxx output port terminal. When "1" is set to the HZRxx register, the corresponding output port terminal becomes high impedance state and when "0" is set, it becomes complementary output.
This control is effective even if the port is set as a special output port.
At initial reset, this register is set to "0" (complimentary).

■ DC output control

R26D: 00FF75H•D6
R27D: 00FF75H•D7
R34D: 00FF76H•D4
R50D: 00FF78H•D0
R51D: 00FF78H•D1

Sets the data output from the output port terminal Rxx.

When "1" is written:	HIGH level output
When "0" is written:	LOW level output
Reading:	Valid

RxxD is the data register for the Rxx output port. When "1" is set to the register, the corresponding output port terminal goes HIGH (V_{DD}), and when "0" is set, it goes LOW (V_{SS}).
At initial reset, R50D is set to "0" (LOW level output). The other registers are set to "1" (HIGH level output).
When R26 and / or R51 are set to the special outputs by mask option, R26D and / or R51D can be used as general-purpose registers that do not affect the output status.

■ Special output control

PTOUT: 00FF30H•D2

Controls the TOUT (programmable timer output clock) output and $\overline{TOUT}$ (TOUT inverted signal) output.

When "1" is written:	TOUT / $\overline{TOUT}$ output
When "0" is written:	HIGH (DC) output [R27] LOW (DC) output [R26]
Reading:	Valid

PTOUT is the output control register for TOUT and $\overline{TOUT}$ signals. When "1" is set to the register, the TOUT ($\overline{TOUT}$) signal is output from the output port terminal R27 (R26). When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{TOUT}$ output.
The $\overline{TOUT}$ signal can be output from R26 only when the function is selected by mask option.
At initial reset, PTOUT is set to "0" (DC output).

FOUTON: 00FF40H•D3

Controls the FOUT (f_{OSC1} / f_{OSC3} dividing clock) signal output.

When "1" is written:	FOUT signal output
When "0" is written:	HIGH level (DC) output
Reading:	Valid

FOUTON is the output control register for FOUT signal. When "1" is set, the FOUT signal is output from the output port terminal R34 and when "0" is set, HIGH (V_{DD}) level is output. At this time, "1" must always be set for the data register R34D.
At initial reset, FOUTON is set to "0" (HIGH level output).

FOUT0, FOUT1, FOUT2: 00FF40H•D4, D5, D6

FOUT signal frequency is set as shown in Table 5.5.6.2.

Table 5.5.6.2 FOUT frequency settings

FOUT2	FOUT1	FOUT0	FOUT frequency
0	0	0	f_{OSC1} / 1
0	0	1	f_{OSC1} / 2
0	1	0	f_{OSC1} / 4
0	1	1	f_{OSC1} / 8
1	0	0	f_{OSC3} / 1
1	0	1	f_{OSC3} / 2
1	1	0	f_{OSC3} / 4
1	1	1	f_{OSC3} / 8

f_{OSC1}: OSC1 oscillation frequency
f_{OSC3}: OSC3 oscillation frequency

At initial reset, this register is set to "0" (f_{OSC1} / 1).

BZON: 00FF44H•D0

Controls the buzzer (BZ and $\overline{BZ}$) signal output.

When "1" is written:	Buzzer signal output
When "0" is written:	LOW(DC) output [R50]
	HIGH (DC) output [R51]
Reading:	Valid

BZON is the output control register for buzzer signal. When "1" is set to the register, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
At initial reset, BZON is set to "0" (DC output).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSHT: 00FF44H•D5

Controls the one-shot buzzer output.

When "1" is written:	Trigger
When "0" is written:	No operation
When "1" is read:	Busy
When "0" is read:	Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate. The BZ ($\overline{BZ}$) signal is output from the R50 (R51) terminal. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed.
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") state. The trigger is invalid during ON (BZON = "1") state. When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON, "1" is read from BZSHTand when the output is OFF, "0" is read.
At initial reset, BZSHT is set to "0" (ready).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSTP: 00FF44H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written:	Forcibly stop
When "0" is written:	No operation
Reading:	Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.5.7 Programming notes

(1) Since the special output signals (TOUT / $\overline{TOUT}$, FOUT, BZ / $\overline{BZ}$) are generated asynchronously from the output control registers (PTOUT, FOUTON, BZON, BZSHT and BZSTP), when the signals is turned ON or OFF by the output control register settings, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the special output signals (TOUT, / $\overline{TOUT}$, FOUT, BZ / $\overline{BZ}$) are in the enable status, an unstable clock is output for the special output at the time of return from the SLEEP state. Consequently, when shifting to the SLEEP state, you should set the special output signal to the disable status prior to executing the SLP instruction.

(3) When the FOUT frequency is made "f_{OSC3} / n", you must turn on the OSC3 oscillation circuit before outputting FOUT. A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, if an abnormality occurs as the result of an unstable FOUT signal being output externally, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before turning outputting FOUT. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF state.

5.6 I/O Ports (P ports)

5.6.1 Configuration of I/O ports

The E0C88816 is equipped with 16 bits of I/O ports (P00–P07 and P10–P17).
Figure 5.6.1.1 shows the structure of an I/O port.

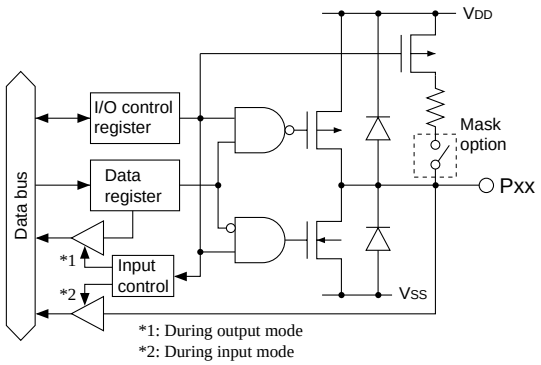


Fig. 5.6.1.1 Structure of I/O port

I/O ports can be set for input or output mode in one bit unit. These settings are performed by writing data to the I/O control registers.
The I/O port terminals P10–P13 are shared with the serial interface input/output terminals and P14–P17 are shared with the A/D converter input terminals. The function of the terminals is switchable by software. For details of the serial interface and A/D converter, see "5.7 Serial Interface" and "5.15 A/D Converter", respectively.
The data registers and I/O control registers of the I/O ports set as serial interface outputs are usable as general purpose registers with read/write capabilities which do not affect I/O activities of the terminal.
The same as above, I/O control registers of the I/O ports set as serial interface or A/D converter inputs are usable as general purpose register.

5.6.2 Mask option

I/O port pull-up resistors

P00	☐ With resistor	☐ Gate direct
P01	☐ With resistor	☐ Gate direct
P02	☐ With resistor	☐ Gate direct
P03	☐ With resistor	☐ Gate direct
P04	☐ With resistor	☐ Gate direct
P05	☐ With resistor	☐ Gate direct
P06	☐ With resistor	☐ Gate direct
P07	☐ With resistor	☐ Gate direct
P10	☐ With resistor	☐ Gate direct
P11	☐ With resistor	☐ Gate direct
P12	☐ With resistor	☐ Gate direct
P13	☐ With resistor	☐ Gate direct
P14	☐ With resistor	☐ Gate direct
P15	☐ With resistor	☐ Gate direct
P16	☐ With resistor	☐ Gate direct
P17	☐ With resistor	☐ Gate direct

I/O ports P00–P07 and P10–P17 are equipped with a pull-up resistor which goes ON in the input mode. Whether this resistor is used or not can be selected for each port (one bit unit).
In cases where the 'With resistor' option is selected, the pull-up resistor goes ON when the port is in input mode.
When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

When the A/D converter is used, select "Gate direct" for I/O ports (P14–P17) which then become input terminals.

For unused I/O ports, select the default setting of "With resistor".

5.6.3 I/O control registers and I/O mode

I/O ports P00–P07 and P10–P17 are set either to input or output modes by writing data to the I/O control registers IOC00–IOC07 and IOC10–IOC17 which correspond to each bit.
To set an I/O port to input mode, write "0" to the I/O control register.
An I/O port which is set to input mode will shift to a high impedance state and functions as an input port. Readout in input mode consists simply of a direct readout of the input terminal state: the data being "1" when the input terminal is at HIGH (V_{DD}) level and "0" when it is at LOW (V_{SS}) level.
When the "With resistor" option is selected using the mask option, the resistor is pulled up onto the port terminal in input mode.
Even in input mode, data can be written to the data registers without affecting the terminal state.
To set an I/O port to output mode, write "1" to the I/O control register. An I/O port which is set to output mode functions as an output port.
When port output data is "1", a HIGH (V_{DD}) level is output and when it is "0", a LOW (V_{SS}) level is output. Readout in output mode consists of the contents of the data register.
At initial reset, I/O control registers are set to "0" (I/O ports are set to input mode).

5.6.4 I/O memory for I/O ports

Table 5.6.4.1 shows the I/O port control bits.

Table 5.6.4.1 I/O port control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF60	D7	IOC07	P07 I/O control register	Output	Input	0	R/W	
	D6	IOC06	P06 I/O control register			0	R/W	
	D5	IOC05	P05 I/O control register			0	R/W	
	D4	IOC04	P04 I/O control register			0	R/W	
	D3	IOC03	P03 I/O control register			0	R/W	
	D2	IOC02	P02 I/O control register			0	R/W	
	D1	IOC01	P01 I/O control register			0	R/W	
	D0	IOC00	P00 I/O control register			0	R/W	
00FF61	D7	IOC17	P17 I/O control register	Output	Input	0	R/W	
	D6	IOC16	P16 I/O control register			0	R/W	
	D5	IOC15	P15 I/O control register			0	R/W	
	D4	IOC14	P14 I/O control register			0	R/W	
	D3	IOC13	P13 I/O control register			0	R/W	
	D2	IOC12	P12 I/O control register			0	R/W	
	D1	IOC11	P11 I/O control register			0	R/W	
	D0	IOC10	P10 I/O control register			0	R/W	
00FF62	D7	P07D	P07 I/O port data	High	Low	1	R/W	
	D6	P06D	P06 I/O port data			1	R/W	
	D5	P05D	P05 I/O port data			1	R/W	
	D4	P04D	P04 I/O port data			1	R/W	
	D3	P03D	P03 I/O port data			1	R/W	
	D2	P02D	P02 I/O port data			1	R/W	
	D1	P01D	P01 I/O port data			1	R/W	
	D0	P00D	P00 I/O port data			1	R/W	
00FF63	D7	P17D	P17 I/O port data	High	Low	1	R/W	
	D6	P16D	P16 I/O port data			1	R/W	
	D5	P15D	P15 I/O port data			1	R/W	
	D4	P14D	P14 I/O port data			1	R/W	
	D3	P13D	P13 I/O port data			1	R/W	
	D2	P12D	P12 I/O port data			1	R/W	
	D1	P11D	P11 I/O port data			1	R/W	
	D0	P10D	P10 I/O port data			1	R/W	

P00D–P07D: 00FF62H
P10D–P17D: 00FF63H

How I/O port terminal data readout and output data settings are performed.

When writing data:

When "1" is written: HIGH level
When "0" is written: LOW level

When the I/O port is set to output mode, the data written is output as is to the I/O port terminal. In terms of port data, when "1" is written, the port terminal goes to HIGH (V_{DD}) level and when "0" is written to a LOW (V_{SS}) level.
Even when the port is in input mode, data can still be written in.

When reading out data:

When "1" is read: HIGH level ("1")
When "0" is read: LOW level ("0")

When an I/O port is in input mode, the voltage level being input to the port terminal is read out. When terminal voltage is HIGH (V_{DD}), it is read as a "1", and when it is LOW (V_{SS}), it is read as a "0". Furthermore, in output mode, the contents of the data register are read out.
At initial reset, this register is set to "1" (HIGH level).

The data registers of I/O ports set for the output terminal of serial interface can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

IOC00–IOC07: 00FF60H
IOC10–IOC17: 00FF61H

Sets the I/O ports to input or output mode.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOC is the I/O control register which correspond to each I/O port in a bit unit.
Writing "1" to the IOC register will switch the corresponding I/O port to output mode, and writing "0" will switch it to input mode.
At initial reset, this register is set to "0" (input mode).

The data registers of I/O ports set for the input terminals of the serial interface and the A/D converter can be used as general purpose registers with read/write capabilities which do not affect I/O activities of the terminals.

5.6.5 Programming note

When changing the port terminal from LOW level to HIGH with the built-in pull-up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull-up resistor and the load capacitance of the terminal. It is necessary to set an appropriate wait time for introduction of an I/O port. Make this wait time the amount of time or more calculated by the following expression.

Wait time = R_{IN} x (C_{IN} + load capacitance on the board) x 1.6 [sec]

R_{IN}: Pull up resistance Max. value
C_{IN}: Terminal capacitance Max. value

5.7 Serial Interface

5.7.1 Configuration of serial interface

The E0C88816 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 5.7.1.1 shows the configuration of the serial interface.

Serial interface input/output terminals, SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are shared with I/O ports P10–P13. In order to utilize these terminals for the serial interface input/output terminals, proper settings have to be made with registers ESIF, SMD0 and SMD1. (At initial reset, these terminals are set as I/O port terminals.)
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 5.7.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P10	SIN
P11	SOUT
P12	$\overline{\text{SCLK}}$
P13	$\overline{\text{SRDY}}$

* The terminals used may vary depending on the transfer mode.

SIN and SOUT are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{\text{SCLK}}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{\text{SRDY}}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are superfluous, the I/O port terminals P12 and P13 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{\text{SRDY}}$ is superfluous, the I/O port terminal P13 can be used as I/O port.

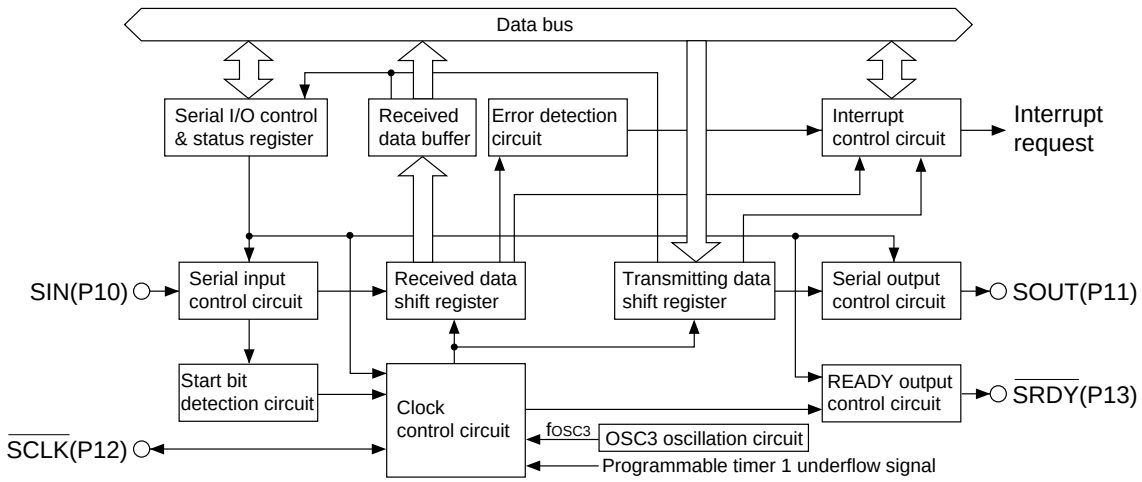


Fig. 5.7.1.1 Configuration of serial interface

5.7.2 Mask option

Since serial interface input/output terminals are shared with the I/O ports, serial interface terminal specifications have necessarily been selected with the mask option for I/O ports.

I/O port pull-up resistors		
P10 (SIN)	☐ With resistor	☐ Gate direct
P12 (SCLK)	☐ With resistor	☐ Gate direct

Each I/O port terminal is equipped with a pull-up resistor which goes ON in input mode. A selection can be made for each port (one bit unit) as to whether or not the resistor will be used. Specifications (whether the pull-up will be used or not) of P10 (SIN) and P12 ($\overline{SCLK}$) which will become input terminals when using the serial interface are decided by settings the options for the I/O port.

When "Gate direct" is selected in the serial I/F mode, be sure that the input terminals do not go into a floating state.

5.7.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMD0 and SMD1 as shown in the table below.

Table 5.7.3.1 Transfer modes

SMD1	SMD0	Mode
1	1	Asynchronous 8-bit
1	0	Asynchronous 7-bit
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 5.7.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUT	$\overline{SCLK}$	$\overline{SRDY}$
Asynchronous 8-bit	Input	Output	P12	P13
Asynchronous 7-bit	Input	Output	P12	P13
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P13

At initial reset, transfer mode is set to clock synchronous master mode.

■ Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and clock synchronous 8-bit serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the $\overline{SCLK}$ terminal which enables control of the external (slave side) serial I/O device. Since the $\overline{SRDY}$ terminal is not utilized in this mode, it can be used as an I/O port.
Figure 5.7.3.1(a) shows the connection example of input/output terminals in the clock synchronous master mode.

■ Clock synchronous slave mode

In this mode, a synchronous clock from the external (master side) serial input/output device is utilized and clock synchronous 8-bit serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the $\overline{SCLK}$ terminal and is utilized by this interface as the synchronous clock.
Furthermore, the $\overline{SRDY}$ signal indicating the transmit-receive ready status is output from the $\overline{SRDY}$ terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCS0 and SCS1 used to select the clock source are invalid.
Figure 5.7.3.1(b) shows the connection example of input/output terminals in the clock synchronous slave mode.

■ Asynchronous 7-bit mode

In this mode, asynchronous 7-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the $\overline{SCLK}$ terminal is not used. Furthermore, since the $\overline{SRDY}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.7.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

■ Asynchronous 8-bit mode

In this mode, asynchronous 8-bit transfer can be performed. Parity check during data reception and addition of parity bit (odd/even/none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the $\overline{SCLK}$ terminal is not used. Furthermore, since the $\overline{SRDY}$ terminal is not utilized either, both of these terminals can be used as I/O ports.
Figure 5.7.3.1(c) shows the connection example of input/output terminals in the asynchronous mode.

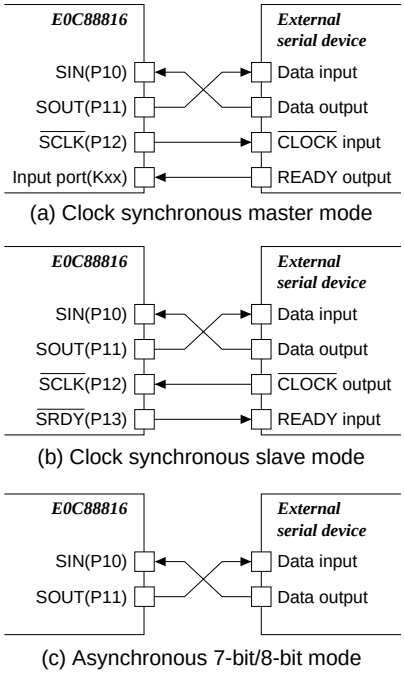


Fig. 5.7.3.1 Connection examples of serial interface I/O terminals

5.7.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCS0 and SCS1 as shown in table below.

Table 5.7.4.1 Clock source

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	fOSC3 / 4
0	1	fOSC3 / 8
0	0	fOSC3 / 16

This register setting is invalid in clock synchronous slave mode and the external clock input from the SCLK terminal is used.
When the "programmable timer" is selected, the programmable timer 1 underflow signal is divided by 1/2 and this signal used as the clock source. With respect to the transfer rate setting, see "5.10 Programmable Timer".
At initial reset, the synchronous clock is set to "fOSC3 / 16".
Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock.
Furthermore, external clock input is used as is for SCLK in clock synchronous slave mode.
Table 5.7.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.
When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

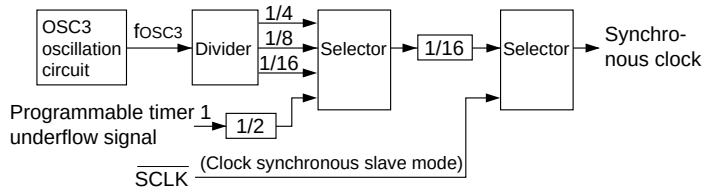


Fig. 5.7.4.1 Division of the synchronous clock

Table 5.7.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	fOSC3 = 3.072 MHz		fOSC3 = 4.608 MHz		fOSC3 = 4.9152 MHz	
	PSC1X	RLD1X	PSC1X	RLD1X	PSC1X	RLD1X
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.7.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

■ Shift register and received data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.

Data being transmitted are written to TRXD0–TRXD7 and converted to serial through the shift register and is output from the SOUT terminal.

In the reception section, a received data buffer is installed separate from the shift register.
Data being received are input to the SIN terminal and is converted to parallel through the shift register and written to the received data buffer. Since the received data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

■ Transmit enable register and transmit control bit

For transmitting control, use the transmit enable register TXEN and transmit control bit TXTRG.

The transmit enable register TXEN is used to set the transmitting enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.

The transmit control bit TXTRG is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRG whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.

In addition, TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.

When not transmitting, set TXEN to "0" to disable transmitting status.

■ Receive enable register, receive control bit

For receiving control, use the receive enable register RXEN and receive control bit RXTRG.
Receive enable register RXEN is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SIN terminal goes to the shift register.
The operation of the receive control bit RXTRG is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit TXTRG is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRG to start receiving. (When "1" is written to RXTRG in slave mode, $\overline{\text{SRDY}}$ switches to "0".)
In an asynchronous system, RXTRG is used to prepare for next data receiving. After reading the received data from the received data buffer, write "1" into RXTRG to signify that the received data buffer is empty. If "1" is not written into RXTRG, the overrun error flag OER will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRG.)
In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXEN to "0" to disable receiving status.

5.7.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCS0 and SCS1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the $\overline{\text{SCLK}}$ terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the $\overline{\text{SCLK}}$ terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line ($\overline{\text{SCLK}}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

Transfer data is fixed at 8 bits and both transmitting and receiving are conducted with the LSB (bit 0) coming first.

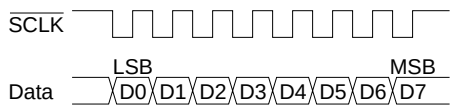


Fig. 5.7.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "5.7.8 Interrupt function".

■ Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input/output ports SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are set as I/O port terminals P10–P13 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.

(3) Setting of transfer mode
Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

Master mode: SMD0 = "0", SMD1 = "0"
Slave mode: SMD0 = "1", SMD1 = "0"

(4) Clock source selection
In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.7.4.1.)
This selection is not necessary in the slave mode.

Since all the registers mentioned in (2)–(4) are assigned to the same address, it's possible to set them all with one instruction. The parity enable register EPR is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control
When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.3 Oscillation Circuits and Operating Mode".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN and the receive enable register RXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRG and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUT terminal. When the final bit (MSB) is output, the SOUT terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

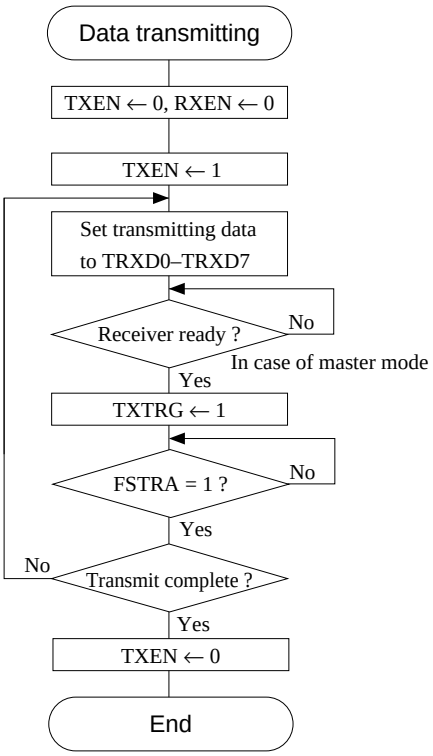


Fig. 5.7.6.2 Transmit procedure in clock synchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN and transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRG and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal. The received data input from the SIN terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the received data buffer and the receiving complete interrupt factor flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

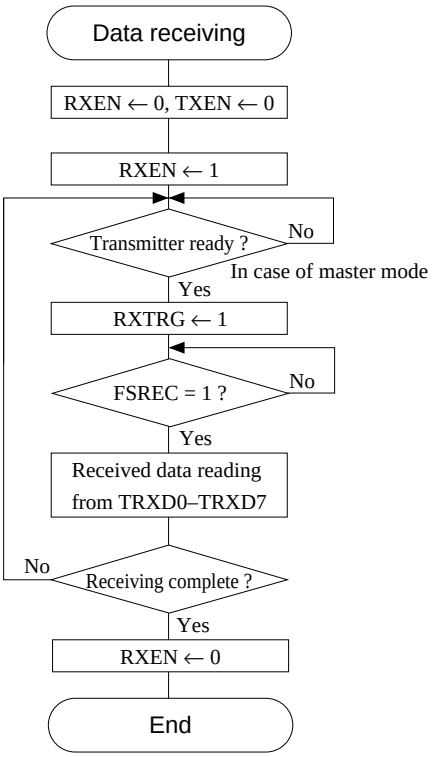


Fig. 5.7.6.3 Receiving procedure in clock synchronous mode

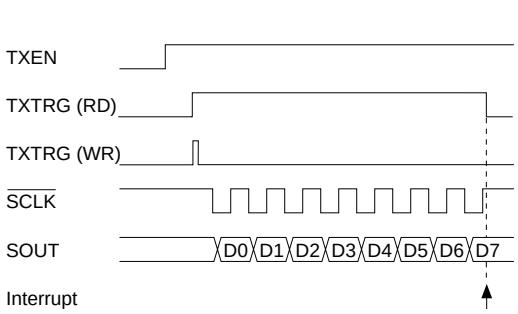
■ Transmit/receive ready ($\overline{\text{SRDY}}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{\text{SRDY}}$ signal is output to indicate whether or not this serial interface can transmit / receive to the master side (external serial input / output device). This signal is output from the $\overline{\text{SRDY}}$ terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (LOW level) and becomes "1" (HIGH level) when there is a BUSY status, such as during transmit / receive operation.

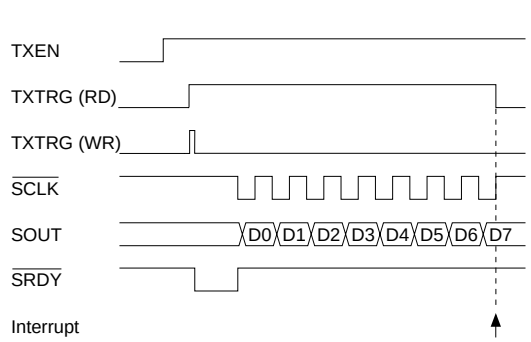
The $\overline{\text{SRDY}}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRG or the receive control bit RXTRG and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge). When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I / O port. At this time, since the $\overline{\text{SRDY}}$ terminal is not set and instead P13 functions as the I / O port, you can apply this port for said control.

■ Timing chart

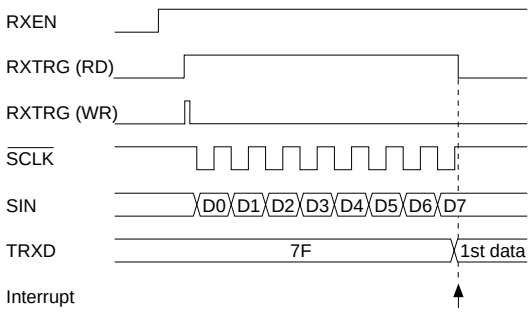
The timing chart for the clock synchronous system transmission is shown in Figure 5.7.6.4.



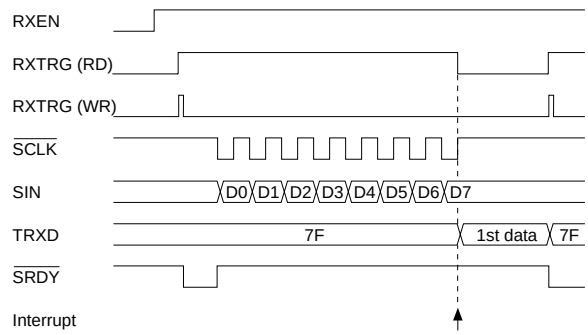
(a) Transmit timing for master mode



(b) Transmit timing for slave mode



(c) Receive timing for master mode



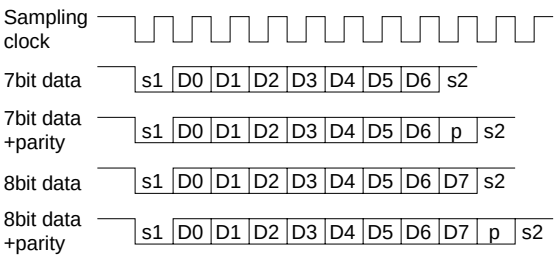
(d) Receive timing for slave mode

Fig. 5.7.6.4 Timing chart (clock synchronous system transmission)

5.7.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

For transfer data in the asynchronous 7-bit mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the asynchronous 8-bit mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit and stop bit are respectively fixed at one bit and data is transmitted and received by placing the LSB (bit 0) at the front.



s1 : Start bit (Low level, 1 bit)
s2 : Stop bit (High level, 1 bit)
p : Parity bit

Fig. 5.7.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "5.7.8 Interrupt function" for the serial interface interrupts.

■ Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable
To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection
Because serial interface input / output terminals SIN and SOUT are set as I / O port terminals P10 and P11 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use. $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P12 and P13.

(3) Setting of transfer mode
Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

7-bit mode: SMD0 = "0", SMD1 = "1"
8-bit mode: SMD0 = "1", SMD1 = "1"

(4) Parity bit selection
When checking and adding parity bits, write "1" into the parity enable register EPR to set to "with parity check". As a result of this setting, in the asynchronous 7-bit mode, it has a 7 bits data + parity bit configuration and in the asynchronous 8-bit mode it has an 8 bits data + parity bit configuration.In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMD.
When "0" is written to the PMD register to select "without parity check" in the asynchronous 7-bit mode, data configuration is set to 7 bits data (no parity) and in the asynchronous 8-bit mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection
Select the clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 5.7.4.1.)
Since all the registers mentioned in (2)–(5) are assigned to the same address, it's possible to set them all with one instruction.

(6) Clock source control
When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "5.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "5.3 Oscillation Circuits and Operating Mode".)

■ Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7. Also, when 7-bit data is selected, the TRXD7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRG and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUT terminal in synchronize to its rising edge. The transmitting data set to the shift register is shifted one bit at a time at each rising edge of the clock thereafter and is output from the SOUT terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag FSTRA is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

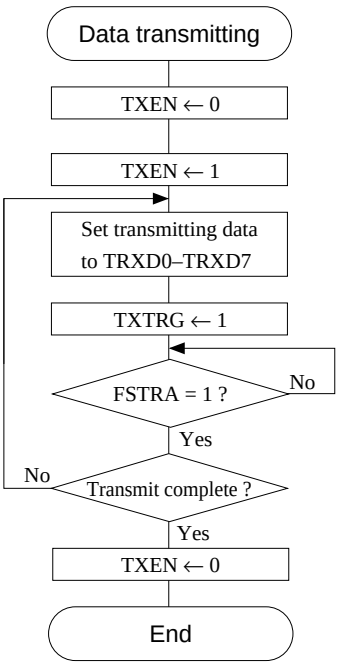


Fig. 5.7.7.2 Transmit procedure in asynchronous mode

■ Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN to set the receiving disable status and to reset the respective PER, OER, FER flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SIN terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag FSERR is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the received data buffer and the receiving complete interrupt flag FSREC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the received data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

(4) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRG to inform that the receive data has been read out. When the following data is received prior to writing "1" to RXTRG, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

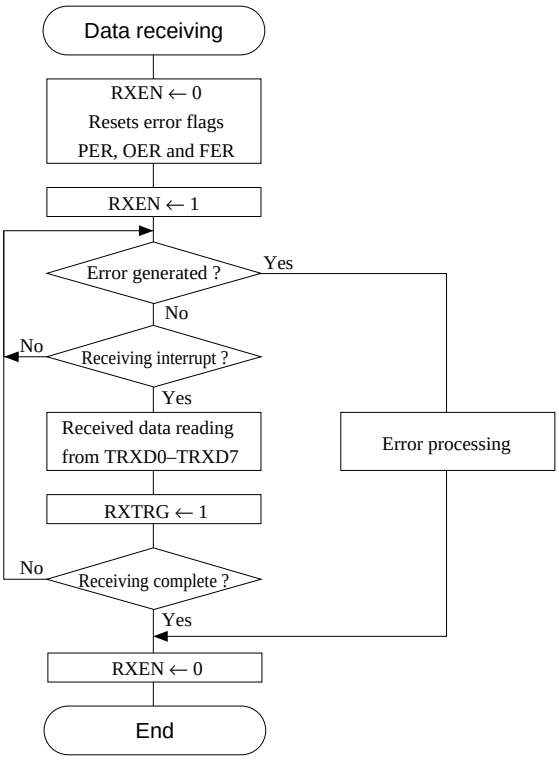


Fig. 5.7.7.3 Receiving procedure in asynchronous mode

■ Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPR register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.

The parity check is performed when data received in the shift register is transferred to the received data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMD register match. When it does not match, it is recognized as an parity error and the parity error flag PER and the error interrupt factor flag FSERR is set to "1".

When interrupt has been enabled, an error interrupt is generated at this point.

The PER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

The received data at this point cannot assured because of the parity error.

(2) Framing error

In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.

The FER flag is reset to "0" by writing "1".

Even when this error has been generated, the received data for it is loaded into the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receipt, such data cannot be assured.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

When the next data is received before "1" is written to RXTRG, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OER and the error interrupt factor flag FSERR are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OER flag is reset to "0" by writing "1" into it.

Even when this error has been generated, the received data corresponding to the error is transferred in the received data buffer and the receive operation also continues.

Furthermore, when the timing for writing "1" to RXTRG and the timing for the received data transfer to the received data buffer overlap, it will be recognized as an overrun error.

■ Timing chart

Figure 5.7.7.4 show the asynchronous transfer timing chart.

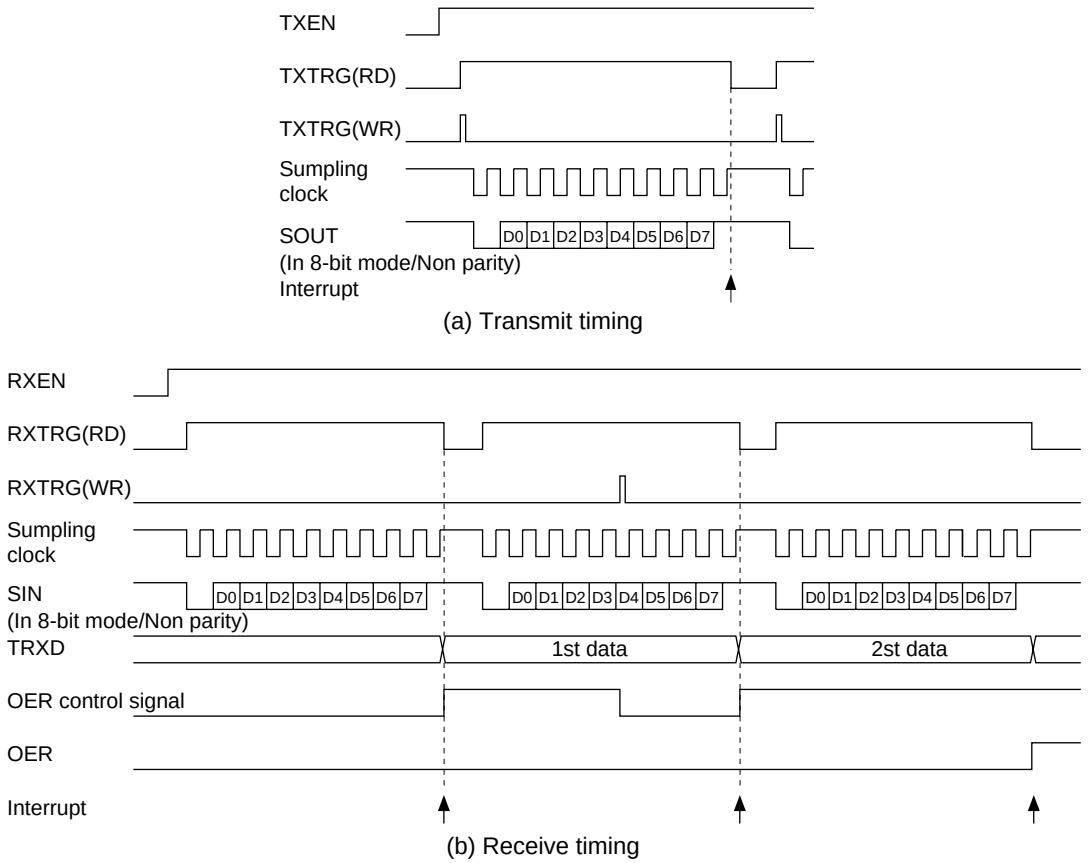


Fig. 5.7.7.4 Timing chart (asynchronous transfer)

5.7.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- **Transmitting complete interrupt**
- **Receiving complete interrupt**
- **Error interrupt**

The interrupt factor flag FSxxx and the interrupt enable register ESxxx for the respective interrupt factors are provided and then the interrupt enable/disable can be selected by the software. In addition, a priority level of the serial interface interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSIF0 and PSIF1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.16 Interrupt and Standby Status".
Figure 5.7.8.1 shows the configuration of the serial interface interrupt circuit.

■ Transmitting complete interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag FSTRA to "1". When set in this manner, if the corresponding interrupt enable register ESTRA is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESTRA and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSTRA is set to "1".
The interrupt factor flag FSTRA is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting start (writing "1" to TXTRG) can be controlled by generation of this interrupt factor.
The exception processing vector address for this interrupt factor is set at 000014H.

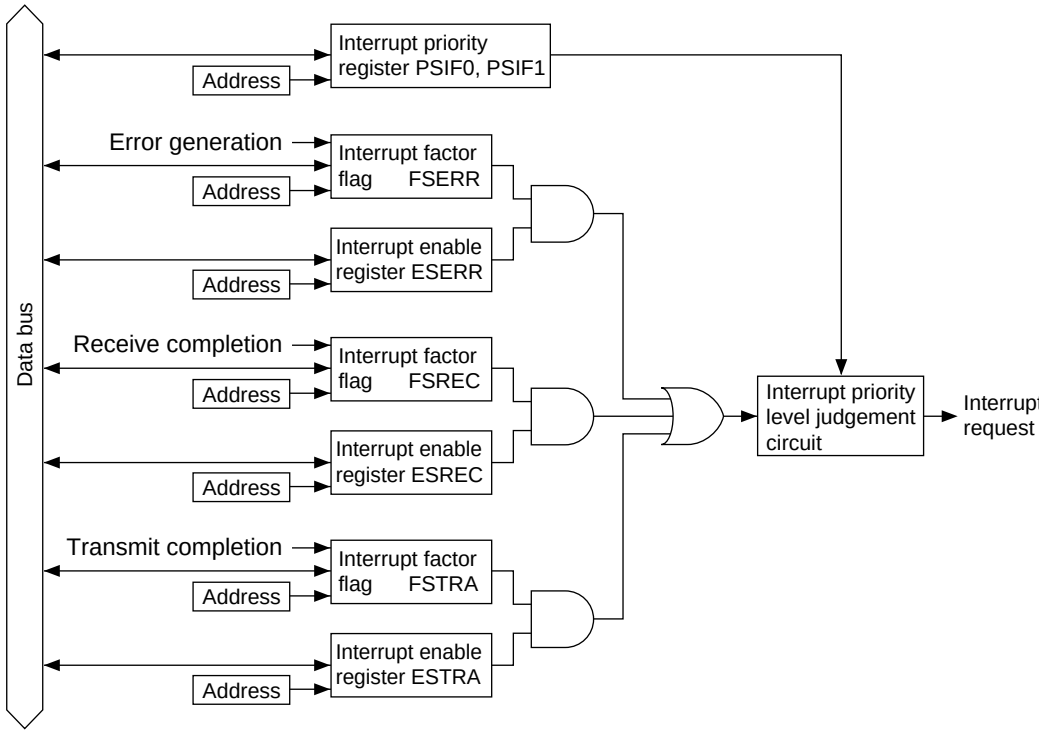


Fig. 5.7.8.1 Configuration of serial interface interrupt circuit

■ Receiving complete interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the received data buffer and it sets the interrupt factor flag FSREC to "1". When set in this manner, if the corresponding interrupt enable register ESREC is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written into the interrupt enable register ESREC and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSREC is set to "1". The interrupt factor flag FSREC is reset to "0" by writing "1".

The generation of this interrupt factor permits the received data to be read.

Also, the interrupt factor flag is set to "1" when a parity error or framing error is generated.

The exception processing vector address for this interrupt factor is set at 000012H.

■ Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag FSERR to "1". When set in this manner, if the corresponding interrupt enable register ESERR is set to "1" and the corresponding interrupt priority registers PSIF0 and PSIF1 are set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
When "0" has been written in the interrupt enable register ESERR and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag FSERR is set to "1". The interrupt factor flag FSERR is reset to "0" by writing "1".

Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PER (parity error), OER (overrun error) and FER (framing error).

The exception processing vector address for this interrupt factor is set at 000010H.

5.7.9 I/O memory for serial interface

Table 5.7.9.1 show the serial interface control bits.

Table 5.7.9.1(a) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF48	D7	–	–	–	–	–		"0" when being read
	D6	EPR	Parity enable register	With parity	Non parity	0	R/W	Only for
	D5	PMD	Parity mode selection	Odd	Even	0	R/W	asynchronous mode
	D4	SCS1	Clock source selection SCS1 SCS0 Clock source 1 1 Programmable timer			0	R/W	In the clock synchronous slave mode, external clock is selected.
	D3	SCS0	1 0 f_{OSC3} / 4 0 1 f_{OSC3} / 8 0 0 f_{OSC3} / 16			0	R/W	
	D2	SMD1	Serial I/F mode selection SMD1 SMD0 Mode 1 1 Asynchronous 8-bit			0	R/W	
	D1	SMD0	1 0 Asynchronous 7-bit 0 1 Clock synchronous slave 0 0 Clock synchronous master			0	R/W	
	D0	ESIF	Serial I/F enable register	Serial I/F	I/O port	0	R/W	
00FF49	D7	–	–	–	–	–		"0" when being read
	D6	FER	Framing error flag R	Error	No error	0	R/W	Only for
			W	Reset (0)	No operation			asynchronous mode
	D5	PER	Parity error flag R	Error	No error	0	R/W	
			W	Reset (0)	No operation			
	D4	OER	Overrun error flag R	Error	No error	0	R/W	
			W	Reset (0)	No operation			
	D3	RXTRG	Receive trigger/status R	Run	Stop	0	R/W	
			W	Trigger	No operation			
	D2	RXEN	Receive enable	Enable	Disable	0	R/W	
	D1	TXTRG	Transmit trigger/status R	Run	Stop	0	R/W	
			W	Trigger	No operation			
	D0	TXEN	Transmit enable	Enable	Disable	0	R/W	
00FF4A	D7	TRXD7	Transmit/Receive data D7 (MSB)	High	Low	X	R/W	
	D6	TRXD6	Transmit/Receive data D6			X	R/W	
	D5	TRXD5	Transmit/Receive data D5			X	R/W	
	D4	TRXD4	Transmit/Receive data D4			X	R/W	
	D3	TRXD3	Transmit/Receive data D3			X	R/W	
	D2	TRXD2	Transmit/Receive data D2			X	R/W	
	D1	TRXD1	Transmit/Receive data D1			X	R/W	
	D0	TRXD0	Transmit/Receive data D0 (LSB)			X	R/W	
00FF20	D7	PK01	K00–K07 interrupt priority register			0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	

PK01 PK00 / PSIF1 PSIF0 / PSW1 PSW0 / PTM1 PTM0 — Priority level

1 1 — Level 3
1 0 — Level 2
0 1 — Level 1
0 0 — Level 0

Table 5.7.9.1(b) Serial interface control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

ESIF: 00FF48H•D0

Sets the serial interface terminals (P10–P13).

When "1" is written: Serial input/output terminal
When "0" is written: I/O port terminal
Reading: Valid

The ESIF is the serial interface enable register and P10–P13 terminals become serial input/output terminals (SIN, SOUT, $\overline{SCLK}$, $\overline{SRDY}$) when "1" is written, and they become I/O port terminals when "0" is written.
Also, see Table 5.7.3.2 for the terminal settings according to the transfer modes.
At initial reset, ESIF is set to "0" (I/O port).

SMD0, SMD1: 00FF48H•D1, D2

Set the transfer modes according to Table 5.7.9.2.

Table 5.7.9.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	Asynchronous system 8-bit
1	0	Asynchronous system 7-bit
0	1	Clock synchronous system slave
0	0	Clock synchronous system master

SMD0 and SMD1 can also read out.
At initial reset, this register is set to "0" (clock synchronous master mode).

SCS0, SCS1: 00FF48H•D3, D4

Select the clock source according to Table 5.7.9.3.

Table 5.7.9.3 Clock source selection

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 4
0	1	f_{OSC3} / 8
0	0	f_{OSC3} / 16

SCS0 and SCS1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0" (f_{OSC3} / 16).

EPR: 00FF48H•D6

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPR, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPR setting becomes invalid in the clock synchronous mode.
At initial reset, EPR is set to "0" (non parity).

PMD: 00FF48H•D5

Selects odd parity / even parity.

When "1" is written:	Odd parity
When "0" is written:	Even parity
Reading:	Valid

When "1" is written to PMD, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPR. When "0" has been written to EPR, the parity setting by PMD becomes invalid.
At initial reset, PMD is set to "0" (even parity).

TXEN: 00FF49H•D0

Sets the serial interface to the transmitting enable status.

When "1" is written:	Transmitting enable
When "0" is written:	Transmitting disable
Reading:	Valid

When "1" is written to TXEN, the serial interface shifts to the transmitting enable status and shifts to the transmitting disable status when "0" is written.
Set TXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, TXEN is set to "0" (transmitting disable).

TXTRG: 00FF49H•D1

Functions as the transmitting start trigger and the operation status indicator (transmitting / stop status).

When "1" is read:	During transmitting
When "0" is read:	During stop
When "1" is written:	Transmitting start
When "0" is written:	Invalid

Starts the transmitting when "1" is written to TXTRG after writing the transmitting data.
TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRG is set to "0" (during stop).

RXEN: 00FF49H•D2

Sets the serial interface to the receiving enable status.

When "1" is written:	Receiving enable
When "0" is written:	Receiving disable
Reading:	Valid

When "1" is written to RXEN, the serial interface shifts to the receiving enable status and shifts to the receiving disable status when "0" is written.
Set RXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, RXEN is set to "0" (receiving disable).

RXTRG: 00FF49H•D3

Functions as the receiving start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read:	During receiving
When "0" is read:	During stop
When "1" is written:	Receiving start / following data receiving preparation
When "0" is written:	Invalid

RXTRG has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRG in the clock synchronous system, is used as the trigger for the receiving start.
Writes "1" into RXTRG to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDY}}$ becomes "0" at the point where "1" has been written into into the RXTRG.)

RSTRG is used in the asynchronous system for preparation of the following data receiving. Reads the received data located in the received data buffer and writes "1" into RXTRG to inform that the received data buffer has shifted to empty. When "1" has not been written to RXTRG, the overrun error flag OER is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRG, an overrun error occurs.)

In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRG is set to "0" (during stop).

TRXD0–TRXD7: 00FF4AH

During transmitting

Write the transmitting data into the transmit shift register.

When "1" is written: HIGH level
When "0" is written: LOW level

Write the transmitting data prior to starting transmitting.
In the case of continuous transmitting, wait for the transmitting complete interrupt, then write the data.
The TRXD7 becomes invalid for the asynchronous 7-bit mode.
Converted serial data for which the bits set at "1" as HIGH (V_{DD}) level and for which the bits set at "0" as LOW (V_{SS}) level are output from the SOUT terminal.

During receiving

Read the received data.

When "1" is read: HIGH level
When "0" is read: LOW level

The data from the received data buffer can be read out. Since the sift register is provided separately from this buffer, reading can be done during the receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)
Read the data after waiting for the receiving complete interrupt.
When performing parity check in the asynchronous 7-bit mode, "0" is loaded into the 8th bit (TRXD7) that corresponds to the parity bit.
The serial data input from the SIN terminal is level converted, making the HIGH (V_{DD}) level bit "1" and the LOW (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER: 00FF49H•D4

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when the receiving of data has been completed prior to the writing of "1" to RXTRG in the asynchronous mode.
OER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", OER is set to "0" (no error).

PER: 00FF49H•D5

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PER is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, if data that does not match the parity is received, a parity error is generated.
PER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", PER is set to "0" (no error).

FER: 00FF49H•D6

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FER is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving of the asynchronous mode has become "0", a framing error is generated.
FER is reset to "0" by writing "1".
At initial reset and when RXEN is "0", FER is set to "0" (no error).

PSIF0, PSIF1: 00FF20H•D4, D5

Sets the priority level of the serial interface interrupt. The two bits PSIF0 and PSIF1 are the interrupt priority register corresponding to the serial interface interrupt. Table 5.7.9.4 shows the interrupt priority level which can be set by this register.

Table 5.7.9.4 Interrupt priority level settings

PSIF1	PSIF0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESTRA, ESREC, ESERR: 00FF23H•D0, D1, D2

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

ESTRA, ESREC and ESERR are interrupt enable registers that respectively correspond to the interrupt factors for transmitting complete, receiving complete and receiving error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSTRA, FSREC, FSERR: 00FF25H•D0, D1, D2

Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FSTRA, FSREC and FSERR are interrupt factor flags that respectively correspond to the interrupts for transmitting complete, receiving complete and receiving error and are set to "1" by generation of each factor.
Transmitting complete interrupt factor is generated at the point where the data transmitting of the shift register has been completed.
Receiving complete interrupt factor is generated at the point where the received data has been transferred into the received data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.7.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmitting / receiving disable status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation. Furthermore, do not execute the SLP instruction. (When executing the SLP instruction, set TXEN = RXEN = "0".)

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.) Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag FSERR is set to "1" prior to the receiving complete interrupt factor flag FSREC for the time indicated in Table 5.7.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag FSREC to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag FSREC is not set to "1" and a receiving complete interrupt is not generated.

Table 5.7.10.1 Time difference between FSERR and FSREC on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

5.8 Clock Timer

5.8.1 Configuration of clock timer

The E0C88816 has built in a clock timer that uses the OSC1 oscillation circuit as clock source. The clock timer is composed of an 8-bit binary counter that uses the 256 Hz signal dividing fOSC1 as its input clock and can read the data of each bit (128–1 Hz) by software.
Normally, this clock timer is used for various timing functions such as clocks.
The configuration of the clock timer is shown in Figure 5.8.1.1.

5.8.2 Interrupt function

The clock timer can generate an interrupt by each of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals.
The configuration of the clock timer interrupt circuit is shown in Figure 5.8.2.1.

Interrupts are generated by respectively setting the corresponding interrupt factor flags FTM32, FTM8, FTM2 and FTM1 at the falling edge of the 32 Hz, 8 Hz, 2 Hz and 1 Hz signals to "1". Interrupt can be prohibited by the setting the interrupt enable registers ETM32, ETM8, ETM2 and ETM1 corresponding to each interrupt factor flag.
In addition, a priority level of the clock timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PTM0 and PTM1.
For details on the above mentioned interrupt control register and the operation following generation of an interrupt, see "5.16 Interrupt and Standby Status".

The exception processing vector addresses for each interrupt factor are respectively set as shown below.

32 Hz interrupt:	00001CH
8 Hz interrupt:	00001EH
2 Hz interrupt:	000020H
1 Hz interrupt:	000022H

Figure 5.8.2.2 shows the timing chart for the clock timer.

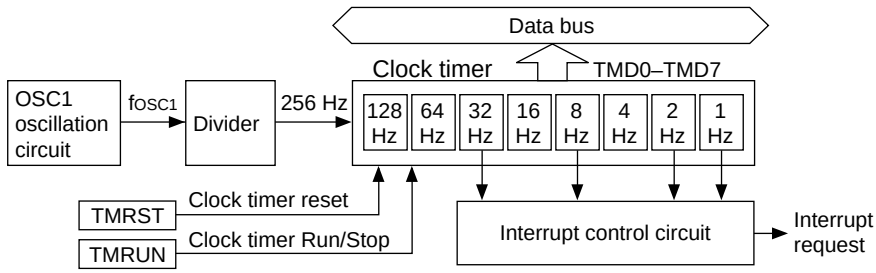


Fig. 5.8.1.1 Configuration of clock timer

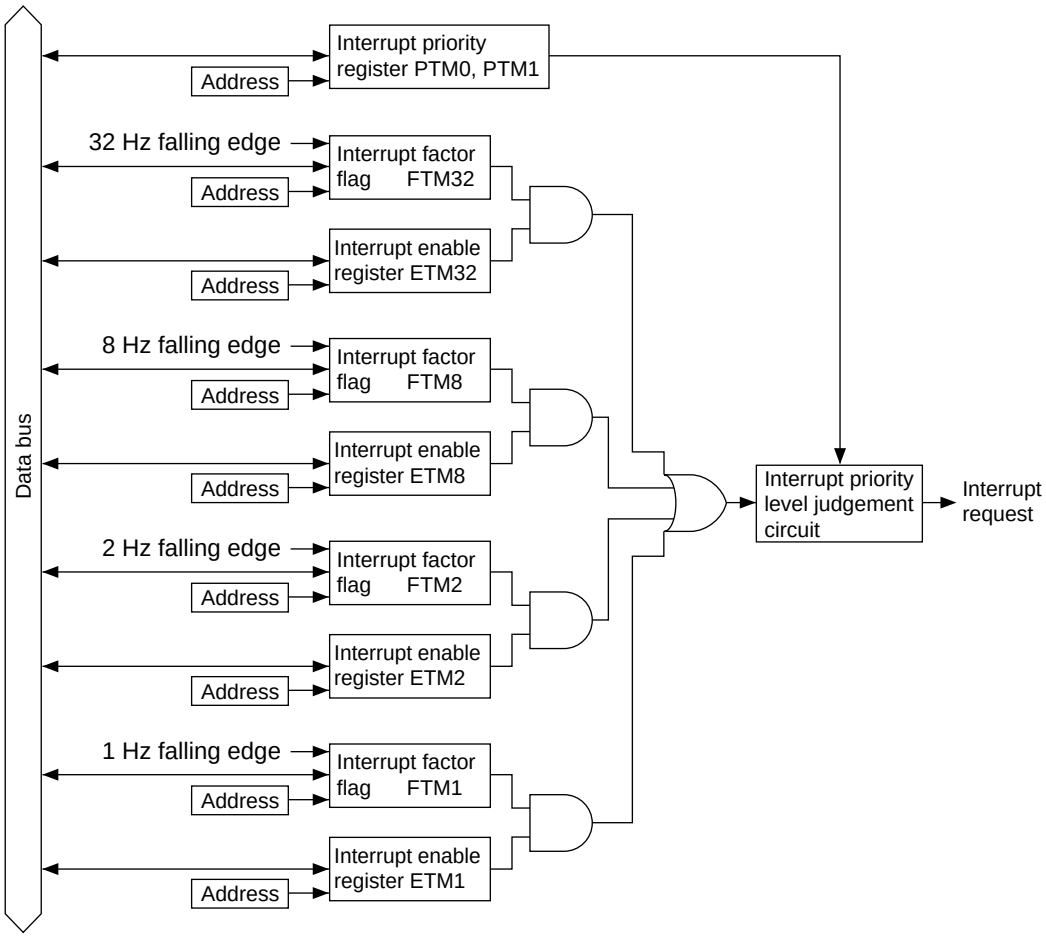


Fig. 5.8.2.1 Configuration of clock timer interrupt circuit

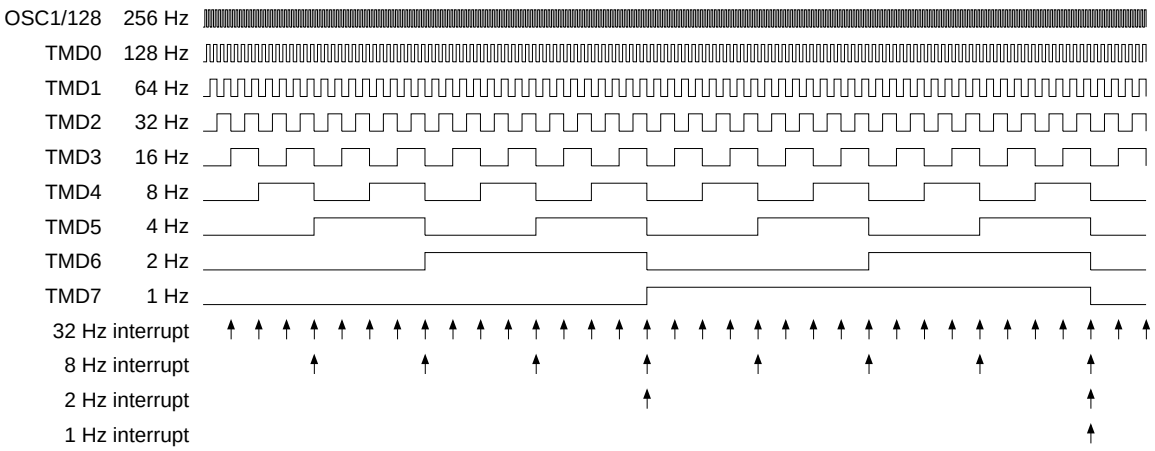


Fig. 5.8.2.2 Timing chart of clock timer

5.8.3 I/O memory for clock timer

Table 5.8.3.1 shows the clock timer control bits.

Table 5.8.3.1 Clock timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF40	D7	–	–	–	–	–		"0" when being read
	D6	FOUT2	FOUT frequency selection FOUT2 FOUT1 FOUT0 Frequency 0 0 0 fOSC1 / 1 0 0 1 fOSC1 / 2 0 1 0 fOSC1 / 4 0 1 1 fOSC1 / 8 1 0 0 fOSC3 / 1 1 0 1 fOSC3 / 2 1 1 0 fOSC3 / 4 1 1 1 fOSC3 / 8			0	R/W	
	D5	FOUT1				0	R/W	
	D4	FOUT0				0	R/W	
	D3	FOUTON	FOUT output control	On	Off	0	R/W	
	D2	WDRST	Watchdog timer reset	Reset	No operation	–	W	Constantly "0" when
	D1	TMRST	Clock timer reset	Reset	No operation	–	W	being read
	D0	TMRUN	Clock timer Run/Stop control	Run	Stop	0	R/W	
00FF41	D7	TMD7	Clock timer data 1 Hz	High	Low	0	R	
	D6	TMD6	Clock timer data 2 Hz			0	R	
	D5	TMD5	Clock timer data 4 Hz			0	R	
	D4	TMD4	Clock timer data 8 Hz			0	R	
	D3	TMD3	Clock timer data 16 Hz			0	R	
	D2	TMD2	Clock timer data 32 Hz			0	R	
	D1	TMD1	Clock timer data 64 Hz			0	R	
	D0	TMD0	Clock timer data 128 Hz			0	R	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 PTM1 PTM0 Priority level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag			0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	

TMD0–TMD7: 00FF41H

The clock timer data can be read out.
Each bit of TMD0–TMD7 and frequency correspondence are as follows:

TMD0:	128 Hz	TMD4:	8 Hz
TMD1:	64 Hz	TMD5:	4 Hz
TMD2:	32 Hz	TMD6:	2 Hz
TMD3:	16 Hz	TMD7:	1 Hz

Since the TMD0–TMD7 is exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

TMRST: 00FF40H•D1

Resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

The clock timer is reset by writing "1" to the TMRST.
When the clock timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the TMRST.
Since the TMRST is exclusively for writing, it always becomes "0" during reading.

TMRUN: 00FF40H•D0

Controls RUN / STOP of the clock timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The clock timer starts up-counting by writing "1" to the TMRUN and stops by writing "0".
In the STOP status, the count data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the TMRUN is set to "0" (STOP).

PTM0, PTM1: 00FF20H•D0, D1

Sets the priority level of the clock timer interrupt. The two bits PTM0 and PTM1 are the interrupt priority register corresponding to the clock timer interrupt. Table 5.8.3.2 shows the interrupt priority level which can be set by this register.

Table 5.8.3.2 Interrupt priority level settings

PTM1	PTM0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ETM1, ETM2, ETM8, ETM32: 00FF22H•D0–D3

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ETM1, ETM2, ETM8 and ETM32 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 2 Hz, 8 Hz and 32 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FTM1, FTM2, FTM8, FTM32: 00FF24H•D0–D3

Indicates the clock timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FTM1, FTM2, FTM8 and FTM32 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 2 Hz, 8 Hz and 32 Hz and are set to "1" at the falling edge of each signal.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.8.4 Programming notes

(1) The clock timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the TMRUN register. Consequently, when "0" is written to the TMRUN, the timer shifts to STOP status when the counter is incremented "1". The TMRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.8.4.1 shows the timing chart of the RUN / STOP control.

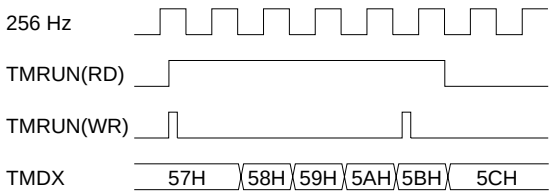


Fig. 5.8.4.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the clock timer is in the RUN status (TMRUN = "1"). The clock timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (TMRUN = "0") prior to executing the SLP instruction.

5.9 Stopwatch Timer

5.9.1 Configuration of stopwatch timer

The E0C88816 has a built-in 1/100 sec and 1/10 sec stopwatch timer. The stopwatch timer is composed of a 4-bit 2 stage BCD counter (1/100 sec units and 1/10 sec units) that makes the 256 Hz signal that divides the fOSC1 the input clock and it can read the count data by software.
Figure 5.9.1.1 shows the configuration of the stopwatch timer.
The stopwatch timer can be used as a timer different from the clock timer and can easily realize stopwatch and other such functions by software.

5.9.2 Count up pattern

The stopwatch timer is respectively composed of the 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.

Figure 5.9.2.1 shows the count up pattern of the stopwatch timer.

The feedback dividing circuit generates an approximate 100 Hz signal at 2/256 sec and 3/256 sec intervals from a 256 Hz signal divided from fOSC1.

The 1/100 sec counter (SWD0–SWD3) generates an approximate 10 Hz signal at 25/256 sec and 26/256 sec intervals by counting the approximate 100 Hz signal generated by the feedback dividing circuit in 2/256 sec and 3/256 sec intervals. The count-up is made approximately 1/100 sec counting by the 2/256 sec and 3/256 sec intervals.

The 1/10 sec counter (SWD4–SWD7) generates a 1 Hz signal by counting the approximate 10 Hz signal generated by the 1/100 sec counter at 25/256 sec and 26/256 sec intervals in 4:6 ratios.

The count-up is made approximately 1/10 sec counting by 25/256 sec and 26/256 sec intervals.

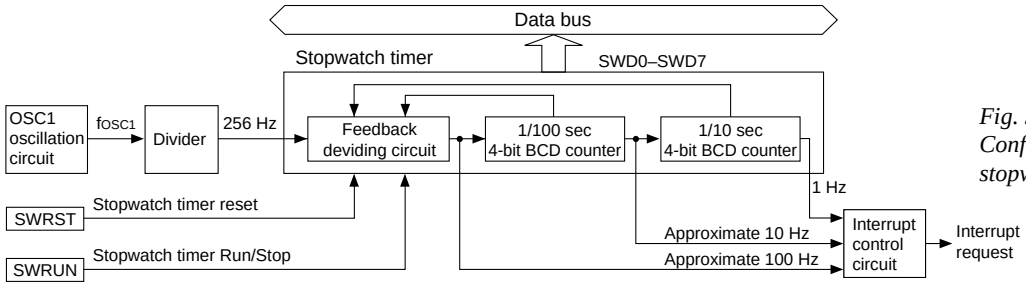


Fig. 5.9.1.1 Configuration of stopwatch timer

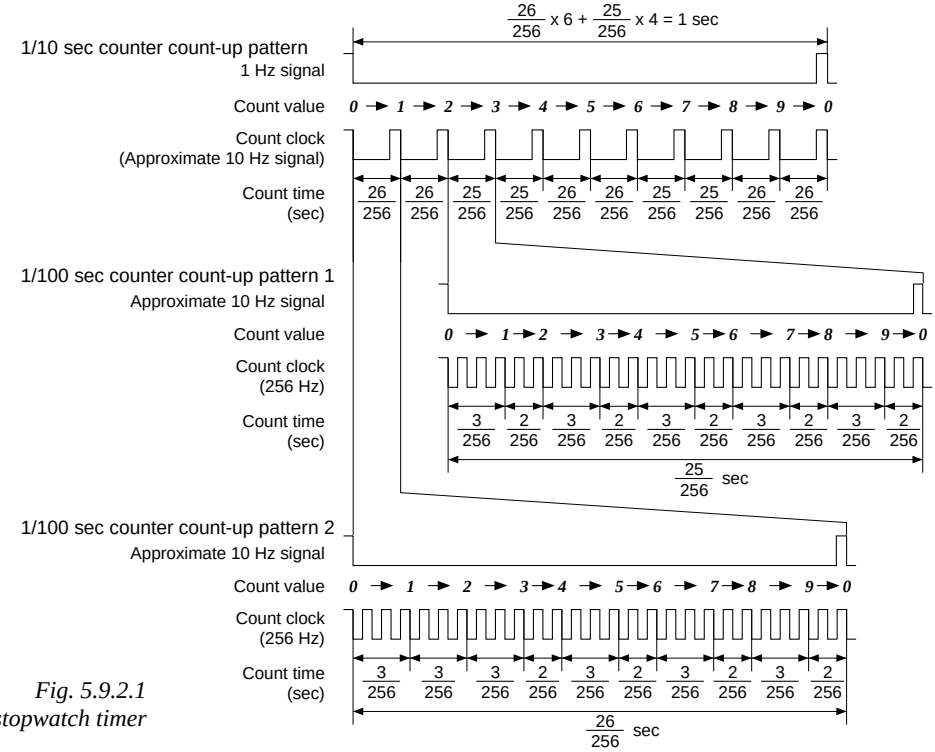


Fig. 5.9.2.1 Count-up pattern of stopwatch timer

5.9.3 Interrupt function

The stopwatch timer can generate an interrupt by each of the 100 Hz (approximately 100 Hz), 10 Hz (approximately 10 Hz) and 1 Hz signals.
Figure 5.9.3.1 shows the configuration of the stopwatch timer interrupt circuit.

The corresponding factor flags FSW100, FSW10 and FSW1 are respectively set to "1" at the falling edge of the 100 Hz, 10Hz and 1Hz signal and an interrupt is generated. Interrupt can be prohibited by the setting of the interrupt enable registers ESW100, ESW10 and ESW1 corresponding to each interrupt factor flag.

In addition, a priority level of the stopwatch timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PSW0 and PSW1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.16 Interrupt and Standby Status".
The exception processing vector addresses of each interrupt factor are respectively set as shown below.

100 Hz interrupt:	000016H
10 Hz interrupt:	000018H
1 Hz interrupt:	00001AH

Figure 5.9.3.2 shows the timing chart for the stopwatch timer.

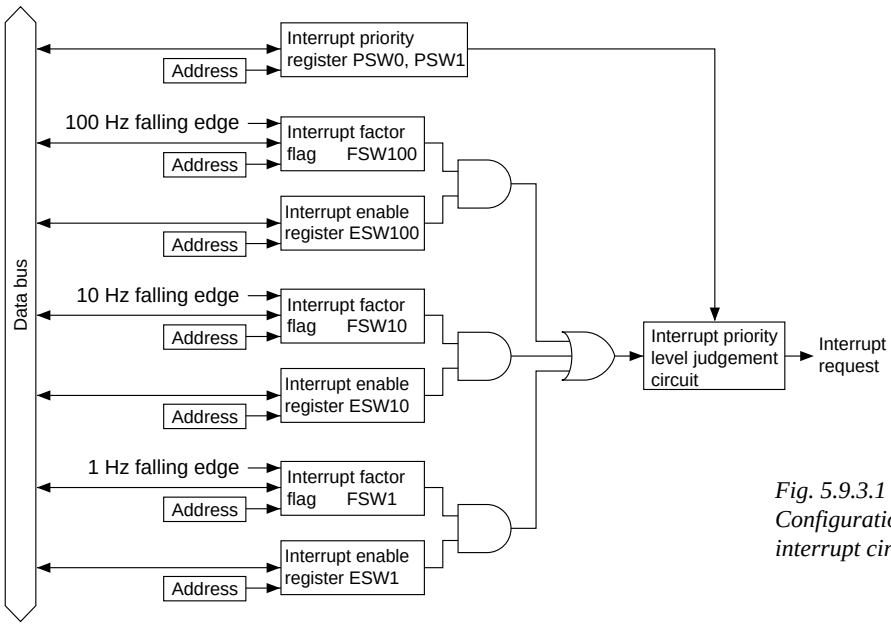


Fig. 5.9.3.1
Configuration of the stopwatch timer interrupt circuit

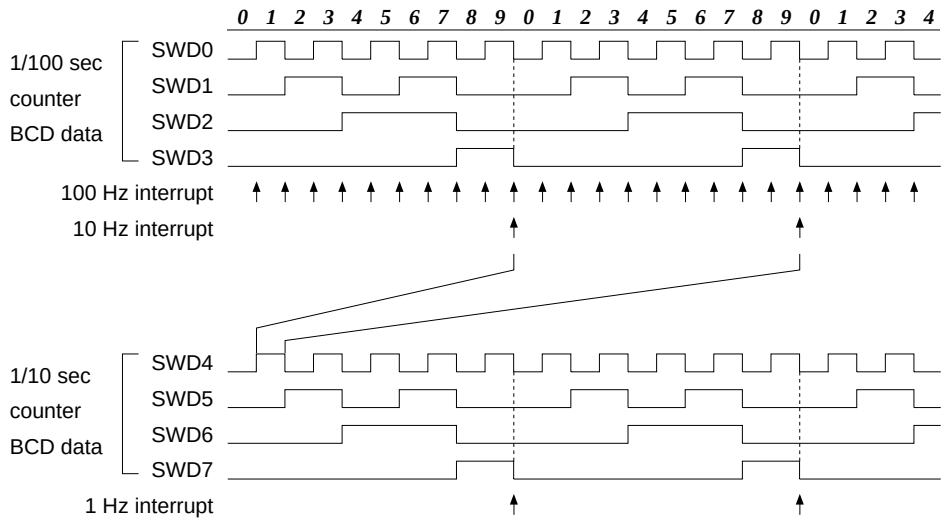


Fig. 5.9.3.2
Stopwatch timer timing chart

5.9.4 I/O memory for stopwatch timer

Table 5.9.4.1 shows the stopwatch timer control bits.

Table 5.9.4.1 Stopwatch timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF42	D7	–	–	–	–	–		Constantly "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	SWRST	Stopwatch timer reset	Reset	No operation	–	W	
	D0	SWRUN	Stopwatch timer Run/Stop control	Run	Stop	0	R/W	
00FF43	D7	SWD7	Stopwatch timer data BCD (1/10 sec)			0	R	
	D6	SWD6				0	R	
	D5	SWD5				0	R	
	D4	SWD4				0	R	
	D3	SWD3	Stopwatch timer data BCD (1/100 sec)			0	R	
	D2	SWD2				0	R	
	D1	SWD1				0	R	
	D0	SWD0				0	R	
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 PSIF1 PSIF0 PSW1 PSW0 Priority PTM1 PTM0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register			0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register			0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register			0	R/W	
	D0	PTM0				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated (W) Reset	(R) No interrupt factor is generated (W) No operation	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag			0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	

SWD0–SWD7: 00FF43H

The stopwatch timer data can be read out.
Higher and lower nibbles and BCD digit correspondence are as follows:

SWD0–SWD3:	BCD (1/100 sec)
SWD4–SWD7:	BCD (1/10 sec)

Since SWD0–SWD7 are exclusively for reading, the write operation is invalid.
At initial reset, the timer data is set to "00H".

SWRST: 00FF42H•D1

Resets the stopwatch timer.

When "1" is written:	Stopwatch timer reset
When "0" is written:	No operation
Reading:	Always "0"

The stopwatch timer is reset by writing "1" to the SWRST. When the stopwatch timer is reset in the RUN status, it restarts immediately after resetting. In the case of the STOP status, the reset data "00H" is maintained.
No operation results when "0" is written to the SWRST.
Since the SWRST is exclusively for writing, it always becomes "0" during reading.

SWRUN: 00FF42H•D0

Controls RUN/STOP of the stopwatch timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

The stopwatch timer starts up-counting by writing "1" to the SWRUN and stops by writing "0".
In the STOP status, the timer data is maintained until it is reset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
At initial reset, the SWRUN is set at "0" (STOP).

PSW0, PSW1: 00FF20H•D2, D3

Sets the priority level of the stopwatch timer interrupt.
The two bits PSW0 and PSW1 are the interrupt priority register corresponding to the stopwatch timer interrupt. Table 5.9.4.2 shows the interrupt priority level which can be set by this register.

Table 5.9.4.2 Interrupt priority level settings

PSW1	PSW0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

ESW1, ESW10, ESW100: 00FF22H•D4, D5, D6

Enables or disables the generation of an interrupt for the CPU.

When "1" is written:	Interrupt enabled
When "0" is written:	Interrupt disabled
Reading:	Valid

The ESW1, ESW10 and ESW100 are interrupt enable registers that respectively correspond to the interrupt factors for 1 Hz, 10 Hz and 100 Hz. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, this register is set to "0" (interrupt disabled).

FSW1, FSW10, FSW100: 00FF24H•D4, D5, D6

Indicates the stopwatch timer interrupt generation status.

When "1" is read:	Interrupt factor present
When "0" is read:	Interrupt factor not present
When "1" is written:	Resets factor flag
When "0" is written:	Invalid

The FSW1, FSW10 and FSW100 are interrupt factor flags that respectively correspond to the interrupts for 1 Hz, 10 Hz and 100 Hz and are set to "1" in synchronization with the falling edge of each signal. When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU. Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is reset to "0".

5.9.5 Programming notes

(1) The stopwatch timer is actually made to RUN / STOP in synchronization with the falling edge of the 256 Hz signal after writing to the SWRUN register. Consequently, when "0" is written to the SWRUN, the timer shifts to STOP status when the counter is incremented "1". The SWRUN maintains "1" for reading until the timer actually shifts to STOP status.
Figure 5.9.5.1 shows the timing chart of the RUN / STOP control.

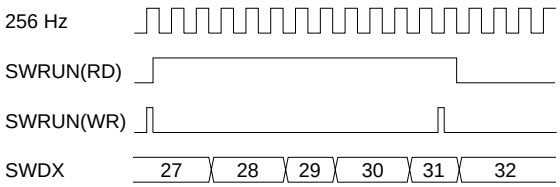


Fig. 5.9.5.1 Timing chart of RUN/STOP control

(2) The SLP instruction is executed when the stopwatch timer is in the RUN status (SWRUN = "1"). The stopwatch timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (SWRUN = "0") prior to executing the SLP instruction.

5.10 Programmable Timer

5.10.1 Configuration of programmable timer

The E0C88816 has two built-in 8-bit programmable timer systems (timer 0 and timer 1).
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channels or 16-bit × 1 channel programmable timer. They also have an event counter function and a pulse width measurement function using the K10 input port terminal.
Figure 5.10.1.1 shows the configuration of the programmable timer.

Programmable setting of the transfer rate is possible, due to the fact that the programmable timer underflow signal can be used as a synchronous clock for the serial interface.
Furthermore, this halved underflow signal (TOUT) can also be output externally from the R27 output port terminal. Furthermore, the R26 output port terminal can be used to output the $\overline{\text{TOUT}}$ signal (TOUT inverted signal) by mask option.

5.10.2 Mask option

$\overline{\text{TOUT}}$ output (R26 port specification)
☐ Use ($\overline{\text{TOUT}}$ output)
☐ Not Use (DC output)

In the E0C88816, the R26 output port can be configured as the $\overline{\text{TOUT}}$ (TOUT inverted signal) output port by mask option. The description for the $\overline{\text{TOUT}}$ output in this section assumes that the R26 output specification is set to the $\overline{\text{TOUT}}$ output.

5.10.3 Count operation and setting basic mode

Here we will explain the basic operation and setting of the programmable timer.

■ Setting of initial value and counting down

The timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are registers that set the initial value of the counter.
By writing "1" to the preset control bit PSET0 (timer 0) or PSET1 (timer 1), the down counter loads the initial value set in the reload register RLD.
Therefore, down-counting is executed from the stored initial value according to the input clock.

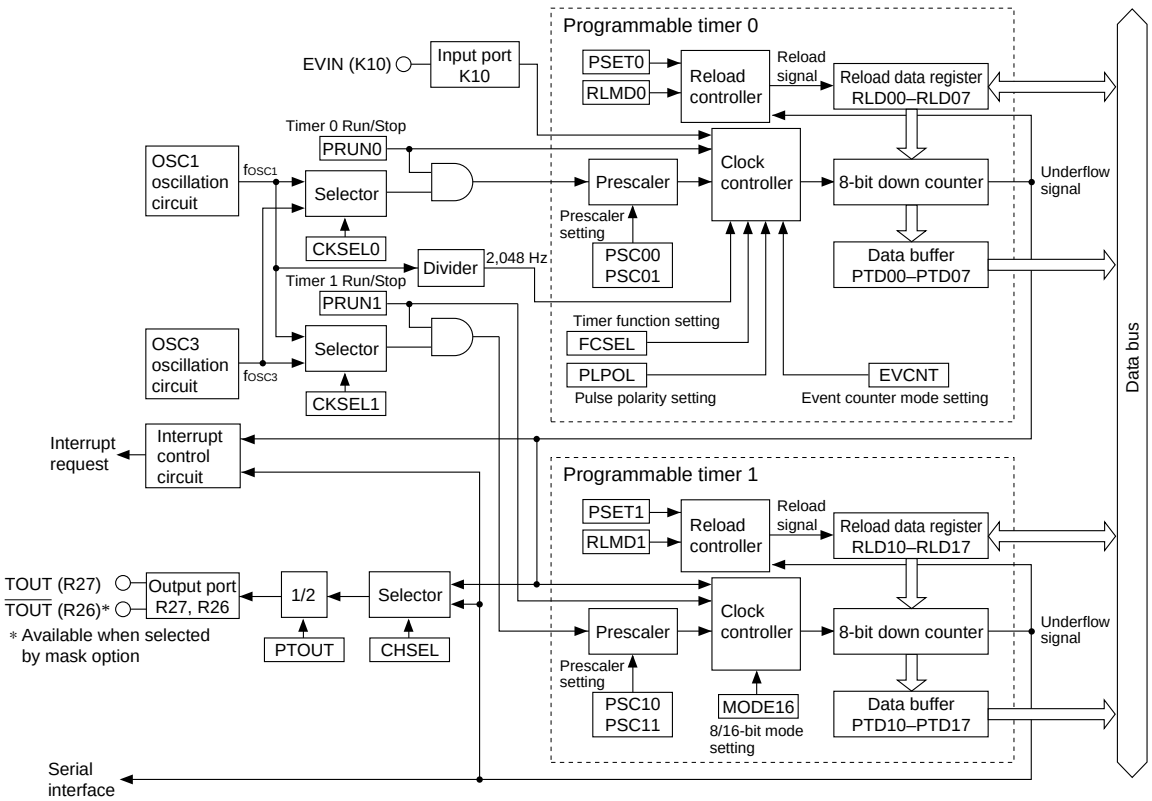


Fig. 5.10.1.1 Configuration of programmable timer

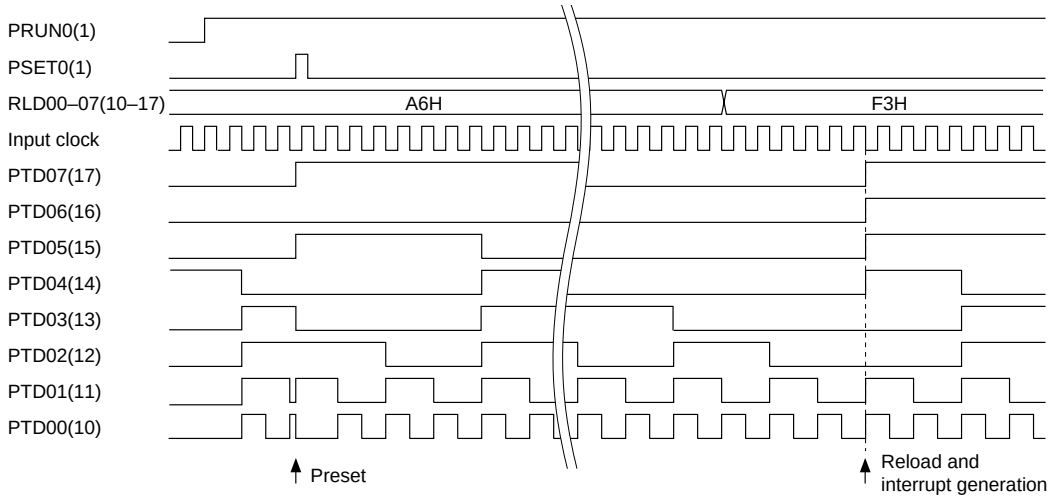


Fig. 5.10.3.1 Basic operation timing of the counter

The registers PRUN0 (timer 0) and PRUN1 (timer 1) are provided to control the RUN / STOP for timers 0 and 1.
After the reload data has been preset into the counter, down-counting is begun by writing "1" to this register. When "0" is written, the clock input is prohibited and the count stops.
The control of this RUN / STOP has no affect on the counter data. The counter data is maintained even during the stoppage of the counter and it can start the count, continuing from that data.

The reading of the counter data can be done through the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) with optional timing.
When the down-counting has progressed and an underflow is generated, the counter reloads the initial value set in the reload data register.
This underflow signal controls an interrupt generation, pulse (TOUT and $\overline{\text{TOUT}}$ signals) output and serial interface clocking, in addition to reloading the counter.

■ Continuous/one-shot mode setting

By writing "1" to the continuous / one-shot mode selection registers CONT0 (timer 0) and CONT1 (timer 1), the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. This mode is suitable when programmable intervals are necessary (such as an interrupt and a synchronous clock for the serial interface).
On the other hand, when writing "0" to the registers CONT0 (timer 0) and CONT1 (timer 1), the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, the RUN / STOP control register PRUN0 (timer 0) and PRUN1 (timer 1) are automatically reset to "0". After the counter stops, a one-shot count can be performed once again by writing "1" to registers PRUN0 (timer 0) and PRUN1 (timer 1). This mode is suitable for single time measurement, for example.

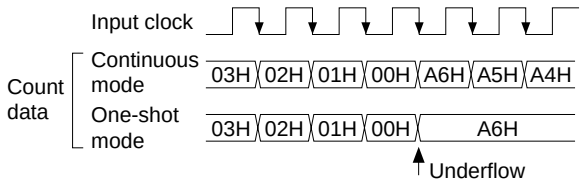


Fig. 5.10.3.2 Continuous mode and one-shot mode

■ 8/16-bit mode setting

By writing "0" to the 8/16-bit mode selection register MODE16, timer 0 and timer 1 are set as independent timers in 8-bit × 2 channels. In this mode, timer 0 and timer 1 can be controlled individually and each of them operates independently.
On the other hand, when writing "1" to the register MODE16, timer 0 and timer1 are set as 1 channel 16-bit timer. This is done by setting timer 0 to the lower 8 bits, and timer 1 to the upper 8 bits. The timer is controlled by timer 0's registers. In this case, the control registers for timer 1 are invalid. (PRUN1 is fixed at "0".)

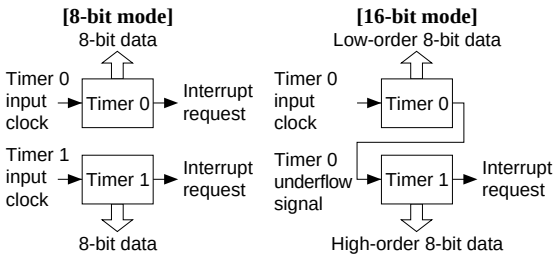


Fig. 5.10.3.3 8/16-bit mode setting and counter configuration

5.10.4 Setting of input clock

Prescalers have been provided for timers 0 and 1. The prescalers generate the input clock for each by dividing the source clock signal from the OSC1 or OSC3 oscillation circuit.
The source clock and the dividing ratio of the prescaler can be selected individually for timer 0 and timer 1 in software.

The input clocks are set by the below sequence.

(1) Selection of source clock

Select the source clock (OSC1 or OSC3) for each prescaler. This is done with the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1): when "0" is written, OSC1 is selected and when "1" is written, OSC3 is selected. When the 16-bit mode is selected, the source clock is selected by register CKSEL0, and the register CKSEL1 setting becomes invalid.
When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(2) Selection of prescaler dividing ratio

Select the dividing ratio of each prescaler from among 4 types. This selection is done by the prescaler dividing ratio selection registers PSC00/PSC01 (timer 0) and PSC10/PSC11 (timer 1). Setting value and dividing ratio correspondence are shown in Table 5.10.4.1.

Table 5.10.4.1 Selection of prescaler dividing ratio

PSC11 PSC01	PSC10 PSC00	Prescaler dividing ratio
1	1	Source clock / 64
1	0	Source clock / 16
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PRUN0 (timer 0) and PRUN1 (timer 1), the source clock is input to the prescaler. Therefore, the clock with selected dividing ratio is input to the timer and the timer starts counting down.
When the 16-bit mode has been selected, the dividing ratio for the source clock is selected by register PSC00/PSC01 and the setting of register PSC10/PSC11 becomes invalid.

5.10.5 Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a timer that obtains fixed cycles using the OSC1 or OSC3 oscillation circuit as a clock source.
See "5.10.3 Count operation and basic mode setting" for basic operation and control, and "5.10.4 Setting input clock" for the clock source and setting of the prescaler.

5.10.6 Event counter mode

Timer 0 includes an even counter function that counts by inputting an external clock (EVIN) to input port K10. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.
When the event counter mode is selected, timer 0 operates as an event counter and timer 1 operates as a normal timer in 8-bit mode. In the 16-bit mode, timer 0 and timer 1 operate as 1 channel 16-bit event counter. In the event counter mode, since the timer 0 is clocked externally, the settings of registers PSC00 / PSC01 become invalid.
Count down timing can be controlled by either the falling edge or rising edge selected by the timer 0 pulse polarity selection register PLPOL. When "0" is written to the register PLPOL, the falling edge is selected, and when "1" is written, the rising edge is selected. The timing is shown in Figure 5.10.6.1.

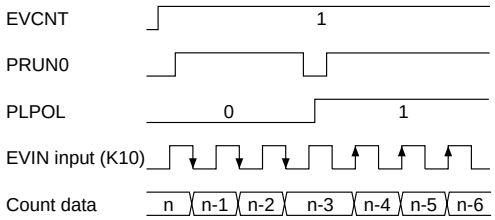


Fig. 5.10.6.1 Timing chart for event counter mode

The event counter also includes a noise rejecter to eliminate noise such as chattering for the external clock (EVIN). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
For a reliable count when "with noise rejecter" is selected, you must allow 0.98 msec or more pulse width for both LOW and HIGH levels. (The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.)
Figure 5.10.6.2 shows the count down timing with the noise rejecter selected.

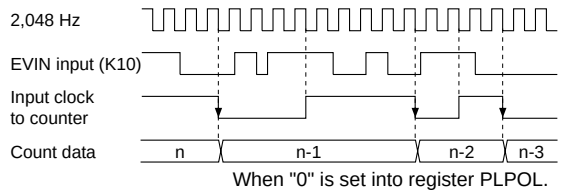


Fig. 5.10.6.2 Count down timing with noise rejecter

The event counter mode is the same as the timer mode except that the clock is external (EVIN).
See "5.10.3 Count operation and setting basic mode" for the basic operation and control.

5.10.7 Pulse width measurement timer mode

Timer 0 includes a pulse width measurement function that measures the width of the input signal to the K10 input port terminal. This function is selected by writing "1" to the timer function selection register FCSEL when in the timer mode (EVCNT = "0").
When the pulse width measurement mode is selected, timer 0 operates as an pulse width measurement and timer 1 operates as a normal timer in 8-bit mode. In the 16-bit mode, timer 0 and timer 1 operate as 1 channel 16-bit pulse width measurement.
The level of the input signal (EVIN) for measurement can be changed either a LOW or HIGH level by the timer 0 pulse polarity selection register PLPOL. When "0" is written to register PLPOL, a LOW level width is measured and when "1" is written, a HIGH level width is measured. The timing is shown in Figure 5.10.7.1.

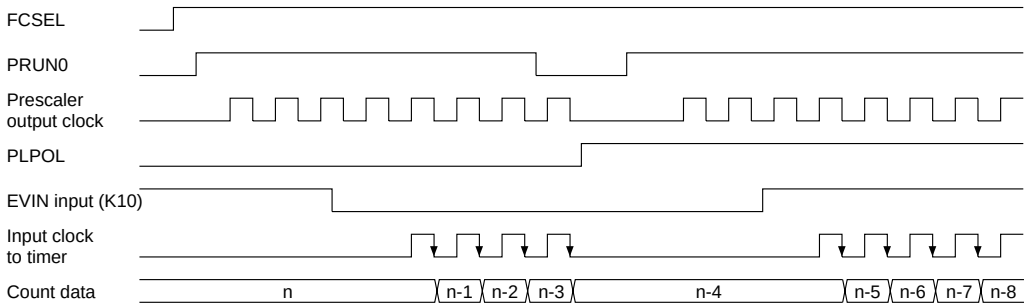


Fig. 5.10.7.1 Timing chart for pulse width measurement timer mode

The pulse width measurement timer mode is the same as the timer mode except that the input clock is controlled by the level of the signal (EVIN) input to the K10 input port terminal.
See "5.10.3 Count operation and setting basic mode" for the basic operation and control.

5.10.8 Interrupt function

The programmable timer can generate an interrupt due to an underflow signal of timer 0 and timer 1. Figure 5.10.8.1 shows the configuration of the programmable timer interrupt circuit.

The respectively corresponding interrupt factor flags FPT0 and FPT1 are set to "1" and an interrupt is generated by an underflow signal of timers 1 and 0. Interrupt can also be prohibited by the setting of the interrupt enable registers EPT0 and EPT1 corresponding to each interrupt flag.

In addition, a priority level of the programmable timer interrupt for the CPU can be optionally set at levels 0 to 3 by the interrupt priority registers PPT0 and PPT1.
For details on the above mentioned interrupt control registers and the operation following generation of an interrupt, see "5.16 Interrupt and Standby Status".

The exception processing vector addresses of each interrupt factor are respectively set as shown below.

Programmable timer 1 interrupt:	000006H
Programmable timer 0 interrupt:	000008H

When the 16-bit mode is selected, the interrupt factor flag FPT0 is not set to "1" and a timer 0 interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 is set to "1" by an underflow of the 16-bit counter.)

5.10.9 Setting of TOUT output

The programmable timer can generate the TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated from the above mentioned underflow signal by halving the frequency. The timer underflow which is to be used can be selected by the TOUT output channel selection register CHSEL. When writing "0" to register CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected. However, in the 16-bit mode, it is fixed in timer 1 (underflow of the 16-bit timer) and the setting of register CHSEL becomes invalid.
Figure 5.10.9.1 shows the TOUT signal waveform when channel switching.

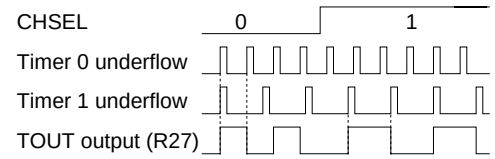


Fig. 5.10.9.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R27 output port terminal, and the programmable clock can be supplied to an external device.
Furthermore, the R26 output port terminal can be used to output the $\overline{\text{TOUT}}$ signal (TOUT inverted signal) by mask option.
The configuration of the output ports R27 and R26 is shown in Figure 5.10.9.2.

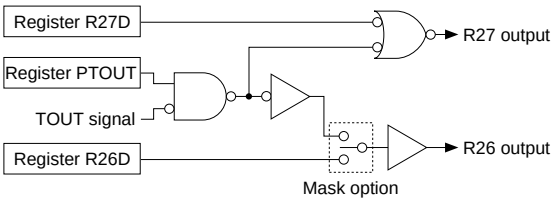


Fig. 5.10.9.2 Configuration of R27 and R26

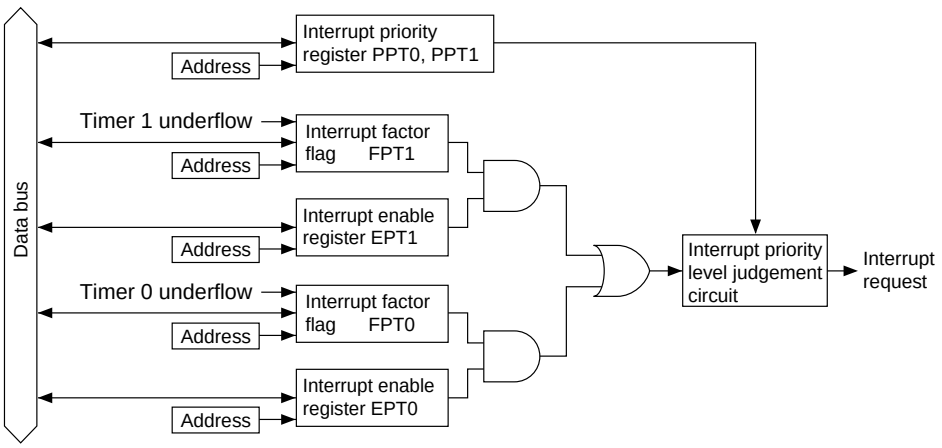


Fig. 5.10.8.1 Configuration of programmable timer interrupt circuit

The output control for the TOUT ($\overline{TOUT}$) signal is done by the register PTOUT. When you set "1" for the PTOUT, the TOUT ($\overline{TOUT}$) signal is output from the R27 (R26) output port terminal. When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{TOUT}$ output.

Since the TOUT signal is generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.
Figure 5.10.9.3 shows the output waveform of TOUT signal.

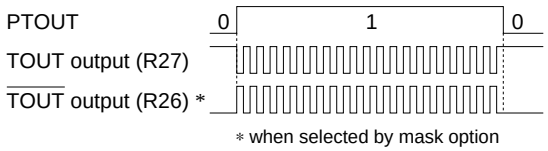


Fig. 5.10.9.3 TOUT output waveform

5.10.10 Transmission rate setting of serial interface

The underflow signal of the timer 1 can be used to clock the serial interface.
The transmission rate setting in this case is made in registers PSC1X and PLD1X, and is used to set the count mode to the reload count mode (RLMD1 = "1").
Since the underflow signal of the timer 1 is divided by 1/32 in the serial interface, the value set in register RLD1X which corresponds to the transmission rate is shown in the following expression:

RLD1X = fosc / (32*bps*4^{PSC1X}) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transmission rate
PSC1X: Setting value to the register PSC1X (0–3)

(00H can be set to RLD1X)

Table 5.10.10.1 shows an example of the transmission rate setting when the OSC3 oscillation circuit is used as a clock source.

Table 5.10.10.1 Example of transmission rate setting

Transfer rate (bps)	OSC3 oscillation frequency / Programmable timer settings					
	f_{OSC3} = 3.072 MHz		f_{OSC3} = 4.608 MHz		f_{OSC3} = 4.9152 MHz	
	PSC1X	RLD1X	PSC1X	RLD1X	PSC1X	RLD1X
9,600	0 (1/1)	09H	0 (1/1)	0EH	0 (1/1)	0FH
4,800	0 (1/1)	13H	0 (1/1)	1DH	0 (1/1)	1FH
2,400	0 (1/1)	27H	0 (1/1)	3BH	0 (1/1)	3FH
1,200	0 (1/1)	4FH	0 (1/1)	77H	0 (1/1)	7FH
600	0 (1/1)	9FH	0 (1/1)	EFH	0 (1/1)	FFH
300	1 (1/4)	4FH	1 (1/4)	77H	1 (1/4)	7FH
150	1 (1/4)	9FH	1 (1/4)	EFH	1 (1/4)	FFH

5.10.11 I/O memory for programmable timer

Table 5.10.11.1 shows the programmable timer control bits.

Table 5.10.11.1(a) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF30	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	MODE16	8/16-bit mode selection	16-bit x 1	8-bit x 2	0	R/W	
	D3	CHSEL	TOUT output channel selection	Timer 1	Timer 0	0	R/W	
	D2	PTOUT	TOUT output control	On	Off	0	R/W	
	D1	CKSEL1	Prescaler 1 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
	D0	CKSEL0	Prescaler 0 source clock selection	f_{OSC3}	f_{OSC1}	0	R/W	
00FF31	D7	EVCNT	Timer 0 counter mode selection	Event counter	Timer	0	R/W	
	D6	FCSEL	Timer 0 function selection: In timer mode	Pulse width measurement	Normal mode	0	R/W	
			Timer 0 function selection: In event counter mode	With noise rejector	Without noise rejector			
	D5	PLPOL	Timer 0 pulse polarity selection: Down count timing in event counter mode	Rising edge of K10 input	Falling edge of K10 input	0	R/W	
			Timer 0 pulse polarity selection: In pulse width measurement mode	High level measurement for K10 input	Low level measurement for K10 input			
	D4	PSC01	Timer 0 prescaler dividing ratio selection			0	R/W	
	D3	PSC00	PSC01 PSC00 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT0	Timer 0 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET0	Timer 0 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN0	Timer 0 Run/Stop control	Run	Stop	0	R/W	
00FF32	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	PSC11	Timer 1 prescaler dividing ratio selection			0	R/W	
	D3	PSC10	PSC11 PSC10 Prescaler dividing ratio 1 1 Source clock / 64 1 0 Source clock / 16 0 1 Source clock / 4 0 0 Source clock / 1			0	R/W	
	D2	CONT1	Timer 1 continuous/one-shot mode selection	Continuous	One-shot	0	R/W	
	D1	PSET1	Timer 1 preset	Preset	No operation	–	W	"0" when being read
	D0	PRUN1	Timer 1 Run/Stop control	Run	Stop	0	R/W	
00FF33	D7	RLD07	Timer 0 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD06	Timer 0 reload data D6			1	R/W	
	D5	RLD05	Timer 0 reload data D5			1	R/W	
	D4	RLD04	Timer 0 reload data D4			1	R/W	
	D3	RLD03	Timer 0 reload data D3			1	R/W	
	D2	RLD02	Timer 0 reload data D2			1	R/W	
	D1	RLD01	Timer 0 reload data D1			1	R/W	
	D0	RLD00	Timer 0 reload data D0 (LSB)			1	R/W	

Table 5.10.11.1(b) Programmable timer control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF34	D7	RLD17	Timer 1 reload data D7 (MSB)	High	Low	1	R/W	
	D6	RLD16	Timer 1 reload data D6			1	R/W	
	D5	RLD15	Timer 1 reload data D5			1	R/W	
	D4	RLD14	Timer 1 reload data D4			1	R/W	
	D3	RLD13	Timer 1 reload data D3			1	R/W	
	D2	RLD12	Timer 1 reload data D2			1	R/W	
	D1	RLD11	Timer 1 reload data D1			1	R/W	
	D0	RLD10	Timer 1 reload data D0 (LSB)			1	R/W	
00FF35	D7	PTD07	Timer 0 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD06	Timer 0 counter data D6			1	R	
	D5	PTD05	Timer 0 counter data D5			1	R	
	D4	PTD04	Timer 0 counter data D4			1	R	
	D3	PTD03	Timer 0 counter data D3			1	R	
	D2	PTD02	Timer 0 counter data D2			1	R	
	D1	PTD01	Timer 0 counter data D1			1	R	
	D0	PTD00	Timer 0 counter data D0 (LSB)			1	R	
00FF36	D7	PTD17	Timer 1 counter data D7 (MSB)	High	Low	1	R	
	D6	PTD16	Timer 1 counter data D6			1	R	
	D5	PTD15	Timer 1 counter data D5			1	R	
	D4	PTD14	Timer 1 counter data D4			1	R	
	D3	PTD13	Timer 1 counter data D3			1	R	
	D2	PTD12	Timer 1 counter data D2			1	R	
	D1	PTD11	Timer 1 counter data D1			1	R	
	D0	PTD10	Timer 1 counter data D0 (LSB)			1	R	
00FF21	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PK11 / PPT0 PK10 / Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10 interrupt priority register			0	R/W	
	D0	PK10				0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated / (W) Reset	(R) No interrupt factor is generated / (W) No operation	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag			0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

MODE16: 00FF30H•D4

Selects the 8 / 16-bit mode.

When "1" is written: 16 bits × 1 channel
When "0" is written: 8 bits × 2 channels
Reading: Valid

Select whether timer 0 and timer 1 will be used as 2 channel independent 8-bit timers or as a 1 channel combined 16-bit timer. When "0" is written to MODE16, 8-bit × 2 channels is selected and when "1" is written, 16-bit × 1 channel is selected.
At initial reset, MODE16 is set to "0" (8-bit × 2 channels).

CKSEL0, CKSEL1: 00FF30H•D0, D1

Select the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

Select whether the source clock of prescaler 0 will be set to OSC1 or OSC3. When "0" is written to CKSEL0, OSC1 is selected and when "1" is written, OSC3 is selected.
In the same way, the source clock of prescaler 1 is selected by CKSEL1.
When event counter mode has been selected, the setting of the CKSEL0 becomes invalid. In the same way, the CKSEL1 setting becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (OSC1 clock).

PSC00, PSC01: 00FF31H•D3, D4
PSC10, PSC11: 00FF32H•D3, D4

Select the dividing ratio of the prescaler.
Two-bit PSC00 and PSC01 is the prescaler dividing ratio selection registers for timer 0, and the two-bit PSC10 and PSC11 correspond to timer 1. The prescaler dividing ratios that can be set by these registers are shown in Table 5.10.11.2.

Table 5.10.11.2 Selection of prescaler dividing ratio

PSC11 PSC01	PSC10 PSC00	Prescaler dividing ratio
1	1	Input clock / 64
1	0	Input clock / 16
0	1	Input clock / 4
0	0	Input clock / 1

When event counter mode has been selected, the setting of the PSC00 and PSC01 becomes invalid. In the same way, the PSC10 and PSC11 setting becomes invalid when 16-bit mode has been selected.
At initial reset, this register is set to "0" (input clock / 1).

EVCNT: 00FF31H•D7

Selects the counter mode for the timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

Select whether timer 0 will be used as an event counter or a timer. When "1" is written to EVCNT, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, EVCNT is set to "0" (timer mode).

FCSEL: 00FF31H•D6

Selects the function for each counter mode of timer 0.

• In timer mode

When "1" is written: Pulse width measurement timer mode
When "0" is written: Normal mode
Reading: Valid

In the timer mode, select whether timer 0 will be used as a pulse width measurement timer or a normal timer. When "1" is written to FCSEL, the pulse width measurement mode is selected and the counting is done according to the level of the signal (EVIN) input to the K10 input port terminal. When "0" is written to FCSEL, the normal mode is selected and the counting is not affected by the K10 input port terminal.

• In event counter mode

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

In the event counter mode, select whether the noise rejecter for the K10 input port terminal will be selected or not.
When "1" is written to FCSEL, the noise rejecter is selected and counting is done by an external clock (EVIN) with 0.98 msec or more pulse width. (The noise rejecter allows clocking counter at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K10 input port terminal. Consequently, the pulse width that can reliably be rejected is 0.48 msec.)
When "0" is written to FCSEL, the noise rejector is not selected and the counting is done directly by an external clock (EVIN) input to the K10 input port terminal.
At initial reset, FCSEL is set to "0".

PLPOL: 00FF31H•D5

Selects the pulse polarity for the K10 input port terminal.

• In event counter mode

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

In the event counter mode, select whether the count timing will be set at the falling edge of the external clock (EVIN) input to the K10 input port terminal or at the rising edge. When "0" is written to PLPOL, the falling edge is selected and when "1" is written, the rising edge is selected.

• In pulse width measurement mode

When "1" is written: High level pulse width measurement
When "0" is written: LOW level pulse width measurement
Reading: Valid

In the pulse width measurement mode, select whether the LOW level width of the signal (EVIN) input to the K10 input port terminal will be measured or the HIGH level will be measured. When "0" is written to PLPOL, the LOW level width measurement is selected and when "1" is written, the HIGH level width measurement is selected.
In the normal mode (EVCNT = FCSEL = "0"), the setting of PLPOL becomes invalid.
At initial reset, PLPOL is set to "0".

CONT0, CONT1: 00FF31H•D2, 00FF32H•D2

Select the continuous / one-shot mode.

When "1" is written: Continuous mode
When "0" is written: One-shot mode
Reading: Valid

Select whether timer 0 will be used in the continuous mode or in the one-shot mode.
By writing "1" to CONT0, the programmable timer is set to the continuous mode. In the continuous mode, the initial counter value is automatically loaded when an underflow is generated, and counting is continued. On the other hand, when writing "0" to CONT0, the programmable timer is set to the one-shot mode. The counter loads an initial value and stops when an underflow is generated. At this time, PRUN0 is automatically reset to "0".
In the same way, the continuous / one-shot mode for timer 1 is selected by CONT1. (In the one-shot mode for timer 1, PRUN1 is automatically reset to "0" when the counter underflow is generated.)
At initial reset, this register is set to "0" (one-shot mode).

RLD00–RLD07: 00FF33H
RLD10–RLD17: 00FF34H

Sets the initial value for the counter.

RLD00–RLD07: Reload data for Timer 0
RLD10–RLD17: Reload data for Timer 1

The reload data set in this register is loaded into the respective counters and is counted down with that as the initial value.
Reload data is loaded to the counter under two conditions, when "1" is written to PSET0 or PSET1 and when the counter underflow automatically loads.
At initial reset, this register is set to "FFH".

PTD00–PTD07: 00FF35H
PTD10–PTD17: 00FF36H

Data of the programmable timer can be read out.

PTD00–PTD07: Timer 0 counter data
PTD10–PTD17: Timer 1 counter data

These bits act as a buffer to maintain the counter data during readout, and the data can be read as optional timing. However, in the 16-bit mode, to avoid a read error, (data error when a borrow from timer 0 to timer 1 is generated in the middle of reading PTD00–PTD07 and PTD10–PTD17), PTD10–PTD17 latches the timer 1 counter data according to the reading of PTD00–PTD07.
The latched status of PTD10–PTD17 is canceled according to the readout of PTD10–PTD17 or when 0.73–1.22 msec (depends on the readout timing) has elapsed. Therefore, in 16-bit mode, be sure to read the counter data of PTD00–PTD07 and PTD10–PTD17 in order.
Since these bits are exclusively for reading, the write operation is invalid.
At initial reset, these bits are set to "FFH".

PSET0, PSET1: 00FF31H•D1, 00FF32H•D1

Presets the reload data to the counter.

When "1" is written: Preset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PSET0, the reload data in PLD00–PLD07 is preset to the counter of timer 0. When the counter of timer 0 is preset in the RUN status, it restarts immediately after presetting.
In the case of STOP status, the reload data that has been preset is maintained.
No operation results when "0" is written.
In the same way, the reload data in PLD10–PLD17 is preset to the counter of timer 1 by PSET1.
When the 16-bit mode is selected, writing "1" to PSET1 is invalid.
This bit is exclusively for writing, it always becomes "0" during reading.

PRUN0, PRUN1: 00FF31H•D0, 00FF32H•D0

Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter of timer 0 starts down-counting by writing "1" to PRUN0 and stops by writing "0". In the STOP status, the counter data is maintained until it is preset or set in the next RUN status. Also, when the STOP status changes to the RUN status, the data that was maintained can be used for resuming the count.
In the same way, the RUN / STOP of the timer 1 counter is controlled by PRUN1.
When the 16-bit mode is selected, PRUN1 is fixed at "0".
At initial reset and when an underflow is generated in the one-shot mode, this register is set to "0" (STOP).

CHSEL: 00FF30H•D3

Selects a channel for generating the TOUT and $\overline{\text{TOUT}}$ signals.

When "1" is written: Timer 0 underflow
When "0" is written: Timer 1 underflow
Reading: Valid

Select whether the timer 0 underflow will be used for the TOUT and $\overline{\text{TOUT}}$ signals or the timer 1 underflow will be used. When "0" is written to CHSEL, timer 0 is selected and when "1" is written, timer 1 is selected.When the 16-bit mode has been selected, it is fixed to timer 1 (underflow of the 16-bit timer), and setting of CHSEL becomes invalid.
At initial reset, CHSEL is set to "0" (timer 1 underflow).

PTOUT: 00FF30H•D2

Controls the TOUT (programmable timer output clock) output and $\overline{\text{TOUT}}$ (TOUT inverted signal) output.

When "1" is written: TOUT / $\overline{\text{TOUT}}$ output
When "0" is written: HIGH (DC) output [R27]
LOW (DC) output [R26]
Reading: Valid

PTOUT is the output control register for TOUT and $\overline{\text{TOUT}}$ signals. When "1" is set to the register, the TOUT ($\overline{\text{TOUT}}$) signal is output from the output port terminal R27 (R26). When "0" is set, the R27 goes HIGH (V_{DD}) and the R26 goes LOW (V_{SS}).
To output the TOUT signal, "1" must always be set for the data register R27D. The data register R26D does not affect the $\overline{\text{TOUT}}$ output.
The $\overline{\text{TOUT}}$ signal can be output from R26 only when the function is selected by mask option.
At initial reset, PTOUT is set to "0" (DC output).

PPT0, PPT1: 00FF21H•D2, D3

Sets the priority level of the programmable timer interrupt.
The two bits PPT0 and PPT1 are the interrupt priority register corresponding to the programmable timer interrupt. Table 5.10.11.3 shows the interrupt priority level which can be set by this register.

Table 5.10.11.3 Interrupt priority level settings

PPT1	PPT0	Interrupt priority level
1	1	Level 3 ($\overline{\text{IRQ3}}$)
1	0	Level 2 ($\overline{\text{IRQ2}}$)
0	1	Level 1 ($\overline{\text{IRQ1}}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EPT0, EPT1: 00FF23H•D6, D7

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Interrupt enabled
When "0" is written: Interrupt disabled
Reading: Valid

The EPT0 and EPT1 are interrupt enable registers that respectively correspond to the interrupt factors for timer 0 and timer 1. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
When the 16-bit mode is selected, setting of EPT0 becomes invalid.
At initial reset, this register is set to "0" (interrupt disabled).

FPT0, FPT1: 00FF25H•D6, D7

Indicates the programmable timer interrupt generation status.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

The FPT0 and FPT1 are interrupt factor flags that respectively correspond to the interrupts for timer 0 and timer 1 and are set to "1" in synchronization with the underflow of each counter.
When set in this manner, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of interrupt flags (I0 and I1), an interrupt will be generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.

To accept the subsequent interrupt after interrupt generation, re-setting of the interrupt flags (set interrupt flag to lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and interrupt factor flag reset are necessary. The interrupt factor flag is reset to "0" by writing "1".
When the 16-bit mode is selected, the interrupt factor flag FPT0 is not set to "1" and a timer 0 interrupt cannot be generated. (In the 16-bit mode, the interrupt factor flag FPT1 is set to "1" by an underflow of the 16-bit counter.)
At initial reset, this flag is reset to "0".

5.10.12 Programming notes

(1) The programmable timer is actually made to RUN / STOP in synchronization with the falling edge of the input clock after writing to the PRUN0(1) register. Consequently, when "0" is written to the PRUN0(1), the timer shifts to STOP status when the counter is decremented "1". The PRUN0(1) maintains "1" for reading until the timer actually shifts to STOP status. Figure 5.10.12.1 shows the timing chart of the RUN / STOP control.

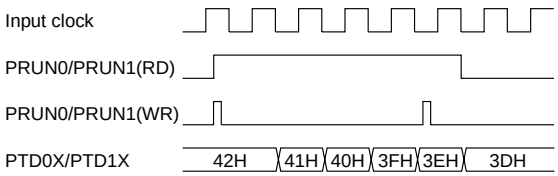


Fig. 5.10.12.1 Timing chart of RUN/STOP control

The event counter mode is excluded from the above note.

(2) The SLP instruction is executed when the programmable timer is in the RUN status (PRUN0(1) = "1"). The programmable timer operation will become unstable when returning from SLEEP status. Therefore, when shifting to SLEEP status, set the clock timer to STOP status (PRUN0(1) = "0") prior to executing the SLP instruction.
In the same way, disable the TOUT and $\overline{\text{TOUT}}$ signal outputs (PTOUT = "0") to avoid an unstable clock output to the R27 and R26 output port terminals.

(3) Since the TOUT and $\overline{\text{TOUT}}$ signals are generated asynchronously from the register PTOUT, when the signal is turned ON or OFF by the register setting, a hazard of a 1 / 2 cycle or less is generated.

(4) When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(5) When the 16-bit mode has been selected, be sure to read the counter data in the order of PTD00–PTD07 and PTD10–PTD17. Moreover, the time interval between reading PTD00–PTD07 and PTD10–PTD17 should be 0.73 msec or less.

5.11 LCD Controller

5.11.1 Configuration of LCD controller

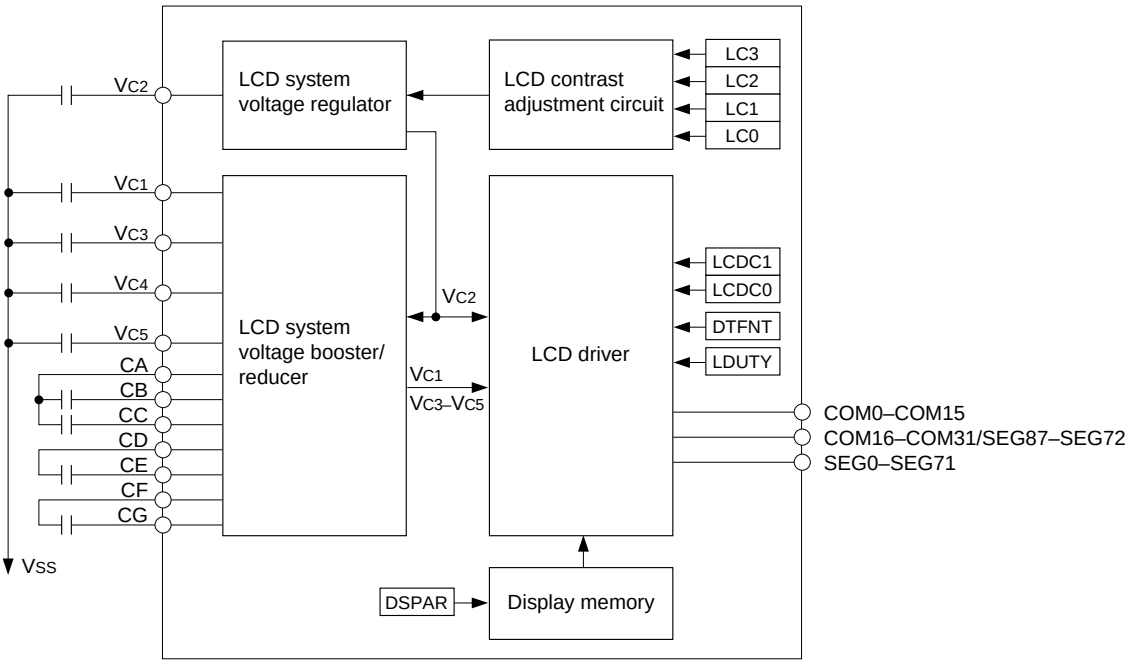
The E0C88816 has a built-in dot matrix LCD driver that can drive an LCD panel with a maximum of 2,304 dots (72 segments × 32 commons).
Figure 5.11.1.1 shows the configuration of the LCD controller and the drive power supply.

5.11.2 Mask option

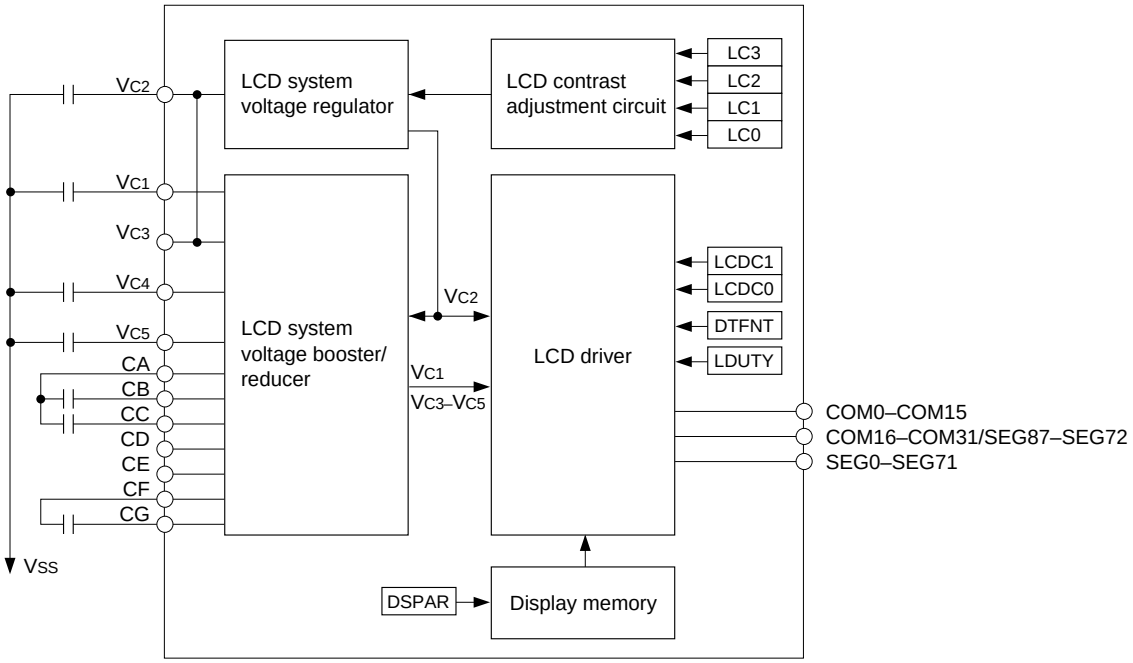
The drive duty for the built-in LCD driver can be selected whether it will be 1/32 and 1/16 software-switched or fixed at 1/8 by mask option.

LCD drive duty
☐ 1/32 & 1/16 duty
☐ 1/8 duty

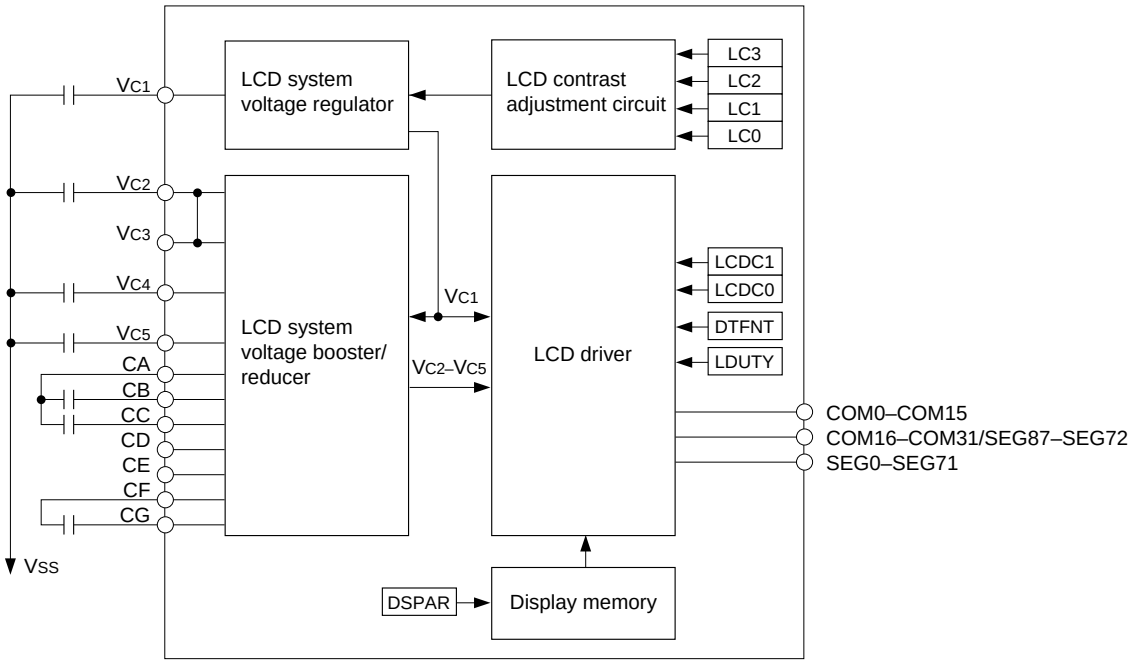
When "1/32 & 1/16 duty" is selected, the drive duty can be selected by software. When "0" is written to the drive duty selection register LDUTY, 1/32 duty is selected and when "1" is written, 1/16 duty is selected.
When "1/8 duty" is selected, the drive duty is fixed at 1/8 and setting of LDUTY becomes invalid.
When the built-in LCD driver is not used, select the default setting of "1/32 & 1/16 duty".



(a) V_{C2} standard (1/5 bias)



(b) V_{C2} standard (1/4 bias)



(c) V_{C1} standard (1/4 bias)

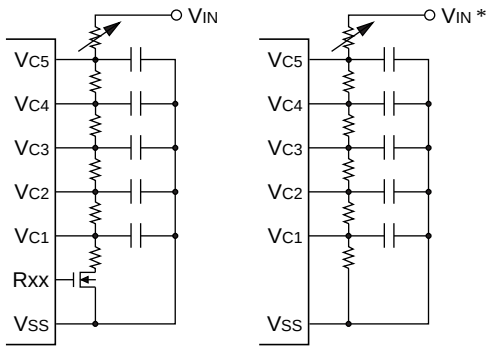
Note: V_{C1} standard can be selected only for 1/4 bias drive.

Fig. 5.11.1.1 Configuration of LCD controller and drive power supply

5.11.3 LCD power supply

Either the internal power supply (built-in LCD system voltage regulator and voltage booster / reducer) or an external power supply can be selected by mask option to supply the LCD drive voltages V_{C1} to V_{C5}. Furthermore, mask option allows selection of an internal power supply type from among four types, TYPE A to TYPE D, according to the LCD panel characteristics.
When 1/4 bias is selected, the voltage regulator generates V_{C1} or V_{C2} (V_{C2} is generated when 1/5 bias is selected) and boosts and/or reduces it to generate three other voltages. Table 5.11.3.1 lists the V_{C1}, V_{C2} (V_{C3} = V_{C2}), V_{C4} and V_{C5} voltages and their boost/reduce status. Selection of V_{C1} standard or V_{C2} standard is a mask option. Note that the number of externally attached parts differs according to the selected bias (1/5 or 1/4).

LCD power supply
- ☐ Internal power supply TYPE A (V_{C2} standard, 1/5 bias, 4.5 V)
- ☐ Internal power supply TYPE B (V_{C2} standard, 1/5 bias, 5.5 V)
- ☐ Internal power supply TYPE C (V_{C2} standard, 1/4 bias, 4.5 V)
- ☐ Internal power supply TYPE D (V_{C1} standard, 1/4 bias, 4.5 V)
- ☐ External power supply



* V_{SS} level or high impedance when LCD is not driven.

Fig. 5.11.3.1 Circuit examples when using an external power supply

The internal power supply is designed for a small scale LCD panel and is not suitable for driving a panel that has large size pixels or for driving a large capacity panel using an external expanded LCD driver. In this case, select external power supply and input the regulated voltage from outside the IC. Figure 5.11.3.1 shows the circuit examples when using an external power supply. Do not set the LCD display control register (LCDC1, LCDC0) to OFF even when an external power supply is used.

5.11.4 LCD driver

The maximum number of dots changes according to the drive duty selection.
When 1/32 duty is selected, the combined common/segment output terminal is switched to the common terminal. An LCD panel with 72 segments × 32 commons (maximum 2,304 dots) can be driven.
When 1/16 duty is selected, the combined common/segment output terminal is switched to the segment terminal. An LCD panel with 88 segments × 16 commons (maximum 1,408 dots) can be driven.
When 1/8 duty is selected, the combined common/segment output terminal is switched to the segment terminal as when 1/16 duty is selected. An LCD panel with 88 segments × 8 commons (maximum 704 dots) can be driven. Furthermore, when 1/8 duty is selected, terminals COM8–COM15 become invalid, in that they always output an OFF signal. Table 5.11.4.1 shows the correspondence between the drive duty and the maximum number of displaying dots.

Figures 5.11.4.1 to 5.11.4.3 show the 1/5 bias drive waveforms (using V_{C1}–V_{C5}).

Table 5.11.3.1 LCD drive voltage (1/4 bias)

LCD drive voltage	V_{DD}=1.8–5.5 V	V_{DD}=2.4–2.6 V	V_{DD}=2.6–5.5 V
V_{C1} (0.975–1.2 V)	V_{C1} (reference)	1/2 × V_{C2}	1/2 × V_{C2}
V_{C2} (1.950–2.4 V)	2 × V_{C1}	(1.95–2.40) × (V_{DD}-0.1)/2.4	V_{C2} (reference)
V_{C3} (2.925–3.6 V)	3 × V_{C1}	3/2 × V_{C2}	3/2 × V_{C2}
V_{C4} (3.900–4.8 V)	4 × V_{C1}	2 × V_{C2}	2 × V_{C2}

Table 5.11.4.1 Correspondence between drive duty and maximum number of displaying dots

Mask option	LDUTY	Duty	Common terminal	Segment terminal	Maximum number of display dots
1/32 & 1/16 duty	0	1/32	COM0–COM31	SEG0–SEG71	2,304 dots
	1	1/16	COM0–COM15	SEG0–SEG71	1,408 dots
1/8 duty	×	1/8	COM0–COM7	SEG72–SEG87	704 dots

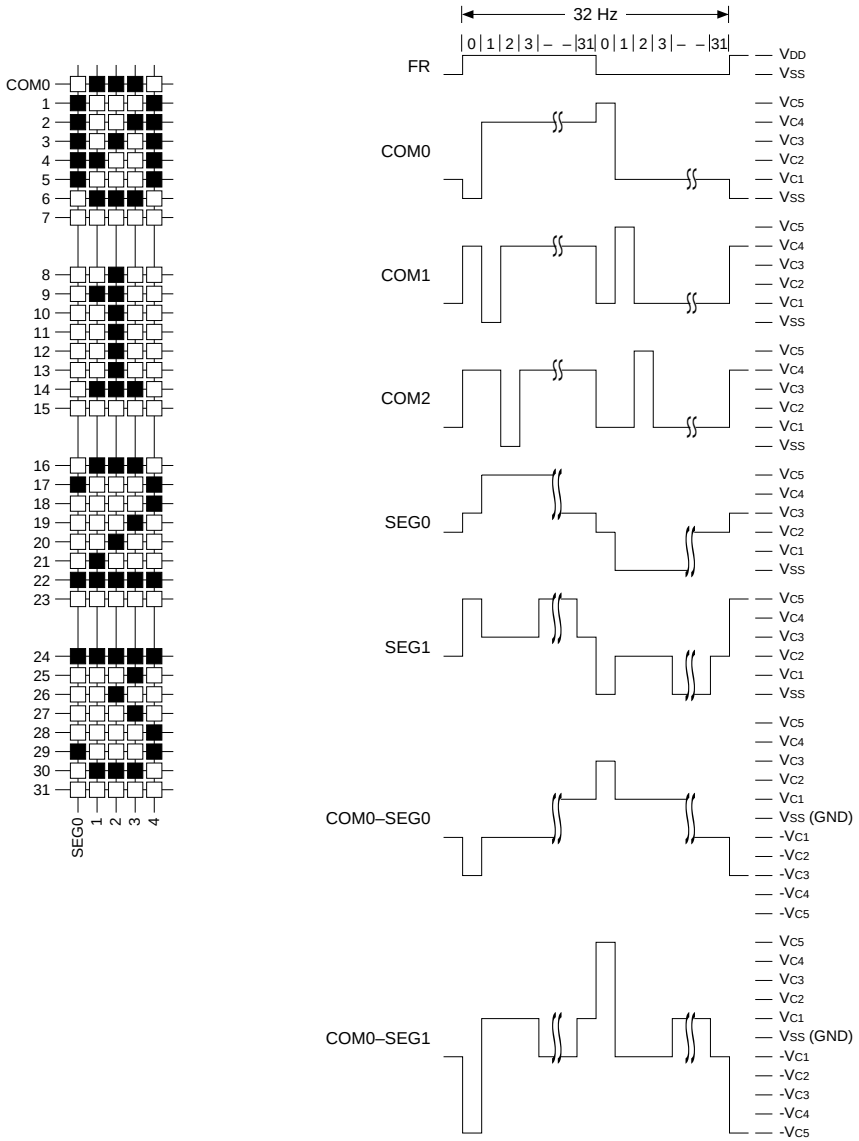


Fig. 5.11.4.1 Drive waveform for 1/32 duty

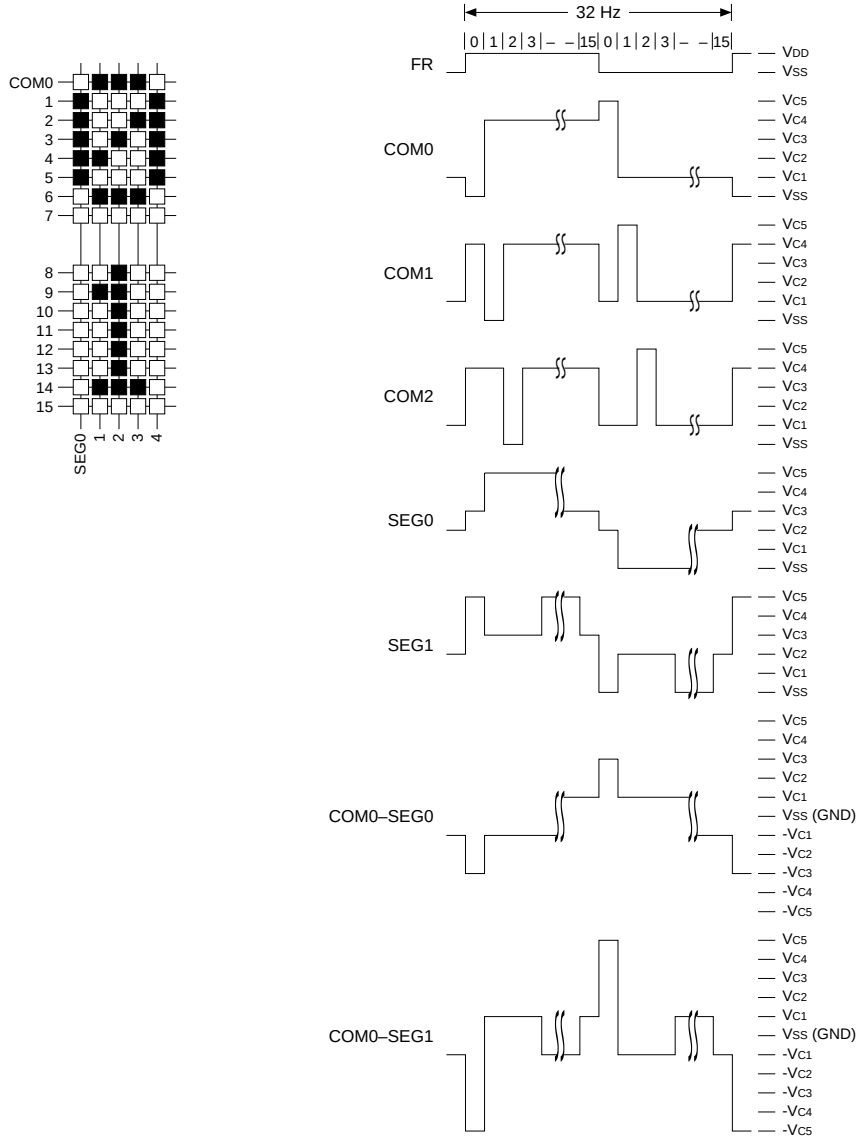


Fig. 5.11.4.2 Drive waveform for 1/16 duty

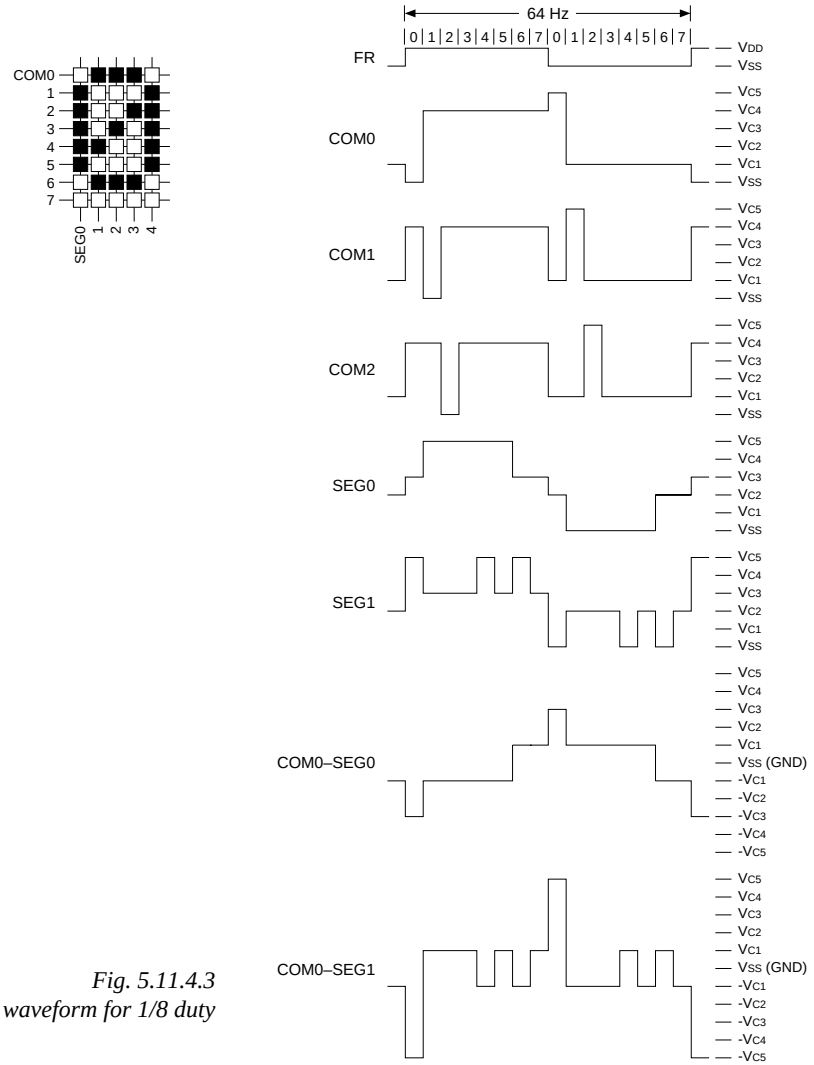


Fig. 5.11.4.3
Drive waveform for 1/8 duty

5.11.5 Display memory

The E0C88816 has a built-in 528-byte display memory. The display memory is allocated to address F800H–FD57H (including unavailable areas) and the correspondence between the memory bits and common / segment terminal is changed according to the selection status of the following items.

(1) Drive duty (1/32, 1/16 or 1/8 duty)
(2) Dot font (5 × 8 or 5 × 5 dots)

When 1 / 16 or 1 / 8 duty is selected for drive duty, two-screen memory can be secured, and the two screens can be switched by the display memory area selection register DSPAR. When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.
Furthermore, memory allocation for 5 × 8 dots and 5 × 5 dots can be selected in order to easily display 5 × 5-dot font characters on the LCD panel.
This selection can be done by the dot font selection register DTFNT: when "0" is written to DTFNT, 5 × 8 dots is selected and when "1" is written, 5 × 5 dots is selected.
The correspondence between the display memory bits set according to the drive duty and font size, and the common / segment terminals are shown in Figures 5.11.5.1–5.11.5.6.
When "1" is written to the display memory bit corresponding to the dot on the LCD panel, the dot goes ON and when "0" is written, it goes OFF. Since display memory is designed to permit reading / writing, it can be controlled in bit units by logical operation instructions and other means (read, modify and write instruction)s.
The display memory bits that have not been assigned can be used as general purpose RAM with read / write capabilities.

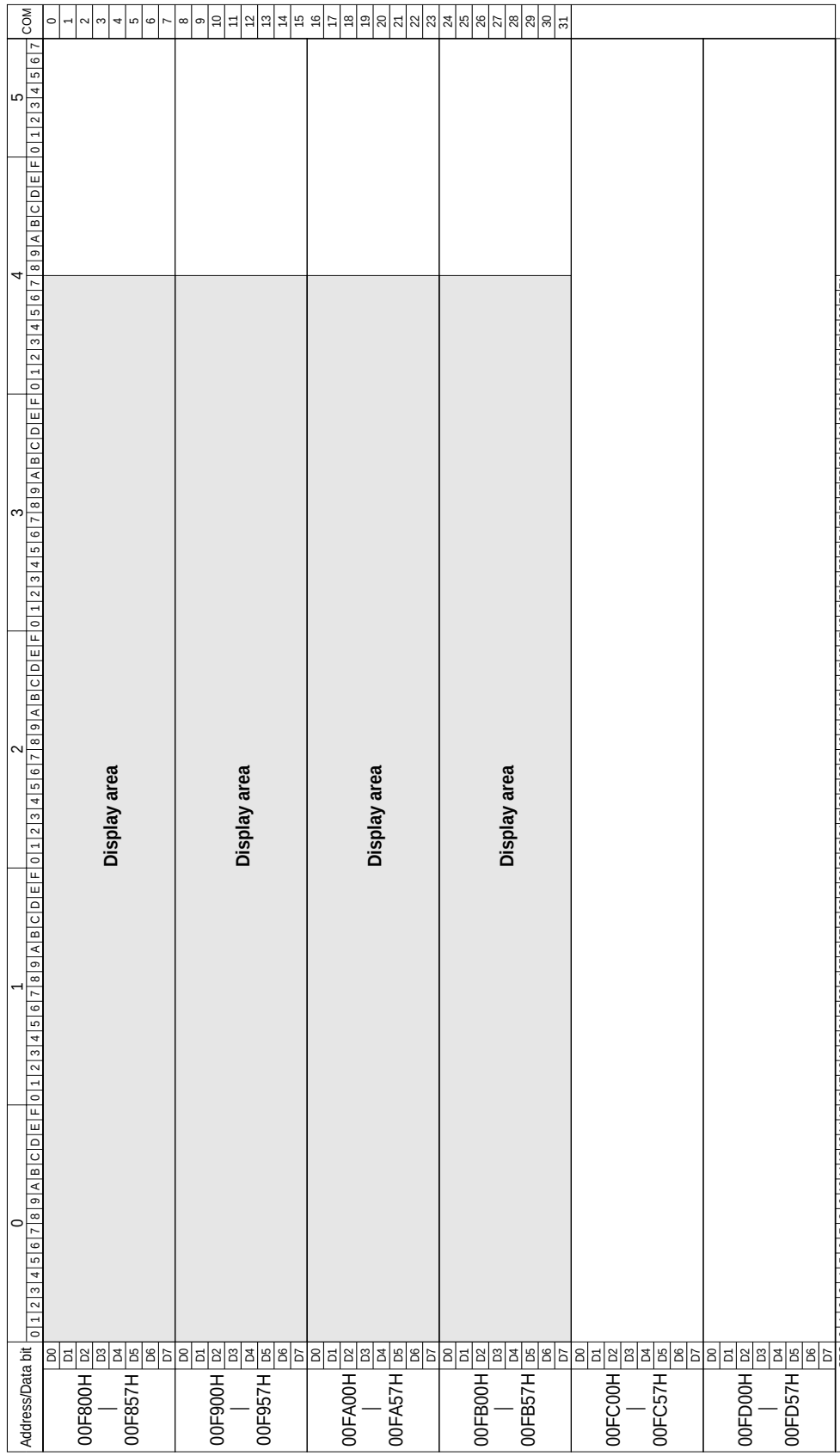


Fig. 5.11.5.1 1/32 duty and 5 × 8 dots display memory map

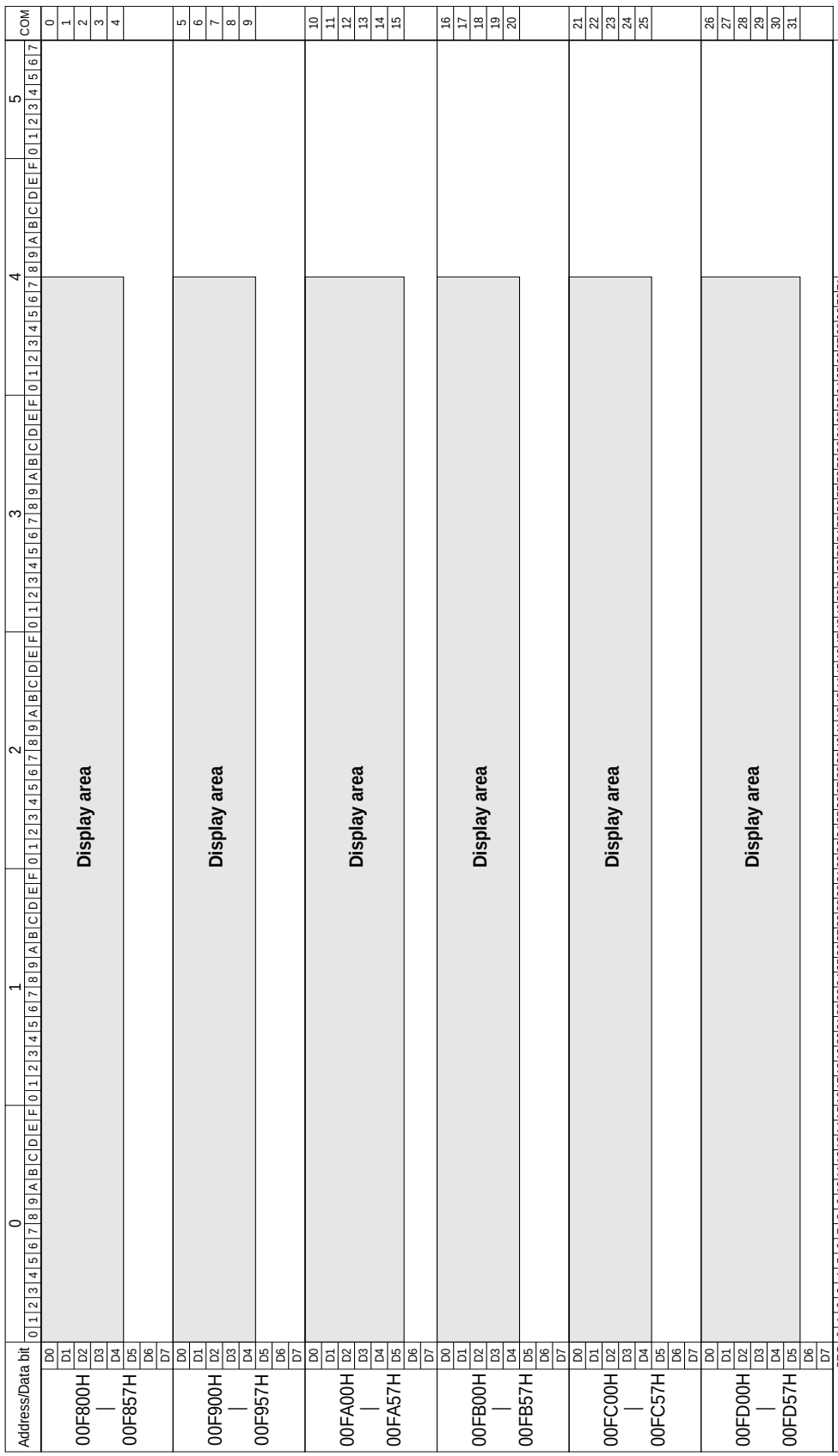


Fig. 5.11.5.2 1/32 duty and 5 × 5 dots display memory map

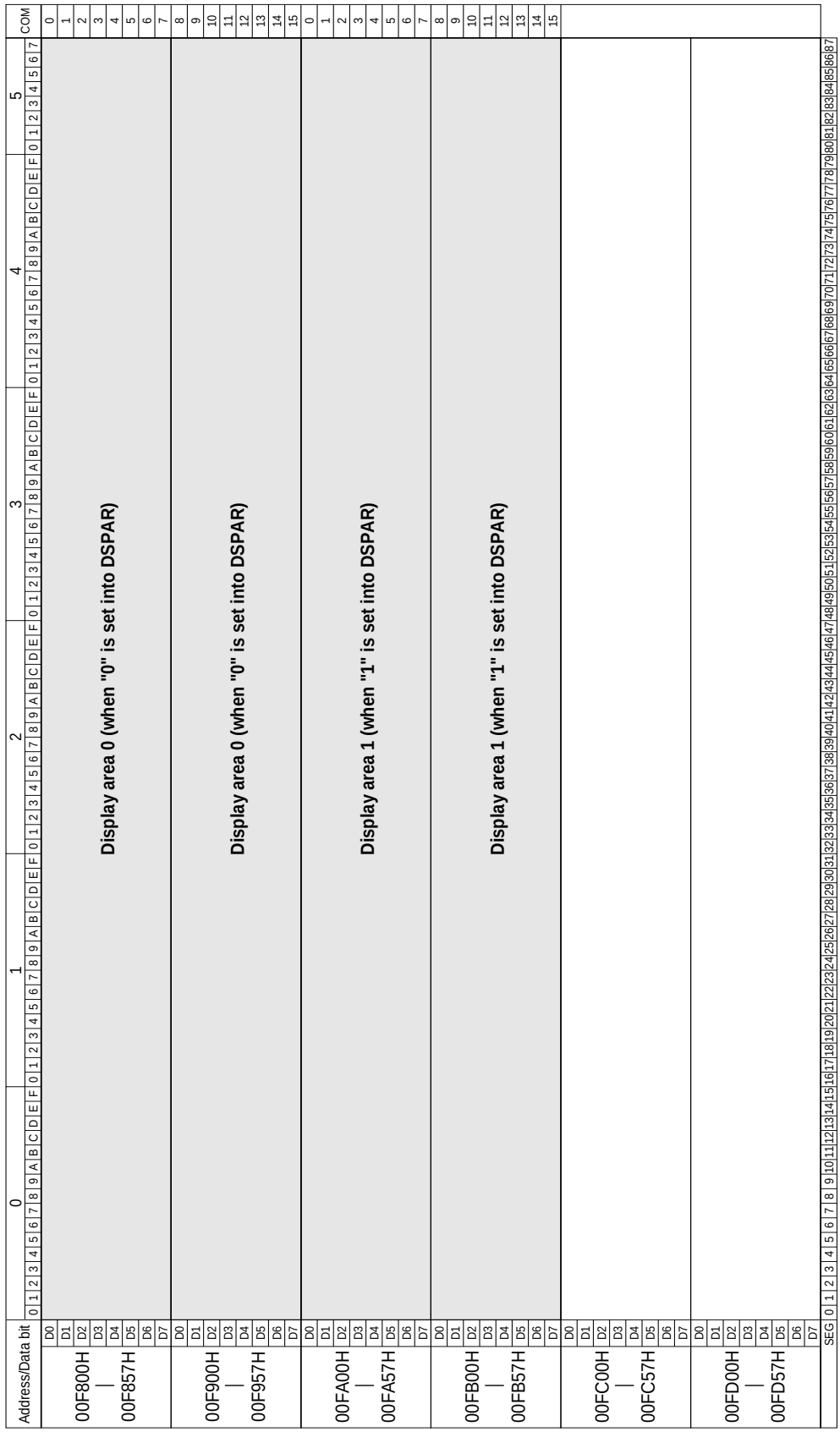


Fig. 5.11.5.3 1/16 duty and 5 × 8 dots display memory map

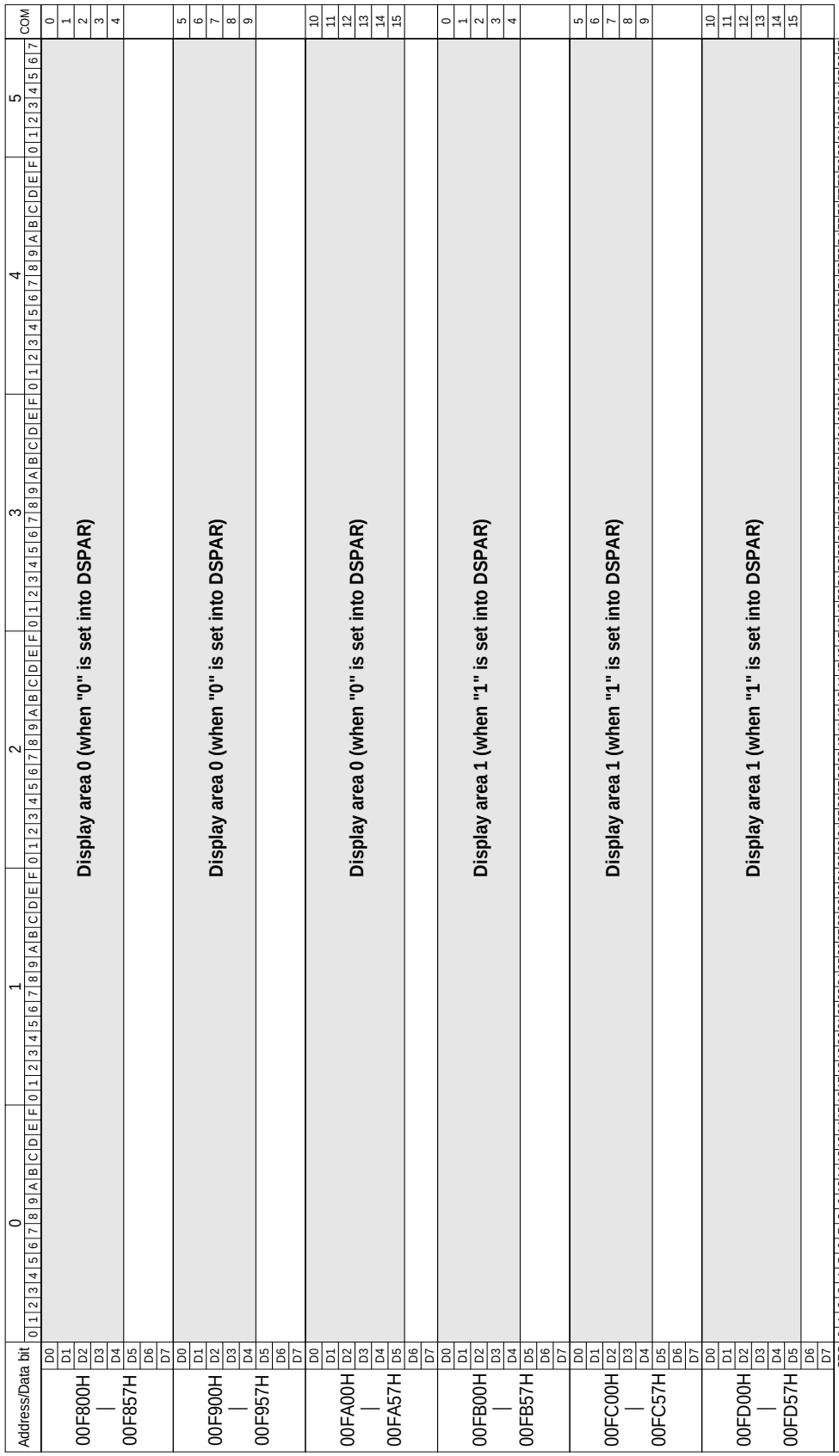


Fig. 5.11.5.4 1/16 duty and 5 × 5 dots display memory map

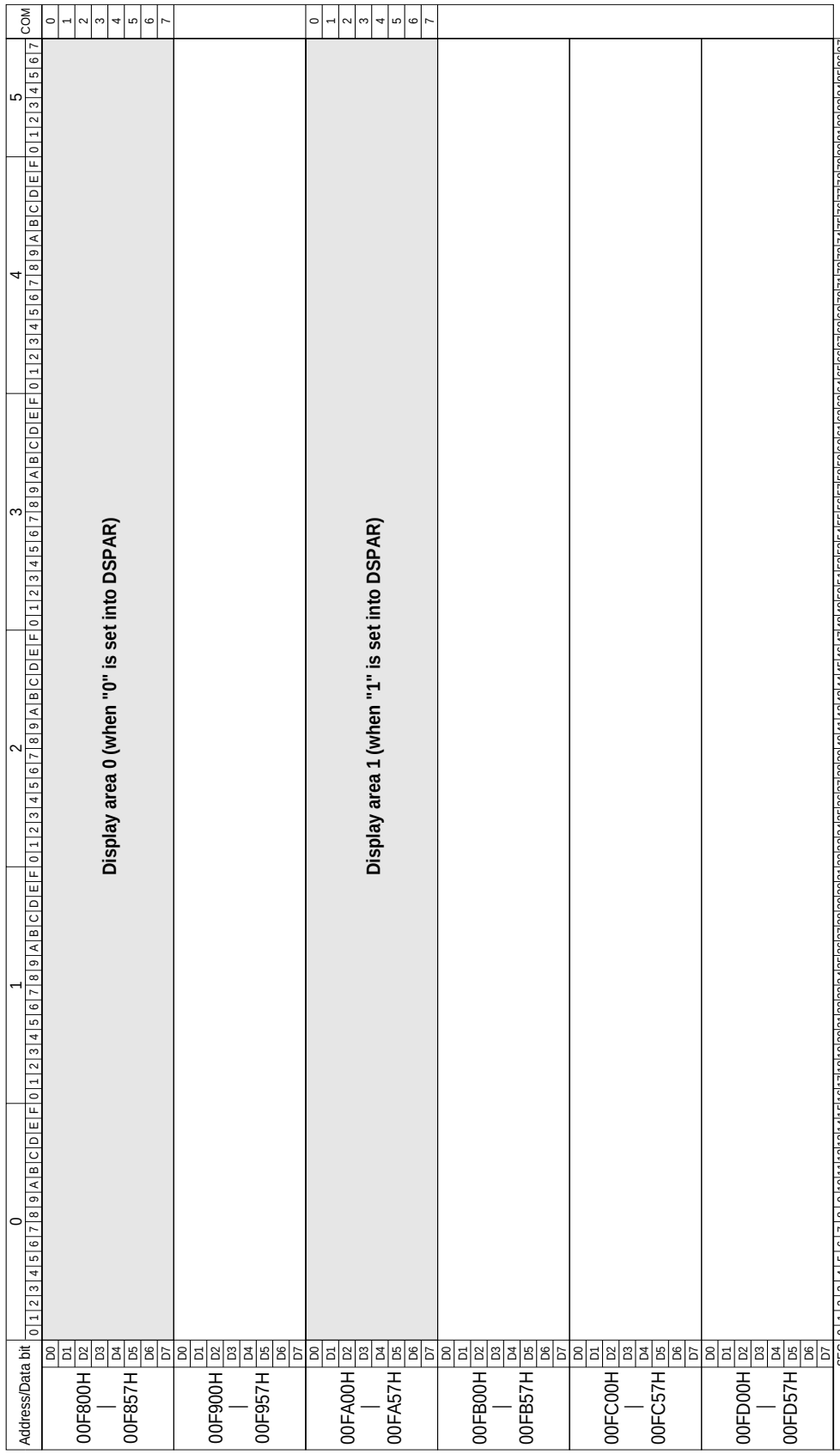


Fig. 5.11.5.5 1/8 duty and 5 × 8 dots display memory map

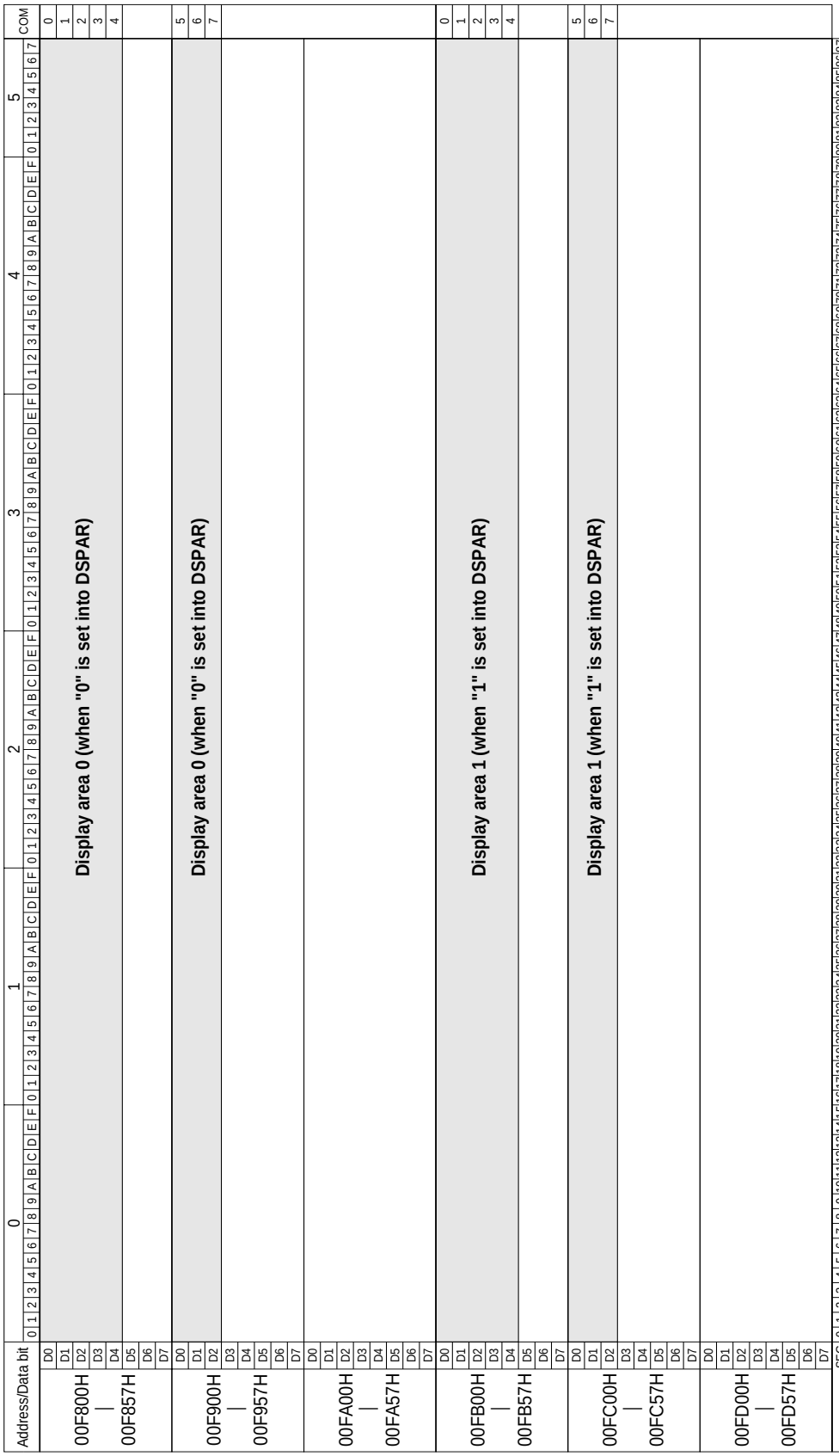


Fig. 5.11.5.6 1/8 duty and 5 × 5 dots display memory map

5.11.6 Display control

The display status of the built-in LCD driver and the contrast adjustment can be controlled with the built-in LCD controller. The LCD display status can be selected by display control registers LCDC0 and LCDC1. Setting the value and display status are shown in Table 5.11.6.1.

Table 5.11.6.1 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

All the dots in the LCD display can be turned on or off directly by the drive waveform output from the LCD driver, and data in the display memory is not changed. Also, since the common terminal at this time is set to static drive when all the dots are on and is set to dynamic drive when they are off, this function can be used as follows:

(1) Since all dots on is binary output (V_{C5} and V_{SS}) with static drive, the common / segment terminal can be used as a monitor terminal for the OSC1 oscillation frequency adjustment.

(2) Since all dots off is dynamic drive, you can brink the entire LCD display without changing display memory data.

Selecting LCD drive OFF turns the LCD drive power circuit OFF and all the V_{C1}–V_{C5} terminals go to V_{SS} level. If external power supply has been selected by the mask option, the V_{C1}–V_{C5} shift to floating status to prevent shortcircuit between the external power supply and the internal power supply. However, do not set LCDC0 and LCDC1 to "0" even when an external power supply is used. Furthermore, when the SLP instruction is executed, registers LCDC0 and LCDC1 are automatically reset to "0" (set to drive off) by hardware.

The LCD contrast can be adjusted in 16 stages. This adjustment is done by the contrast adjustment register LC0–LC3, and the setting values correspond to the contrast as shown in Table 5.11.6.2. However, if external power supply has been selected by the mask option, the contrast adjustment register LC0–LC3 is ineffective and contrast adjustment cannot be done.

Table 5.11.6.2 LCD contrast adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
:	:	:	:	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

5.11.7 I/O memory for LCD controller

Table 5.11.7.1 shows the LCD controller control bits.

Table 5.11.7.1 LCD controller control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF10	D7	–	–	–	–	–		Constantry "0" when being read
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		
	D4	LCCLK	General-purpose register	1	0	0	R/W	Reserved register
	D3	LCFRM	General-purpose register			0	R/W	
	D2	DTFNT	LCD dot font selection	5 x 5 dots	5 x 8 dots	0	R/W	
	D1	LDUTY	LCD drive duty selection	1/16 duty	1/32 duty	0	R/W	*1
	D0	SGOUT	General-purpose register	1	0	0	R/W	Reserved register
00FF11	D7	–	–	–	–	–		"0" when being read
	D6	DSPAR	LCD display memory area selection	Display area 1	Display area 0	0	R/W	
	D5	LCDC1	LCD display control LCDC1 LCDC0 LCD display 1 1 All LCDs lit 1 0 All LCDs out 0 1 Normal display 0 0 Drive off			0	R/W	These bits are reset to (0, 0) when SLP instruction is executed.
	D4	LCDC0				0	R/W	
	D3	LC3	LCD contrast adjustment LC3 LC2 LC1 LC0 Contrast 1 1 1 1 Dark 1 1 1 0 : : : : : : 0 0 0 0 Light			0	R/W	
	D2	LC2				0	R/W	
	D1	LC1				0	R/W	
	D0	LC0				0	R/W	

*1 When 1/8 duty has been selected by mask option, setting of this register becomes invalid.

LDUTY: 00FF10H•D1

Selects the drive duty.

When "1" is written: 1/16 duty
When "0" is written: 1/32 duty
Reading: Valid

When "1/32 & 1/16 duty" is selected by the mask option, select whether the drive duty will be 1/32 or 1/16.
When "0" is written to LDUTY, 1/32 duty is selected and the combined common/segment output terminal is switched to the common terminal.
When "1" is written to LDUTY, 1/16 duty is selected and the combined common/segment output terminal is switched to the segment terminal.
When "1/8 duty" is selected by the mask option, the combined common/segment terminals are fixed to the segment terminals and the setting of LDUTY becomes invalid.
The correspondence between the display memory bits set according to the drive duty, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.6.
At initial reset, LDUTY is set to "0" (1/32 duty).

DTFNT: 00FF10H•D2

Selects the dot font.

When "1" is written: 5 × 5 dots
When "0" is written: 5 × 8 dots
Reading: Valid

Select 5 × 8 dots or 5 × 5 dots type for the display memory area.
When "0" is written to DTFNT, 5 × 8 dots is selected and when "1" is written, 5 × 5 dots is selected.
The correspondence between the display memory bits set according to the dot font, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.6.
At initial reset, DTFNT is set to "0" (5 × 8 dots).

DSPAR: 00FF11H•D6

Selects the display area.

When "1" is written: Display area 1
When "0" is written: Display area 0
Reading: Valid

Selects which display area is secured for two screens in the display memory, will be displayed when 1/16 or 1/8 duty is selected.
When "0" is written to DSPAR, display area 0 is selected and when "1" is written, display area 1 is selected.

When 1/32 duty is selected, since the display area is only for one screen, the setting of DSPAR becomes invalid.
The correspondence between the display memory bits set according to the display area, and the common/segment terminals are shown in Figures 5.11.5.1–5.11.5.6.
At initial reset, DSPAR is set to "0" (display area 0).

LCDC0, LCDC1: 00FF11H•D4, D5

Controls the LCD display.

Table 5.11.7.2 LCD display control

LCDC1	LCDC0	LCD display
1	1	All LCDs lit (Static)
1	0	All LCDs out (Dynamic)
0	1	Normal display
0	0	Drive OFF

The four settings mentioned above can be made without changing the display memory data.
At initial reset and in the SLEEP status, this register is set to "0" (drive off).

LC0–LC3: 00FF11H•D0–D3

Adjusts the LCD contrast.

Table 5.11.7.3 LCD contrast adjustment

LC3	LC2	LC1	LC0	Contrast
1	1	1	1	Dark
1	1	1	0	↑
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	↓
0	0	0	0	Light

The contrast can be adjusted in 16 stages as mentioned above. This adjustment changes the drive voltage on terminals V_{C1}–V_{C5}.
At initial reset, this register is set to "0".

Note: If external power supply has been selected by the mask option, the contrast adjustment register LC0–LC3 is ineffective.

5.11.8 Programming note

When the SLP instruction is executed, display control registers LCDC0 and LCDC1 are automatically reset to "0" by hardware.

5.12 Sound Generator

5.12.1 Configuration of sound generator

The E0C88816 has a built-in sound generator for generating buzzer signals.
The buzzer signals (BZ and $\overline{BZ}$) generated by this circuit are output from the R50 and R51 output port terminals. Furthermore, the melody output terminals (MOUT and $\overline{MOUT}$) can be used for output. See "5.13 Melody Generator" for using the melody output terminals.
Aside permitting the respective setting of the buzzer signal frequency and sound level (duty adjustment) to 8 stages, it permits the adding of a digital envelope by means of duty ratio control. It also has a one-shot output function for outputting key operated sounds.
Figure 5.12.1.1 shows the configuration of the sound generator.

5.12.2 Mask option

$\overline{BZ}$ output (R51 port specification)
☐ Use ($\overline{BZ}$ output)
☐ Not Use (DC output)

In the E0C88816, the R51 output port can be configured as the $\overline{BZ}$ (BZ inverted signal) output port by mask option. The description for the $\overline{BZ}$ output in this section assumes that the R51 output specification is set to the $\overline{BZ}$ output.

5.12.3 Control of buzzer output

The BZ signal can be output from the R50 output port terminal. Furthermore, the R51 output port terminal can be used to output the $\overline{BZ}$ signal (BZ inverted signal) by mask option.

The configuration of the output ports R50 and R51 is shown in Figure 5.12.3.1.

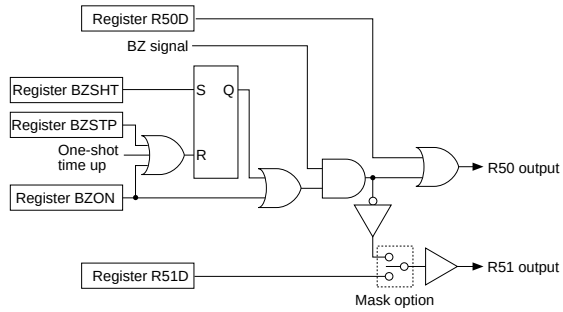


Fig. 5.12.3.1 Configuration of R50 and R51

The output control for the buzzer signal generated by the sound generator is done by the buzzer output control register BZON, one-shot buzzer trigger bit BZSHT and one-shot buzzer forced stop bit BZSTP. When "1" is set to BZON or BZSTP, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the buzzer signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
Figure 5.12.3.2 shows the output waveform of the buzzer signal.

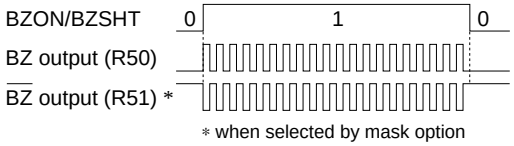


Fig. 5.12.3.2 Buzzer output waveform

Note: Since the buzzer signal is generated asynchronously from the registers BZON, BZSHT and BZSTP, when the signal is turned ON or OFF by the register settings, a hazard of a 1/2 cycle or less is generated.

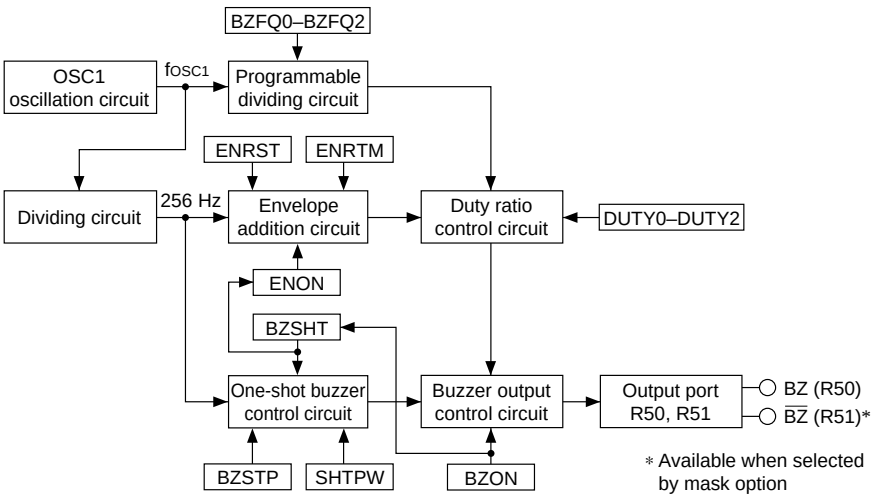


Fig. 5.12.1.1 Configuration of sound generator

5.12.4 Setting of buzzer frequency and sound level

The buzzer signal is divided signal using the OSC1 oscillation circuit (32.768 kHz) as the clock source and 8 frequencies can be selected. This selection is done by the buzzer frequency selection register BZFQ0–BZFQ2. The setting value and buzzer frequency correspondence is shown in Table 5.12.4.1.

By selecting the duty ratio of the buzzer signal from among 8 types, the buzzer sound level can be adjusted. This selection is made in the duty ratio selection register DUTY0–DUTY2. The setting value and duty ratio correspondence is shown in Table 5.12.4.2.

Table 5.12.4.1 Buzzer signal frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

Table 5.12.4.2 Duty ratio settings

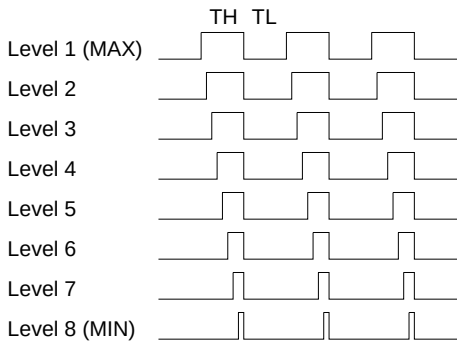
Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0	3276.8	2730.7	2340.6
				2048.0	1638.4	1365.3	1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

Duty ratio refers to the ratio of pulse width to the pulse cycle; given that HIGH level output time is TH, and LOW level output time is TL the BZ signal duty ratio becomes TH / (TH+TL) and the $\overline{BZ}$ signal duty ratio becomes TL / (TH+TL).
When DUTY0–DUTY2 have all been set to "0", the duty ratio becomes maximum and the sound level also becomes maximum.

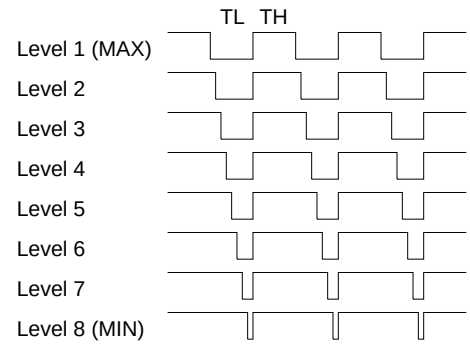
Conversely, when DUTY0–DUTY2 have all been set to "1", the duty ratio becomes minimum and the sound level also becomes minimum.

Note that the duty ratio setting differ depending on frequency. See Table 5.12.4.2.

Note: When using the digital envelope, the DUTY0–DUTY2 setting becomes invalid.



(a) BZ signal



(b) $\overline{BZ}$ signal

Fig. 5.12.4.1 Duty ratio of buzzer signal waveform

5.12.5 Digital envelope

A digital envelope with duty control can be added to the buzzer signal.
The envelope can be realized by staged changing of the same duty ratio as detailed in Table 5.12.4.2 in the preceding section from level 1 (maximum) to level 8 (minimum).
The addition of an envelope to the buzzer signal can be done by writing "1" to the envelope control register ENON. When "0" is written, the duty ratio is set at the level selected in DUTY0–DUTY2.

By writing "1" to ENON to turn the buzzer output ON (writing "1" to BZON), the buzzer signal with a level 1 duty ratio is output, and then the duty ratio can be attenuated in stages to level 8. The attenuated envelope can be returned to level 1 by writing "1" to the envelope reset bit ENRST. When attenuated to level 8, the duty level remains at level 8 until the buzzer output is turned OFF (writing "0" to BZON) or writing "1" to ENRST.
The stage changing time for the envelope level can be selected either 125 msec or 62.5 msec by the envelope attenuation time selection register ENRTM.
Figure 5.12.5.1 shows the timing chart of the digital envelope.

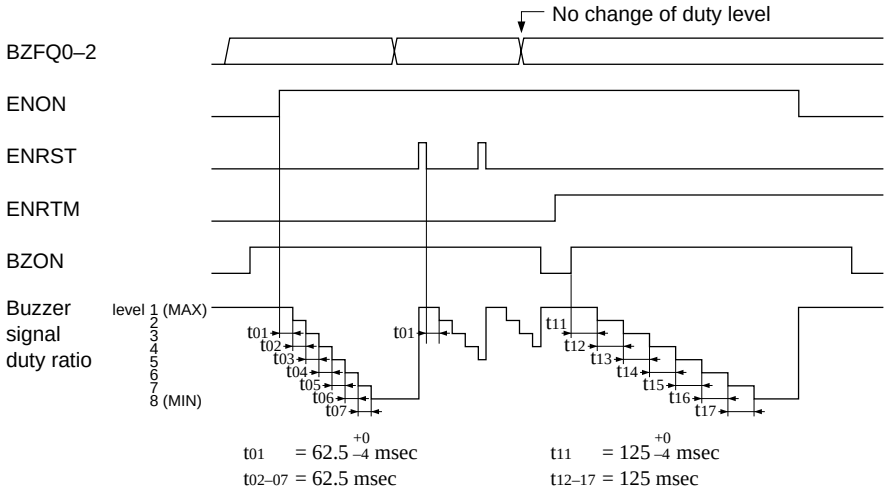


Fig. 5.12.5.1 Timing chart of digital envelope

5.12.6 One-shot output

The sound generator has a built-in one-shot output function for outputting a short duration buzzer signal for key operation sounds and similar effects. Either 125 msec or 31.25 msec can be selected by the one-shot buzzer duration selection register SHTPW for buzzer signal output time.
The output control of the one-shot buzzer is done by writing "1" to the one-shot buzzer trigger BZSHT, then the buzzer signal is output in synchronization with the internal 256 Hz signal from the output port terminal. Thereafter, when the set time has elapsed, the buzzer signal in synchronization with the 256 Hz signal automatically goes OFF in the same manner.
The BZSHT can be read to determine status. When BZSHT is "1", it indicates a BUSY status (during one-shot output) and when BZSHT is "0", it indicates a READY status (during stop).
When you want to turn the buzzer signal OFF prior to the elapse of the set time, the buzzer signal can be immediately stopped (goes OFF in asynchonization with 256 Hz signal) by writing "1" to the one-shot forced stop bit BZSTP.

Since the one-shot output has a short duration, an envelope cannot be added. (When "1" is written to BZSHT, ENON is automatically reset to "0".) Consequently, only the frequency and sound level can be set for one-shot output.

The control for the one-shot output is invalid during normal buzzer output.

Figure 5.12.6.1 shows the timing chart of the one-shot output.

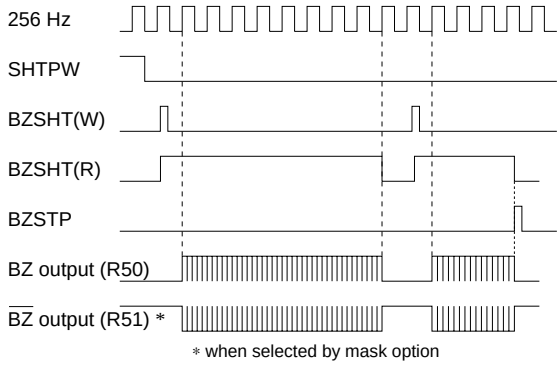


Fig. 5.12.6.1 Timing chart of one-shot output

5.12.7 I/O memory for sound generator

Table 5.12.7.1 shows the sound generator control bits.

Table 5.12.7.1 Sound generator control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF44	D7	–	–	–	–	–		Constantry "0" when
	D6	BZSTP	One-shot buzzer forcibly stop	Forcibly stop	No operation	–	W	being read
	D5	BZSHT	One-shot buzzer trigger/status R	Busy	Ready	0	R/W	
			W	Trigger	No operation			
	D4	SHTPW	One-shot buzzer duration width selection	125 msec	31.25 msec	0	R/W	
	D3	ENRTM	Envelope attenuation time	1 sec	0.5 sec	0	R/W	
	D2	ENRST	Envelope reset	Reset	No operation	–	W	"0" when being read
	D1	ENON	Envelope On/Off control	On	Off	0	R/W	*1
	D0	BZON	Buzzer output control	On	Off	0	R/W	
00FF45	D7	–	–	–	–	–		"0" when being read
	D6	DUTY2	Buzzer signal duty ratio selection			0	R/W	
	D5	DUTY1				0	R/W	
	D4	DUTY0				0	R/W	
	D3	–	–	–	–	–		"0" when being read
	D2	BZFQ2	Buzzer frequency selection			0	R/W	
	D1	BZFQ1				0	R/W	
	D0	BZFQ0				0	R/W	

DUTY2–1 / Buzzer frequency (Hz)

2	1	0	4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
0	0	0	8/16	8/20	12/24	12/28
0	0	1	7/16	7/20	11/24	11/28
0	1	0	6/16	6/20	10/24	10/28
0	1	1	5/16	5/20	9/24	9/28
1	0	0	4/16	4/20	8/24	8/28
1	0	1	3/16	3/20	7/24	7/28
1	1	0	2/16	2/20	6/24	6/28
1	1	1	1/16	1/20	5/24	5/28

BZFQ2 / BZFQ1 / BZFQ0 / Frequency (Hz)

BZFQ2	BZFQ1	BZFQ0	Frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

*1 Reset to "0" during one-shot output.

BZON: 00FF44H•D0

Controls the buzzer (BZ and $\overline{BZ}$) signal output.

When "1" is written: Buzzer signal output
When "0" is written: LOW (DC) output [R50]
HIGH (DC) output [R51]
Reading: Valid

BZON is the output control register for buzzer signal. When "1" is set to the register, the BZ ($\overline{BZ}$) signal is output from the output port terminal R50 (R51). When "0" is set, the R50 goes LOW (V_{SS}) and the R51 goes HIGH (V_{DD}).
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
At initial reset, BZON is set to "0" (DC output).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZFQ0–BZFQ2: 00FF45H•D0–D2

Selects the buzzer signal frequency.

Table 5.12.7.2 Buzzer frequency settings

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

The buzzer frequency can be selected from among the above 8 types that have divided the OSC1 clock. At initial reset, this register is set at "0" (4096.0 Hz).

DUTY0–DUTY2: 00FF45H•D4–D6

Selects the duty ratio of the buzzer signal.

Table 5.12.7.3 Duty ratio settings

Level	DUTY2	DUTY1	DUTY0	Duty ratio by buzzer frequencies (Hz)			
				4096.0 2048.0	3276.8 1638.4	2730.7 1365.3	2340.6 1170.3
Level 1 (Max)	0	0	0	8/16	8/20	12/24	12/28
Level 2	0	0	1	7/16	7/20	11/24	11/28
Level 3	0	1	0	6/16	6/20	10/24	10/28
Level 4	0	1	1	5/16	5/20	9/24	9/28
Level 5	1	0	0	4/16	4/20	8/24	8/28
Level 6	1	0	1	3/16	3/20	7/24	7/28
Level 7	1	1	0	2/16	2/20	6/24	6/28
Level 8 (Min)	1	1	1	1/16	1/20	5/24	5/28

The buzzer sound level can be adjusted by selecting the duty ratio from among the above 8 types. However, when the envelope has been set to ON (ENON = "1"), this setting becomes invalid.
At initial reset, this register is set to "0" (level 1).

ENRST: 00FF44H•D2

Resets the envelope.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

The envelope is reset by writing "1" to ENRST and the duty ratio returns to level 1 (maximum). Writing "0" to ENRST and writing "1" when an envelope has not been added become invalid. Since ENRST is exclusively for writing, it always becomes "0" during reading.

ENON: 00FF44H•D1

Controls the addition of an envelope to the buzzer signal.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

By writing "1" to ENON, an envelope can be added to buzzer signal output. When "0" is written, an envelope is not added and the buzzer signal is fixed at the duty ratio selected in DUTY0–DUTY2.
At initial reset and when "1" is written to BZSHT, ENON is set to "0" (OFF).

ENRTM: 00FF44H•D3

Selects the envelope attenuation time that is added to the buzzer signal.

When "1" is written: 1.0 sec
(125 msec × 7 = 875 msec)
When "0" is written: 0.5 sec
(62.5 msec × 7 = 437.5 msec)
Reading: Valid

The attenuation time of the digital envelope is determined by the time for changing the duty ratio. The duty ratio is changed in 125 msec (8 Hz) units when "1" is written to ENRTM and in 62.5 msec (16 Hz) units, when "0" is written.
This setting becomes invalid when an envelope has been set to OFF (ENON = "0").
At initial reset, ENRTM is set to "0" (0.5 sec).

SHTPW: 00FF44H•D4

Selects the output duration width of the one-shot buzzer.

When "1" is written: 125 msec
When "0" is written: 31.25 msec
Reading: Valid

The one-shot buzzer output duration width is set to 125 msec when "1" is written to SHTPW and 62.5 msec, when "0" is written.
At initial reset, SHTPW is set to "0" (31.25 msec).

BZSHT: 00FF44H•D5

Controls the one-shot buzzer output.

When "1" is written: Trigger
When "0" is written: No operation

When "1" is read: Busy
When "0" is read: Ready

Writing "1" into BZSHT causes the one-shot output circuit to operate. The BZ ($\overline{BZ}$) signal is output from the R50 (R51) terminal. The buzzer output is automatically turned OFF after the time set by SHTPW has elapsed.
To output the BZ signal, "0" must always be set for the data register R50D. The data register R51D does not affect the $\overline{BZ}$ output.
The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") state. The trigger is invalid during ON (BZON = "1") state.
When a re-trigger is assigned during a one-shot output, the one-shot output time set with SHTPW is measured again from that point. (time extension)
The operation status of the one-shot output circuit can be confirmed by reading BZSHT, when the one-shot output is ON, "1" is read from BZSHTand when the output is OFF, "0" is read.
At initial reset, BZSHT is set to "0" (ready).
The $\overline{BZ}$ signal can be output from R51 only when the function is selected by mask option.

BZSTP: 00FF44H•D6

Forcibly stops the one-shot buzzer output.

When "1" is written: Forcibly stop
When "0" is written: No operation
Reading: Constantly "0"

By writing "1" into BZSTP, the one-shot buzzer output can be stopped prior to the elapsing of the time set with SHTPW.
Writing "0" is invalid and writing "1" except during one-shot output is also invalid.
When "1" is written to BZSHT and BZSTP simultaneously, BZSTP takes precedence and one-shot output becomes stop status.
Since BZSTP is for writing only, during readout it is constantly set to "0".

5.12.8 Programming notes

(1) Since the buzzer signal is generated asynchronously from the register BZON, when the signal is turned ON or OFF by the register setting, a hazard of a 1/2 cycle or less is generated.

(2) The SLP instruction has executed when the buzzer signal output is in the enable status (BZON = "1" or BZSHT = "1"), unstable clock is output from the output terminal at the time of return from the SLEEP status. Consequently, when shifting to the SLEEP status, you should set the buzzer signal output to the disable status (BZON = BZSHT = "0") prior to executing the SLP instruction.

(3) The one-shot output is only valid when the normal buzzer output is OFF (BZON = "0") status. The trigger is invalid during ON (BZON = "1") status.

(4) When driving an external bipolar transistor with the BZ signal to sound a buzzer, select "heavy load protection mode during buzzer output" by mask option. Note that the LCD driver current will be increased about 20 µA.
When direct driving a piezoelectric buzzer using the BZ/$\overline{BZ}$ or MOUT/$\overline{MOUT}$ terminals, select "normal mode" by mask option to reduce current consumption.

5.13 Melody Generator

5.13.1 Features and configuration of melody generator

The E0C88816 has a built-in melody generator for generating melody signals. General melody generators often use a ROM to store scale and note data, therefore melody data cannot be rewritten. The E0C88816 uses a RAM for this purpose allowing rewriting of melody data from the external ports through the CPU.
The principal features are listed below.

- **Melody RAM size:**
  Scale RAM 256 words × 8 bits (00D000H to 00D0FFH)
  Note RAM 256 words × 8 bits (00D100H to 00D1FFH)
- **Number of storable melodies:**
  Any within the melody RAM
- **Address control:**
  Free allocable word size for each melody
- **Playback output:**
  1 square-wave tone
- **Scale (3 octaves):**
  C4 to G6 with reference to A4 = 440 Hz
  C4 to C7# with reference to C4 = 256 Hz
- **Note:** 8 types (half note to sixteenth note)
- **Tempo:** Selectable from 16 tempos (4 bits)
- **Reference signal frequency:** 32.768 kHz
- **Driving a piezoelectric buzzer:**
  MOUT and $\overline{\text{MOUT}}$ are used
  MOUT = $\overline{\text{MOUT}}$ = LOW at initial reset
- **Switching to sound output:**
  Melody output terminals can be switched for sound generator output by software

Figure 5.13.1.1 shows the configuration of the sound generator.

The melody signal generated by the melody generator is output from the MOUT and $\overline{\text{MOUT}}$ terminals. Furthermore, the MOUT and $\overline{\text{MOUT}}$ terminals can output the buzzer signal generated by the sound generator.
At initial reset, the MOUT and $\overline{\text{MOUT}}$ terminals go LOW.
Using the two terminals MOUT and $\overline{\text{MOUT}}$ allows direct driving of a piezoelectric buzzer. In this case, connect a piezoelectric buzzer between the MOUT and $\overline{\text{MOUT}}$ via the protective resistors (100 Ω) as shown in Figure 5.13.1.2.

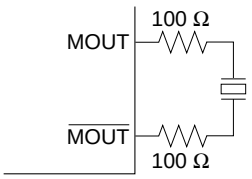


Fig.5.13.1.2 Direct driving a piezoelectric buzzer

The buzzer can be driven with one terminal by connecting it to the MOUT terminal via a transistor. However, direct driving a piezoelectric buzzer is recommended for lower current consumption.

The CPU accesses the scale RAM and note RAM individually when data is read and written from / to the RAM since they have different addresses. During a melody output, the scale RAM and note RAM are accessed as a RAM configured with 256 words × 16 bits.

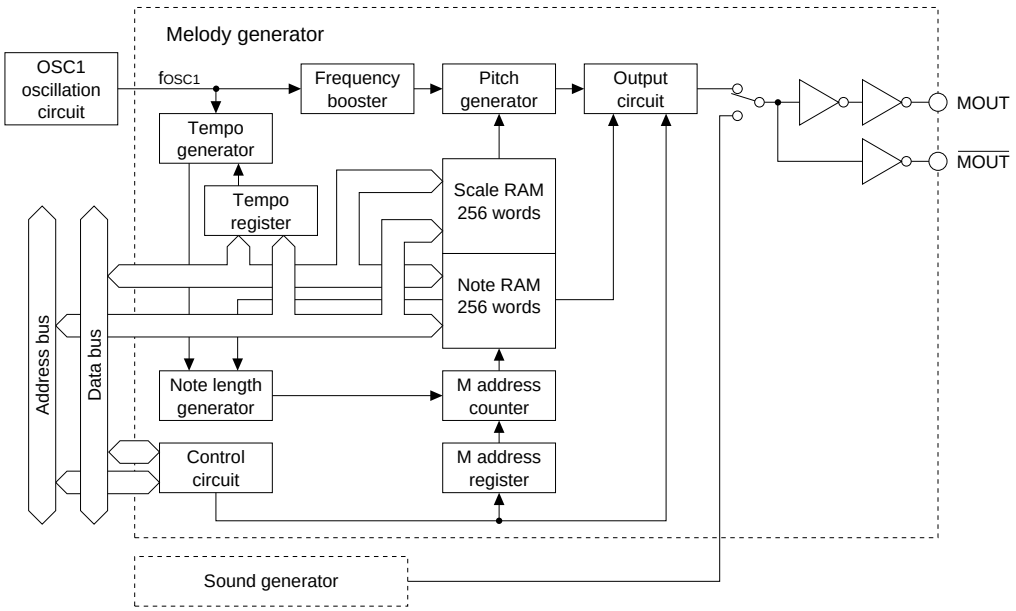


Fig. 5.13.1.1 Configuration of the sound generator

5.13.2 Programming melodies

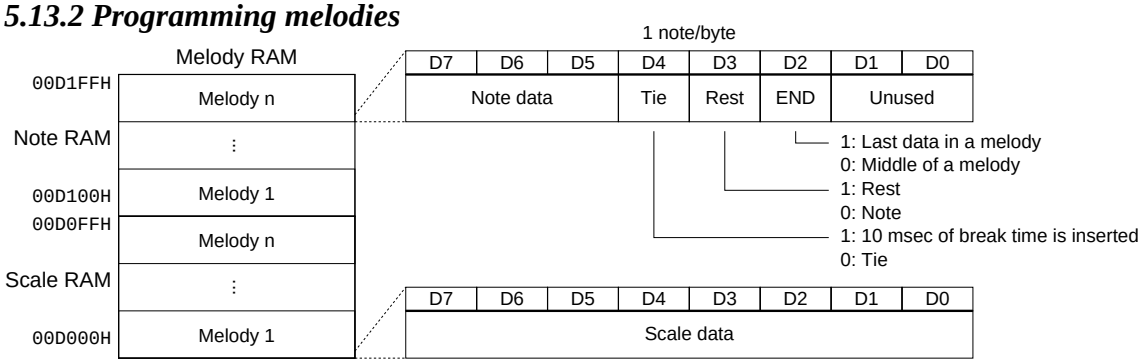


Fig. 5.13.2.1 Contents of melody RAM

Melodies are programmed by writing data to the note RAM and scale RAM.

Each word in the note RAM and scale RAM represents a note or rest and it corresponds between two RAMs one to one. In other words, the data stored in the same low-order 8-bit address of the note and scale RAMs correspond to a note on the musical score.
Melody data should be written from the start address of each RAM continuously by notes.

Note: The melody RAM cannot be rewritten while a melody is playing.

■ Setting the note RAM

First, the following describes data to be set in the note RAM.

(1) Note (note RAM: D7 to D5)

The 3 high-order bits (D7 to D5) in the note RAM specify a type of note or rest. Table 5.13.2.1 shows the correspondence between the setting value and note / rest.

Table 5.13.2.1 Types of notes/rests

D7	D6	D5	Note	Rest	Division ratio
0	0	0	𝅝	𝄻	1/8
0	0	1	𝅗𝅥..	𝄽..	1/7
0	1	0	𝅗𝅥.	𝄽.	1/6
0	1	1	♩𝅘𝅥𝅯	𝄽𝄿	1/5
1	0	0	♩	𝄽	1/4
1	0	1	𝅘𝅥𝅮.	𝄾.	1/3
1	1	0	𝅘𝅥𝅮	𝄾	1/2
1	1	1	𝅘𝅥𝅯	𝄿	1/1

A length of sound shorter than a sixteenth note that is not included in the table above may be specified using two available notes and the tie bit.

(2) Tie (note RAM: D4)

When the D4 bit in the note RAM is set to "1", a silent period of approximately 10 msec will be inserted between the previous and concerned notes for playing discretely between notes. When the D4 bit is set to "0", no silent period will be inserted, and the previous and concerned notes will play continuously. This is used to specify a tie. The notes to be tied must be the same pitch and the D4 bit cannot be used to specify a slur.
Do not specify a tie (do not set the D4 bit in the note RAM to "0") for the note beginning a melody. Writing "0" may cause improper operation as there is no previous note.

(3) Rest (note RAM: D3)

When the D3 bit in the note RAM is set to "1", the data at that address is assumed as a rest and a break time with the length specified using the D7 to D5 bits will be inserted. When the D3 bit is set to "0", the data will be played as a note. When specifying a rest, set 00H or an available scale data to the corresponding scale RAM address. Writing FFH may cause improper operation.

(4) END (note RAM: D2)

Set "1" to the D2 bit in the note RAM, if that address is the last note or rest of a melody. This bit controls the end of play. The D2 bits in the middle of a melody must be set to "0".

■ Setting the scale RAM

Each word in the scale RAM corresponds to the word in the note RAM one to one and represents the pitch of the note.
The address corresponding to a rest must have data other than FFH. Writing 00H is recommended for rests.

The melody generator supports two equal temperament scales referencing to A4 = 440 Hz or C4 = 256 Hz using a 32.768 kHz (f_{OSC1}) as the reference signal frequency and either one can be selected.

The specifiable scale range is as follows:
1) Equal temperament scale referencing to A4 = 440 Hz
   C4 (262.144 Hz) to G6 (1560.381 Hz)
2) Equal temperament scale referencing to C4 = 256 Hz
   C4 (256 Hz) to C7# (2184.533 Hz)

The absolute error from the actual frequency is less than 1% for all pitches.

Note: Be aware that fluctuation of the oscillation frequency affects the pitch when CR oscillation is selected for the OSC1 oscillation circuit.

Tables 5.13.2.2 and 5.13.2.3 list the output frequencies and the specified value for the equal temperament scales referencing to A4 = 440 Hz and C4 = 256 Hz, respectively.

Table 5.13.2.2 Equal temperament scale referencing to A4 = 440 Hz

Pitch	Output frequency	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Division ratio
C4	262.144	0	0	0	0	1	0	1	0	0A	1/250
C4#	277.695	0	0	0	1	1	0	0	0	18	1/236
D4	293.883	0	0	1	0	0	1	1	1	27	1/223
D4#	310.597	0	0	1	1	0	0	1	1	33	1/211
E4	329.327	0	0	1	1	1	1	1	1	3F	1/199
F4	348.596	0	1	0	0	1	0	0	0	48	1/188
F4#	370.260	0	1	0	1	0	1	0	1	55	1/177
G4	392.431	0	1	0	1	1	1	1	1	5F	1/167
G4#	414.785	0	1	1	0	0	1	1	0	66	1/158
A4	439.839	0	1	1	1	0	0	0	1	71	1/149
A4#	464.794	0	1	1	1	1	0	0	1	79	1/141
B4	492.752	1	0	0	0	0	0	0	1	81	1/133
C5	524.288	1	0	0	0	1	0	0	1	89	1/125
C5#	555.390	1	0	0	0	1	1	1	0	8E	1/118
D5	585.143	1	0	0	1	0	1	0	0	94	1/112
D5#	624.152	1	0	0	1	1	1	0	1	9D	1/105
E5	661.980	1	0	1	0	0	0	1	1	A3	1/99
F5	697.191	1	0	1	0	0	1	1	0	A6	1/94
F5#	736.360	1	0	1	0	1	1	1	0	AD	1/89
G5	780.190	1	0	1	1	0	0	0	0	B0	1/84
G5#	829.570	1	0	1	1	0	1	1	1	B7	1/79
A5	885.622	1	0	1	1	1	0	1	0	BA	1/74
A5#	936.229	1	0	1	1	1	1	1	0	BE	1/70
B5	992.970	1	1	0	0	0	0	1	0	C2	1/66
C6	1040.254	1	1	0	0	0	1	1	1	C7	1/63
C6#	1110.780	1	1	0	0	1	0	1	1	CB	1/59
D6	1170.286	1	1	0	0	1	1	0	0	CC	1/56
D6#	1236.528	1	1	0	1	0	0	0	1	D1	1/53
E6	1310.720	1	1	0	1	0	0	1	0	D2	1/50
F6	1394.383	1	1	0	1	0	1	1	1	D7	1/47
F6#	1489.455	1	1	0	1	1	0	0	0	D8	1/44
G6	1560.381	1	1	0	1	1	0	1	0	DA	1/42

Table 5.13.2.3 Equal temperament scale referencing to C4 = 256 Hz

Pitch	Output frequency	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Division ratio
C4	256.000	0	0	0	0	0	1	0	0	04	1/256
C4#	270.810	0	0	0	1	0	0	1	0	12	1/242
D4	287.439	0	0	1	0	0	0	0	0	20	1/228
D4#	304.819	0	0	1	0	1	1	1	1	2F	1/215
E4	322.837	0	0	1	1	1	0	1	1	3B	1/203
F4	341.333	0	1	0	0	0	1	0	0	44	1/192
F4#	362.077	0	1	0	1	0	0	0	1	51	1/181
G4	383.251	0	1	0	1	1	0	1	1	5B	1/171
G4#	407.056	0	1	1	0	0	1	0	1	65	1/161
A4	431.158	0	1	1	0	1	1	0	0	6C	1/152
A4#	455.111	0	1	1	1	0	1	0	0	74	1/144
B4	481.882	0	1	1	1	1	1	0	0	7C	1/136
C5	512.000	1	0	0	0	0	1	0	0	84	1/128
C5#	541.620	1	0	0	0	1	1	0	1	8D	1/121
D5	574.877	1	0	0	1	0	0	1	0	92	1/114
D5#	606.815	1	0	0	1	1	0	0	0	98	1/108
E5	642.510	1	0	0	1	1	1	1	0	9E	1/102
F5	682.667	1	0	1	0	0	1	0	0	A4	1/96
F5#	720.176	1	0	1	0	1	0	1	1	AB	1/91
G5	771.012	1	0	1	1	0	0	0	1	B1	1/85
G5#	809.086	1	0	1	1	0	1	0	1	B5	1/81
A5	862.316	1	0	1	1	1	0	0	0	B8	1/76
A5#	910.222	1	0	1	1	1	1	0	0	BC	1/72
B5	963.765	1	1	0	0	0	0	0	0	C0	1/68
C6	1024.000	1	1	0	0	0	1	0	0	C4	1/64
C6#	1092.267	1	1	0	0	1	0	0	0	C8	1/60
D6	1149.754	1	1	0	0	1	1	0	1	CD	1/57
D6#	1213.630	1	1	0	0	1	1	1	0	CE	1/54
E6	1285.020	1	1	0	1	0	0	1	1	D3	1/51
F6	1365.333	1	1	0	1	0	1	0	0	D4	1/48
F6#	1456.356	1	1	0	1	1	0	0	1	D9	1/45
G6	1524.093	1	1	0	1	1	0	1	1	DB	1/43
G6#	1638.400	1	1	0	1	1	1	0	0	DC	1/40
A6	1724.632	1	1	0	1	1	1	1	0	DE	1/38
A6#	1820.444	1	1	1	0	0	0	0	0	E0	1/36
B6	1927.529	1	1	1	0	0	0	1	0	E2	1/34
C7	2048.000	1	1	1	0	0	1	0	0	E4	1/32
C7#	2184.533	1	1	1	0	0	1	1	0	E6	1/30

5.13.3 Controlling melody output

This section explains the play control method after programming of the note and scale RAM has finished.

■ Selecting a melody

Select a melody before playback can be started. Writing a melody start address (0 to FFH) to the scale / note RAM address register MCAD0–MCAD7 selects it as the melody to be played next. The specified value is used as the low-order 8-bit address for the note and scale RAMs.
Writing 00H specifies address 00D000H of the scale RAM and address 00D100H of the note RAM.
Writing FFH specifies address 00D0FFH of the scale RAM and address 00D1FFH of the note RAM.
Since the melody RAM data has no parameter that specifies a beginning of a melody, any play start position can be specified using this register.

■ Selecting a tempo

The tempo for playing a melody can be selected from among 16 types shown in Table 5.13.3.1 using the tempo selection register MTT0–MTT3.

Table 5.13.3.1 Tempo selection

MTT3	MTT2	MTT1	MTT0	Tempo ♩ =	Division ratio
1	1	1	1	480	1/1
1	1	1	0	240	1/2
1	1	0	1	160 (Vivace)	1/3
1	1	0	0	120 (Allegro)	1/4
1	0	1	1	96	1/5
1	0	1	0	80 (Andantino)	1/6
1	0	0	1	68.6	1/7
1	0	0	0	60 (Adagio)	1/8
0	1	1	1	53.3 (Lento)	1/9
0	1	1	0	48	1/10
0	1	0	1	43.6 (Largo)	1/11
0	1	0	0	40	1/12
0	0	1	1	36.9	1/13
0	0	1	0	34.3	1/14
0	0	0	1	32	1/15
0	0	0	0	30	1/16

The selected tempo will be set to the play control circuit at the start of play. Therefore, the tempo cannot be changed in the middle of play. When the MTT0–MTT3 register is changed during play, the selected tempo will be applied at the start of the next play.

■ Selecting a play mode and start/stop of play

The melody generator supports two play modes (level-hold play and one-shot play), and either one can be selected using the play mode selection register MLEV before starting play. The melody output control register MTC is used to control play and the control method differs according to the play mode.

Before play can be controlled using the MTC register, the output selection register MOSEL must be set to "1" so that the MOUT and $\overline{\text{MOUT}}$ terminals can output the melody signals.

(1) Control of level-hold play

The level-hold play mode can be selected by writing "0" to the MLEV register.
In this mode, writing "1" to the MTC register starts playing and writing "0" stops playing. The melody output continues until MTC is set to "0" even if the melody is changed while MTC is "1". (The play sequence returns to the beginning of the melody if the END bit has been set in the note RAM.)
Accessing across the melody RAM end address returns the sequence to the melody RAM start address to continue play.

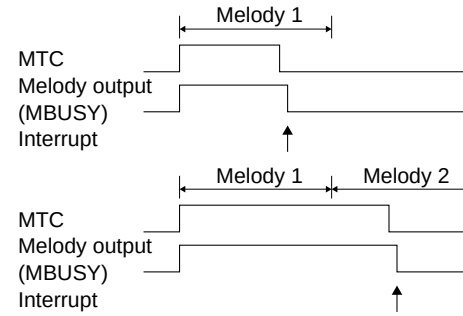


Fig. 5.13.3.1 Level-hold play mode

(2) Control of one-shot play

The one-shot play mode can be selected by writing "1" to the MLEV register.
In this mode, writing "1" to the MTC register starts playing and play is stopped at the end of the melody (when the END bit is set to "1" in the note RAM).
When "0" is written to the MTC register in the middle of a melody, the play stops immediately. Note that the END bit stops play but it does not reset the MTC register to "0". Therefore, write "0" to MTC after play has finished by the END bit.

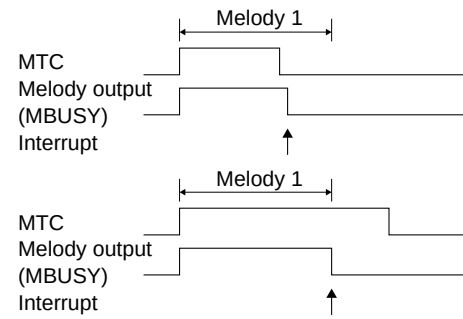


Fig. 5.13.3.2 One-shot play mode

During play, the melody play status bit MBUSY goes "1" for both the play modes. It is reset to "0" when a play stops completely and an interrupt occurs at the same time.
A melody continues until the note being played has finished even if MTC is set to "0". Use MBUSY or an interrupt to check if play has actually finished. Be especially sure when rewriting the melody RAM after play has finished.

■ **Sound generator output during playing**

The melody output terminals MOUT and $\overline{\text{MOUT}}$ can also be used to output the buzzer signal generated by the sound generator. Use the output selection register MOSEL for this purpose.
When "1" is written to MOSEL, the $\overline{\text{MOUT}}$ and MOUT terminals are configured as the melody output only ports. When "0" is written to MOSEL, the MOUT and $\overline{\text{MOUT}}$ terminals output the buzzer signal generated by the sound generator.
When the MOSEL is set to "0" during melody play, the melody play sequence continues. If the buzzer signal is not output from the sound generator while MOSEL is "0", a silent signal is output.

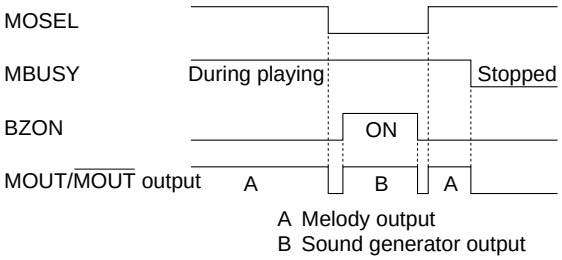


Fig. 5.13.3.3 Buzzer priority output

5.13.4 Interrupt function

The melody generator can generate an interrupt when play has finished.
Figure 5.13.4.1 shows the configuration of the melody generator interrupt circuit.

The melody generator sets the interrupt factor flag FMDY to "1" when a melody output stops completely.
At this time, if the interrupt enable register EMDY is "1" and the interrupt priority register PMDY (2 bits) is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
By setting the EMDY register to "0", the interrupt to the CPU can also be disabled. However, the interrupt factor flag is set to "1" when play has finished regardless of the interrupt enable register and interrupt priority register settings.
The interrupt factor flag set in "1" is reset to "0" by writing "1".
Refer to Section 5.16, "Interrupt and Standby Status", for details of the interrupt control registers and operations subsequent to interrupt generation.
The exception processing vector address for the melody play completion interrupt has been set in 000026H.

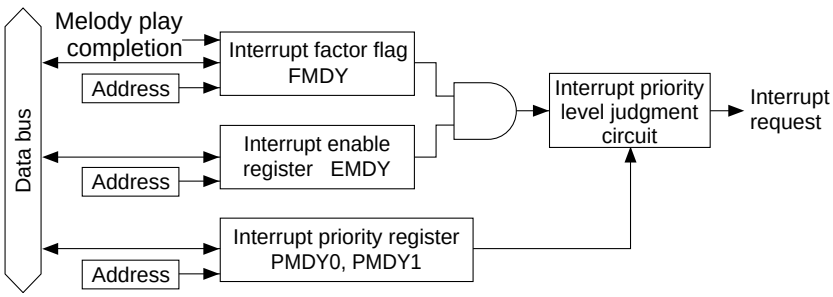


Fig. 5.13.4.1 Configuration of melody generator interrupt circuit

5.13.5 I/O memory for melody generator

Table 5.13.5.1 shows the melody generator control bits.

Table 5.13.5.1 Melody generator control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF46	D7	MCAD7	Note/scale RAM address D7 (MSB)				0	R/W	ADC7
	D6	MCAD6	Note/scale RAM address D6				0	R/W	ADC6
	D5	MCAD5	Note/scale RAM address D5				0	R/W	ADC5
	D4	MCAD4	Note/scale RAM address D4				0	R/W	ADC4
	D3	MCAD3	Note/scale RAM address D3				0	R/W	ADC3
	D2	MCAD2	Note/scale RAM address D2				0	R/W	ADC2
	D1	MCAD1	Note/scale RAM address D1				0	R/W	ADC1
	D0	MCAD0	Note/scale RAM address D0 (LSB)				0	R/W	ADC0
00FF47	D7	MTT3	Tempo selection register MTT3 MTT2 MTT1 MTT0 Tempo 1 1 1 1 480 1 1 1 0 240 1 1 0 1 160 1 1 0 0 120 1 0 1 1 96 1 0 1 0 80 1 0 0 1 68.6 1 0 0 0 60 0 1 1 1 53.3 0 1 1 0 48 0 1 0 1 43.6 0 1 0 0 40 0 0 1 1 36.9 0 0 1 0 34.3 0 0 0 1 32 0 0 0 0 30				0	R/W	TT3
	D6	MTT2					0	R/W	TT2
	D5	MTT1					0	R/W	TT1
	D4	MTT0					0	R/W	TT0
	D3	MLEV	Play mode selection		One shot	Level hold	0	R/W	
	D2	MOSEL	Output selection		MOUT	BZ priority	0	R/W	MOUTSEL
	D1	MBUSY	Melody play status		Busy	Ready	0	R	
	D0	MTC	Melody output control		Play	Stop	0	R/W	MT
00FF28	D7	PADC1	A/D converter interrupt priority register		PADC1 PADC0 Priority PMDY1 PMDY0 level 1 1 Level 3 1 0 Level 2 0 1 Level 1 0 0 Level 0		0	R/W	
	D6	PADC0					0	R/W	
	D5	PMDY1	Melody interrupt priority register				0	R/W	
	D4	PMDY0					0	R/W	
	D3	–	–		–	–	–		
	D2	–	–		–	–	–		Constantly "0" when
	D1	–	–		–	–	–		being read
	D0	–	–		–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register		Interrupt	Interrupt	0	R/W	
	D6	EMDY	Melody interrupt enable register		enable	disable	0	R/W	
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	–	–		–	–	–		
	D0	–	–		–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag	R	Generated	Not generated	0	R/W	
	D6	FMDY	Melody interrupt factor flag	W	Reset	No operation	0	R/W	
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	–	–		–	–	–		
	D0	–	–		–	–	–		

MCAD0–MCAD7: 00FF46H

Sets the play start address of the melody RAM data (0–FFH).
The specified value is used as the low-order 8-bit address for the note and scale RAMs.
Writing 00H specifies address 00D000H of the scale RAM and address 00D100H of the note RAM.
Writing FFH specifies address 00D0FFH of the scale RAM and address 00D1FFH of the note RAM.
Since the melody RAM data has no parameter that specifies the beginning of a melody, any play start position can be specified using this register.
At initial reset, this register is set to "00H".

MTT0–MTT3: 00FF47H•D4–D7

Selects a tempo.

Table 5.13.5.2 Tempo selection

MTT3	MTT2	MTT1	MTT0	Tempo ♩ =	Division ratio
1	1	1	1	480	1/1
1	1	1	0	240	1/2
1	1	0	1	160 (Vivace)	1/3
1	1	0	0	120 (Allegro)	1/4
1	0	1	1	96	1/5
1	0	1	0	80 (Andantino)	1/6
1	0	0	1	68.6	1/7
1	0	0	0	60 (Adagio)	1/8
0	1	1	1	53.3 (Lento)	1/9
0	1	1	0	48	1/10
0	1	0	1	43.6 (Largo)	1/11
0	1	0	0	40	1/12
0	0	1	1	36.9	1/13
0	0	1	0	34.3	1/14
0	0	0	1	32	1/15
0	0	0	0	30	1/16

The selected tempo will be set to the play control circuit at the start of play. Therefore, the tempo cannot be changed in the middle of play. When this register is changed during play, the selected tempo will be applied at the start of the next play.
At initial reset, this register is set to "0" (30).

MLEV: 00FF47H•D3

Selects a play mode.

When "1" is written: One-shot play mode
When "0" is written: Level-hold play mode
Reading: Valid

When "1" is written to MLEV, one-shot play mode is selected. When "0" is written, level-hold play mode is selected.
At initial reset, this register is set to "0" (level-hold play mode).

MOSEL: 00FF47H•D2

Selects an output signal from the MOUT and $\overline{\text{MOUT}}$ terminals.

When "1" is written: Melody output
When "0" is written: Buzzer output
Reading: Valid

When "1" is written to MOSEL, the MOUT and $\overline{\text{MOUT}}$ terminals are configured as the melody output only ports. When "0" is written to MOSEL, the MOUT and $\overline{\text{MOUT}}$ terminals output the buzzer signal generated by the sound generator.
When the MOSEL is set to "0" during a melody play, the melody play sequence continues.
At initial reset, this register is set to "0" (buzzer output).

MBUSY: 00FF47H•D1

Indicates a melody play status.

When "1" is written: During play
When "0" is written: Stopped
Reading: Invalid

MBUSY goes "1" while a melody is playing. The melody RAM cannot be rewritten in this period. MBUSY maintains "1" until the last note has finished even if MTC is set to "0". MBUSY is reset to "0" when play stops completely
At initial reset, MBUSY is set to "0" (stopped).

MTC: 00FF47H•D0

Controls play (melody output).

When "1" is written: Start
When "0" is written: Stop
Reading: Invalid

In the level-hold play mode, writing "1" to the MTC register starts playing and writing "0" stops playing. The melody output continues until MTC is set to "0" even if the melody is changed while MTC is "1". (The play sequence returns to the beginning of the melody if the END bit has been set in the note RAM.) Accessing across the melody RAM end address returns the sequence to the melody RAM start address to continue playing.

In the one-shot play mode, writing "1" to the MTC register starts playing and the play is stopped at the end of the melody (when the END bit is set to "1" in the note RAM). When "0" is written to the MTC register in the middle of a melody, the play stops immediately. Note that the END bit stops play but it does not reset the MTC register to "0". Therefore, write "0" to MTC after the END bit finishes play.
At initial reset, this register is set to "0" (stop).

PMDY0, PMDY1: 00FF28H•D4, D5

Sets the priority level of the melody interrupt.
Table 5.13.5.3 shows the interrupt priority level that can be set by the PMDY register.

Table 5.13.5.3 Interrupt priority level settings

PMDY1	PMDY0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EMDY: 00FF2AH•D6

Enables or disables the melody interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The EMDY register is the interrupt enable register corresponding to the melody completion interrupt factor. When this register is set to "1", the interrupt is enabled, and when it is set to "0", the interrupt is disabled.
At initial reset, this register is set to "0" (interrupt is disabled).

FMDY: 00FF2CH•D6

Indicates the generation of a melody completion interrupt factor.

When "1" is read: Int. factor present
When "0" is read: Int. factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FMDY is the interrupt factor flag corresponding to the melody interrupt and is set to "1" when play is completed.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, this flag is set to "0".

5.13.6 Programming notes

(1) Tempo cannot be changed in the middle of a melody.

(2) The note RAM and scale RAM cannot be accessed from the CPU while a melody is playing (MBUSY = "1").
A melody play continues until the note being played has finished even if MTC is set to "0". Make sure that a melody play has actually finished using MBUSY or an interrupt before the melody RAM can be accessed.

(3) Do not set a tie to the first note of a melody to prevent improper operation.

(4) Set 00H or an available scale data to the scale RAM address corresponding to a rest. Writing FFH may cause improper operation.

(5) When the SLP instruction is executed during a melody play, an unstable signal will be output from the MOUT and $\overline{MOUT}$ terminals at the time of returning from SLEEP status. Therefore, set MTC to "0" and make sure that MBUSY goes "0" before setting the CPU into SLEEP status.

(6) Direct driving a piezoelectric buzzer is recommended for melody output for lower current consumption.
When driving an external bipolar transistor with the melody signal, select "heavy load protection mode during melody output" by mask option. Note that the LCD driver current will be increased about 20 µA.
When direct driving a piezoelectric buzzer, select "normal mode" by mask option to reduce current consumption.

(7) The E0C88816 melody generator uses a RAM for storing melody data. Therefore, the user must arrange for permission to use the melodies to be stored if they are copyrighted.

5.14 Supply Voltage Detection (SVD) Circuit

5.14.1 Configuration of SVD circuit

The E0C88816 has a built-in supply voltage detection (SVD) circuit configured with a 4-bit successive approximation A / D converter.
The SVD circuit has 16 sampling levels (level 0–level 15) for supply voltage, and this can be controlled by software.
In addition, an initial reset signal can be generated when the supply voltage drops to level 0 or less. This is selected by the mask option.
Figure 5.14.1.1 shows the configuration of the SVD circuit.

5.14.2 Operation of SVD circuit

■ Sampling control of the SVD circuit

The SVD circuit has two operation modes: continuous sampling and 1 / 4 Hz auto-sampling mode. Operation mode selection is done by the SVD control registers SVDON and SVDSP as shown in Table 5.14.2.1. When both bits of SVDON and SVDSP are set to "1", continuous sampling is selected.

Table 5.14.2.1 Correspondence between control register and operation mode

SVDON	SVDSP	Operating mode
0	0	SVD circuit OFF
0	1	1/4 Hz auto-sampling ON
1	×	Continuous sampling ON

In both operation modes, reading SVDON can confirm whether the SVD circuit is operating (BUSY) or on standby (READY); "1" indicates BUSY and "0" indicates READY.
When executing an SLP instruction while the SVD circuit is operating, the stop operation of the OSC1 oscillation circuit is kept waiting until the sampling is completed. The two bits of SVDON and SVDSP are automatically reset to "0" by hardware while waiting for completion of sampling.
To reduce current consumption, turn the SVD circuit OFF when it is not necessary.

■ Detection result

The SVD circuit A / D converts the supply voltage (V_{DD}–V_{SS}) by 4-bit resolution and sets the result thereof into the SVD0–SVD3 register.
The data in SVD0–SVD3 correspond to the detection levels as shown in Table 5.14.2.2 and the detection data is maintained until the next sampling.

For the correspondence between the detection level and the supply voltage, see "7 ELECTRICAL CHARACTERISTICS".
An interval of 7.8 msec (f_{OSC1} = 32.768 kHz) is required from the start of supply voltage sampling by the SVD circuit to completion by writing the result into SVD0–SVD3. Therefore, when reading SVD0–SVD3 before sampling is finished, the previous result will be read.

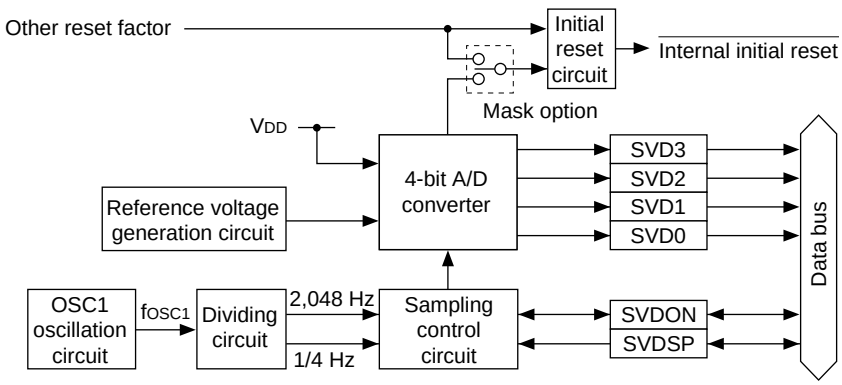


Fig. 5.14.1.1 Configuration of SVD circuit

Table 5.14.2.2 Supply voltage detection results

SVD3	SVD2	SVD1	SVD0	Detection level
1	1	1	1	Level 15
1	1	1	0	Level 14
1	1	0	1	Level 13
1	1	0	0	Level 12
1	0	1	1	Level 11
1	0	1	0	Level 10
1	0	0	1	Level 9
1	0	0	0	Level 8
0	1	1	1	Level 7
0	1	1	0	Level 6
0	1	0	1	Level 5
0	1	0	0	Level 4
0	0	1	1	Level 3
0	0	1	0	Level 2
0	0	0	1	Level 1
0	0	0	0	Level 0

■ Timing of sampling

Next, we will explain the timing for two operation modes.

(1) Continuous sampling mode

This mode is selected when "1" is written to SVDON and sampling of the supply voltage is done continuously in 7.8 msec cycles.
The SVD circuit starts operation in synchronization with the internal 2,048 Hz signal and performs one sampling in 16 clock cycles.
The sampling is done continuously without setting the standby time and the result is latched to SVD0–SVD3 in every 16 clock cycles.
Cancellation of continuous sampling is done by writing "0" to SVDON. The SVD circuit maintains ON status until completion of sampling and then goes OFF.
After writing "0" to SVDON, SVDON reads "1" until the SVD circuit actually goes OFF.
Figure 5.14.2.1 shows the timing chart of the continuous sampling.

(2) 1/4 Hz auto-sampling mode

This mode is selected when "0" is written to SVDON and "1" is written to SVDSP. In this case, supply voltage sampling is done in every 4 seconds.
The sampling time is 7.8 msec as in continuous sampling, and the result in SVD0–SVD3 is updated every 4 seconds.
Cancellation of 1/4 Hz auto-sampling is done by writing "0" to SVDSP. If the SVD circuit is sampling, SVD circuit waits until completion and then turns OFF. In addition, "1" is read from SVDON while the SVD circuit is sampling.
Figure 5.14.2.2 shows the timing chart of the 1/4 Hz auto-sampling.

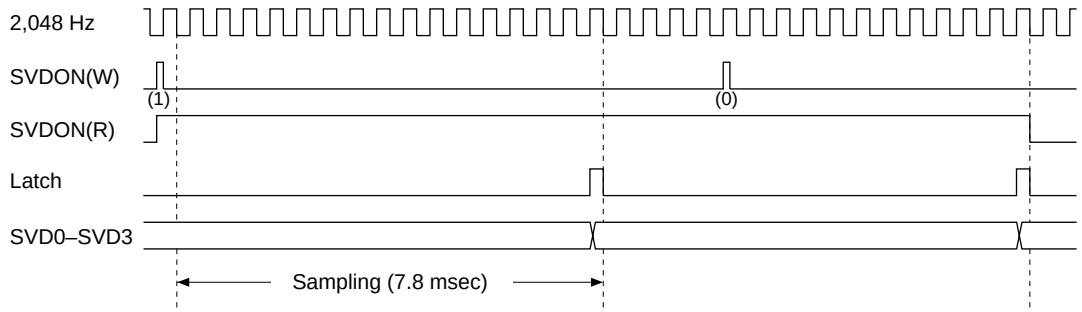


Fig. 5.14.2.1 Timing chart of continuous sampling

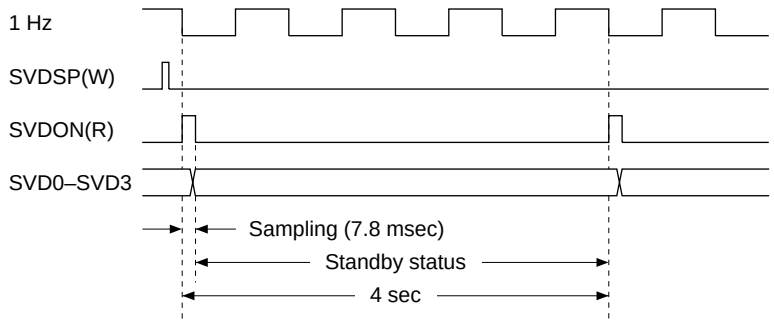


Fig. 5.14.2.2 Timing chart of 1/4 Hz auto-sampling

■ Reset function at low voltage detection

To avoid CPU runaway due to a supply voltage drop, an initial reset function when the supply voltage drops to level 0 or less can be selected by the mask option.
The SVD circuit shifts to continuous sampling status when it detects level 0 (SVD3–SVD0 = 0000B) four successive times. At this time, the internal initial reset signal is generated. The reset status continues until the supply voltage returns to level 2 (SVD3–SVD0 = 0010B) or higher.
When the reset status is canceled by the restoration of the supply voltage, the SVD circuit returns to its previous status. Continuous sampling status continues in case of the previous status was continuous sampling. Then CPU starts the reset exception processing.
Figure 5.14.2.3 shows the timing chart of the initial reset signal generation. (Example when using 1/4 Hz auto-sampling.)

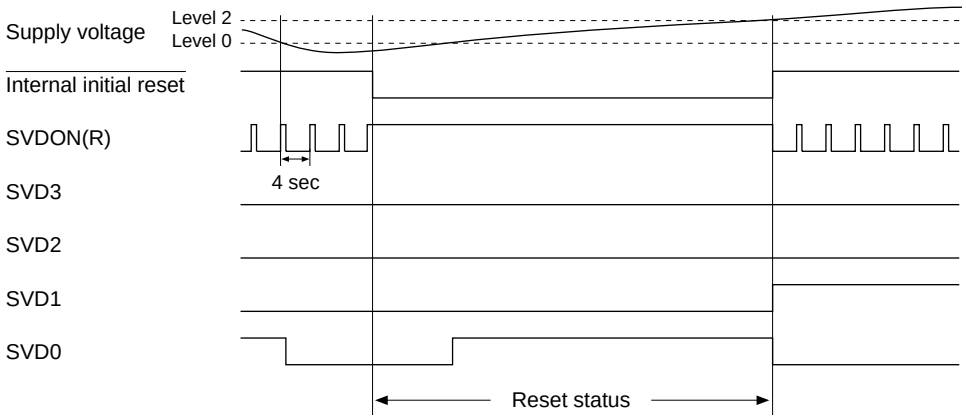


Fig. 5.14.2.3 Timing chart of the initial reset signal generation

5.14.3 I/O memory for SVD circuit

Table 5.14.3.1 shows the SVD circuit control bits.

Table 5.14.3.1 SVD circuit control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF12	D7	–	–	–	–	–		Constantry "0" when
	D6	–	–	–	–	–		being read
	D5	SVDSP	SVD auto-sampling control	On	Off	0	R/W	These registers are reset to "0" when SLP instruction is executed.
	D4	SVDON	SVD continuous sampling control/status R	Busy	Ready	1→0*1	R/W	
			W	On	Off	0		
	D3	SVD3	SVD detection level			X	R	*2
	D2	SVD2	SVD3 SVD2 SVD1 SVD0 Detection level			X	R	
	D1	SVD1	1 1 1 1 Level 15			X	R	
	D0	SVD0	1 1 1 0 Level 14			X	R	
			: : : : :					
			0 0 0 0 Level 0					

*1 After initial reset, this status is set "1" until conclusion of hardware first sampling.
*2 Initial values are set according to the supply voltage detected at first sampling by hardware.
Until conclusion of first sampling, SVD0–SVD3 data are undefined.

SVDON: 00FF12H•D4

Controls the turning ON / OFF of the continuous sampling mode.

When "1" is written: Continuous sampling ON
When "0" is written: Continuous sampling OFF

When "1" is read: BUSY
When "0" is read: READY

The continuous sampling mode goes ON when "1" is written to SVDON and goes OFF, when "0" is written.
In the ON status, sampling of the supply voltage is done continuously in 7.8 msec cycles and the detection result is latched to SVD0–SVD3.
SVDON can be read, and "1" indicates SVD circuit operation (BUSY) and "0" indicates standby (READY).
At initial reset and in the SLEEP status, SVDON is set to "0" (continuous sampling OFF / READY).

SVDSP: 00FF12H•D5

Controls the turning ON / OFF of the 1 / 4 Hz auto-sampling mode.

When "1" is written: Auto-sampling ON
When "0" is written: Auto-sampling OFF
Reading: Valid

The 1 / 4 Hz auto-sampling mode goes ON when "1" is written to SVDSP and goes OFF, when "0" is written.
In the ON status, sampling is done in every 4 seconds and "1" is read from SVDON during the actual sampling period (7.8 msec).
At initial reset and in the SLEEP status, SVDSP is set to "0" (auto-sampling OFF).

SVD0–SVD3: 00FF12H•D0–D3

The detection result of the SVD is set.
The reading data correspond to the detection levels as shown in Table 5.14.3.2 and the data is maintained until the next sampling.

Table 5.14.3.2 Supply voltage detection results

SVD3	SVD2	SVD1	SVD0	Detection level
1	1	1	1	Level 15
1	1	1	0	Level 14
1	1	0	1	Level 13
1	1	0	0	Level 12
1	0	1	1	Level 11
1	0	1	0	Level 10
1	0	0	1	Level 9
1	0	0	0	Level 8
0	1	1	1	Level 7
0	1	1	0	Level 6
0	1	0	1	Level 5
0	1	0	0	Level 4
0	0	1	1	Level 3
0	0	1	0	Level 2
0	0	0	1	Level 1
0	0	0	0	Level 0

For the correspondence between the detection level and the supply voltage, see "7 ELECTRICAL CHARACTERISTICS".
The initial value at initial reset is set according to the supply voltage detected at first sampling by hardware. Data of this bit is undefined until this sampling is completed.

5.14.4 Programming notes

(1) To reduce current consumption, turn the SVD circuit OFF (SVDON = SVDSP = "0") when it is not necessary.

(2) When executing an SLP instruction while the SVD circuit is operating, the stop operation of the OSC1 oscillation circuit is kept waiting until the sampling is completed. The two bits of SVDON and SVDSP are automatically reset to "0" by hardware while waiting for completion of sampling.

5.15 A/D Converter

5.15.1 Characteristics and configuration of A/D converter

The E0C88816 has a built-in A / D converter with the following characteristics.

- Conversion formula: Successive-approximation type
- Resolution: 10 bits
- Input channel: Maximum 4 channels
- Conversion time: Minimum 11 µsec (in 2 MHz operation)
- Setting of analog conversion voltage range is possible with reference voltage terminal (AVREF)
- A / D conversion result is possible to read from 10-bit data register
- Sample & hold circuit built-in
- A / D conversion completion generates an interrupt

Figure 5.15.1.1 shows the configuration of the A / D converter.

5.15.2 Terminal configuration of A/D converter

The terminals used with the A / D converter are as follows:

■ AVDD, AGND, AVSS (power supply terminals)

The AVDD, AGND and AVSS terminals are power supply terminals for the A / D converter. The voltage should be input as AVDD ≤ VDD and AGND ≤ AVSS = VSS.

■ AVREF (reference voltage input terminal)

The AVREF terminal is the reference voltage terminal of the analog block. Input voltage range of the A / D conversion is decided by this input. The voltage should be input as AVREF ≤ AVDD.

■ AD4–AD7 (analog input terminals)

The analog input terminals AD4–AD7 are shared with the I / O port terminals P14–P17. Therefore, it is necessary to set them for the A / D converter by software when using them as analog input terminals. This setting can be done for each terminal. (Refer to Section 5.15.4 for setting.)
At initial reset, all the terminals are set in the I / O port terminal.
Analog voltage value AVIN that can be input is in the range of AVSS ≤ AGND ≤ AVIN ≤ AVREF.

5.15.3 Mask option

■ Pull-up resistor

I/O port pull-up resistors		
P14 (AD4)	☐ With resistor	☑ Gate direct
P15 (AD5)	☐ With resistor	☑ Gate direct
P16 (AD6)	☐ With resistor	☑ Gate direct
P17 (AD7)	☐ With resistor	☑ Gate direct

The input terminals of the A / D converter are shared with the I / O port terminals P14–P17. Therefore, the terminal specification of the A / D converter is decided by setting the I / O port mask option. Select "Gate direct" for the port corresponding to the channel to be used to obtain the conversion precision.

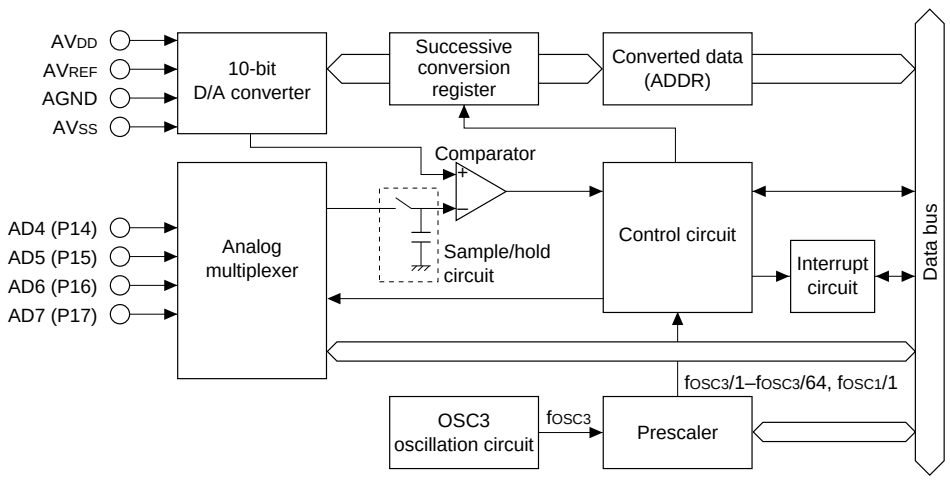


Fig. 5.15.1.1 Configuration of A/D converter

5.15.4 A/D conversion

■ Setting the A/D input terminal

When using the A / D converter, it is necessary to set up the terminals used for analog input from the P14–P17 initialized as the I / O port terminals. Four terminals can all be used as analog input terminals.

The PAD (PAD4–PAD7) register is used to set analog input terminals. When the PAD register bits are set to "1", the corresponding terminals function as the analog input terminals.

Table 5.15.4.1 Correspondence between A/D input terminal and PAD register

Terminal	A/D input control register
P14 (AD4)	PAD4
P15 (AD5)	PAD5
P16 (AD6)	PAD6
P17 (AD7)	PAD7

■ Setting the input clock

The A / D conversion clock can be selected from eight types shown in Table 5.15.4.2. The selection is done using the PSAD register.

Table 5.15.4.2 Input clock selection

Selection register			Division ratio	Output control
PSAD2	PSAD1	PSAD0		
1	1	1	f_{OSC1}/1	PRAD register "1": ON "0": OFF
1	1	0	f_{OSC3}/64	
1	0	1	f_{OSC3}/32	
1	0	0	f_{OSC3}/16	
0	1	1	f_{OSC3}/8	
0	1	0	f_{OSC3}/4	
0	0	1	f_{OSC3}/2	
0	0	0	f_{OSC3}/1	

The selected clock is input to the A / D converter by writing "1" to the PRAD register.

Note: • When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the A/D converter.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

- *The frequency of the input clock should be lower than the maximum value shown in Section 7.8, "A/D Converter Characteristics".*
- *The input clock should be set when the A/D converter stops. Changing in the A/D converter operation may cause a malfunction.*
- *To prevent malfunction, do not start A/D conversion (writing to the CHS register) when the A/D conversion clock is not being input to the A/D converter, and do not turn the clock off during A/D conversion.*

■ Selecting the input signal

The analog signals from the AD4 (P14)–AD7 (P17) terminals are input to the multiplexer, and the analog input channel for A / D conversion is selected by software. This selection can be done using the CHS register as shown in Table 5.15.4.3.

Table 5.15.4.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD7
1	0	AD6
0	1	AD5
0	0	AD4

■ A/D conversion operation

An A / D conversion starts by writing data to the ADRUN register. For example, when performing A / D conversion using AD7 as the analog input, write "1" (1, 1) to the CHS register (CHS1, CHS0) and then write "1" to the ADRUN register. The A / D input channel is selected and the A / D conversion starts. However, it is necessary that the P17 terminal has been set as an analog input terminal.
The built-in sample & hold circuit starts sampling of the analog input specified from t_{AD} after writing. When the sampling is completed, the held analog input voltage is converted into a 10-bit digital value in successive-approximation architecture.
The conversion result is loaded into the ADDR (ADDR0–ADDR9) register. ADDR0 is the LSB and ADDR9 is the MSB.

Note: If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A/D conversion does not result in a correct converted value.

Example)
Terminal setting:
PAD5=1, PAD7=PAD6=PAD4=0
(AD5 terminal is used)
Selection of input channel:
CHS1=0, CHS0=0
(AD4 is selected)

In a setting like this, the A/D conversion result will be invalid because the contents of the settings are not matched.

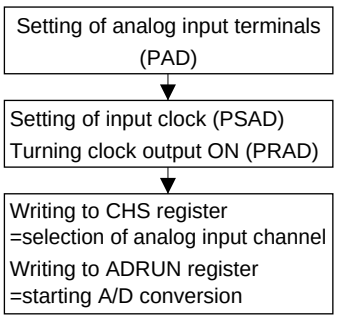


Fig. 5.15.4.1 Flowchart for starting A/D conversion

An A/D conversion is completed when the conversion result is loaded into the ADDR register. At that point, the A/D converter generates an interrupt (explained in the next section).

Figure 5.15.4.2 shows the timing chart of A/D conversion.

5.15.5 Interrupt function

The A/D converter can generate an interrupt when an A/D conversion has completed.
Figure 5.15.5.1 shows the configuration of the A/D converter interrupt circuit.

The A/D converter sets the interrupt factor flag FAD to "1" when it stores the conversion.
At this time, if the interrupt enable register EAD is "1" and the interrupt priority register PADC (2 bits) is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
By setting the EAD register to "0", the interrupt to the CPU can also be disabled. However, the interrupt factor flag is set to "1" when an A/D conversion has completed regardless of the interrupt enable register and interrupt priority register settings.
The interrupt factor flag set in "1" is reset to "0" by writing "1".
Refer to Section 5.16, "Interrupt and Standby Status", for details of the interrupt control registers and operations subsequent to interrupt generation.
The exception processing vector address for the A/D conversion completion interrupt has been set in 000024H.

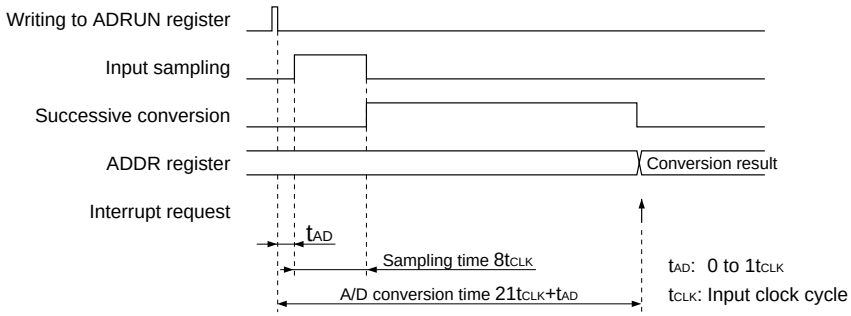


Fig. 5.15.4.2 Timing chart of A/D conversion

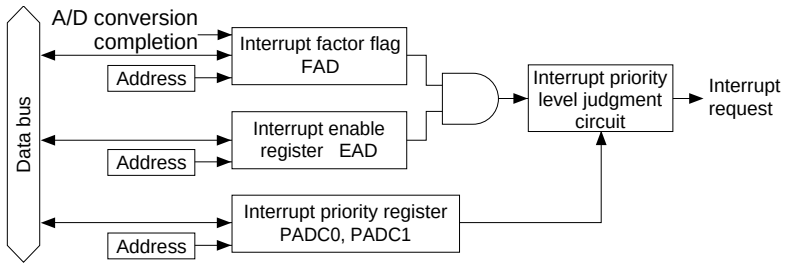


Fig. 5.15.5.1 Configuration of A/D converter interrupt circuit

5.15.6 I/O memory for A/D converter

Table 5.15.6.1 shows the A / D converter control bits.

Table 5.15.6.1(a) A/D converter control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF80	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when
	D5	–	–	–	–	–		being read
	D4	–	–	–	–	–		
	D3	PRAD	A/D converter clock control	On	Off	0	R/W	
	D2	PSAD2	A/D converter division ratio			0	R/W	
	D1	PSAD1	PSAD2 PSAD1 PSAD0 Division ratio 1 1 1 fOSC1 / 1 1 1 0 fOSC3 / 64 1 0 1 fOSC3 / 32 1 0 0 fOSC3 / 16 0 1 1 fOSC3 / 8 0 1 0 fOSC3 / 4 0 0 1 fOSC3 / 2 0 0 0 fOSC3 / 1			0	R/W	
	D0	PSAD0				0	R/W	
00FF81	D7	PAD7	P17 A/D converter input control	A/D converter input	I/O port	0	R/W	
	D6	PAD6	P16 A/D converter input control			0	R/W	
	D5	PAD5	P15 A/D converter input control			0	R/W	
	D4	PAD4	P14 A/D converter input control			0	R/W	
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		Constantly "0" when
	D1	–	–	–	–	–		being read
	D0	–	–	–	–	–		
00FF82	D7	ADRUN	A/D conversion start control register	Start	Invalid	0	W	
	D6	–	–	–	–	–	–	
	D5	–	–	–	–	–	–	Constantry "0" when
	D4	–	–	–	–	–	–	being read
	D3	–	–	–	–	–	–	
	D2	–	–	–	–	–	–	
	D1	CHS1	Analog input channel selection			0	R/W	
	D0	CHS0	CHS1 CHS0 Input channel 1 1 AD7 1 0 AD6 0 1 AD5 0 0 AD4			0	R/W	
00FF83	D7	ADDR9	A/D conversion result D9 (MSB)			–	R	
	D6	ADDR8	A/D conversion result D8			–	R	
	D5	ADDR7	A/D conversion result D7			–	R	
	D4	ADDR6	A/D conversion result D6			–	R	
	D3	ADDR5	A/D conversion result D5			–	R	
	D2	ADDR4	A/D conversion result D4			–	R	
	D1	ADDR3	A/D conversion result D3			–	R	
	D0	ADDR2	A/D conversion result D2			–	R	
00FF84	D7	–	–	–	–	–		
	D6	–	–	–	–	–		
	D5	–	–	–	–	–		Constantly "0" when
	D4	–	–	–	–	–		being read
	D3	–	–	–	–	–		
	D2	–	–	–	–	–		
	D1	ADDR1	A/D conversion result D1			–	R	
	D0	ADDR0	A/D conversion result D0 (LSB)			–	R	

Table 5.15.6.1(b) A/D converter control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF28	D7	PADC1	A/D converter interrupt priority register		PADC1 PADC0 Priority PMDY1 PMDY0 level		0	R/W	
	D6	PADC0			1 1 Level 3		0	R/W	
	D5	PMDY1	Melody interrupt priority register		1 0 Level 2		0	R/W	
	D4	PMDY0			0 1 Level 1 0 0 Level 0		0	R/W	
	D3	–	–		–	–	–		
	D2	–	–		–	–	–		Constantly "0" when
	D1	–	–		–	–	–		being read
	D0	–	–		–	–	–		
00FF2A	D7	EAD	A/D converter interrupt enable register		Interrupt	Interrupt	0	R/W	
	D6	EMDY	Melody interrupt enable register		enable	disable	0	R/W	
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	–	–		–	–	–		
	D0	–	–		–	–	–		
00FF2C	D7	FAD	A/D converter interrupt factor flag	R	Generated	Not generated	0	R/W	
	D6	FMDY	Melody interrupt factor flag	W	Reset	No operation	0	R/W	
	D5	–	–		–	–	–		
	D4	–	–		–	–	–		
	D3	–	–		–	–	–		Constantly "0" when
	D2	–	–		–	–	–		being read
	D1	–	–		–	–	–		
	D0	–	–		–	–	–		

PAD4–PAD7: 00FF81H•D4–D7

Sets the P14–P17 terminals as the analog input terminals for the A / D converter.

When "1" is written: A / D converter input
When "0" is written: I / O port
Reading: Valid

When "1" is written to PADn, the P1n terminal is set to the analog input terminal ADn. (n=4–7)
When "0" is written, the terminal is used with the I / O port.
At initial reset, this register is set to "0" (I / O port).

PSAD0–PSAD2: 00FF80H•D0–D2

Selects the clock for the A / D converter.

Table 5.15.6.2 Input clock selection

Selection register			Division ratio	Output control
PSAD2	PSAD1	PSAD0		
1	1	1	$f_{OSC1}/1$	PRAD
1	1	0	$f_{OSC3}/64$	register
1	0	1	$f_{OSC3}/32$	
1	0	0	$f_{OSC3}/16$	"1": ON
0	1	1	$f_{OSC3}/8$	"0": OFF
0	1	0	$f_{OSC3}/4$	
0	0	1	$f_{OSC3}/2$	
0	0	0	$f_{OSC3}/1$	

This setting controls the division ratio of the prescaler.
At initial reset, this register is set to "0" (f_{OSC3} / 1).

PRAD: 00FF80H•D3

Controls the clock supply to the A / D converter.

When "1" is written: ON
When "0" is written: OFF
Reading: Invalid

By writing "1" to the PRAD register, the clock selected with the PSAD register is input to the A / D converter.
When "0" is written, the clock is not input to the A / D converter.
At initial reset, this register is set to "0" (OFF).

ADRUN: 00FF82H•D7

Starts A / D conversion.

When "1" is written: Start A / D conversion
When "0" is written: Invalid
Reading: Always "0"

By writing "1" to this register, the A / D converter starts A / D conversion of the channel selected by the CHS register, and stores the conversion result to the ADDR register.

CHS0, CHS1: 00FF82H•D0, D1

Selects an analog input channel.

Table 5.15.6.3 Selection of analog input channel

CHS1	CHS0	Input channel
1	1	AD7
1	0	AD6
0	1	AD5
0	0	AD4

At initial reset, this register is set to "0" (AD4).

ADDR0–ADDR9: 00FF84H•D0, D1, 00FF83H

A / D conversion result is stored.
ADDR0 is the LSB and ADDR9 is the MSB.
ADDR0 and ADDR1 are assigned in D0 bit and D1 bit of the address 00FF84H. D2–D7 bits in this address are always "0" when being read.
At initial reset, data is undefined.

PADC0, PADC1: 00FF28H•D6, D7

Sets the priority level of the A / D conversion completion interrupt.
Table 5.15.6.4 shows the interrupt priority level which can be set by the PADC register.

Table 5.15.6.4 Interrupt priority level settings

PADC1	PADC0	Interrupt priority level
1	1	Level 3 ($\overline{IRQ3}$)
1	0	Level 2 ($\overline{IRQ2}$)
0	1	Level 1 ($\overline{IRQ1}$)
0	0	Level 0 (None)

At initial reset, this register is set to "0" (level 0).

EAD: 00FF2AH•D7

Enables or disables the A / D conversion completion interrupt generation to the CPU.

When "1" is written: Interrupt is enabled
When "0" is written: Interrupt is disabled
Reading: Valid

The EAD register is the interrupt enable register corresponding to the A / D conversion completion interrupt factor. When this register is set to "1", the interrupt is enabled, and when it is set to "0", the interrupt is disabled.
At initial reset, this register is set to "0" (interrupt is disabled).

FAD: 00FF2CH•D7

Indicates the generation of A / D conversion completion interrupt factor.

When "1" is read: Interrupt factor present
When "0" is read: Interrupt factor not present

When "1" is written: Resets factor flag
When "0" is written: Invalid

FAD is the interrupt factor flag corresponding to the A / D conversion completion interrupt. It is set to "1" when an A / D conversion is completed.
At this point, if the corresponding interrupt enable register is set to "1" and the corresponding interrupt priority register is set to a higher level than the setting of the interrupt flags (I0 and I1), an interrupt is generated to the CPU.
Regardless of the interrupt enable register and interrupt priority register settings, the interrupt factor flag is set to "1" when the interrupt generation condition is met.
To accept the subsequent interrupt after an interrupt generation, it is necessary to re-set the interrupt flags (set the interrupt flag to a lower level than the level indicated by the interrupt priority registers, or execute the RETE instruction) and to reset the interrupt factor flag. The interrupt factor flag is reset to "0" by writing "1".
At initial reset, the FAD flag is reset to "0".

5.15.7 Programming notes

(1) When the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the A / D converter.
From the time the OSC3 oscillation circuit is turning ON until oscillation stabilizes, an interval of several msec to several 10 msec is necessary. Consequently, you should allow an adequate waiting time after turning the OSC3 oscillation circuit ON before starting the count of the programmable timer. (The oscillation start time will vary somewhat depending on the oscillator and on external parts. Refer to the oscillation start time example indicated in Chapter 7, "ELECTRICAL CHARACTERISTICS".)
At initial reset, OSC3 oscillation circuit is set to OFF status.

(2) When SLEEP mode is set during A / D conversion, correct A / D conversion result cannot be obtained because the OSC3 oscillation circuit stops. Do not set in SLEEP mode during A / D conversion.

(3) The input clock and analog input terminals should be set when the A / D converter stops. Changing in the A / D converter operation may cause a malfunction.

(4) The frequency of the input clock should be lower than the maximum value shown in Section 7.8, "A / D Converter Characteristics".

(5) To prevent malfunction, do not start A / D conversion (writing to the CHS register) when the A / D conversion clock is not being input to the A / D converter, and do not turn the clock off during A / D conversion.

(6) If the CHS register selects an input channel which is not included in the analog input terminals set by the PAD register (the PAD register can select several terminals simultaneously), the A / D conversion does not result in a correct converted value.

(7) During A / D conversion, do not operate the P1n terminals which are not used for analog inputs of the A / D converter (for input / output of digital signal etc.). It affects the A / D conversion precision.

5.16 Interrupt and Standby Status

■ Types of interrupts

Eight systems and 17 types of interrupts have been provided for the E0C88816.

External interrupt

- K00–K07 input interrupt (2 types)
- K10 input interrupt (1 type)

Internal interrupt

- Clock timer interrupt (4 types)
- Stopwatch interrupt (3 types)
- Programmable timer interrupt (2 types)
- Serial interface interrupt (3 types)
- Melody interrupt (1 type)
- A / D converter interrupt (1 type)

An interrupt factor flag that indicates the generation of an interrupt factor and an interrupt enable register that sets enable / disable for interrupt requests have been provided for each interrupt and interrupt generation can be optionally set for each factor.
In addition, an interrupt priority register has been provided for each system of interrupts and the priority of interrupt processing can be set to 3 levels in each system.
Figure 5.16.1 shows the configuration of the interrupt circuit.

Refer to the explanations of the respective peripheral circuits for details on each interrupt.

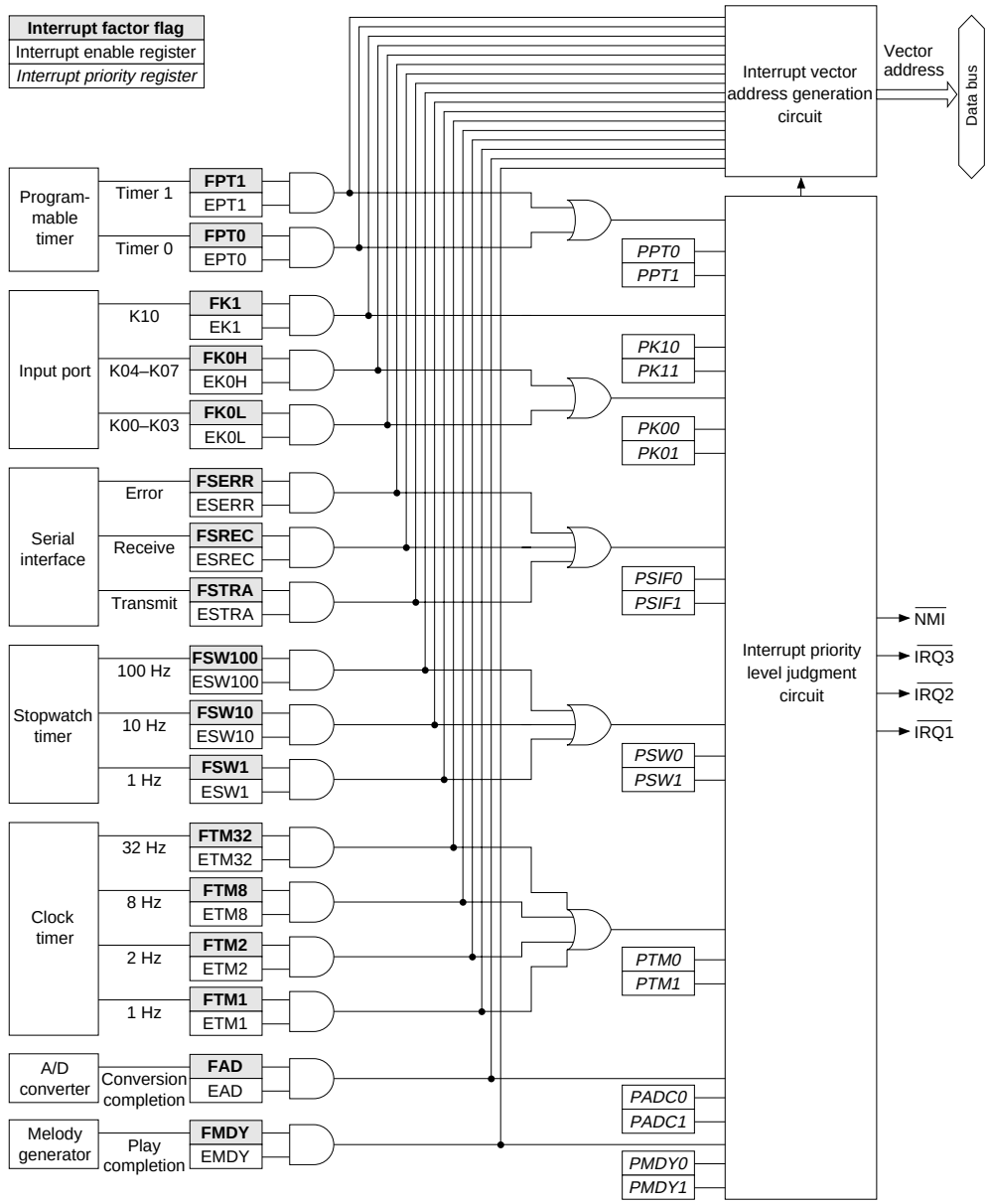


Fig. 5.16.1 Configuration of interrupt circuit

■ HALT status

By executing the program's HALT instruction, the E0C88816 shifts to the HALT status.
Since CPU operation stops in the HALT status, power consumption can be reduced with only peripheral circuit operation.
Cancellation of the HALT status is done by initial reset or an optional interrupt request, and the CPU restarts program execution from an exception processing routine.
See the "E0C88 Core CPU Manual" for the HALT status and reactivation sequence.

■ SLEEP status

By executing the program's SLP instruction, the E0C88816 shifts to the SLEEP status.
Since the operation of the CPU and peripheral circuits stop completely in the SLEEP status, power consumption can be reduced even more than in the HALT status.
Cancellation of the SLEEP status is done by initial reset or an input interrupt from the input port. The CPU reactivates after waiting 8,192 / f_{OSC1} seconds of oscillation stabilization time. At this time, the CPU restarts program execution from an exception processing routine (input interrupt routine).

Note: Since oscillation is unstable for a short time after reactivation from the SLEEP status, the wait time is not always 250 msec even when using the 32.768 kHz crystal oscillator for the OSC1 oscillation circuit.

5.16.1 Interrupt generation conditions

The interrupt factor flags that indicate the generation of their respective interrupt factors are provided for the previously indicated 8 systems and 17 types of interrupts and they will be set to "1" by the generation of a factor.

In addition, interrupt enable registers with a 1 to 1 correspondence to each of the interrupt factor flags are provided. An interrupt is enabled when "1" is written and interrupt is disabled when "0" is written.

The CPU manages the enable / disable of interrupt requests at the interrupt priority level. An interrupt priority register that sets the priority level is provided for each of the interrupts of the 8 systems and the CPU accepts only interrupts above the level that has been indicated with the interrupt flags (I0 and I1).
Consequently, the following three conditions are necessary for the CPU to accept the interrupt.

(1) The interrupt factor flag has been set to "1" by generation of an interrupt factor.
(2) The interrupt enable register corresponding to the above has been set to "1".
(3) The interrupt priority register corresponding to the above has been set to a priority level higher than the interrupt flag (I0 and I1) setting.

The CPU initially samples the interrupt for the first op-code fetch cycle of each instruction. Thereupon, the CPU shifts to the exception processing when the above mentioned conditions have been established.
See the "E0C88 Core CPU Manual" for the exception processing sequence.

5.16.2 Interrupt factor flag

Table 5.16.2.1 shows the correspondence between the factors generating an interrupt and the interrupt factor flags.
The corresponding interrupt factor flags are set to "1" by generation of the respective interrupt factors.
The corresponding interrupt factor can be confirmed by reading the flags through software.

Table 5.16.2.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 underflow	FPT1	(00FF25 D7)
Programmable timer 0 underflow	FPT0	(00FF25 D6)
Non matching of the K10 input and the input comparison register KCP10	FK1	(00FF25 D5)
Non matching of the K04–K07 inputs and the input comparison registers KCP04–KCP07	FK0H	(00FF25 D4)
Non matching of the K00–K03 inputs and the input comparison registers KCP00–KCP03	FK0L	(00FF25 D3)
Serial interface receiving error (in asynchronous mode)	FSERR	(00FF25 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)
Falling edge of the stopwatch timer 100 Hz signal	FSW100	(00FF24 D6)
Falling edge of the stopwatch timer 10 Hz signal	FSW10	(00FF24 D5)
Falling edge of the stopwatch timer 1 Hz signal	FSW1	(00FF24 D4)
Rising edge of the clock timer 32 Hz signal	FTM32	(00FF24 D3)
Rising edge of the clock timer 8 Hz signal	FTM8	(00FF24 D2)
Rising edge of the clock timer 2 Hz signal	FTM2	(00FF24 D1)
Rising edge of the clock timer 1 Hz signal	FTM1	(00FF24 D0)
A/D conversion completion	FAD	(00FF2C D7)
Melody play completion	FMDY	(00FF2C D6)

Interrupt factor flag that has been set to "1" is reset to "0" by writing "1".
At initial reset, the interrupt factor flags are reset to "0".

Note: When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

5.16.3 Interrupt enable register

The interrupt enable register has a 1 to 1 correspondence with each interrupt factor flag and enable / disable of interrupt requests can be set.

When "1" is written to the interrupt enable register, an interrupt request is enabled, and is disabled when "0" is written. This register also permits reading, thus making it possible to confirm that a status has been set.
At initial reset, the interrupt enable registers are set to "0" and shifts to the interrupt disable status.
Table 5.16.3.1 shows the correspondence between the interrupt enable registers and the interrupt factor flags.

5.16.4 Interrupt priority register and interrupt priority level

The interrupt priority registers shown in Table 5.16.4.1 are set to each system of interrupts and the interrupt priority levels for the CPU can be set to the optional priority level (0–3). As a result, it is possible to have multiple interrupts that match the system's interrupt processing priority levels.

The interrupt priority level between each system can optionally be set to three levels by the interrupt priority register. However, when more than one system is set to the same priority level, they are processed according to the default priority level.

Table 5.16.4.2 Setting of interrupt priority level

P*1	P*0	Interrupt priority level	
1	1	Level 3	($\overline{IRQ3}$)
1	0	Level 2	($\overline{IRQ2}$)
0	1	Level 1	($\overline{IRQ1}$)
0	0	Level 0	(non)

Table 5.16.3.1 Interrupt enable registers and interrupt factor flags

Interrupt	Interrupt factor flag		Interrupt enable register	
Programmable timer 1	FPT1	(00FF25 D7)	EPT1	(00FF23 D7)
Programmable timer 0	FPT0	(00FF25 D6)	EPT0	(00FF23 D6)
K10 input	FK1	(00FF25 D5)	EK1	(00FF23 D5)
K04–K07 input	FK0H	(00FF25 D4)	EK0H	(00FF23 D4)
K00–K03 input	FK0L	(00FF25 D3)	EK0L	(00FF23 D3)
Serial interface receiving error	FSERR	(00FF25 D2)	ESERR	(00FF23 D2)
Serial interface receiving completion	FSREC	(00FF25 D1)	ESREC	(00FF23 D1)
Serial interface transmitting completion	FSTRA	(00FF25 D0)	ESTRA	(00FF23 D0)
Stopwatch timer 100 Hz	FSW100	(00FF24 D6)	ESW100	(00FF22 D6)
Stopwatch timer 10 Hz	FSW10	(00FF24 D5)	ESW10	(00FF22 D5)
Stopwatch timer 1 Hz	FSW1	(00FF24 D4)	ESW1	(00FF22 D4)
Clock timer 32 Hz	FTM32	(00FF24 D3)	ETM32	(00FF22 D3)
Clock timer 8 Hz	FTM8	(00FF24 D2)	ETM8	(00FF22 D2)
Clock timer 2 Hz	FTM2	(00FF24 D1)	ETM2	(00FF22 D1)
Clock timer 1 Hz	FTM1	(00FF24 D0)	ETM1	(00FF22 D0)
A/D conversion completion	FAD	(00FF2C D7)	EAD	(00FF2A D7)
Melody play completion	FMDY	(00FF2C D6)	EMDY	(00FF2A D6)

Table 5.16.4.1 Interrupt priority register

Interrupt	Interrupt priority register	
Programmable timer interrupt	PPT0, PPT1	(00FF21 D2, D3)
K10 input interrupt	PK10, PK11	(00FF21 D0, D1)
K00–K07 input interrupt	PK00, PK01	(00FF20 D6, D7)
Serial interface interrupt	PSIF0, PSIF1	(00FF20 D4, D5)
Stopwatch timer interrupt	PSW0, PSW1	(00FF20 D2, D3)
Clock timer interrupt	PTM0, PTM1	(00FF20 D0, D1)
A/D converter interrupt	PADC0, PADC1	(00FF28 D6, D7)
Melody generator interrupt	PMDY0, PMDY1	(00FF28 D4, D5)

At initial reset, the interrupt priority registers are all set to "0" and each interrupt is set to level 0. Furthermore, the priority levels in each system have been previously decided and they cannot be changed.
The CPU can mask each interrupt by setting the interrupt flags (I0 and I1). The relation between the interrupt priority level of each system and interrupt flags is shown in Table 5.16.4.3, and the CPU accepts only interrupts above the level indicated by the interrupt flags.
The $\overline{\text{NMI}}$ (watchdog timer) that has level 4 priority, is always accepted regardless of the setting of the interrupt flags.

Table 5.16.4.3 Interrupt mask setting of CPU

I1	I0	Acceptable interrupt
1	1	Level 4 ($\overline{\text{NMI}}$)
1	0	Level 4, Level 3 ($\overline{\text{IRQ3}}$)
0	1	Level 4, Level 3, Level 2 ($\overline{\text{IRQ2}}$)
0	0	Level 4, Level 3, Level 2, Level 1 ($\overline{\text{IRQ1}}$)

After an interrupt has been accepted, the interrupt flags are written to the level of that interrupt. However, interrupt flags after an $\overline{\text{NMI}}$ has been accepted are written to level 3 (I0 = I1 = "1").

Table 5.16.4.4 Interrupt flags after acceptance of interrupt

Accepted interrupt priority level		I1	I0
Level 4	($\overline{\text{NMI}}$)	1	1
Level 3	($\overline{\text{IRQ3}}$)	1	1
Level 2	($\overline{\text{IRQ2}}$)	1	0
Level 1	($\overline{\text{IRQ1}}$)	0	1

The set interrupt flags are reset to their original value on return from the interrupt processing routine. Consequently, multiple interrupts up to 3 levels can be controlled by the initial settings of the interrupt priority registers alone. Additional multiplexing can be realized by rewriting the interrupt flags and interrupt enable register in the interrupt processing routine.

Note: Beware. If the interrupt flags have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

5.16.5 Exception processing vectors

When the CPU accepts an interrupt request, it starts exception processing following completion of the instruction being executed. In exception processing, the following operations branch the program.

(1) In the minimum mode, the program counter (PC) and system condition flag (SC) are moved to stack and in the maximum mode, the code bank register (CB), PC and SC are moved.

(2) The branch destination address is read from the exception processing vector corresponding to each exception processing (interrupt) factor and is placed in the PC.

An exception vector is 2 bytes of data in which the top address of each exception (interrupt) processing routine has been stored and the vector addresses correspond to the exception processing factors as shown in Table 5.16.5.1.

Table 5.16.5.1 Vector address and exception processing correspondence

Vector address	Exception processing factor	Priority
000000H	Reset	High
000002H	Zero division	↑
000004H	Watchdog timer ($\overline{\text{NMI}}$)	
000006H	Programmable timer 1 interrupt	
000008H	Programmable timer 0 interrupt	
00000AH	K10 input interrupt	
00000CH	K04–K07 input interrupt	
00000EH	K00–K03 input interrupt	
000010H	Serial I/F error interrupt	
000012H	Serial I/F receiving complete interrupt	
000014H	Serial I/F transmitting complete interrupt	
000016H	Stopwatch timer 100 Hz interrupt	
000018H	Stopwatch timer 10 Hz interrupt	
00001AH	Stopwatch timer 1 Hz interrupt	
00001CH	Clock timer 32 Hz interrupt	
00001EH	Clock timer 8 Hz interrupt	
000020H	Clock timer 2 Hz interrupt	
000022H	Clock timer 1 Hz interrupt	
000024H	A/D conversion complete interrupt	↓
000026H	Melody play complete interrupt	Low
000028H	System reserved (cannot be used)	No priority rating
00002AH : 0000FEH	Software interrupt	

Note: An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the top portion of an exception processing routine must be described within the common area (000000H–007FFFH).

5.16.6 I/O memory for interrupt

Table 5.16.6.1 shows the interrupt control bits.

Table 5.16.6.1(a) Interrupt control bits

Address	Bit	Name	Function	1	0	SR	R/W	Comment
00FF20	D7	PK01	K00–K07 interrupt priority register	PK01 PK00 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D6	PK00				0	R/W	
	D5	PSIF1	Serial interface interrupt priority register	PSIF1 PSIF0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D4	PSIF0				0	R/W	
	D3	PSW1	Stopwatch timer interrupt priority register	PSW1 PSW0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PSW0				0	R/W	
	D1	PTM1	Clock timer interrupt priority register	PTM1 PTM0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D0	PTM0				0	R/W	
00FF21	D7	–	–	–	–	–		
	D6	–	–	–	–	–		Constantly "0" when being read
	D5	–	–	–	–	–		
	D4	–	–	–	–	–		
	D3	PPT1	Programmable timer interrupt priority register	PPT1 PPT0 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D2	PPT0				0	R/W	
	D1	PK11	K10 interrupt priority register	PK11 PK10 Priority level: 1 1 Level 3; 1 0 Level 2; 0 1 Level 1; 0 0 Level 0		0	R/W	
	D0	PK10				0	R/W	
00FF22	D7	–	–	–	–	–		"0" when being read
	D6	ESW100	Stopwatch timer 100 Hz interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D5	ESW10	Stopwatch timer 10 Hz interrupt enable register			0	R/W	
	D4	ESW1	Stopwatch timer 1 Hz interrupt enable register			0	R/W	
	D3	ETM32	Clock timer 32 Hz interrupt enable register			0	R/W	
	D2	ETM8	Clock timer 8 Hz interrupt enable register			0	R/W	
	D1	ETM2	Clock timer 2 Hz interrupt enable register			0	R/W	
	D0	ETM1	Clock timer 1 Hz interrupt enable register			0	R/W	
00FF23	D7	EPT1	Programmable timer 1 interrupt enable register	Interrupt enable	Interrupt disable	0	R/W	
	D6	EPT0	Programmable timer 0 interrupt enable register			0	R/W	
	D5	EK1	K10 interrupt enable register			0	R/W	
	D4	EK0H	K04–K07 interrupt enable register			0	R/W	
	D3	EK0L	K00–K03 interrupt enable register			0	R/W	
	D2	ESERR	Serial I/F (error) interrupt enable register			0	R/W	
	D1	ESREC	Serial I/F (receiving) interrupt enable register			0	R/W	
	D0	ESTRA	Serial I/F (transmitting) interrupt enable register			0	R/W	
00FF24	D7	–	–	–	–	–		"0" when being read
	D6	FSW100	Stopwatch timer 100 Hz interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D5	FSW10	Stopwatch timer 10 Hz interrupt factor flag			0	R/W	
	D4	FSW1	Stopwatch timer 1 Hz interrupt factor flag			0	R/W	
	D3	FTM32	Clock timer 32 Hz interrupt factor flag			0	R/W	
	D2	FTM8	Clock timer 8 Hz interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FTM2	Clock timer 2 Hz interrupt factor flag			0	R/W	
	D0	FTM1	Clock timer 1 Hz interrupt factor flag			0	R/W	
00FF25	D7	FPT1	Programmable timer 1 interrupt factor flag	(R) Interrupt factor is generated	(R) No interrupt factor is generated	0	R/W	
	D6	FPT0	Programmable timer 0 interrupt factor flag			0	R/W	
	D5	FK1	K10 interrupt factor flag			0	R/W	
	D4	FK0H	K04–K07 interrupt factor flag			0	R/W	
	D3	FK0L	K00–K03 interrupt factor flag			0	R/W	
	D2	FSERR	Serial I/F (error) interrupt factor flag	(W) Reset	(W) No operation	0	R/W	
	D1	FSREC	Serial I/F (receiving) interrupt factor flag			0	R/W	
	D0	FSTRA	Serial I/F (transmitting) interrupt factor flag			0	R/W	

Table 5.16.6.1(b) Interrupt control bits

Address	Bit	Name	Function		1	0	SR	R/W	Comment
00FF28	D7	PADC1	A/D converter interrupt priority register		PADC1 PMDY1	PADC0 PMDY0	Priority level	0	R/W	
	D6	PADC0			1	1	Level 3	0	R/W	
	D5	PMDY1	Melody interrupt priority register		1	0	Level 2	0	R/W	
	D4	PMDY0			0	1	Level 1			
					0	0	Level 0	0	R/W	
	D3	–	–		–	–		–		
	D2	–	–		–	–		–		Constantly "0" when
	D1	–	–		–	–		–		being read
	D0	–	–		–	–		–		
00FF2A	D7	EAD	A/D converter interrupt enable register		Interrupt	Interrupt		0	R/W	
	D6	EMDY	Melody interrupt enable register		enable	disable		0	R/W	
	D5	–	–		–	–		–		
	D4	–	–		–	–		–		
	D3	–	–		–	–		–		Constantly "0" when
	D2	–	–		–	–		–		being read
	D1	–	–		–	–		–		
	D0	–	–		–	–		–		
00FF2C	D7	FAD	A/D converter interrupt factor flag	R	Generated	Not generated		0	R/W	
	D6	FMDY	Melody interrupt factor flag	W	Reset	No operation		0	R/W	
	D5	–	–		–	–		–		
	D4	–	–		–	–		–		
	D3	–	–		–	–		–		Constantly "0" when
	D2	–	–		–	–		–		being read
	D1	–	–		–	–		–		
	D0	–	–		–	–		–		

Refer to the explanations on the respective peripheral circuits for the setting content and control method for each bit.

5.16.7 Programming notes

(1) When executing the RETE instruction without resetting the interrupt factor flag after an interrupt has been generated, the same interrupt will be generated. Consequently, the interrupt factor flag corresponding to that routine must be reset (writing "1") in the interrupt processing routine.

(2) Beware. If the interrupt flags (I0 and I1) have been rewritten (set to lower priority) prior to resetting an interrupt factor flag after an interrupt has been generated, the same interrupt will be generated again.

(3) An exception processing vector is fixed at 2 bytes, so it cannot specify a branch destination bank address. Consequently, to branch from multiple banks to a common exception processing routine, the front portion of an exception processing routine must be described within the common area (000000H–007FFFH).

(4) Do not execute the SLP instruction for 2 msec after a $\overline{\text{NMI}}$ interrupt has occurred (when f_{OSC1} is 32.768 kHz).

5.17 Notes for Low Current Consumption

The E0C88816 can turn circuits, which consume a large amount of power, ON or OFF by control registers.
You can reduce power consumption by creating a program that operates the minimum necessary circuits using these control registers.

Next, which circuit systems' operation can be controlled and their control registers (instructions) are explained. You should refer to these when programming.

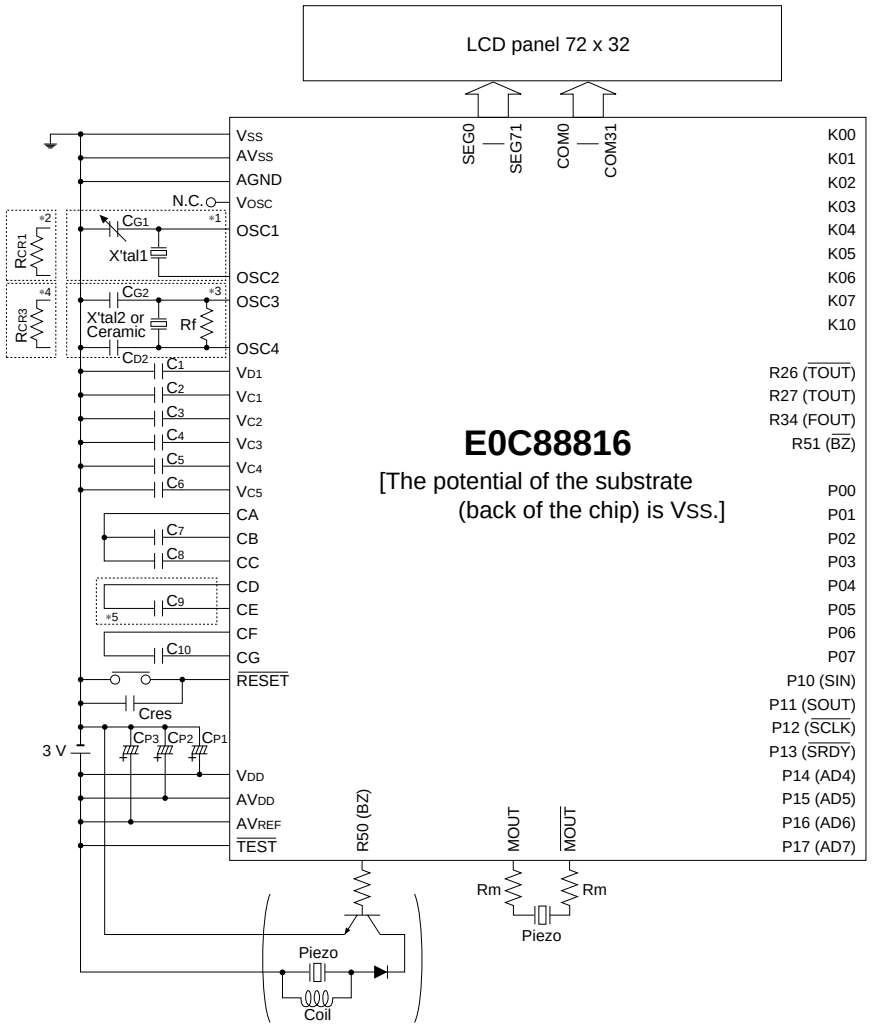
See Chapter 7, "ELECTRICAL CHARACTERISTICS" for the current consumption.

Table 5.17.1 Circuit systems and control registers

Circuit type	Control register (Instruction)	Status at time of initial resetting
CPU	HALT and SLP instructions	Operation status
Oscillation circuit	CLKCHG, OSCC	OSC1 clock (CLKCHG = "0") OSC3 oscillation OFF (OSCC = "0")
Operating mode	VDC0, VDC1	Normal mode (VDC0 = VDC1 = "0")
LCD controller	LCDC0, LCDC1	Drive OFF (LCDC0 = LCDC1 = "0")
SVD circuit	SVDON, SVDSP	OFF status (SVDON = SVDSP = "0")

6 BASIC EXTERNAL WIRING DIAGRAM

● When V_{C2} standard and 1/5 bias are selected



Recommended values for external parts

Symbol	Name	Recommended value
X'tal1	Crystal oscillator	32.768 kHz, CI(Max.)=35 kΩ
C_{G1}	Trimmer capacitor	5–30 pF
R_{CR1}	Resistor for CR oscillation	1 MΩ
X'tal2	Crystal oscillator	4 MHz
Ceramic	Ceramic oscillator	4 MHz
Rf	Feedback resistor	1 MΩ
C_{G2}	Gate capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
C_{D2}	Drain capacitor	15 pF (Crystal oscillator) 30 pF (Ceramic oscillator)
R_{CR3}	Resistor for CR oscillation	20 kΩ

Symbol	Name	Recommended value
C_1	Capacitor between V_{SS} and V_{D1}	0.1 µF
C_2	Capacitor between V_{SS} and V_{C1}	0.1 µF
C_3	Capacitor between V_{SS} and V_{C2}	0.1 µF
C_4	Capacitor between V_{SS} and V_{C3}	0.1 µF
C_5	Capacitor between V_{SS} and V_{C4}	0.1 µF
C_6	Capacitor between V_{SS} and V_{C5}	0.1 µF
C_7–C_{10}	Booster/reducer capacitors	0.1 µF
C_{P1}–C_{P3}	Capacitors for power supply	3.3 µF
Cres	Capacitor for $\overline{\text{RESET}}$ terminal	0.47 µF
Rm	Protective resistors for piezo	100 Ω

∗ The connection diagram shown above is an example of when mask option settings are as follows:
LCD power source: Internal power supply, $\overline{\text{RESET}}$ terminal: With pull-up resistor,
R51 specification: General-purpose output port

∗1 OSC1 = Crystal oscillation, ∗2 OSC1 = CR oscillation, ∗3 OSC3 = Crystal / Ceramic oscillation,
∗4 OSC3 = CR oscillation, ∗5 Unnecessary for 1 / 4 bias drive

Note: The above table is simply an example. Refer to Chapter 7, "ELECTRICAL CHARACTERISTICS", for detailed characteristics.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(V_{SS} = 0 V)

Item	Symbol	Condition	Rated value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	1
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	2
Operating temperature	Topr		-40 to +85	°C	
Storage temperature	Tstg		-65 to +150	°C	
Soldering temperature / time	Tsol		260°C, 10sec (lead section)	–	

Note) 1 Case that to Nch open drain output by the mask option is included.
2 In case of plastic package.

7.2 Recommended Operating Conditions

(V_{SS} = 0 V, Ta = -40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal mode)	V_{DD}		2.4		5.5	V	
Operating power voltage (Low power mode)	V_{DD}		1.8		5.5	V	
Operating power voltage (High speed mode)	V_{DD}		3.5		5.5	V	
Analog power voltage	AV_{DD}	$AV_{DD} \geq 2.7$ V	V_{DD}-0.05		V_{DD}+0.05	V	
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		4.2	MHz	1
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	1
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	1
	f_{OSC3}		0.03		8.2	MHz	1
Liquid crystal power voltage	V_{C5}	$V_{C5} \geq V_{C4} \geq V_{C3} \geq V_{C2} \geq V_{C1} \geq V_{SS}$			6.0	V	2
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3
Capacitor between CF and CG	C_{10}			0.1		µF	3

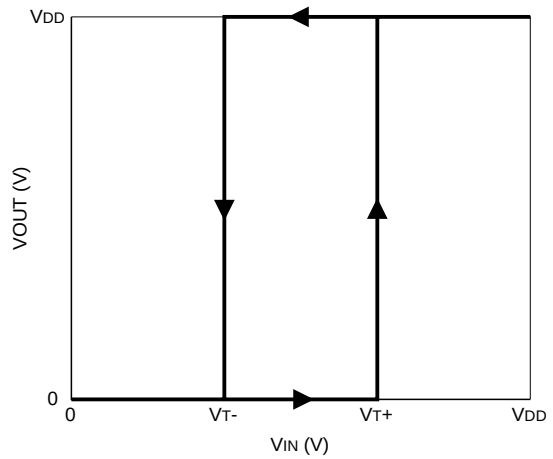
Note) 1 When an external clock is input from the OSC1 terminal by the mask option, leave the OSC2 terminal open, and when an external clock is input from the OSC3 terminal, leave the OSC4 terminal open.
2 When external power supply is selected by the mask option.
3 When LCD drive power is not used, the capacitor is not necessary.
In this case, leave the V_{C1} to V_{C5} and CA to CG terminals open.

7.3 DC Characteristics

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage (1)	V_{IH1}	Kxx, Pxx	0.8V_{DD}		V_{DD}	V	
Low level input voltage (1)	V_{IL1}	Kxx, Pxx,	0		0.2V_{DD}	V	
High level input voltage (2) (Normal mode)	V_{IH2}	OSC3	1.6		V_{DD}	V	1
High level input voltage (2)	V_{IH2}	OSC1	1.0		V_{DD}	V	1
High level input voltage (2) (High speed mode)	V_{IH2}	OSC3	2.4		V_{DD}	V	1
Low level input voltage (2) (Normal mode)	V_{IL2}	OSC3	0		0.6	V	1
Low level input voltage (2)	V_{IL2}	OSC1	0		0.3	V	1
Low level input voltage (2) (High speed mode)	V_{IL2}	OSC3	0		0.9	V	1
High level schmitt input voltage	V_{T+}	$\overline{RESET}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{RESET}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, V_{OH} = 0.9 V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, V_{OL} = 0.1 V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, $\overline{RESET}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, $\overline{RESET}$	100	300	500	kΩ	2
Input terminal capacitance	C_{IN}	Kxx, Pxx V_{IN} = 0 V, f = 1 MHz, Ta = 25°C		7	15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1 V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1 V	5			µA	

Note) 1 When external clock is selected by mask option.
2 When pull-up resistor is added by mask option.



7.4 Analog Circuit Characteristics

■ LCD drive circuit

The Typ. values of the LCD drive voltage shown in the following table shift in difference of panel load (panel size, drive duty, display segment number, display pattern). Therefore, these should be evaluated by connecting to the actual panel to be used. See "7.9 Characteristics Curves" for the load characteristics.

Unless otherwise specified: V_{DD} = V_{C2} (LCX = FH) + 0.1 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, C_1–C_{10} = 0.1 µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage (V_{C2} standard)	V_{C2}	When 1 MΩ load resistor is connected between V_{SS} and V_{C2} (no panel load)			0.412V_{C5}		V	
	V_{C5} TYPE A (4.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	3.52	Typ×1.06	V	1
			LCX = 1H		3.64		V	
			LCX = 2H		3.76		V	
			LCX = 3H		3.88		V	
			LCX = 4H		4.00		V	
			LCX = 5H		4.12		V	
			LCX = 6H		4.24		V	
			LCX = 7H		4.37		V	
			LCX = 8H		4.51		V	
			LCX = 9H		4.63		V	
			LCX = AH		4.75		V	
			LCX = BH		4.87		V	
			LCX = CH		5.00		V	
			LCX = DH		5.12		V	
			LCX = EH		5.24		V	
			LCX = FH		5.36		V	
	V_{C5} TYPE B (5.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	4.20	Typ×1.06	V	1
			LCX = 1H		4.34		V	
			LCX = 2H		4.49		V	
			LCX = 3H		4.63		V	
			LCX = 4H		4.78		V	
			LCX = 5H		4.92		V	
			LCX = 6H		5.07		V	
			LCX = 7H		5.21		V	
			LCX = 8H		5.36		V	
			LCX = 9H		5.50		V	
			LCX = AH		5.65		V	
			LCX = BH		5.80		V	
			LCX = CH		5.94		V	
			LCX = DH		6.09		V	
			LCX = EH		6.23		V	
			LCX = FH		6.38		V	
LCD drive voltage (V_{C1} standard)	V_{C1}	When 1 MΩ load resistor is connected between V_{SS} and V_{C1} (no panel load)			0.260V_{C5}		V	
	V_{C5} TYPE A (4.5V)	When 1 MΩ load resistor is connected between V_{SS} and V_{C5} (no panel load)	LCX = 0H	Typ×0.94	3.80	Typ×1.06	V	1
			LCX = 1H		3.88		V	
			LCX = 2H		3.96		V	
			LCX = 3H		4.03		V	
			LCX = 4H		4.15		V	
			LCX = 5H		4.22		V	
			LCX = 6H		4.30		V	
			LCX = 7H		4.38		V	
			LCX = 8H		4.45		V	
			LCX = 9H		4.53		V	
			LCX = AH		4.65		V	
			LCX = BH		4.72		V	
			LCX = CH		4.80		V	
			LCX = DH		4.88		V	
			LCX = EH		4.95		V	
			LCX = FH		5.07		V	

Note) 1 Fixing the LCD contrast is not recommended. A contrast adjustment function should be included in the software.

■ SVD circuit

Unless otherwise specified: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0	Typ×0.92	1.82	Typ×1.08	V	1
		Level 2 → Level 1		2.00		V	1
		Level 3 → Level 2		2.18		V	1
		Level 4 → Level 3		2.36		V	2
		Level 5 → Level 4		2.54		V	2
		Level 6 → Level 5		2.72		V	2
		Level 7 → Level 6		2.90		V	3
		Level 8 → Level 7		3.08		V	3
		Level 9 → Level 8		3.26		V	3
		Level 10 → Level 9	Typ×0.88	3.45	Typ×1.12	V	4
		Level 11 → Level 10		3.65		V	4
		Level 12 → Level 11		3.85		V	4
		Level 13 → Level 12		4.00		V	4
		Level 14 → Level 13		4.15		V	4
		Level 15 → Level 14		4.35		V	4

$V_{SVD\ (Level\ 0)} < V_{SVD\ (Level\ 1)} < V_{SVD\ (Level\ 2)} < V_{SVD\ (Level\ 3)} < V_{SVD\ (Level\ 4)} < V_{SVD\ (Level\ 5)} < V_{SVD\ (Level\ 6)} < V_{SVD\ (Level\ 7)}$
$< V_{SVD\ (Level\ 8)} < V_{SVD\ (Level\ 9)} < V_{SVD\ (Level\ 10)} < V_{SVD\ (Level\ 11)} < V_{SVD\ (Level\ 12)} < V_{SVD\ (Level\ 13)} < V_{SVD\ (Level\ 14)} < V_{SVD\ (Level\ 15)}$

Note) 1 Low power operating mode only
2 Low power operating mode or Normal operating mode only
3 Normal operating mode only
4 Normal operating mode or High speed operating mode only

7.5 Power Current Consumption

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C, OSC1 = 32.768 kHz crystal oscillation, C_G = 25 pF, OSC3 = crystal/ceramic oscillation, Non heavy load protection mode, C_1–C_{10} = 0.1 µF, No panel load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status *1		0.45	1.6	µA	
	I_{DD2}	In HALT status *2		1.5	3.5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		7	10	µA	
	I_{DD4}	CPU is in operating (4 MHz) *4		0.9	1.1	mA	
Power current (Low power mode)	I_{DD1}	In SLEEP status *1		0.30	1	µA	
	I_{DD2}	In HALT status *2		1	2.5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		5	7	µA	
Power current (High speed mode)	I_{DD1}	In SLEEP status *1		1	3	µA	
	I_{DD2}	In HALT status *2		2	5	µA	
	I_{DD3}	CPU is in operating (32.768 kHz) *3		12	16	µA	
	I_{DD4}	CPU is in operating (8 MHz) *5		3.3	3.9	mA	
LCD drive circuit current	I_{LCDN}			6	10	µA	1
	I_{LCDH}	In heavy load protection mode		37	45	µA	2
SVD circuit current	I_{SVDN}	V_{DD} = 3.0 V		27	40	µA	3
OSC1 CR oscillation current (R_{CR1} = 500 kΩ)	I_{CR1}	In HALT status (50 kHz)		10	15	µA	4

*1 OSC1: Stop, OSC3 = Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status

*2 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: HALT status, Clock timer: Operating, Others: Stop status

*3 OSC1: Oscillating, OSC3 = Stop, CPU, ROM, RAM: Operating in 32.768 kHz, Clock timer: Operating, Others: Stop status

*4 OSC1: Oscillating, OSC3 = Oscillating, CPU, ROM, RAM: Operating in 4 MHz, Clock timer: Operating, Others: Stop status
See "7.9 Characteristics Curves" for current consumption with an operating frequency other than 4 MHz.

*5 OSC1: Oscillating, OSC3 = Oscillating, CPU, ROM, RAM: Operating in 8 MHz, Clock timer: Operating, Others: Stop status
See "7.9 Characteristics Curves" for current consumption with an operating frequency other than 8 MHz.

Note) 1 The LCD drive circuit current varies according to the display patterns.

2 Heavy load protection circuit current in heavy load protection mode
When the OSC3 oscillation circuit is turned ON, the IC always enters heavy load protection mode.
The mode while the buzzer or melody signals are being output can be selected by mask option. When using a bipolar transistor as the example of the R50 terminal shown in "6 BASIC EXTERNAL WIRING DIAGRAM", select heavy load protection mode. When direct driving a piezoelectric buzzer as the example of the MOUT and /MOUT terminals, select normal mode.

3 The value in ***x*** V can be found by the following expression: I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 20) - 30 (Typ. value),
I_{SVDN} (V_{DD} = ***x*** V) = (***x*** × 30) - 30 (Max. value)

4 When OSC1 CR oscillation circuit is selected by the mask option.

7.6 AC Characteristics

■ External memory access

Condition: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency (Normal mode)	f_{OSC1}	V_{DD} = 2.4 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		4.2	MHz	
Operating frequency (Low power mode)	f_{OSC1}	V_{DD} = 1.8 to 5.5 V	30.000	32.768	80.000	kHz	
Operating frequency (High speed mode)	f_{OSC1}	V_{DD} = 3.5 to 5.5 V	30.000	32.768	80.000	kHz	
	f_{OSC3}		0.03		8.2	MHz	
Instruction execution time (during operation with OSC1 clock)	tcy	1-cycle instruction	25	61	67	µS	
		2-cycle instruction	50	122	133	µS	
		3-cycle instruction	75	183	200	µS	
		4-cycle instruction	100	244	267	µS	
		5-cycle instruction	125	305	333	µS	
		6-cycle instruction	150	366	400	µS	
Instruction execution time Normal mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.5		66.7	µS	
		2-cycle instruction	1.0		133.3	µS	
		3-cycle instruction	1.4		200.0	µS	
		4-cycle instruction	1.9		266.7	µS	
		5-cycle instruction	2.4		333.3	µS	
		6-cycle instruction	2.9		400.0	µS	
Instruction execution time High speed mode (during operation with OSC3 clock)	tcy	1-cycle instruction	0.2		66.7	µS	
		2-cycle instruction	0.5		133.3	µS	
		3-cycle instruction	0.7		200.0	µS	
		4-cycle instruction	1.0		266.7	µS	
		5-cycle instruction	1.2		333.3	µS	
		6-cycle instruction	1.5		400.0	µS	

■ Serial interface

• Clock synchronous master mode (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			200	nS	
Receiving data input set-up time	tsms	500			nS	
Receiving data input hold time	tsmh	200			nS	

• Clock synchronous master mode (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			100	nS	
Receiving data input set-up time	tsms	250			nS	
Receiving data input hold time	tsmh	100			nS	

• Clock synchronous master mode (Low power operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tsmd			5	µS	
Receiving data input set-up time	tsms	10			µS	
Receiving data input hold time	tsmh	5			µS	

• Clock synchronous slave mode (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			500	nS	
Receiving data input set-up time	tsss	200			nS	
Receiving data input hold time	tssh	200			nS	

• Clock synchronous slave mode (High speed operating mode)

Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			250	nS	
Receiving data input set-up time	tsss	100			nS	
Receiving data input hold time	tssh	100			nS	

• Clock synchronous slave mode (Low power operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, V_{OL} = 0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitting data output delay time	tssd			10	µS	
Receiving data input set-up time	tsss	5			µS	
Receiving data input hold time	tssh	5			µS	

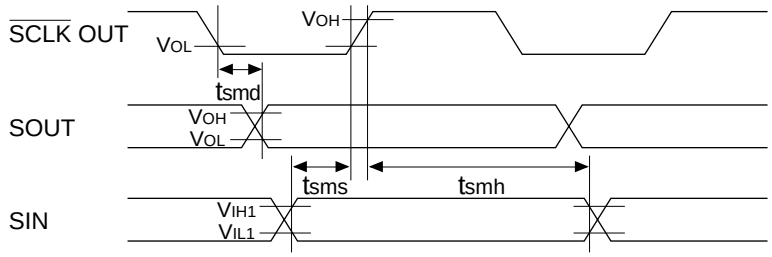
• Asynchronous system (All operating mode)

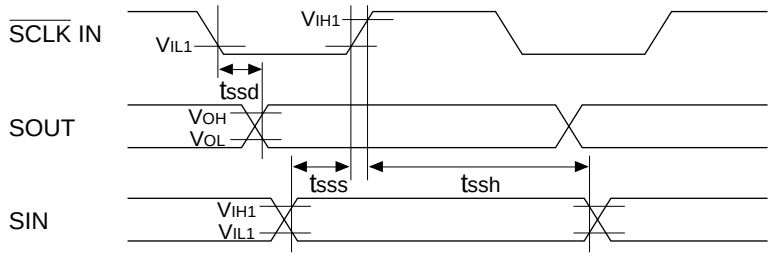
Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

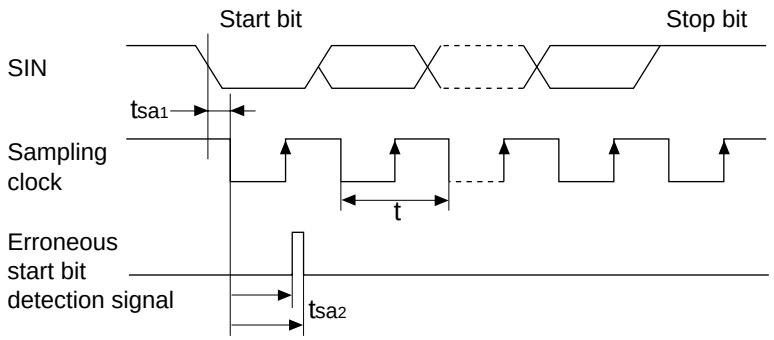
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Start bit detection error time	t_{sa1}	0		t/16	S	1
Erroneous start bit detection range time	t_{sa2}	9t/16		10t/16	S	2

Note) 1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started.
When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)







■ Input clock

• OSC1, OSC3 external clock (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 1.6 V, V_{IL2} = 0.6 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	250		32,000	nS	
	"H" pulse width	t_{O3H}	125		16,000	nS	
	"L" pulse width	t_{O3L}	125		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1, OSC3 external clock (High speed operating mode)

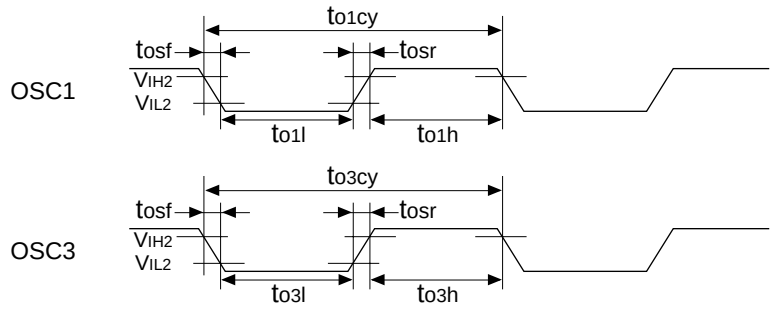
Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 2.4 V, V_{IL2} = 0.9 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
OSC3 input clock time	Cycle time	t_{O3CY}	125		32,000	nS	
	"H" pulse width	t_{O3H}	62.5		16,000	nS	
	"L" pulse width	t_{O3L}	62.5		16,000	nS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	

• OSC1 external clock (Low power operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH2} = 1.0 V, V_{IL2} = 0.3 V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
OSC1 input clock time	Cycle time	t_{O1CY}	12		32	µS	
	"H" pulse width	t_{O1H}	6		16	µS	
	"L" pulse width	t_{O1L}	6		16	µS	
Input clock rising time		t_{OSR}			25	nS	
Input clock falling time		t_{OSF}			25	nS	



• $\overline{SCLK}$, EVIN input clock (Normal operating mode)

Condition: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	4			µS	
	"H" pulse width	tsch	2			µS	
	"L" pulse width	tscl	2			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	4			µS	
	"H" pulse width	tevh	2			µS	
	"L" pulse width	tevl	2			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{SCLK}$, EVIN input clock (High speed operating mode)

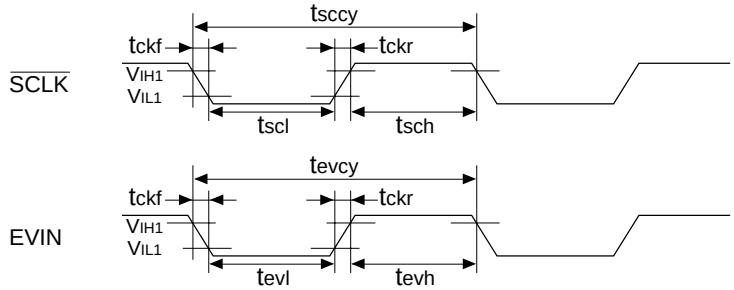
Condition: V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	2			µS	
	"H" pulse width	tsch	1			µS	
	"L" pulse width	tscl	1			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	2			µS	
	"H" pulse width	tevh	1			µS	
	"L" pulse width	tevl	1			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	

• $\overline{SCLK}$, EVIN input clock (Low power operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH1} = 0.8V_{DD}, V_{IL1} = 0.2V_{DD}

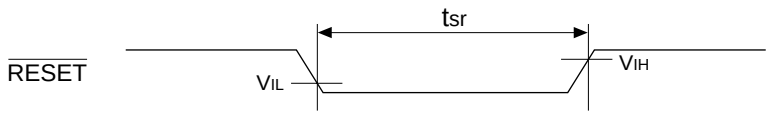
Item		System	Min.	Typ.	Max.	Unit	Note
$\overline{SCLK}$ input clock time	Cycle time	tsccy	100			µS	
	"H" pulse width	tsch	50			µS	
	"L" pulse width	tscl	50			µS	
EVIN input clock time (With noise rejector)	Cycle time	tevcy	64 / f_{OSC1}			S	
	"H" pulse width	tevh	32 / f_{OSC1}			S	
	"L" pulse width	tevl	32 / f_{OSC1}			S	
EVIN input clock time (Without noise rejector)	Cycle time	tevcy	100			µS	
	"H" pulse width	tevh	50			µS	
	"L" pulse width	tevl	50			µS	
Input clock rising time		tckr			25	nS	
Input clock falling time		tckf			25	nS	



• $\overline{\text{RESET}}$ input clock (All operating mode)

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C, V_{IH} = 0.5V_{DD}, V_{IL} = 0.1V_{DD}

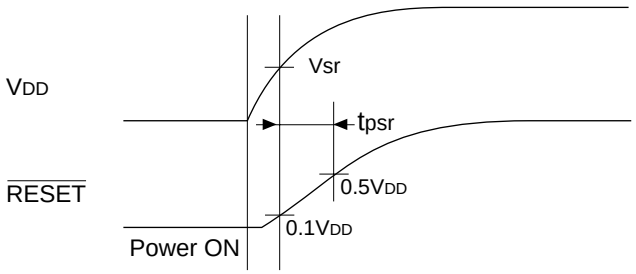
Item	Symbol	Min.	Typ.	Max.	Unit	Note
$\overline{\text{RESET}}$ input time	tsr	100			µS	

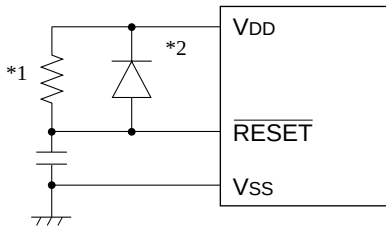


■ Power ON reset

Condition: V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating power voltage	Vsr	2.4			V	
$\overline{\text{RESET}}$ input time	tpsr	10			mS	





*1 When the built-in pull up resistor is not used.

*2 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

■ Operating mode switching

Condition: V_{DD} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Stabilization time	tvdc	5			mS	1

Note) 1 Stabilization time is the time from switching on the operating mode until operating mode is stabilized. For example, when turning the OSC3 oscillation circuit on, stabilization time is needed after the operating mode is switched on.

7.7 Oscillation Characteristics

Oscillation characteristics change depending on conditions (board pattern, components used, etc.). Use the following characteristics as reference values. In particular, when a ceramic oscillator is used for OSC3, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance. The oscillation start time is important because it becomes the wait time when OSC3 clock is used. (If OSC3 is used as CPU clock before oscillation stabilizes, the CPU may malfunction.)

■ OSC1 (Crystal)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = C2-TYPE*, C_{G1} = 25 pF (external), C_{D1} = Built-in

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	S	
External gate capacitance	C_{G1}	Including board capacitance	5		30	pF	1
Built-in gate capacitance	C_{G1}	In case of the chip		12		pF	2
Built-in drain capacitance	C_{D1}	In case of the chip		12		pF	
Frequency/IC deviation	∂f/∂IC	V_{DD} = constant	-10		10	ppm	
Frequency/power voltage deviation	∂f/∂V				1	ppm/V	
Frequency adjustment range	∂f/∂C_G	V_{DD} = constant, C_G = 5 to 30 pF	25	55		ppm	1
Frequency/operating mode deviation	∂f/∂MD	V_{DD} = constant			20	ppm	

* C2-TYPE Made by Seiko Epson corporation

Note) 1 When crystal oscillation (external gate capacitor type) is selected by mask option.
2 When crystal oscillation (gate capacitor built-in type) is selected by mask option.

■ OSC1 (CR)

Unless otherwise specified: V_{DD} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time	tsta				3	mS	
Frequency/IC deviation	∂f/∂IC	R_{CR} = constant	-25		25	%	

■ OSC3 (Crystal)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Crystal oscillator = CA-301 4MHz / CA-301 8MHz*, R_F = 1 MΩ, C_{G2} = C_{D2} = 15 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz crystal oscillator			20	mS	1
Oscillation start time (High speed mode)	tsta	8.0 MHz crystal oscillator			20	mS	1

* CA-301 4MHz / CA-301 8MHz Made by Seiko Epson corporation

Note) 1 The crystal oscillation start time changes by the crystal oscillator to be used, C_{G2} and C_{D2}.

■ OSC3 (Ceramic)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = 25°C,
Ceramic oscillator = CSA4.00MG / CSA8.00MTZ*, R_F = 1 MΩ, C_{G2} = C_{D2} = 30 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta	4.0 MHz ceramic oscillator			5	mS	
Oscillation start time (High speed mode)	tsta	8.0 MHz ceramic oscillator			5	mS	

* CSA4.00MG / CSA8.00MTZ Made by Murata Mfg. corporation

■ OSC3 (CR)

Unless otherwise specified: V_{DD} = Within the operating voltage in each operating mode, V_{SS} = 0 V, Ta = -40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Oscillation start time (Normal mode)	tsta				1	mS	
Oscillation start time (High speed mode)	tsta				1	mS	
Frequency/IC deviation (Normal mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	
Frequency/IC deviation (High speed mode)	∂f/∂IC	R_{CR} = constant	-25		25	%	

7.8 A/D Converter Characteristics

The following characteristics apply to the plastic package model only.

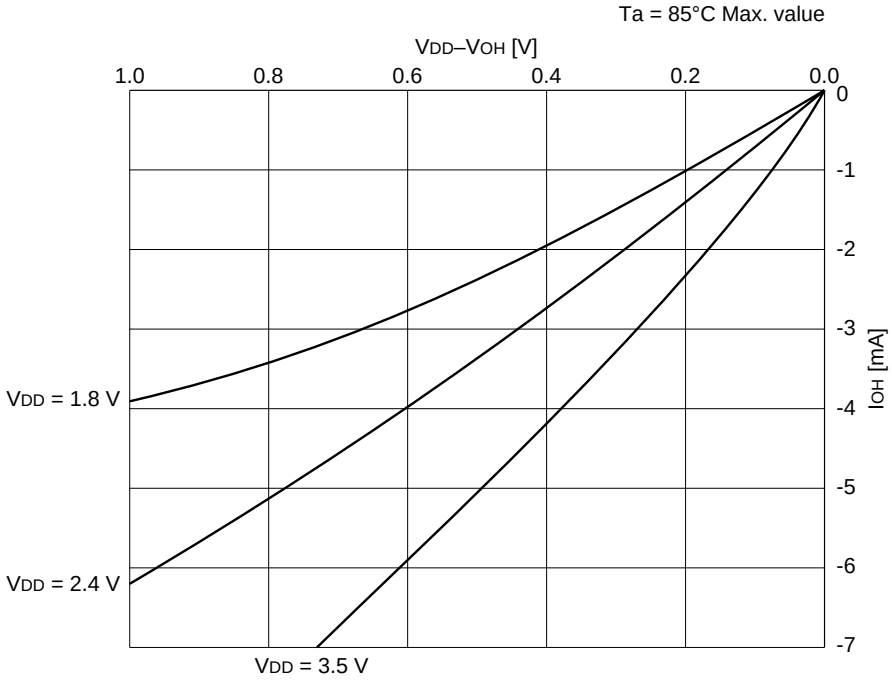
Unless otherwise specified: V_{DD} = AV_{DD} = AV_{REF} = 5.0 V, V_{SS} = AV_{SS} = AGND = 0 V, f_{OSC1} = 32.768 kHz, f_{OSC3} = 4.0 MHz, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Zero-scale error	Ezs	V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 5.5 V, ADCLK = 2 MHz, Ta = 25°C	-1.50		1.50	LSB	
Full-scale error	Efs		-1.50		1.50	LSB	
Non-linearity error	El		-1.50		1.50	LSB	
Total error	Et		-3.00		3.00	LSB	
A/D converter current consumption	I_{AD}	V_{DD} = AV_{DD} = AV_{REF} = 3.0 V, ADCLK = 2 MHz, Ta = 25°C AV_{REF} and ADCLK divider current not included		0.50	1.00	mA	
		V_{DD} = AV_{DD} = AV_{REF} = 5.0 V, ADCLK = 2 MHz, Ta = 25°C AV_{REF} and ADCLK divider current not included		1.80	3.50	mA	
Input clock frequency	f	V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.0 V, Ta = 25°C			2	MHz	
		V_{DD} = AV_{DD} = AV_{REF} = 3.0 to 5.5 V, Ta = 25°C			4	MHz	

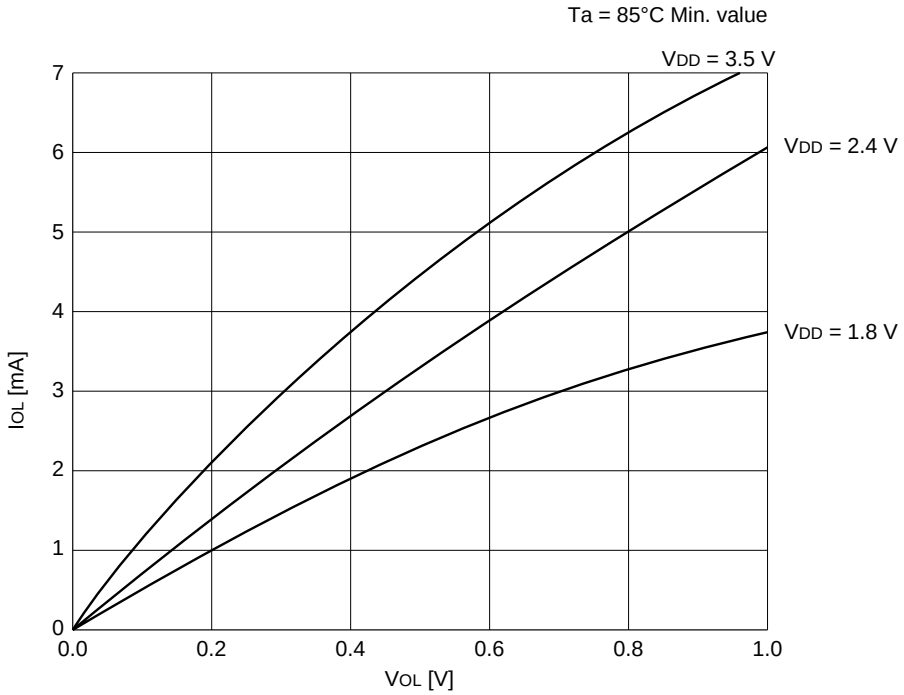
* Zero-scale error: Ezs = deviation from the ideal value at zero point
* Full-scale error: Efs = deviation from the ideal value at the full scale point
* Non-linearity error: El = deviation of the real conversion curve from the end point line
* Total error: Et = max(Ezs, Efs, Eabs), Eabs = deviation from the ideal line (including quantization error)

7.9 Characteristics Curves (reference value)

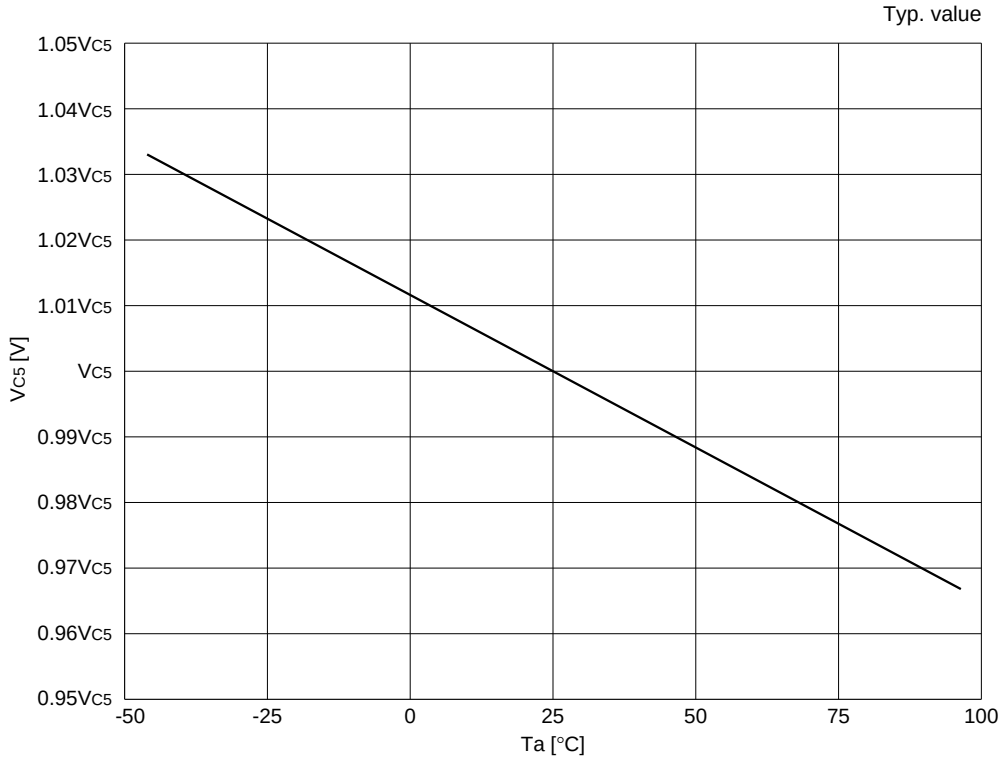
■ High level output current-voltage characteristic



■ Low level output current-voltage characteristic

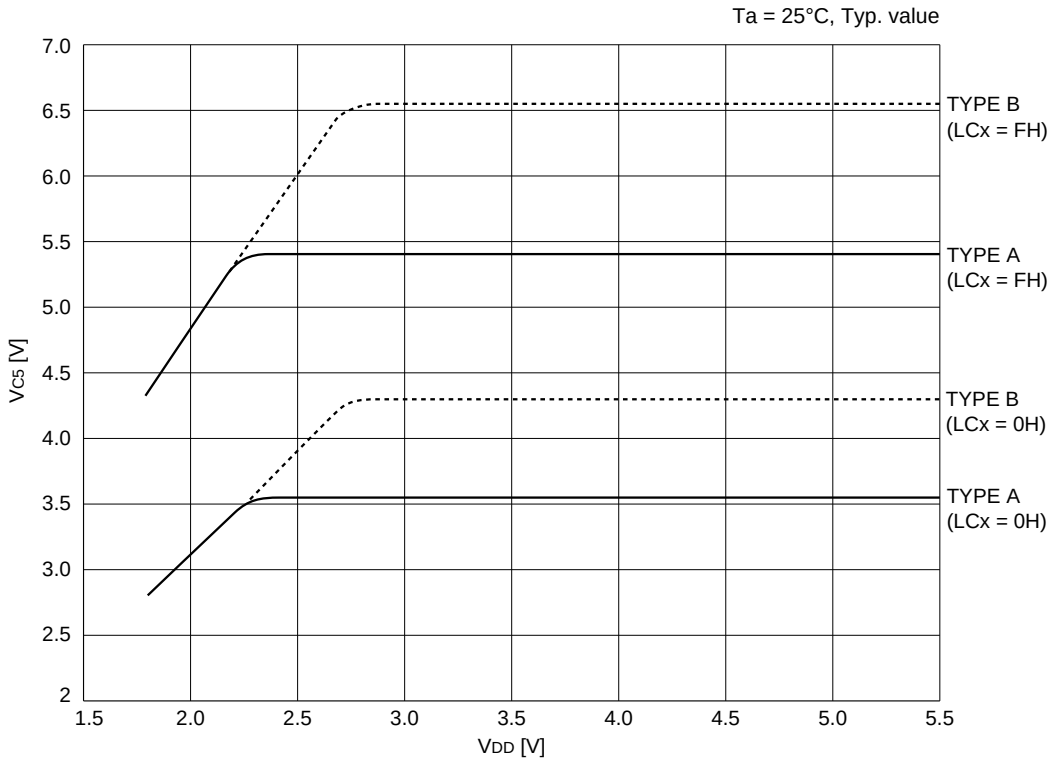


■ LCD drive voltage-ambient temperature characteristic

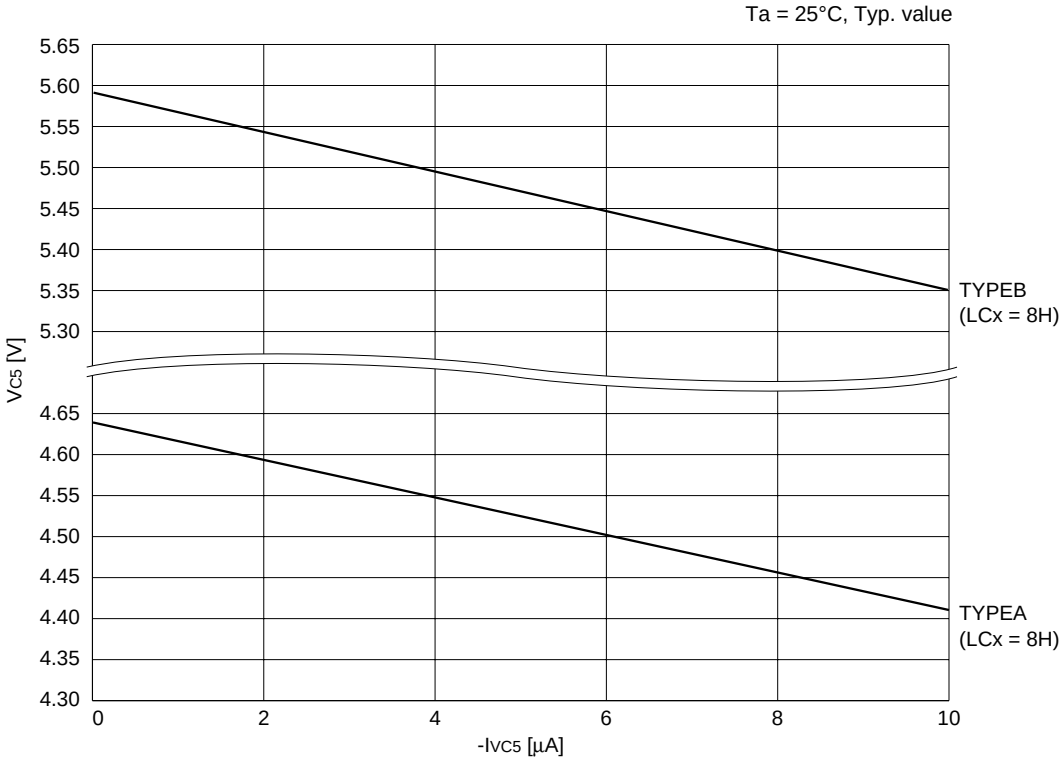


■ LCD drive voltage-supply voltage characteristic

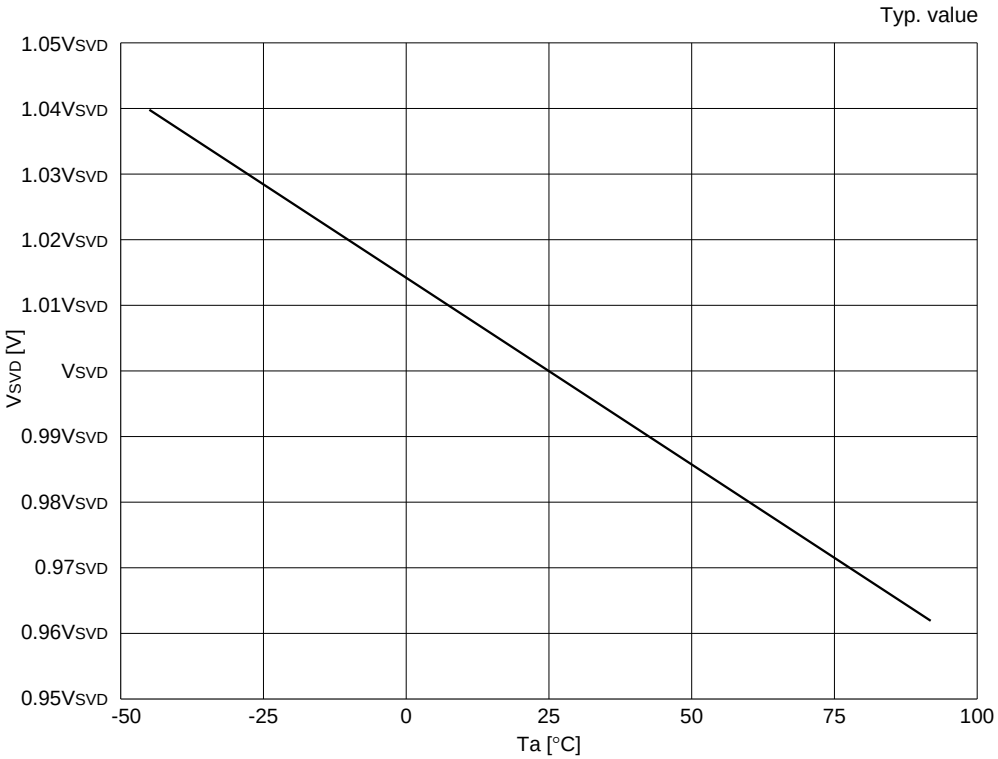
When 1 MΩ load resistor is connected between VSS and VC5 (no panel load)



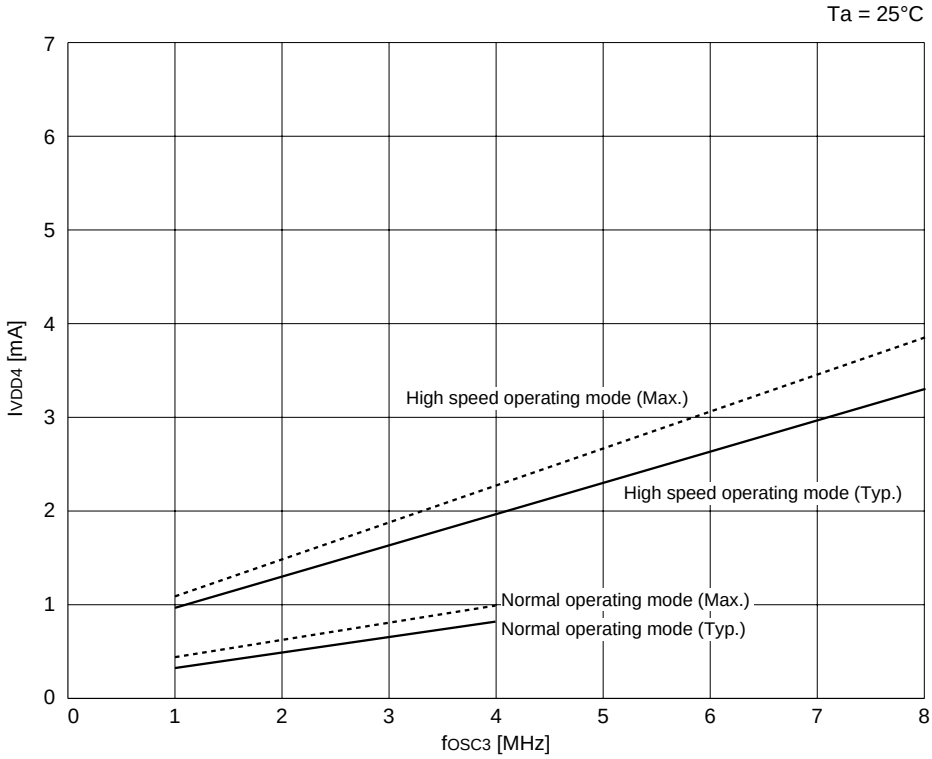
■ LCD drive voltage-load characteristic



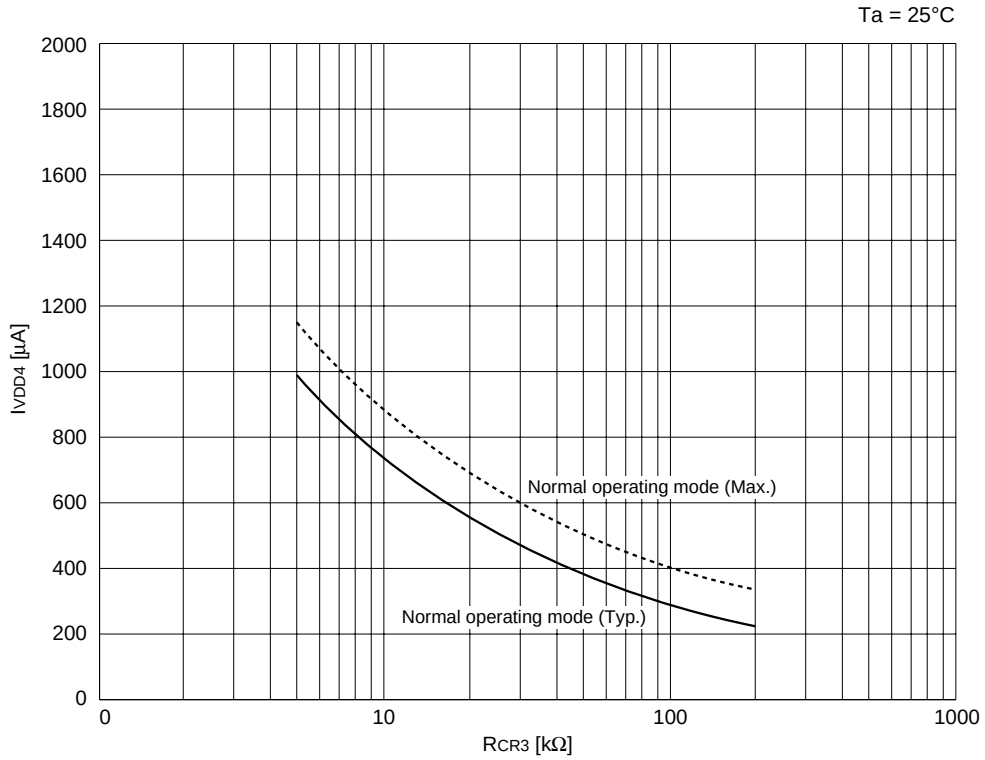
■ SVD voltage-ambient temperature characteristic



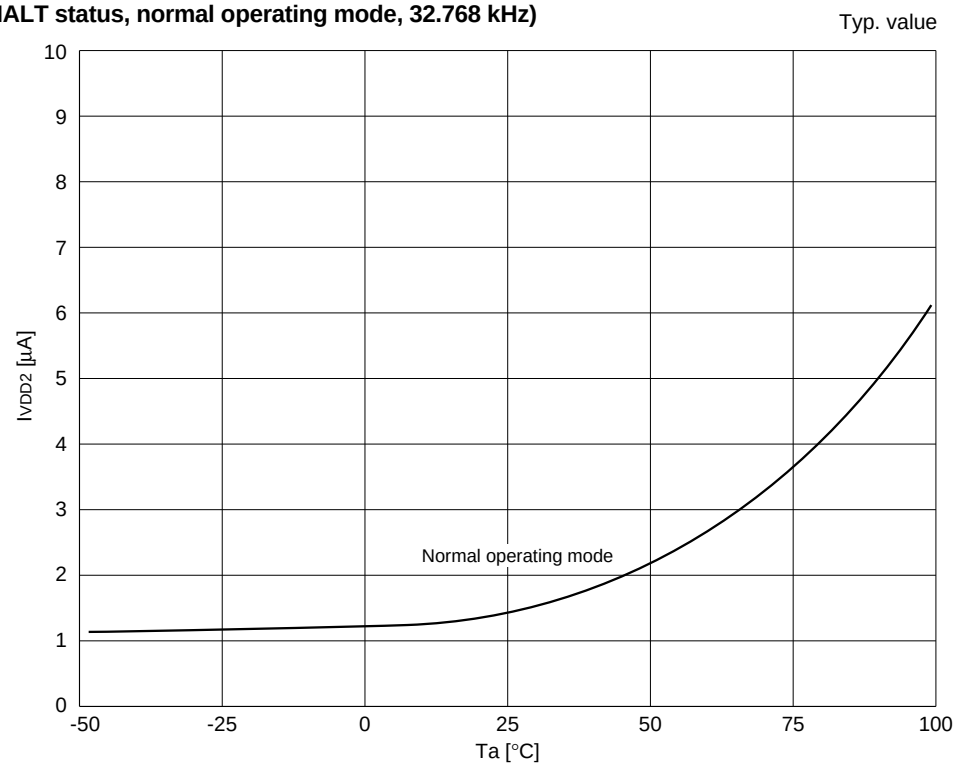
■ Power current (CPU is in operating) <OSC3 crystal/ceramic oscillation>



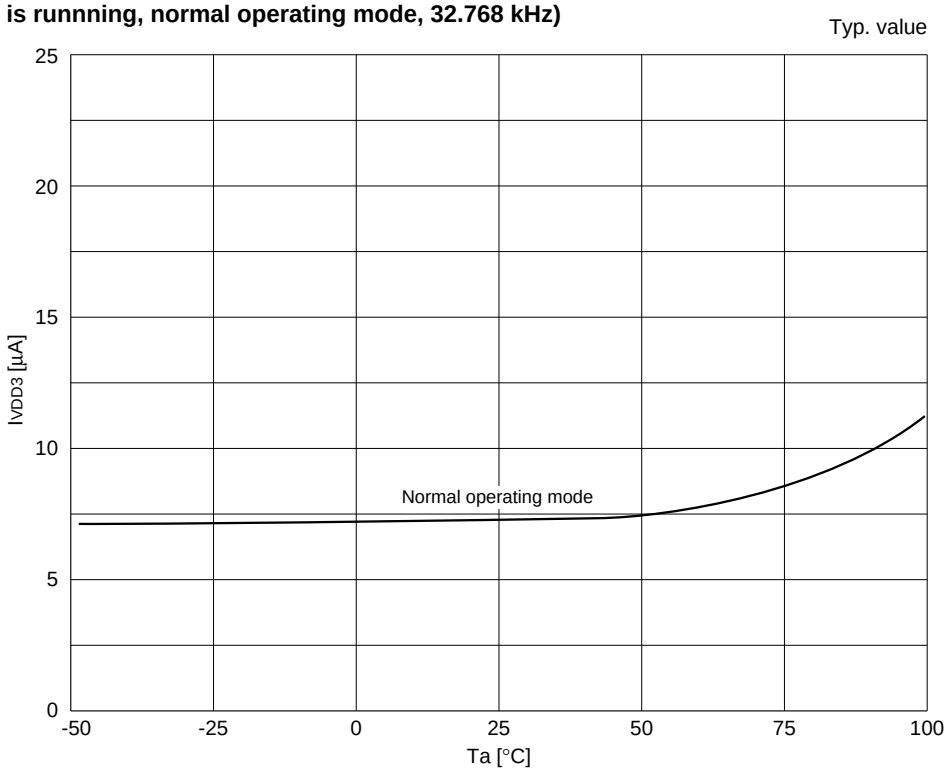
■ Power current (CPU is in operating) <OSC3 CR oscillation>



■ Power current-ambient temperature characteristic
(In HALT status, normal operating mode, 32.768 kHz)



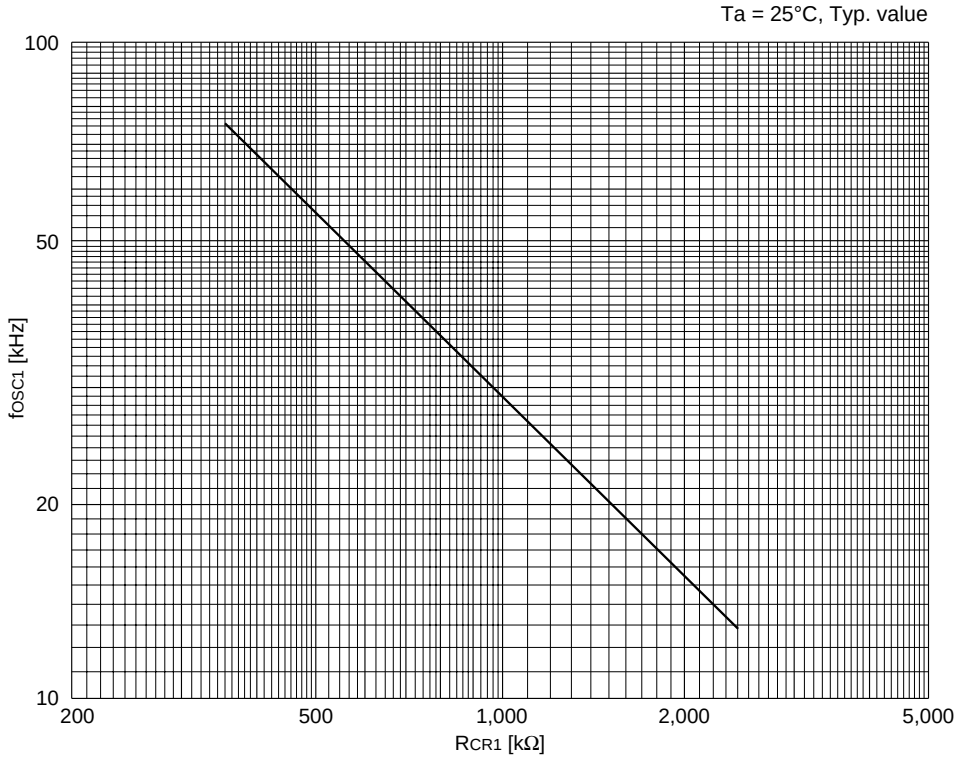
■ Power current-ambient temperature characteristic
(CPU is runnning, normal operating mode, 32.768 kHz)



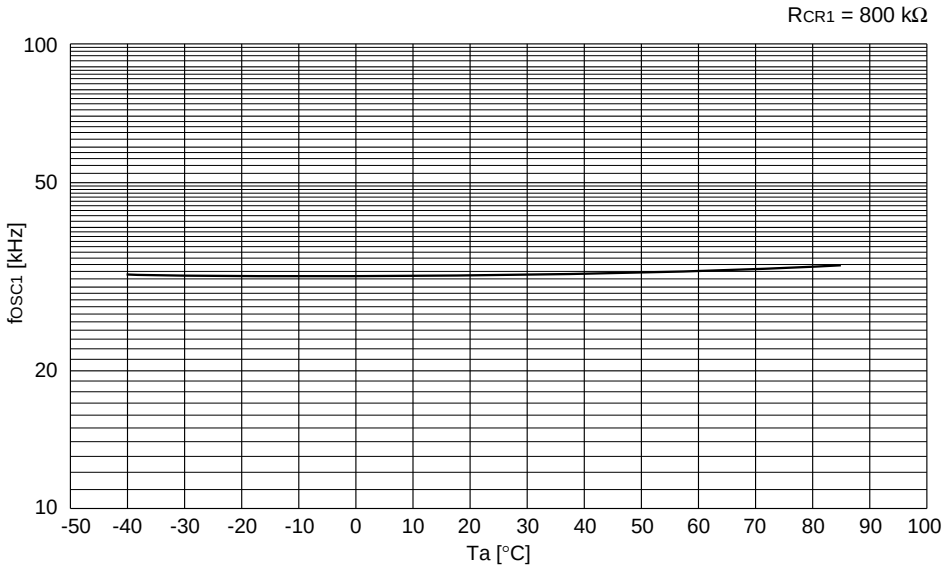
■ CR oscillation frequency characteristic

Note: Oscillation frequency changes depending on the conditions (components used, board pattern, etc.). In particular, the OSC3 oscillation frequency changes extensively depending on the product form (chip, plastic package or ceramic package) and board capacitance. Therefore, use the following charts for reference only and select the resistance value after evaluating the actual product. (The resistance value should be set to $R_{CR3} \geq 15$ kΩ.)

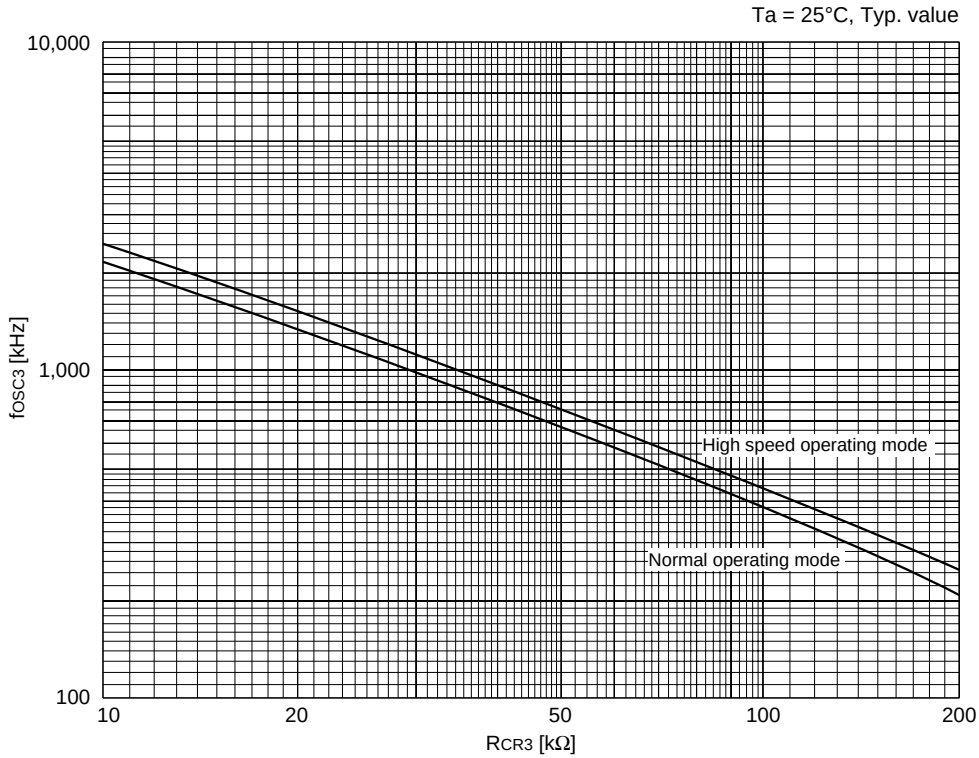
• Oscillation frequency resistor characteristic (OSC1)



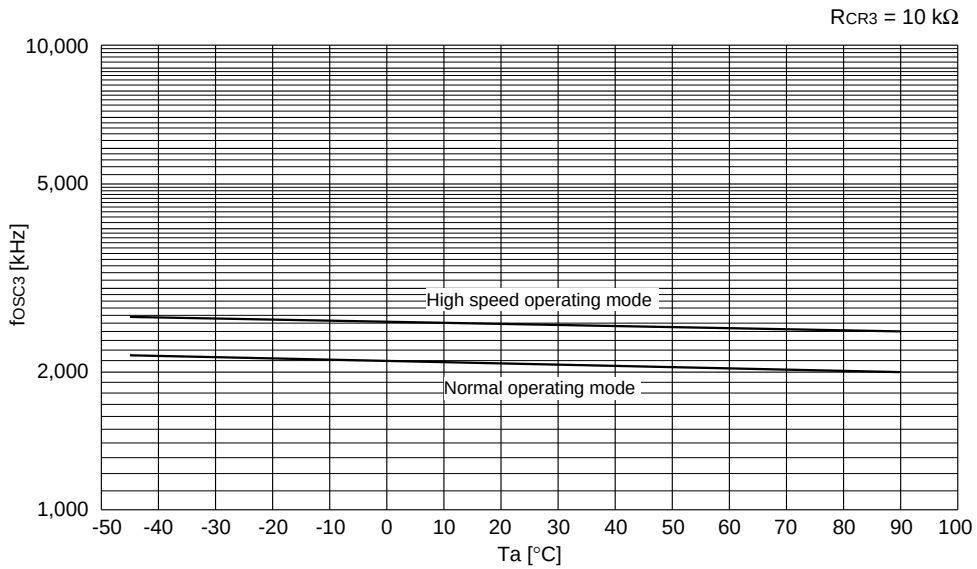
• Oscillation frequency temperature characteristic (OSC1)



- **Oscillation frequency resistor characteristic (OSC3)**



- **Oscillation frequency temperature characteristic (OSC3)**

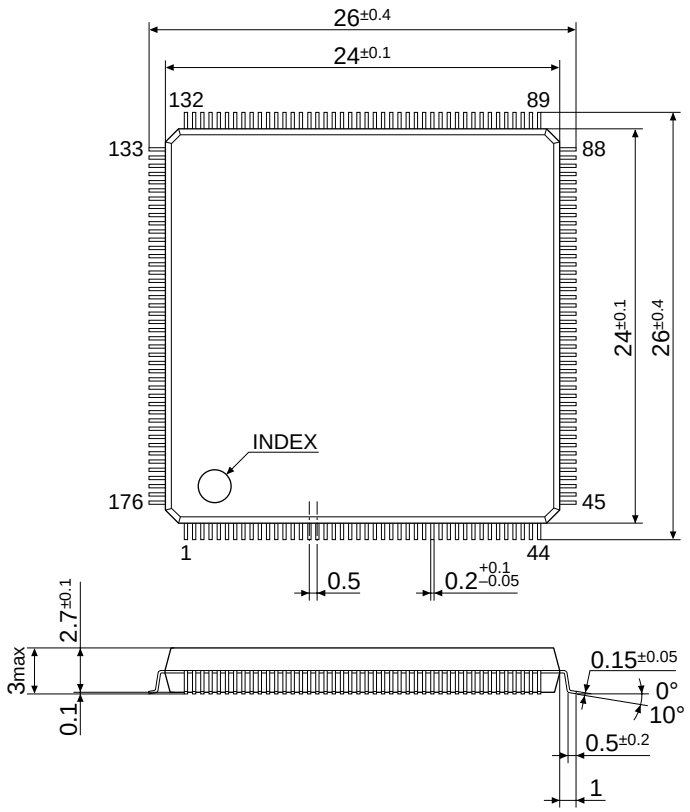


8 PACKAGE

8.1 Plastic Package

QFP18-176pin

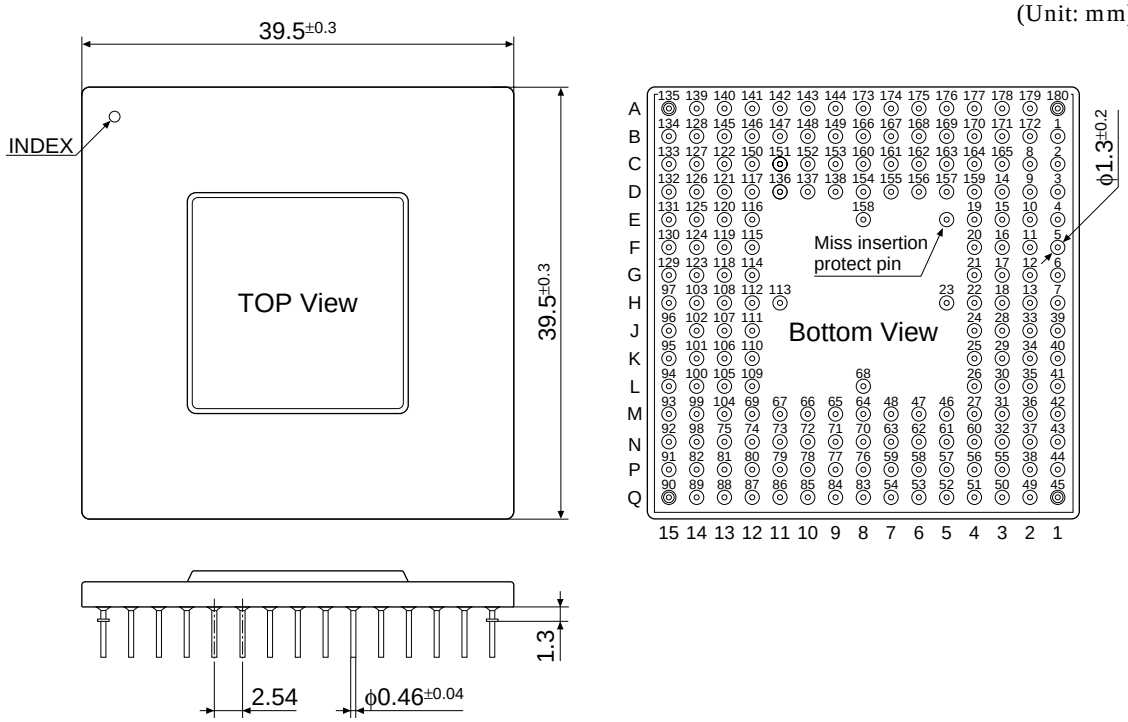
(Unit: mm)



8.2 Ceramic Package

PGA-181pin

(Unit: mm)

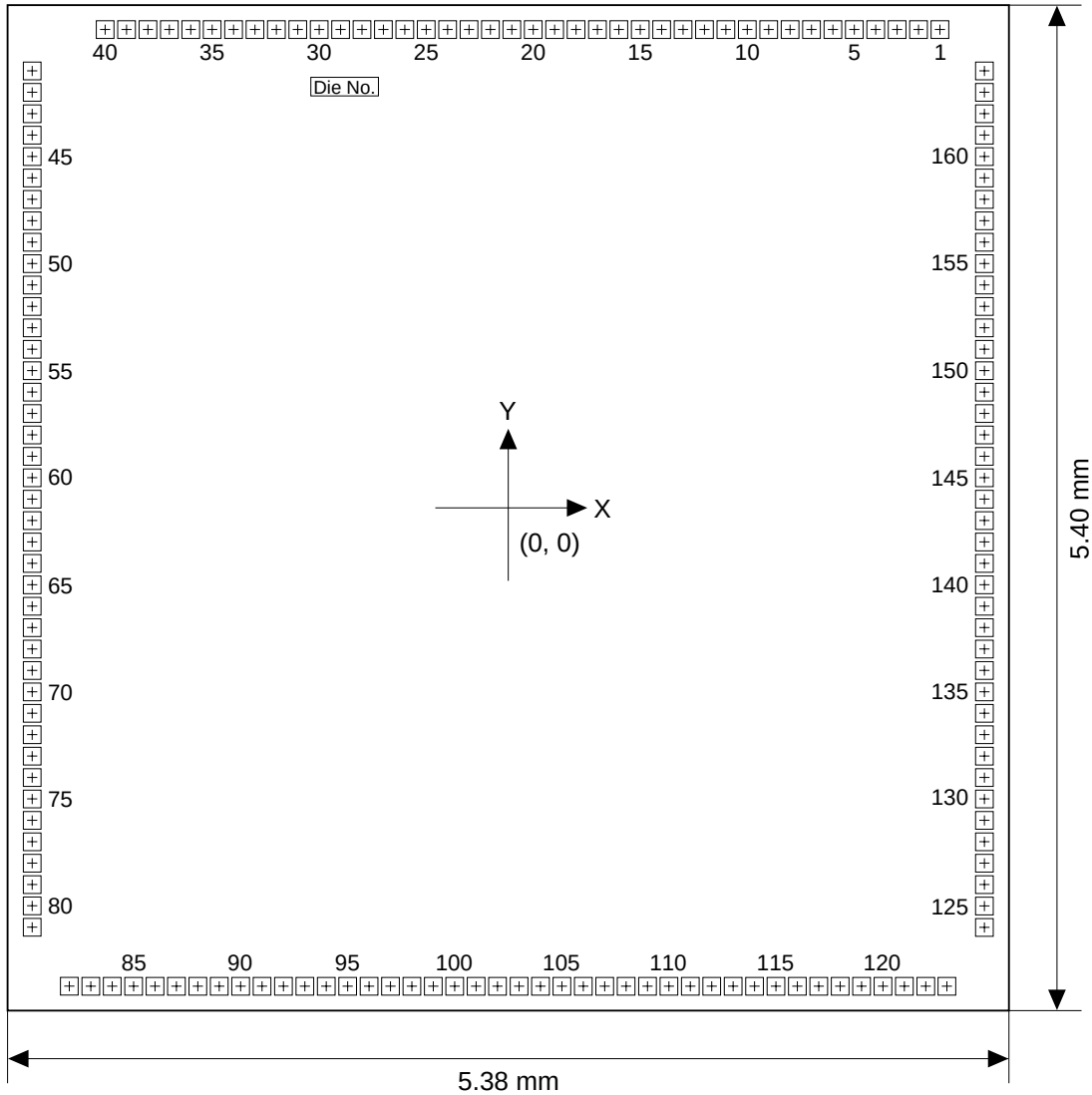


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	N.C.	37	SEG49	73	COM22/SEG81	109	K06	145	R50/$\overline{BZ}$
2	N.C.	38	SEG50	74	COM21/SEG82	110	K05	146	R51/$\overline{BZ}$
3	N.C.	39	SEG51	75	COM20/SEG83	111	K04	147	COM0
4	SEG16	40	SEG52	76	COM19/SEG84	112	K03	148	COM1
5	SEG17	41	SEG53	77	COM18/SEG85	113	K02	149	COM2
6	SEG18	42	SEG54	78	COM17/SEG86	114	K01	150	COM3
7	SEG19	43	SEG55	79	COM16/SEG87	115	K00	151	COM4
8	SEG20	44	N.C.	80	CG	116	P17/AD7	152	COM5
9	SEG21	45	N.C.	81	CF	117	P16/AD6	153	COM6
10	SEG22	46	N.C.	82	CE	118	P15/AD5	154	COM7
11	SEG23	47	N.C.	83	CD	119	P14/AD4	155	COM8
12	SEG24	48	SEG56	84	CC	120	P13/$\overline{SRDY}$	156	COM9
13	SEG25	49	SEG57	85	CB	121	P12/$\overline{SCLK}$	157	COM10
14	SEG26	50	SEG58	86	CA	122	P11/SOUT	158	COM11
15	SEG27	51	SEG59	87	V_{C5}	123	P10/SIN	159	COM12
16	SEG28	52	SEG60	88	V_{C4}	124	AV_{DD}	160	COM13
17	SEG29	53	SEG61	89	N.C.	125	AGND	161	COM14
18	SEG30	54	SEG62	90	N.C.	126	AV_{SS}	162	COM15
19	SEG31	55	SEG63	91	N.C.	127	AV_{REF}	163	SEG0
20	SEG32	56	SEG64	92	N.C.	128	P07	164	SEG1
21	SEG33	57	SEG65	93	N.C.	129	P06	165	SEG2
22	SEG34	58	SEG66	94	V_{C3}	130	P05	166	SEG3
23	SEG35	59	SEG67	95	V_{C2}	131	P04	167	SEG4
24	SEG36	60	SEG68	96	V_{C1}	132	P03	168	SEG5
25	SEG37	61	SEG69	97	OSC3	133	P02	169	SEG6
26	SEG38	62	SEG70	98	OSC4	134	N.C.	170	SEG7
27	SEG39	63	SEG71	99	V_{D1}	135	N.C.	171	SEG8
28	SEG40	64	COM31/SEG72	100	V_{DD}	136	N.C.	172	SEG9
29	SEG41	65	COM30/SEG73	101	V_{SS}	137	N.C.	173	SEG10
30	SEG42	66	COM29/SEG74	102	V_{OSC}	138	P01	174	SEG11
31	SEG43	67	COM28/SEG75	103	OSC1	139	P00	175	SEG12
32	SEG44	68	COM27/SEG76	104	OSC2	140	MOUT	176	SEG13
33	SEG45	69	COM26/SEG77	105	$\overline{TEST}$	141	$\overline{MOUT}$	177	SEG14
34	SEG46	70	COM25/SEG78	106	$\overline{RESET}$	142	R26/$\overline{TOUT}$	178	SEG15
35	SEG47	71	COM24/SEG79	107	K10/EVIN	143	R27/TOUT	179	N.C.
36	SEG48	72	COM23/SEG80	108	K07	144	R34/FOUT	180	N.C.

N.C.: No Connection

9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 0.4 mm
Pad opening: 95 µm

9.2 Pad Coordinates

Table 9.2.1 Pad coordinates

(Unit: µm)

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	V_{C3}	2,319	2,569	41	P01	-2,558	2,347	82	*	*	*	124	SEG56	2,558	-2,253
2	V_{C2}	2,204	2,569	42	P00	-2,558	2,232	83	SEG16	-2,243	-2,569	125	SEG57	2,558	-2,138
3	V_{C1}	2,089	2,569	43	MOUT	-2,558	2,117	84	SEG17	-2,128	-2,569	126	SEG58	2,558	-2,023
4	OSC3	1,974	2,569	44	$\overline{\text{MOUT}}$	-2,558	2,002	85	SEG18	-2,013	-2,569	127	SEG59	2,558	-1,908
5	OSC4	1,859	2,569	45	R26/$\overline{\text{TOUT}}$	-2,558	1,887	86	SEG19	-1,898	-2,569	128	SEG60	2,558	-1,793
6	V_{D1}	1,744	2,569	46	R27/TOUT	-2,558	1,772	87	SEG20	-1,783	-2,569	129	SEG61	2,558	-1,678
7	V_{DD}	1,629	2,569	47	R34/FOUT	-2,558	1,657	88	SEG21	-1,668	-2,569	130	SEG62	2,558	-1,563
8	V_{SS}	1,514	2,569	48	R50/BZ	-2,558	1,542	89	SEG22	-1,553	-2,569	131	SEG63	2,558	-1,448
9	V_{OSC}	1,399	2,569	49	R51/$\overline{\text{BZ}}$	-2,558	1,427	90	SEG23	-1,438	-2,569	132	SEG64	2,558	-1,333
10	OSC1	1,284	2,569	50	COM0	-2,558	1,312	91	SEG24	-1,323	-2,569	133	SEG65	2,558	-1,218
11	OSC2	1,169	2,569	51	COM1	-2,558	1,197	92	SEG25	-1,208	-2,569	134	SEG66	2,558	-1,103
12	$\overline{\text{TEST}}$	1,054	2,569	52	COM2	-2,558	1,082	93	SEG26	-1,093	-2,569	135	SEG67	2,558	-988
13	$\overline{\text{RESET}}$	939	2,569	53	COM3	-2,558	967	94	SEG27	-978	-2,569	136	SEG68	2,558	-873
14	K10/EVIN	824	2,569	54	COM4	-2,558	852	95	SEG28	-863	-2,569	137	SEG69	2,558	-758
15	K07	709	2,569	55	COM5	-2,558	737	96	SEG29	-748	-2,569	138	SEG70	2,558	-643
16	K06	594	2,569	56	COM6	-2,558	622	97	SEG30	-633	-2,569	139	SEG71	2,558	-528
17	K05	479	2,569	57	COM7	-2,558	507	98	SEG31	-518	-2,569	140	COM31/SEG72	2,558	-413
18	K04	364	2,569	58	COM8	-2,558	392	99	SEG32	-403	-2,569	141	COM30/SEG73	2,558	-298
19	K03	249	2,569	59	COM9	-2,558	277	100	SEG33	-288	-2,569	142	COM29/SEG74	2,558	-183
20	K02	134	2,569	60	COM10	-2,558	162	101	SEG34	-173	-2,569	143	COM28/SEG75	2,558	-68
21	K01	19	2,569	61	COM11	-2,558	47	102	SEG35	-58	-2,569	144	COM27/SEG76	2,558	47
22	K00	-96	2,569	62	COM12	-2,558	-68	103	SEG36	58	-2,569	145	COM26/SEG77	2,558	162
23	P17/AD7	-211	2,569	63	COM13	-2,558	-183	104	SEG37	173	-2,569	146	COM25/SEG78	2,558	277
24	P16/AD6	-326	2,569	64	COM14	-2,558	-298	105	SEG38	288	-2,569	147	COM24/SEG79	2,558	392
25	P15/AD5	-441	2,569	65	COM15	-2,558	-413	106	SEG39	403	-2,569	148	COM23/SEG80	2,558	507
26	P14/AD4	-556	2,569	66	SEG0	-2,558	-528	107	SEG40	518	-2,569	149	COM22/SEG81	2,558	622
27	P13/$\overline{\text{SRDY}}$	-671	2,569	67	SEG1	-2,558	-643	108	SEG41	633	-2,569	150	COM21/SEG82	2,558	737
28	P12/$\overline{\text{SCLK}}$	-786	2,569	68	SEG2	-2,558	-758	109	SEG42	748	-2,569	151	COM20/SEG83	2,558	852
29	P11/SOUT	-901	2,569	69	SEG3	-2,558	-873	110	SEG43	863	-2,569	152	COM19/SEG84	2,558	967
30	P10/SIN	-1,016	2,569	70	SEG4	-2,558	-988	111	SEG44	978	-2,569	153	COM18/SEG85	2,558	1,082
31	AV_{DD}	-1,131	2,569	71	SEG5	-2,558	-1,103	112	SEG45	1,093	-2,569	154	COM17/SEG86	2,558	1,197
32	AGND	-1,246	2,569	72	SEG6	-2,558	-1,218	113	SEG46	1,208	-2,569	155	COM16/SEG87	2,558	1,312
33	AV_{SS}	-1,361	2,569	73	SEG7	-2,558	-1,333	114	SEG47	1,323	-2,569	156	CG	2,558	1,427
34	AV_{REF}	-1,476	2,569	74	SEG8	-2,558	-1,448	115	SEG48	1,438	-2,569	157	CF	2,558	1,542
35	P07	-1,591	2,569	75	SEG9	-2,558	-1,563	116	SEG49	1,553	-2,569	158	CE	2,558	1,657
36	P06	-1,706	2,569	76	SEG10	-2,558	-1,678	117	SEG50	1,668	-2,569	159	CD	2,558	1,772
37	P05	-1,821	2,569	77	SEG11	-2,558	-1,793	118	SEG51	1,783	-2,569	160	CC	2,558	1,887
38	P04	-1,936	2,569	78	SEG12	-2,558	-1,908	119	SEG52	1,898	-2,569	161	CB	2,558	2,002
39	P03	-2,051	2,569	79	SEG13	-2,558	-2,023	120	SEG53	2,013	-2,569	162	CA	2,558	2,117
40	P02	-2,166	2,569	80	SEG14	-2,558	-2,137	121	SEG54	2,128	-2,569	163	V_{C5}	2,558	2,232
–				81	SEG15	-2,558	-2,252	122	SEG55	2,243	-2,569	164	V_{C4}	2,558	2,347
–				–				123	*	*	*	–			

∗ Do not bond No.82 and 123 pads since they are used for factory inspection at shipment.

10 PRECAUTIONS ON MOUNTING

<Oscillation Circuit>

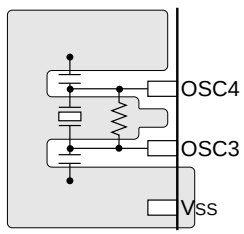
- Oscillation characteristics change depending on conditions (board pattern, components used, etc.).
  In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3, OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a V_{SS} pattern as large as possible at circumscription of the OSC1, OSC2, OSC3, OSC4 terminals and the components connected to these terminals.
  Furthermore, do not use this V_{SS} pattern for any purpose other than the oscillation system.

Sample V_{SS} pattern (OSC3)



  (3) When supplying an external clock to the OSC1 (OSC3) terminal, the clock source should be connected to the OSC1 (OSC3) terminal in the shortest line.
  Furthermore, do not connect anything else to the OSC2 (OSC4) terminal.

- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 (OSC3) and V_{DD}, please keep enough distance between OSC1 (OSC3) and V_{DD} or other signals on the board pattern.

<Reset Circuit>

- The power-on reset signal which is input to the $\overline{RESET}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor is added to the $\overline{RESET}$ terminal by mask option, take into consideration dispersion of the resistance for setting the constant.

- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{RESET}$ terminal in the shortest line.

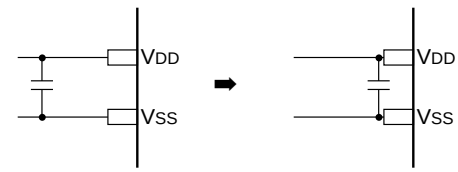
<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

(1) The power supply should be connected to the V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, AGND and AV_{REF} terminals with patterns as short and large as possible.
In particular, the power supply for AV_{DD}, AV_{SS}, AGND and AV_{REF} affects A / D conversion accuracy.

(2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.

Bypass capacitor connection example



(3) Components which are connected to the V_{D1}, V_{C1}–V_{C5} and CA–CG terminals, such as capacitors, should be connected in the shortest line.
In particular, the V_{C1}–V_{C5} voltages affect the display quality.

- Do not connect anything to the V_{C1}–V_{C5} and CA–CG terminals when the LCD driver is not used.

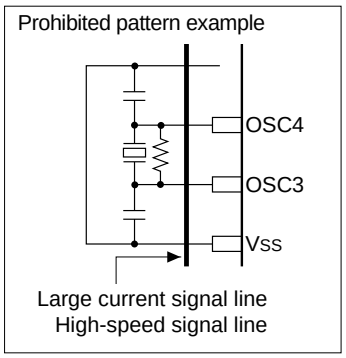
<A/D Converter>

- When the A / D converter is not used, the power supply terminals for the analog system should be connected as shown below.
  AVDD → VDD
  AVSS → VSS
  AVREF → VSS
  AGND → VSS

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation and analog input unit.

- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation and analog input unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

(1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

(2) The inspection process of the product needs an environment that shields the IC from visible radiation.

(3) As well as the face of the IC, shield the back and side too.

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Issue DECEMBER 2000, Printed in Japan Ⓜ A