MF1030-02

EPSON

MLS Driver Chip Set

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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NOTICE

CONTENTS

FEATURE

This chip set works to support the MLS (Multi Line Selection) drive method capable of making high-speed responses consisting of multiple numbers of SED1580, SED1590, SED1751, SED1360 and SCI7500 ICs. Since the indication data are stored in the indication RAM built into the X-driver to issue LCD drive signals, transference of indication data from the controller will be interrupted except for the period when the indications are being revised. Also, the complicated processings necessary for MLS drive are completed between the X-driver and the Y-driver so users need not be concerned about them. Consequently, the existing interface is usable.
Moreover, we are preparing exclusive power ICs to help configure the display systems for handy, high performance equipment.

CHIP SET CONFIGURATION

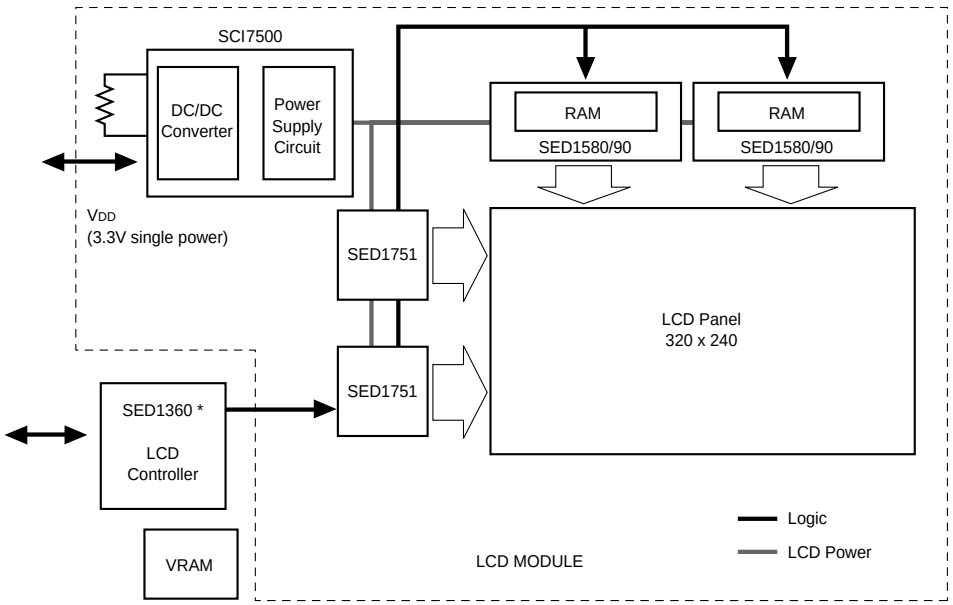
- SED1360F0A LCD controller (applicable to drivers with display RAM)
- SED1580T0A/D0B 160-output, 4-line distributed MLS drive method LCD segment driver
- SED1590T0A/D0B 160-output, 4-line distributed MLS drive method LCD segment driver + controller
- SED1751T0A/D0B 120/100-output, 4-line distributed MLS drive method LCD common driver
- SCI7500F0A 4-line MLS driver with exclusive power supply

FEATURES OF CHIP SETS

- Ultra-low power consumption with newly power circuits.
  – About 5mW with 320 × 240 dots FTN reflection monochrome display.
- Single power supply : 3.3V, on chip DC/DC converter.
- Two types of interface.
- High contrast, High quality with no flicker.

BLOCK DIAGRAM

: SED1360 is not necessary using SED1590.



SED1360F0A LCD CONTROLLER (applicable to drivers with built-in indication RAM)

Power supply	: Logic channel 2.7 – 5.5V
Package	: GFP6-60 pin

SED1580T0A/D0B MLS drive method LCD segment driver

Number of LCD outputs	: 160 outputs
Driving duty	: 1/240 duty
Built-in indication RAM	: 160 × 240 bits
Power supply	: Logic channel 3.0 – 3.6V
	LCD channel 6.0 – 7.2V
Package	: TCP or Au bump chip

SED1590T0A/D0B MLS drive method LCD segment driver + controller

Number of LCD outputs	: 160 outputs
Driving duty	: 1/240 duty
Built-in indication RAM	: 160 × 240 bits
Power supply	: Logic channel 2.7 – 3.6V
	LCD channel 5.4 – 7.2V
Package	: TCP (under development) or Au bump chip
Others	: Built-in LCD controller function (with 31 types of commands)

SED1751T0A/D0B MLS DRIVE METHOD LCD COMMON DRIVER

Number of LCD outputs	: 120 outputs/100-output changeover
Driving duty	: 1/480 duty
Built-in indication RAM	: 160 × 240 bits
Power supply	: Logic channel 2.7 – 5.5V
	LCD channel 14 – 42V
Package	: TCP or Au bump chip

SCI7500F0A 4-line MLS driver with exclusive power supply

Incorporating a built-in DC/DC converter with a voltage conversion circuit and a bias circuit necessary for quintuple (1/200 duty) and sextuple boosted (1/240 duty) 4-line MLS driving.

Power supply	: 2.4 – 3.6V single power input
Package	: GFP12-48 pin

SED1360 Series

Contents

INTRODUCTION

Scope

This is the Functional Specification for SED1360 3.3 V Ultra Low Power LCD Controller Chip.

Objectives

(1) To specify functions and interface requirements of the chip.
(2) To allow review of the functions of the chip, as a preliminary specification.

FEATURES

Technology

- ultra low power CMOS process
- 3.3 volt operation
- chip supply with aluminum pad
- 64 pin QFP6 surface mount package

System

- Direct connection to the 68 family CPUs.
- minimum CPU Interface pin count.
- no buffers are required in a 3.3 V-System.
- internal oscillator with external Capacitance and Resistance, or external oscillator for a low frequency input source.
- interfaces to 64 kb and, or 256 kb SRAMs.
- controls Seiko Epson's RAM integrated Segment Drivers.
- self-controlled Doze Mode.
- optimized Hardware for low to medium resolution LCDs.
- ultra low power consumption.

OVERVIEW DESCRIPTION

SED1360 is an ultra low power 3.3 V LCD controller which is optimized to drive low to medium resolution LCD panels. SED1360 can interface to the 68 family CPUs in the Port Peripheral Timing.

Typical System Block Diagram

The following figure shows typical system implementation with SED1360.

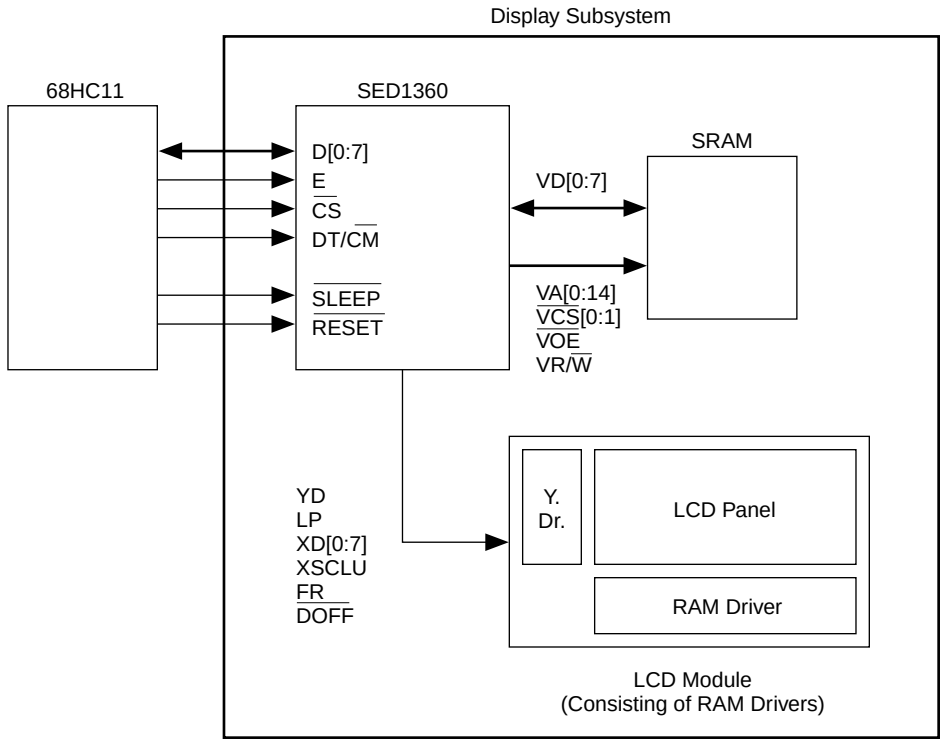


Figure 1. Typical System Block Diagram

SED1360

(1) 3.3 V operational low power LCD Controller Chip.
(2) receives Data from CPU.
(3) stores the Display Data into SRAM.
(4) reads the Data written in the SRAM to update LCD Display.
(5) transfers the read Data to LCD Module automatically.
(6) controls entering to Doze Mode and returning to Active Mode automatically.
(7) supports local oscillation or low frequency input to realize the Ultra Low Power LCD Display Subsystem.
(8) supports Hardware Suspend Mode.

LCD Module

(1) 3.3 V operational low power LCD Module.
(2) consists of Seiko Epson's RAM integrated Segment Drivers, Common Drivers and an LCD panel.
(3) The LCD Module enters into Power Save Mode automatically, if "XSCLU" is not provided.

SRAM

(1) SED1360 uses the SRAM to store the Display Data written by CPU in order to arbitrate between CPU access and LCD Display refresh.
(2) has to be 3.3 V operational.

SED1360 Internal Block Diagram

The following figure shows an overview of the LCD Controller chip SED1360.

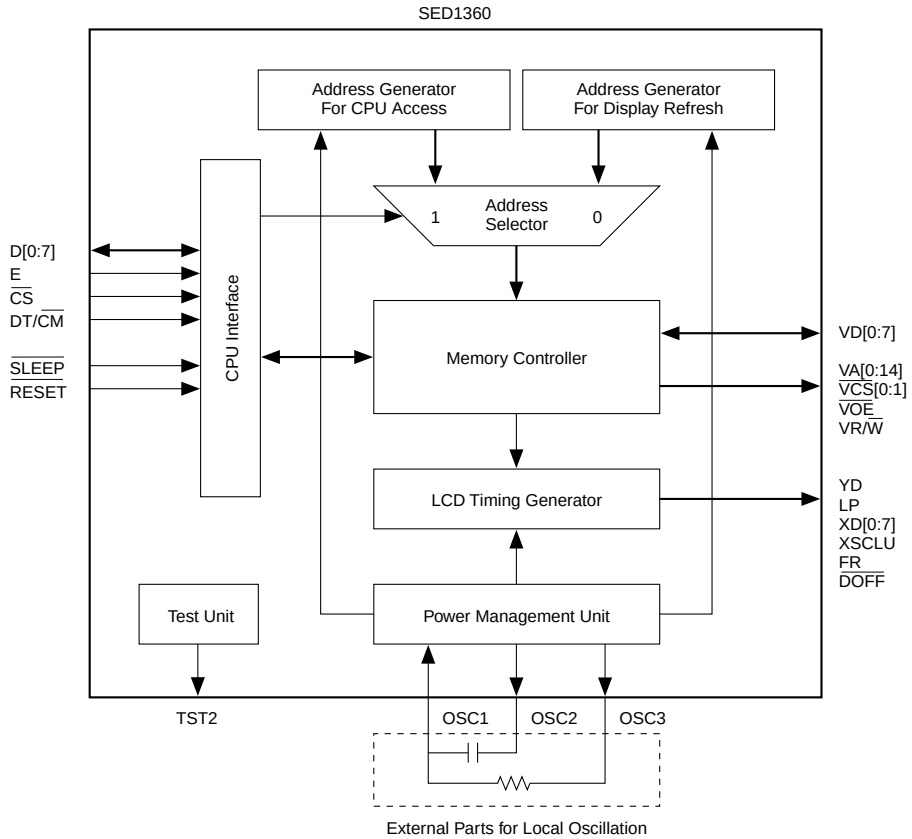


Figure 2. SED1360 Internal Block Diagram

CPU Interface

(1) 3.3 V 68XX dedicated CPU Interface.
(2) 8 bit Data are used to transfer Data or Commands.
(3) The rising edge of "$\overline{CS}$" signal is used to execute the Data Transfer.
(4) "DT/$\overline{CM}$" is used for CPU to indicate either Data or Command is on the bus.
(5) "$\overline{SLEEP}$" signal is used to set the chip in Sleep Mode.
(6) No other signals are required for the normal operation.
(7) "$\overline{RESET}$" is used to initialize the chip.

Address Generator for CPU Access

(1) The internal CPU Write Start Address can be set by the command.
(2) After every single CPU Display Data Write Access, the internal CPU Write Address Counter is increased by one.

Address Generator for Display Refresh

(1) "E" is used to generate the Display Refresh Address.
(2) Address Generator begins when the immediate Frame comes after the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) Address Generation stops if no CPU Display Data Write Access occurs for two LCD Frame period.

Address Selector

When CPU Display Data Write Access occurs, the internal CPU Write Address is selected to generate the address for SRAM.

Memory Controller

(1) When CPU Display Data Write Access occurs, Memory Controller stores the data into SRAM.
(2) The Memory Controller begins reading the data stored in the SRAM to transfer to the LCD Module when the immediate Frame comes after the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) The Memory Controller stops reading the data from the SRAM if no CPU Display Data Write Access occurs for two LCD Frame period.

LCD Timing Generator

(1) Local oscillation is directly used to generate "LP" (Horizontal Sync. Pulse), "YD" (Vertical Sync. Pulse) and "FR" (LCD voltage alternation signal).
(2) The updated data stored in the SRAM is transferred through the Memory Controller and the LCD Timing Generator to the LCD Module, if the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) The LCD Timing Generator uses "E" to generate "XSCLU".
(4) "XSCLU" is automatically controlled by the CPU Display Data Write Access or setting the "Display Data Transfer" command.

Power Management Unit

(1) Power Management Unit monitors the occurrence of CPU Display Data Write Access, the execution of the "Display Data Transfer" command, the internal state of LCD Frame period and the "$\overline{SLEEP}$" signal in order to determine entering to Doze Mode and returning to Active Mode. And this unit also controls local oscillation.

Test Unit

Test Unit controls test functions of the chip if the chip is in Test Mode.

PINOUT DIAGRAM

SED1360D0A

The following figure shows a pinout placement.

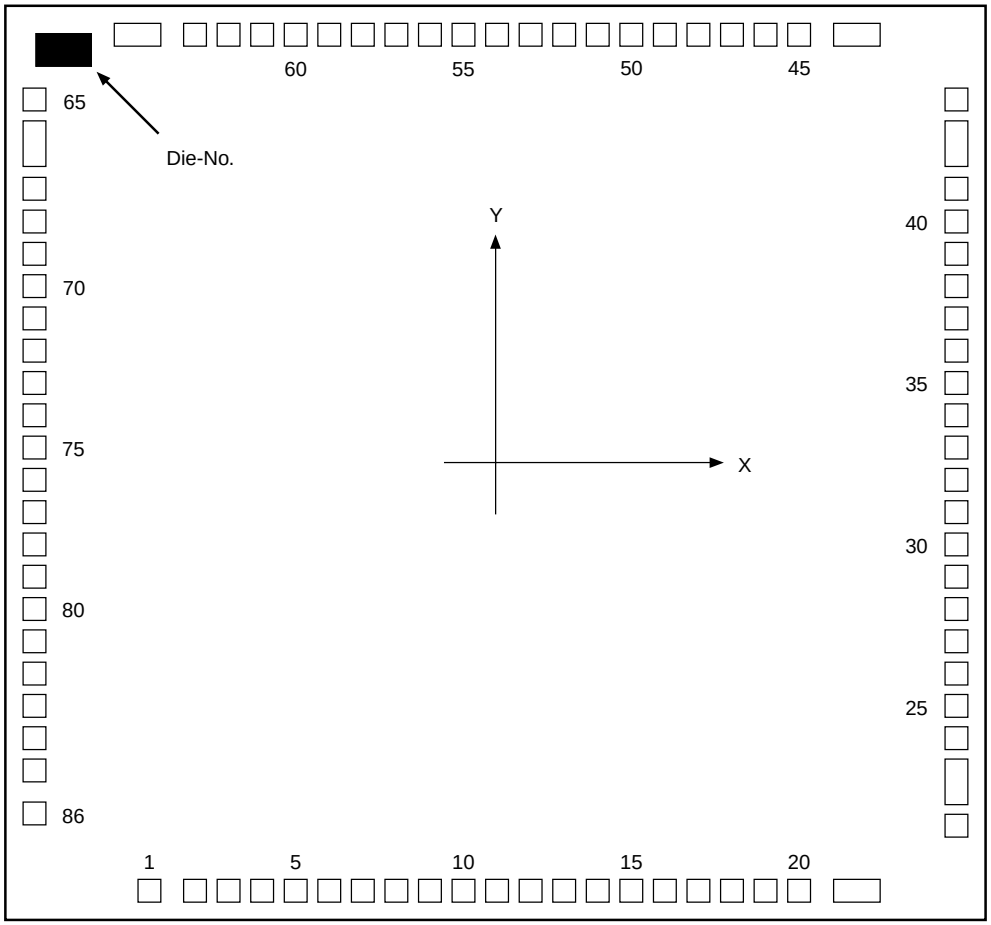


Figure 3. SED1360D0A Pinout Diagram

chip size	4.21 mm × 4.11 mm
chip thickness	400 µm
pad pich (min.)	136 µm
pad size (min.)	100 µm × 100 µm

Table 1. SED1360D0A Pin Coordinates

Pin No.	X (μm)	Y (μm)
1	–1425	–1913
2	–1221	
3	–1085	
4	–949	
5	–813	
6	–677	
7	–541	
8	–405	
9	–269	
10	–133	
11	3	
12	139	
13	275	
14	411	
15	547	
16	683	
17	819	
18	955	
19	1091	
20	1227	
21	1506	
22	1964	–1560
23		–1359
24		–1159
25		–1023
26		–887
27		–751
28		–615
29		–479
30		–343
31		–207
32		–71
33		65
34		201
35		337
36		473
37		609
38		745
39		881
40		1017
41		1153
42		1359
43		1564

Pin No.	X (μm)	Y (μm)
44	1506	1913
45	1227	
46	1091	
47	955	
48	819	
49	683	
50	547	
51	411	
52	275	
53	139	
54	3	
55	–133	
56	–269	
57	–405	
58	–541	
59	–677	
60	–813	
61	–949	
62	–1085	
63	–1221	
64	–1476	
65	–1964	1547
66		1350
67		1153
68		1017
69		881
70		745
71		609
72		473
73		337
74		201
75		65
76		–71
77		–207
78		–343
79		–479
80		–615
81		–751
82		–887
83		–1023
84		–1159
85		–1295
86		–1499

SED1360F0A

The following figure shows a pinout placement.

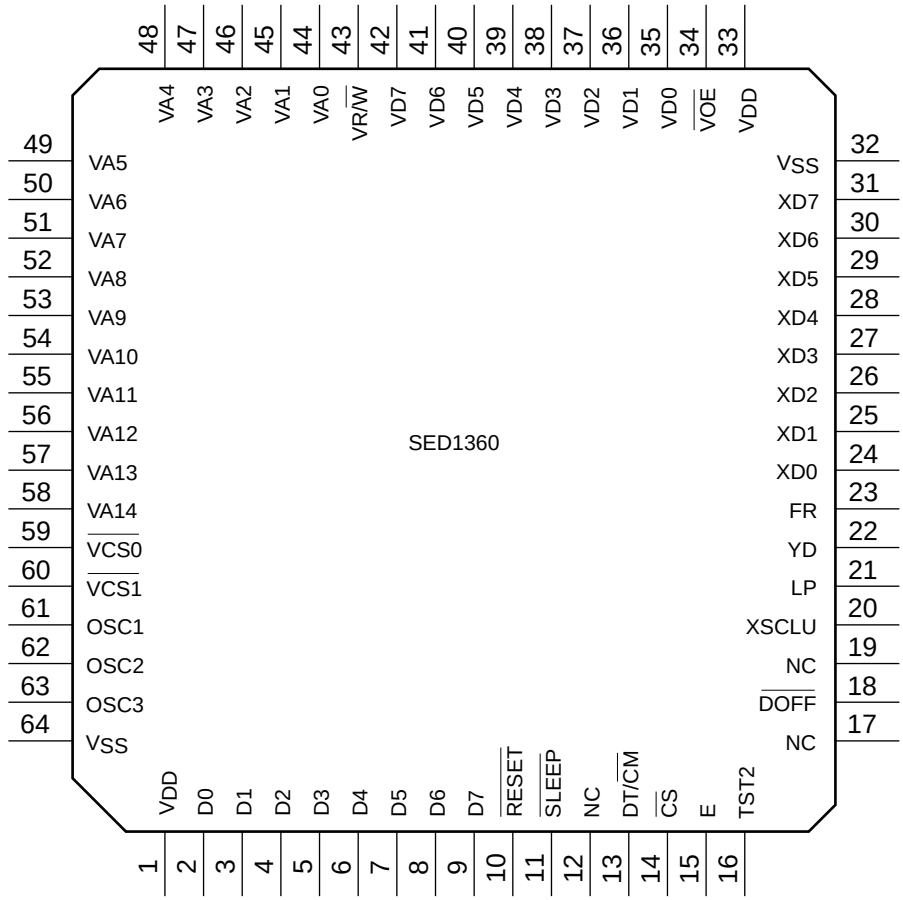


Figure 4. SED1360F0A Pinout Diagram

Note: Pinout placement subject to change.
Package type: 64 pin surface mount QFP6 NC pins are left unconnected.

PIN DESCRIPTION

Key
C = CMOS level input
CS = CMOS level input with hysteresis
COSC = CMOS level input for an internal oscillation inverter
T = TTL level input
OX = CMOS output, x denotes output driver type.
OOSC = CMOS output for an internal oscillation inverter
PU = integrated pull-up resistor
PD = integrated pull-down resistor

CPU Interface

The CPU interface signals are placed on one side of the chip for easy connection to CPU. And the input levels of all CPU Interface pins are unified with CMOS level to allow easy connection to 3.3 V 68 family CPUs.

Table 2. CPU Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
D [0:7]	I	2…9	C	Data inputs. The data is captured into an SED1360's input data register by the rising edge of "$\overline{CS}$".
E	I	15	C	In Active Mode, "E" is used to write or read the CPU data to from SRAM and transfer the data written in the SRAM to the LCD Module.
$\overline{CS}$	I	14	C	The rising edge of this signal is used to capture the state of "D [0:7] and "DT/$\overline{CM}$" into SED1360. When "$\overline{CS}$" is high, no data captures occur.
DT/$\overline{CM}$	I	13	C	If this signal is high, Data is on the bus. If this signal is low, Command is on the bus.
$\overline{SLEEP}$	I	11	C	If this signal is pulled low, the chip enters Sleep Mode. In the Sleep Mode, internal oscillation is disabled, all of the input signals are masked and all of the output signals are controlled to inactive state.
$\overline{RESET}$	I	10	CS	The active low "$\overline{RESET}$" signal from the system clears all internal registers.

SRAM Interface

The SRAM Interface signals are basically placed on two sides of the chip. The input level of "VD [0:7]" is met with TTL level to connect with generic 3.3 V SRAMs. And also "VD [0:7]" have integrated pull-up resistors to eliminate current consumption at the input buffers in Doze Mode.

Table 3. SRAM Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
VD [0:7]	I/O	35…42	T O2 PU	The "VD [0:7]" signals are connected to SRAM's 8 bit data. The captured display data in SED1360 are stored in the SRAM through "VD [0:7]" by the "VR/$\overline{W}$" signal.
VA [0:14]	O	44…58	O2	The "VA [0:14]" signals are connected to SRAM's address lines. "VA [0:14]" generate either CPU Display Data Write Address or Display Refresh Address depending upon operation modes.
$\overline{VCS}$ [0:1]	O	59, 60	O2	SED1360 manages up to 64 kb of SRAM as a frame buffer memory. SED1360 is configured to primarily use two 256 kb SRAMs. "$\overline{VCS0}$" is active when 1st 32 kb is selected. "$\overline{VCS1}$" is active when the rest 32 kb is selected. "$\overline{VCS}$ [0:1]" are connected to SRAM's chip select inputs (active low). Those signals are inactie (high), if the chip is in Sleep Mode.
$\overline{VOE}$	O	34	O2	The "$\overline{VOE}$" signal is connected to SRAM's data output enable input.
VR/$\overline{W}$	O	43	O2	The "VR/$\overline{W}$" signal is connected to SRAM's write strobe input.

LCD Interface

The LCD interface signals are placed on the rest one side of the chip. The output type of all signals is optimized to drive the Ultra Low Power LCD Module properly.

Table 4. LCD Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
XD [0:7]	O	24…31	O1	The "XD [0:7]" signals are connected to the display data inputs of the LCD Module. During Doze Mode, the signals are driven low. "XD [0:7] are transferred to the LCD Module by the falling edge of "XSCLU".
XSCLU	O	20	O1	The "XSCLU" signal is connected to the display data shift clock of the LCD Module. During Doze Mode, the signal is driven low to force the RAM integrated Segment Drivers to be in Power Save Mode.
LP	O	21	O1	The "LP" signal is connected to te input, which drives the data latching pulse of the segment drivers and the scanning clock of the common drivers, of the LCD Module. The "LP" period is directly generated by the signal which is input through "OSC1".
YD	O	22	O1	The "YD" is connected to the frame start pulse signal of the LCD Module.
FR	O	23	O1	The "FR" signal is connected to the signal which alternates the LCD voltage in the LCD Module.
$\overline{DOFF}$	O	18	O1	This signal outputs low if the chip is in Sleep Mode.

Oscillation

The oscillation pins are used to generate the low frequency which directly generates the “LP” signal.

Table 5. Oscillation Pin Description

Pin Name	Type	Pin No.	Drv	Description
OSC1	I	61	COSC	The pin is connected to the one node of the capacitance and the one node of the resistance. If an external oscillator is used as a clock source, then this pin is the clock input.
OSC2	O	62	OOSC	This pin is connected to the other node of the capacitance. If an external oscillator is used as a clock source, then this pin should be left unconnected.
OSC3	O	63	OOSC	This pin is connected to the other node of the resistance. If an external oscillator is used as a clock source, then this pin should be left unconnected.

Test

The test signals are prepared for testing the chip itself.

Table 6. Test Pin Description

Pin Name	Type	Pin No.	Drv	Description
NC	—	12, 17, 19	—	NC pins are not connected to the chip. These pins should be left unconnected.
TST2	O	16	O1	This pin should be left unconnected.

Power Supply

Table 7. Power Supply Pin Description

Pin Name	Type	Pin No.	Drv	Description
VDD	P	1, 33		VDD supply for the chip. Normally 3.3 volt.
VSS	P	32, 64		VSS supply for the chip. Normally 0 volt.

D.C. CHARACTERISTICS

Conditions: V_{DD} = 3.0 V ~ 3.6 V, Ta = –10°C to 70°C unless otherwise specified

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	V_{SS} – 0.3 to 5.0	Volts
Input Voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	Volts
Output Voltage	V_{OUT}	V_{SS} to V_{DD}	Volts
Operating Temperature	T_{OPR}	–10 to +70	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Soldering Temperature/Time	T_{SOL}	260 for 10 sec max. at lead	°C

Recommended Operating Conditions

Table 9. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	V_{DD}	V_{SS} = 0 V	3.0	3.3	3.6	V
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V

Input Specification

Table 10. Input Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low Level Input Voltage for type C input pins	V_{IL1} (C)	V_{DD} = MIN			0.6	V
High Level Input Voltage for type C input pins	V_{IH1} (C)	V_{DD} = MAX	2.5			V
High Level Input Voltage for type CS input pins	V_{IL2} (CS)	V_{DD} = 3.3 V			0.5	V
High Level Input Voltage for type CS input pins	V_{IH2} (CS)	V_{DD} = 3.3 V	2.9			V
Hysteresis Voltage for type CS input pins	V_{HYS} (CS)	V_{DD} = 3.3 V		0.1		V
High Level Input Voltage for type T input pins	V_{IL3} (T)	V_{DD} = MIN			0.5	V
High Level Input Voltage for type T input pins	V_{IH3} (T)	V_{DD} = MAX	1.7			V
Low Level Input Voltage for type COSC input pins	V_{IL4} (COSC)	V_{DD} = MIN			0.6	V
Low Level Input Voltage for type COSC input pins	V_{IH4} (COSC)	V_{DD} = MAX	2.5			V
Input Leakage Current	I_{IZ}	V_{DD} = MAX $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$	–1.0		1.0	µA
Input Pin Capacitance	C_{IN}			10		pF
Pull Down Resistance	R_{PD} (PU)	V_{DD} = 3.3 V	90		1100	kΩ
Pull Up Resistance	R_{PU} (PU)	V_{DD} = 3.3 V	90		1100	kΩ

Output Specifications

Table 11. Output Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low Level Output Voltage for type O1 output pins	V_{OL1} (O1)	V_{DD} = MIN I_{OL} = 1.0 mA	V_{SS} +0.3			V
Low Level Output Voltage for type O1 output pins	V_{OH1} (O1)	V_{DD} = MIN I_{OH} = –0.5 mA			V_{DD} –0.3	V
Low Level Output Voltage for type O2 output pins	V_{OL2} (O2)	V_{DD} = MIN I_{OL} = 3.0 mA	V_{SS} +0.3			V
Low Level Output Voltage for type O2 output pins	V_{OH2} (O2)	V_{DD} = MIN I_{OH} = –1.5 mA			V_{DD} –0.3	V
Low Level Output Voltage for type OOSC output pins	V_{OL3} (OOSC)	V_{DD} = MIN I_{OL} = 100 µA	V_{SS} +0.3			V
Low Level Output Voltage for type OOSC output pins	V_{OH3} (OOSC)	V_{DD} = MIN I_{OH} = –100 µA			V_{DD} –0.3	V
Output Leakage Current	I_{OZ}	V_{DD} = MAX $V_{OH} = V_{DD}$, $V_{OL} = V_{SS}$	–1.0		1.0	µA
Output Pin Capacitance	C_{OUT}			10		pF

Power Consumption

Table 12. Power Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Consumption in Active Mode with CPU write access	I_{OP1}	V_{DD} = 3.3 V t_{CYCE} = 500 ns f_{OSC} = 24 kHz		5		mA
Current Consumption in Active Mode with no CPU write access	I_{OP2}	V_{DD} = 3.3 V t_{CYCE} = 500 ns "$\overline{CS}$" = high f_{OSC} = 24 kHz		1		mA
Current Consumption in Doze Mode with CPU write access	I_{OP3}	V_{DD} = 3.3 V t_{CYCE} = 500 ns f_{OSC} = 24 kHz		4		mA
Current Consumption in Doze Mode with no CPU write access	I_{OP4}	V_{DD} = 3.3 V t_{CYCE} = 500 ns "$\overline{CS}$" = high f_{OSC} = 24 kHz		150		µA
Current Consumption in Sleep Mode	I_{OP5}	V_{DD} = 3.3 V No input signals toggle.		1		µA

Note: The above table shows the target power consumption.

A.C. CHARACTERISTICS

Conditions: V_{DD} = 3.3 V, Ta = 0°C to 70°C unless otherwise specified
Tr, Tf for all inputs must be –10 ns (10% to 90%)
C_L = 10 pF (SRAM Interface)
C_L = 20 pF (LCD Interface)

A single 1.5 V threshold voltage is used for the A.C. measurements.

CPU Interface Timing

Table 13. CPU Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"$\overline{CS}$" period	t_{cycCS}	t_{cycE}			ns
"$\overline{CS}$" low pulse width	t_{lCS}	170			ns
"$\overline{CS}$" high pulse width	t_{hCS}	100			ns
"DT/$\overline{CM}$" setup to "$\overline{CS}$"	t_{dsu1}	20			ns
"DT/$\overline{CM}$" hold from "$\overline{CS}$"	t_{dh1}	0			ns
"D [0:7]" setup to "$\overline{CS}$"	t_{dsu2}	70			ns
"D [0:7]" hold from "$\overline{CS}$"	t_{dh2}	0			ns

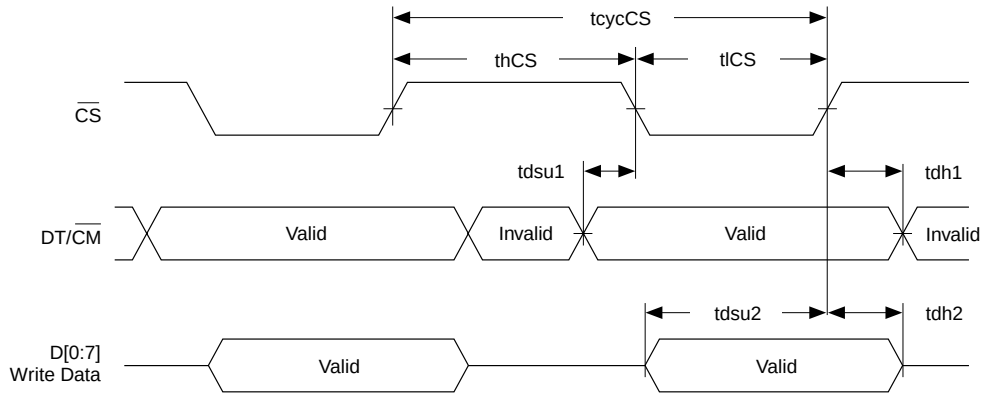


Figure 5. CPU Interface Timing

SRAM Interface Timing

Table 14. SRAM Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"E" period	t_{cycE}	333			ns
"E" low pulse width	t_{lE}	142			ns
"E" high pulse width	t_{hE}	137			ns
"VR/$\overline{W}$" period	t_{cycVW}	t_{cycE}			ns
"VR/$\overline{W}$" low pulse width	t_{lVW}		t_{hE}-40		ns
"VR/$\overline{W}$" high pulse width	t_{hVW}		t_{lE}		ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" setup to "VR/$\overline{W}$"	t_{asuVW}	0			ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" hold from "VR/$\overline{W}$"	t_{ahVW}	0			ns
"VD [0:7]" setup to "VR/$\overline{W}$"	t_{dsuVW}	t_{lVW}-20	t_{lVW}-10		ns
"VD [0:7]" hold from "VR/$\overline{W}$"	t_{dhVW}	0			ns
valid address period for the Display Refresh	t_{aVR}	t_{lE}-15	t_{lE}		ns
valid address period for the CPU data write	t_{aVW}	t_{hE}-15	t_{hE}		ns
SRAM read data access from the valid address	t_{accV}			t_{aVR}-25	ns
SRAM read data hold time from the valid address	t_{pdhV}	0			ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" setup to "$\overline{VOE}$"	t_{asuOE}	0			ns
"$\overline{VOE}$" hold from "VA [0:14]", "$\overline{VCS}$ [0:1]"	t_{ahOE}	0			ns
"$\overline{VOE}$" low pulse width	t_{lOE}		t_{lE}		ns
"$\overline{VOE}$" high pulse width	t_{hOE}		t_{hE}		ns
"VR/$\overline{W}$" delay from "$\overline{VOE}$"	t_{pdOW}	0			ns
"$\overline{VOE}$" delay from "VR/$\overline{OW}$"	t_{pdWO}	0			ns

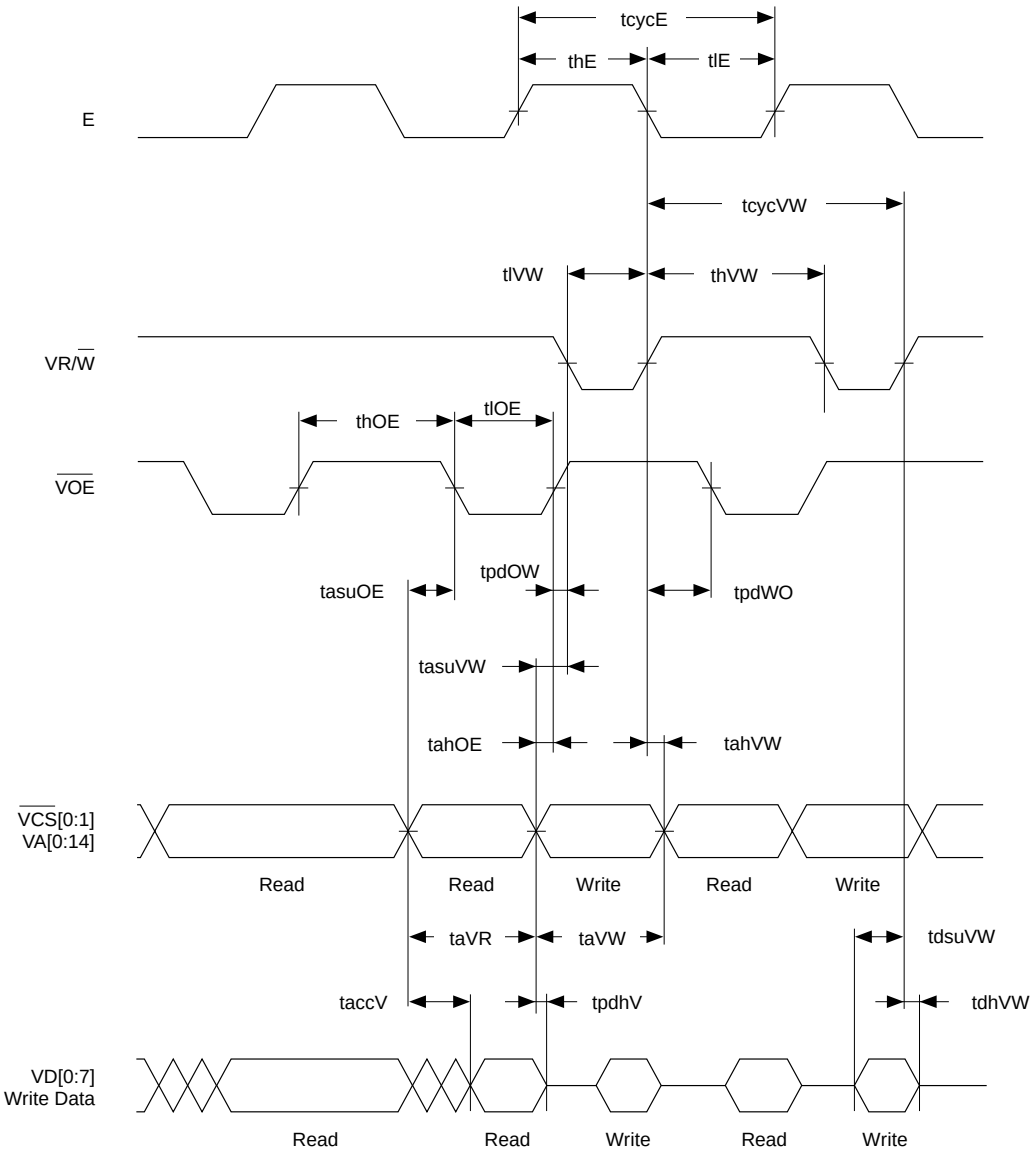


Figure 6. SRAM Interface Timing

LCD Interface Timing

Table 15. LCD Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"XSCLU" period	t_{cycXC}	t_{cycE}			ns
"XSCLU" low pulse width	t_{lXC}		t_{lE}		ns
"XSCLU" high pulse width	t_{hXC}		t_{hE}		ns
"XD [0:7]" setup to "XSCL"	t_{dsuXC}		t_{hE}		ns
"XD [0:7]" hold from "XSCL"	t_{dhXC}		t_{lE}		ns
"YD" delay from "LP"	t_{pdLY}	0			ns
"LP" period	t_{cycLP}	t_{cycOSC}	$2t_{cycOSC}$	$4t_{cycOSC}$	ns
"LP" high pulse width	t_{hLP}	500	700	1200	ns
"XSCL" delay from "LP"	t_{pdLXC}	$3t_{cycE}$ $+t_{hE}$-50	$4t_{cycE}$	$4t_{cycE}$ $+t_{hE+50}$	ns
"LP" delay from "XSCL"	t_{pdXCL}				ns
"XSCL" enabled	t_{XSCL}		[(Hor. size/8)-1] $\times t_{cyE}+t_{hE}$		ns
"YD" period	t_{cycYD}		(Ver.size) $\times t_{cycLP}$		ns
"FR" high or Low time	t_{cycFR}		t_{cycYD}		ns
"FR" delay from "LP"	t_{pdLF}	10	0	200	ns

Notes: 1. t_{cycOSC} is a period of frequency given to or generated at "OSC1".
2. Hor.size is described in the section Display Size.
3. Ver.size is described in the section Display Size.

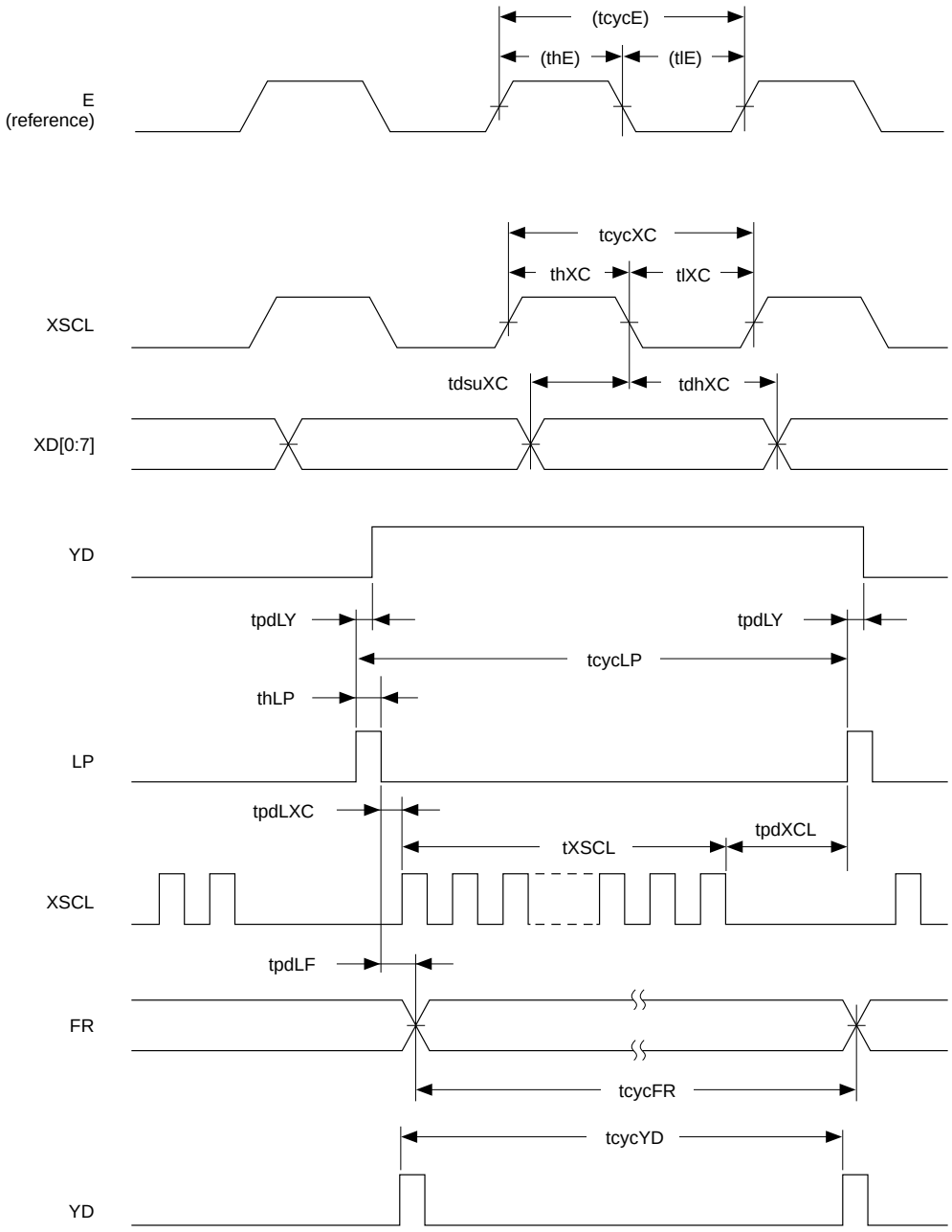


Figure 7. LCD Interface Timing

Oscillation Timing

Table 16. LCD Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"OSC1" period	t_{cycOSC}	20 t_{OSC} = 50 kHz	41.7 f_{OSC} = 24 kHz	50 f_{OSC} = 20 kHz	µs
"OSC1" low width if external oscillation is used.	t_{lOSC}		$0.5t_{cycOSC}$		µs
"OSC1" high width if external oscillation is used.	t_{hOSC}		$0.5t_{cycOSC}$		µs

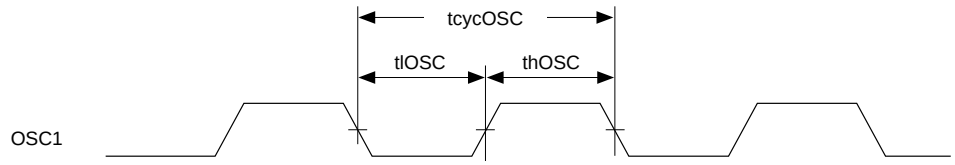


Figure 8. LCD Interface Timing

OPERATION DESCRIPTION

CPU Write Data Transfer

The following figure gives a basic timing for SED1360 to receive the CPU Write Data and relationship between CPU Data and pixels on the LCD panel. It is assumed that both CPU Write Start Address and Display Refresh Start Address are the same and the 320 × 200 dot LCD is used in the following figure.

(1) The rising edge of "$\overline{CS}$" is used for SED1360 to latch the CPU data.
(2) The CPU Data Write, after the "Display Data Write" command is executed, will be stored in the SRAM according to the internal CPU Write Address.
(3) The first 40 Byte data will be stored in SRAM and displayed continuously on the same line.
(4) The data will be displayed at the most left position on the next line on the panel every 40 Byte data.

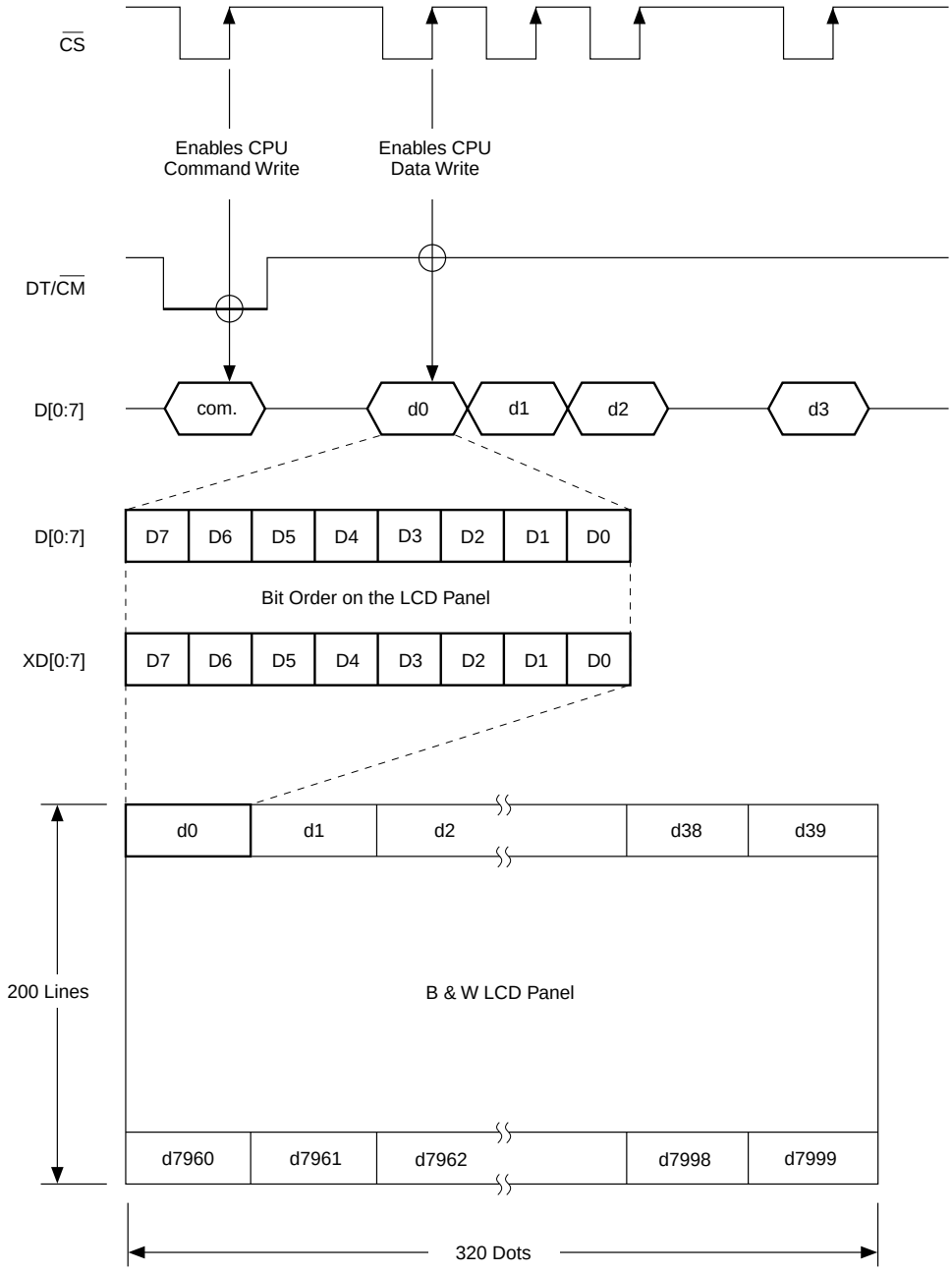


Figure 9. CPU Write Data Transfer

Display Data Transfer Modes

Display Data Auto Transfer Mode

The following figure gives a basic operation mode which SED1360 switches automatically. The figure assumes that the chip is configured in Display Data Auto Transfer Mode.

(1) If CPU Display Data Write Access occurs, then the next Frame period will be Active Mode. That is the Active Mode is initiated by the CPU Display Data Write Access, if the chip is configured in Display Data Auto Transfer Mode.
(2) If no CPU Display Data Write Access occurs in one Frame period, then the next Frame period will be Doze Mode.
(3) SED1360 switches the whole LCD Display Subsystem between Doze Mode and Active Mode.
(4) In the Active Mode, SED1360 reads the data from the SRAM, enables “XSCLU” in order to transfer the data stored in the SRAM to the LCD Module, then the RAM integrated Segment Drivers wake up from the power save mode.
(5) In the Doze Mode, SED1360 stops reading the data from the SRAM, disables “XSCLU” in order for the RAM integrated Segment Drivers to enter into the Power Save Mode.

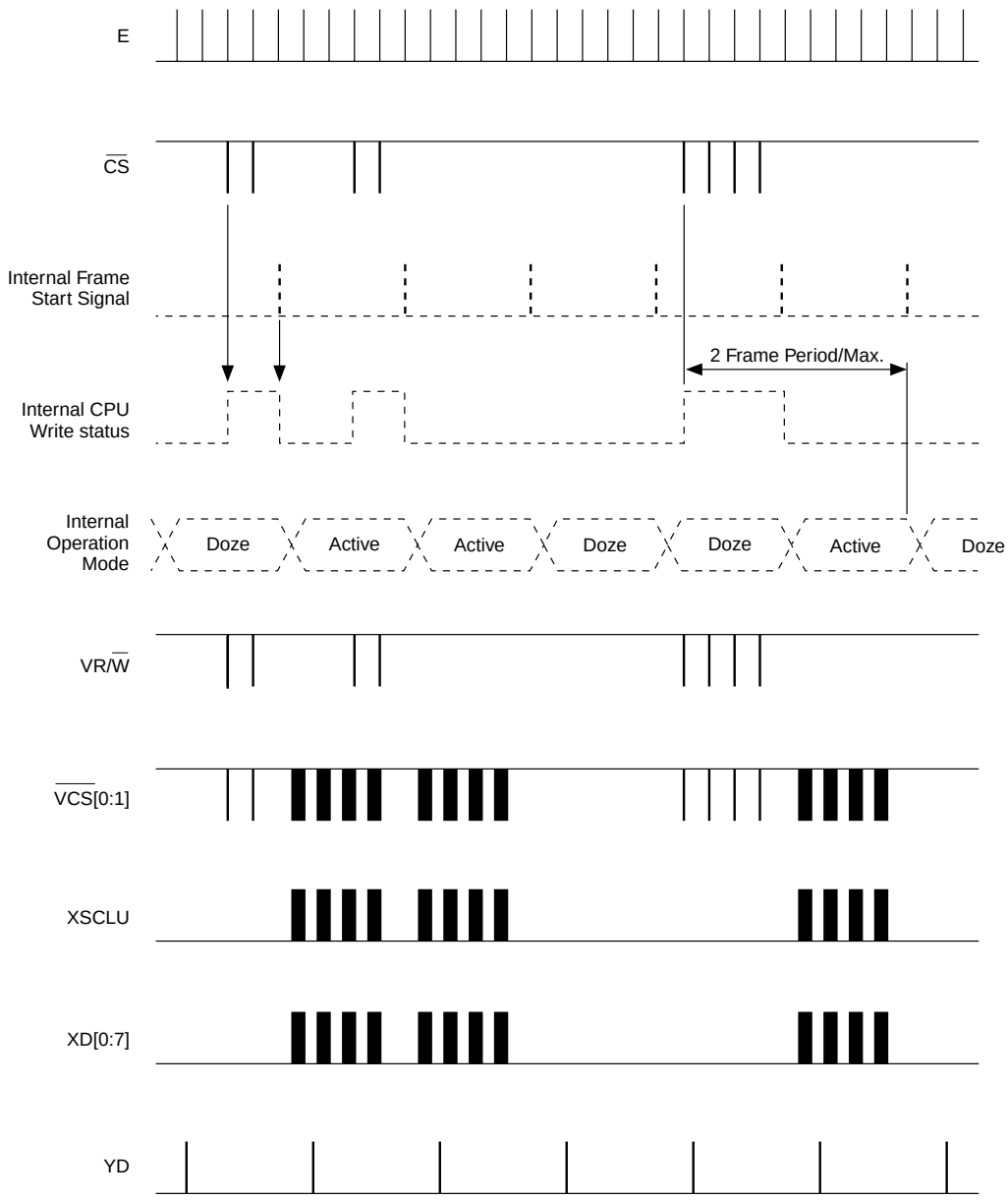


Figure 10. Display Data Auto Transfer Mode

Display Data Manual Transfer Mode

The following figure gives another basic operation mode which SED1360 controls Active Mode with the "Display Data Transfer" command. The figure assumes that the chip is configured in Display Data Manual Transfer Mode.

(1) If the "Display Data Transfer" command is set to the chip, then the next Frame period will be Active Mode. That is the Active Mode is initiated by the Display Data Transfer" command, if the chip is configured in Display Data Manual Transfer Mode.
(2) Once one Frame of display data, which are in the SRAM, are transferred to the LCD Module, the chip switches to Doze Mode and it keeps the Doze Mode until next "Display Data Transfer" command is executed. But if the next "Display Data Transfer" command is set without having any other commands between these two "Display Data Transfer" commands, the next "Display Data Transfer" command is ignored. That is in this case the next "Display Data Transfer" command does not set the chip in the Active Mode.
(3) SED1360 switches the whole LCD Display Subsystem between Doze Mode and Active Mode.
(4) In the Active Mode, SED1360 reads the data from the SRAM, enables "XSCLU" in order to transfer the data stored in the SRAM to the LCD Module, then the RAM integrated Segment Drivers wake up from the power save mode.
(5) In the Doze Mode, SED1360 stops reading the data from the SRAM, disables "XSCLU" in order for the RAM integrated Segment Drivers to enter into the Power Save Mode.

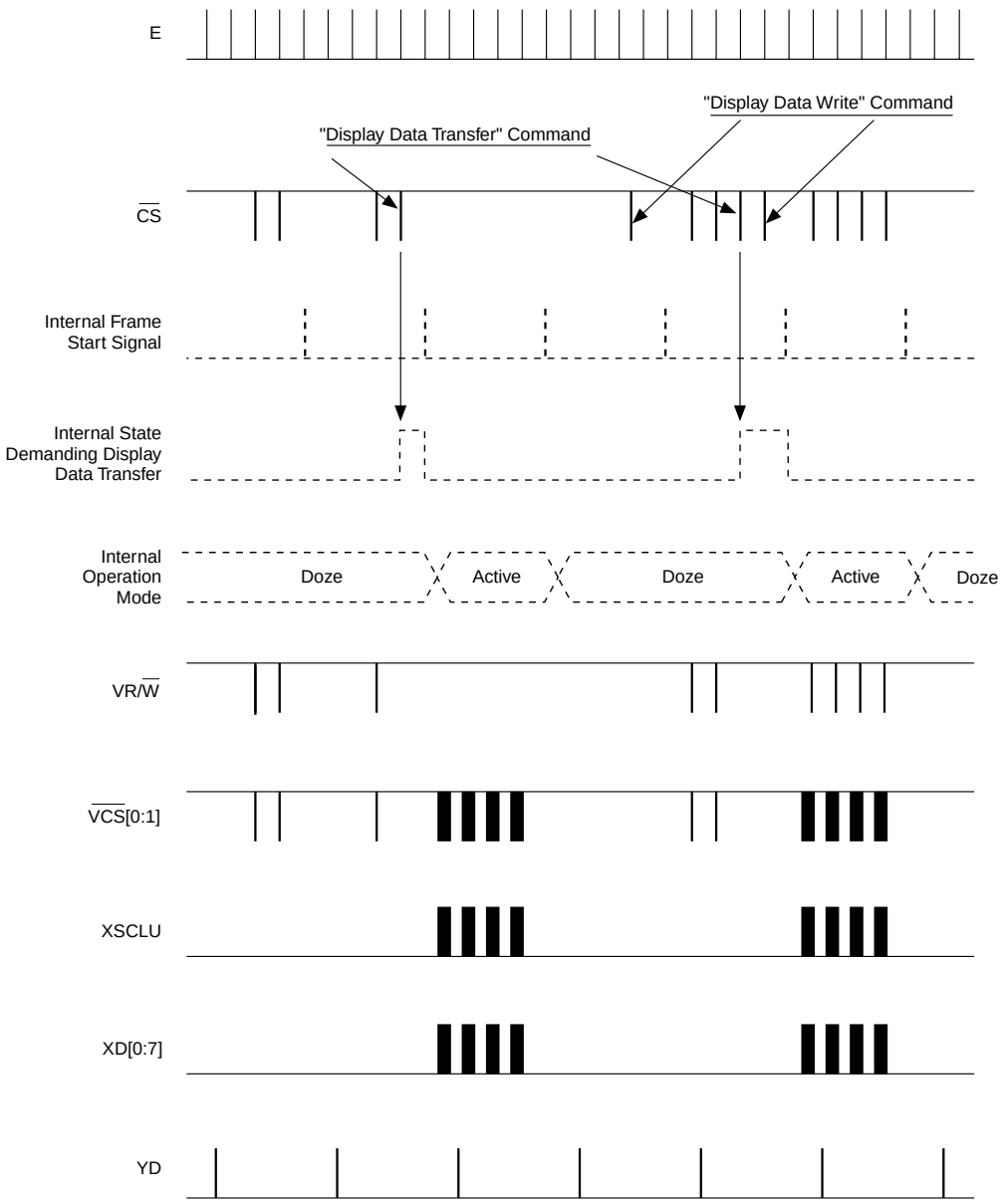


Figure 11. Display Data Manual Transfer Mode

Sleep Mode

SED1360 can enter into the Sleep Mode by setting the "$\overline{\text{SLEEP}}$" signal low. This mode is prepared to shut the whole LCD Display Subsystem off with keeping the data in the SRAM. In the Sleep Mode, the chip will be in the following state.

(1) The internal oscillation is displayed.
(2) VA [0:14] output low, $\overline{\text{VCS}}$ [0:1] output high, VD [0:7] will be high impedance (pins are pulled high by the integrated pull-up resisters).
(3) "FR", "YD", "LP", "XSCLU", "XD [0:7]" and "$\overline{\text{DOFF}}$" output low. $\overline{\text{VOE}}$, VR/$\overline{\text{W}}$ output high.
(4) "D [0:7]", "E" "$\overline{\text{CS}}$", "DT/$\overline{\text{CM}}$" and "$\overline{\text{RESET}}$" are internally masked but they also should be kept in invalid state.

OSCILLATION DESCRIPTION

SED1360's Hardware is optimized to display 320 × 200 LCD panel driven by RAM integrated Segment Drivers as a default chip configuraiton. This section describes how to determine the frequency which is input to OSC1 and how to generate the frequency by using the internal oscillation function.

OSC1 Frequency Determination

Conditions: 320 × 200 single scan LCD panel assumes 60 Hz as an LCD frame frequency

(1) "LP" period is obtained by the following calculation.
$60 \times 200 = 12$ kHz
(2) If an external oscillator is used, the OSC1 frequency can be the same as "LP". Then 12 kHz is the required frequency for OSC1.
(3) If an internal oscillator is used, the oscillation frequency has to be doubled to be 24 kHz. The internal oscillation might be unstable below 24 kHz. So if the required frequency is below 20 kHz, it is recommended to generate doubled frequency. There is a register which divides the internal oscillation frequency by two, four or eight.

Internal Oscillation

The following figure shows how to connect a capacitance and a resistance to the oscillation pins. The values of C and R have to be determined on the actual system.

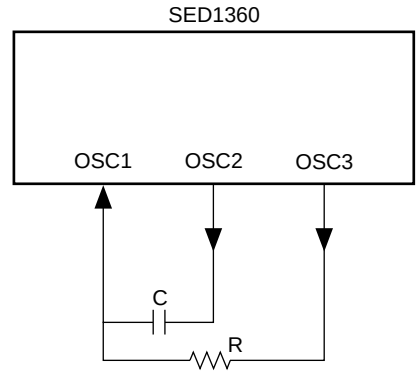


Figure 12. Internal Oscillation Implementation

COMMAND DESCRIPTION

SED1360 has several commands which can manipulate the data transfer procedure between CPU, SRAM, LCD Module and SED1360.

Display Size

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	1	01H

data; DT/$\overline{CM}$ = 1

0	0	HC5	HC4	HC3	HC2	HC1	HC0	data1
VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	data2

(1) This command sets the size of the display.
(2) This command requires two bytes of data which follow this command.
(3) The first data defines a horizontal size of the display in byte unit, and the second data defines a vertical size of the display in line unit.
(4) The horizontal size is set 320 dots and the vertical size is set 200 lines when the "$\overline{RESET}$" signal is set low.

Table 17. Horizontal Size

Hor. size	HC [5:0]
8	00h
16	01h
24	02h
240	1Dh
320	27h
512	3Fh

Table 18. Vertical Size

Ver. size	VC [7:0]
1	00h
2	01h
3	02h
200	C7h
240	Efh
256	Ffh

Display Data Auto Transfer Mode

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	02H

(1) This command configures the chip in the Display Data Auto Transfer Mode. Detailed functional explanation is described in "Display Data Auto Transfer Mode".

Display Data Manual Transfer Mode

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	1	03H

(1) This command configures the chip in the Display Data Manual Transfer Mode. Detailed functional explanation is described in “Display Manual Transfer Mode”.

Display Data Transfer

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	0	04H

(1) This command force the chip to go into the Active Mode so that the chip can start transferring the display data to the LCD Module. Detailed functional explanation is described in “Display Data Manual Transfer Mode”. This command is executable in not only Display Data Manual Transfer Mode but also Display Data Auto Transfer Mode.

Display Data Write

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	1	05H

data; DT/$\overline{CM}$ = 1

*	*	*	*	*	*	*	*	data1
*	*	*	*	*	*	*	*	data2
*	*	*	*	*	*	*	*	datan

(1) This command enables the chip to receive the data as the display data which are stored in SRAM.
(2) Data (data1,…datan) which follow this command are stored in SRAM until other commands are executed. If any other command breaks Display Data Write Access to the SRAM through the chip, this command has to be set again before starting Display Data Write Access.

CPU Write Start Address

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	1	0	06H

data; DT/$\overline{CM}$ = 1

WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA1	data1
WA15	WA14	WA13	WA12	WA11	WA10	WA9	WA8	data2

(1) This command sets the SRAM address which CPU Display Data can be stored.
(2) This command requires two bytes of data which follow this command.
(3) The order of two byte data is that the first data is lower byte and second data is higher byte.
(4) The two bytes of data are temporarily set to the internal CPU Write Address Counter by this command. And the CPU Write Address Counter is increased by one, when CPU Display Data Write Access occurs.

Display Refresh Start Address

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	1	1	07H

data; DT/$\overline{CM}$ = 1

RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA1	data1
RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	data2

(1) This command sets the SRAM address which SED1360 starts reading the data from, to transfer the display data to the LCD Module in Active Mode.
(2) This command requires two bytes of data which follow this command.
(3) The order of two byte data is that the first data is lower byte and second data is higher byte.
(4) The two bytes of data are set to the internal Display Data Refresh Address Counter by this command.

Display ON/$\overline{OFF}$

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	0	0	0	0	ON/$\overline{OFF}$	81H 80H

(1) This command controls "$\overline{DOFF}$" output.
(2) If the ON/$\overline{OFF}$ is set to high "$\overline{DOFF}$" outputs high. If the ON/$\overline{OFF}$ is set to low "$\overline{DOFF}$" outputs low.
(3) The ON/$\overline{OFF}$ is set to low at the reset.

LP Configuration

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	0	0	08H

data; DT/$\overline{CM}$ = 1

0	0	0	0	0	0	FS1	FS0	data1

(1) This command selects "LP" period.
(2) FS1,0 select the period of the signal "LP". The following table shows how to select the required frequency for the signal "LP".
(3) FS [1,0] = [0,0] is set when the "$\overline{RESET}$" signal is set low.

Table 19. LP Frequency

FS1	FS0	LP frequency
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

ERRORTA

This version has one error. About CPU Write Start Address, Values which CPU wrote is increased by one. So, you should set values which is decreased by one.

NOTICE

SED1580

Contents

OVERVIEW

Description

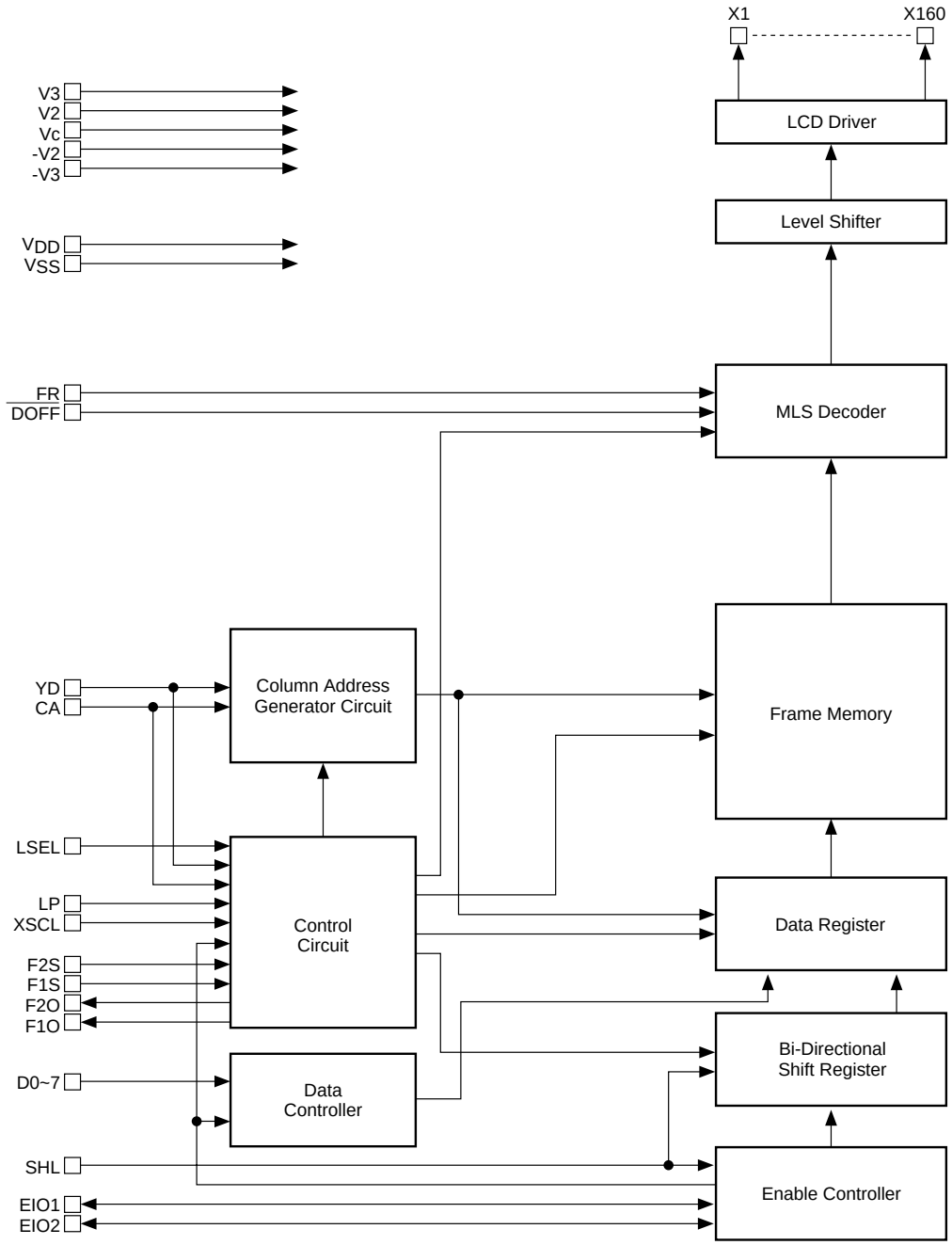
The SED1580 is a 160-output, 5-level segment (column) driver for MLS (Multi-Line Selection) driving, able to drive with both high contrast and high speed. It is used in conjunction with the SED1751. When paired with the SED1751 it can be connected to the SED1360 LCD controller.
Because the SED1580 stores display data in its internal display RAM and generates LC drive signals, display data transmission from the controller can be suspended except for when there are changes to the display, thereby enabling an ultra low power display system.
The SED1580 uses a slim package, facilitating the construction of thinner LCD panels, and the low-voltage operation of its logic power source makes it appropriate to a wide range of applications.

FEATURES

- Number of simultaneous line selects: 4 Lines
- Drive duty ratio (MAX) 1/240 duty
- LCD driver outputs 160 outputs
- Internal display RAM 160×240 bit
- Extremely low consumption current
- Power Source Voltages Logic System: 3.0 to 3.6V (Max)
  LCD System: 6.0 to 7.2V (Max)
- High speed, low power data transmission possible through the 4-bit/8-bit switchable bus enable chain method
- Non-biased display off function
- Output shift direction pin select supported
- Slim chip shape
- Shipment status:
  In CHIP form SED1580D0B
  In TCP form SED1580T0A
- This product is not designed for resistance to light or radiation

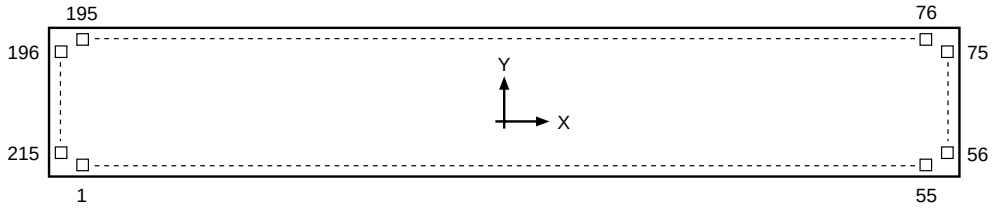
BLOCK DIAGRAM

Block Diagram



PIN CONFIGURATION

Pad Layout



Chip size 12.89 mm × 2.77 mm
Bump pitch: 103 microns (Min.)
Chip thickness: 625 microns ± 15 µm

Bump size (Unit: µm)

Pad number		
	X	Y
56 to 215	67	63
1, 7 to 16, 18 to 36, 38 to 49, 55	74	74
2 to 6, 17, 37, 50 to 54	110	74
22	110	75

Bump specifications (reference values)

Items	Specifications		
	MIN	TYP	MAX
Bump size specifications	–4 µm	Bump size	+4 µm
Bump height specifications	–5.5 µm	22.5 µm	+5.5 µm
Bump strength	30g		

Pin Coordinates

SED1580 Bump Center Coordinates

Units: µm

Pin	Name	X	Y
1	EIO2	–5378	–1240
2	$-V_3$	–5222	
3	$-V_2$	–5044	
4	VC	–4866	
5	V_2	–4688	
6	V_3	–4510	
7	NC	–4322	
8	NC	–4144	
9	NC	–3966	
10	NC	–3789	
11	NC	–3611	
12	F1O	–3449	
13	F2O	–2915	
14	NC	–2266	
15	SHL	–2086	
16	TEST	–1906	
17	V_{SS}	–1726	
18	BSEL	–1546	
19	LSEL	–1366	
20	FR	–1186	
21	YD	–1006	
22	NC	–826	
23	CA	–546	
24	LP	–466	
25	XSCL	–286	
26	D0	163	
27	D1	343	
28	D2	523	
29	D3	703	
30	D4	883	
31	D5	1063	
32	D6	1243	
33	D7	1423	
34	F2S	1603	
35	F1S	1783	
36	$\overline{DOFF}$	1963	
37	V_{DD}	2143	
38	NC	2387	
39	NC	2564	
40	NC	2742	
41	NC	2920	
42	NC	3098	
43	NC	3275	
44	NC	3453	
45	NC	3631	
46	NC	3809	
47	NC	3986	
48	NC	4164	
49	NC	4342	
50	V_3	4722	
51	V_2	4900	
52	V_C	5077	
53	$-V_2$	5255	
54	$-V_3$	5433	
55	EIO1	5629	
56	X1	6303	–1009
57	X2		–903
58	X3		–797
59	X4		–690
60	X5		–584
61	X6		–478
62	X7		–371
63	X8		–265
64	X9		–159
65	X10		–53
66	X11		53
67	X12		159
68	X13		265
69	X14		372
70	X15		478
71	X16		584
72	X17		690
73	X18		797
74	X19		903
75	X20		1009
76	X21	6098	1246
77	X22	5995	
78	X23	5893	
79	X24	5790	
80	X25	5688	
81	X26	5585	
82	X27	5483	
83	X28	5380	
84	X29	5278	
85	X30	5175	
86	X31	5073	
87	X32	4970	
88	X33	4868	
89	X34	4765	
90	X35	4663	
91	X36	4560	
92	X37	4458	
93	X38	4355	
94	X39	4253	
95	X40	4150	
96	X41	4048	
97	X42	3945	
98	X43	3843	
99	X44	3740	
100	X45	3637	
101	X46	3535	
102	X47	3432	
103	X48	3330	
104	X49	3227	
105	X50	3125	
106	X51	3022	
107	X52	2920	
108	X53	2817	
109	X54	2715	
110	X55	2612	
111	X56	2510	
112	X57	2407	
113	X58	2305	
114	X59	2202	
115	X60	2100	
116	X61	1997	
117	X62	1895	
118	X63	1792	
119	X64	1690	
120	X65	1587	
121	X66	1485	
122	X67	1382	
123	X68	1280	
124	X69	1177	
125	X70	1075	1246
126	X71	972	
127	X72	870	
128	X73	767	
129	X74	665	
130	X75	562	
131	X76	460	
132	X77	357	
133	X78	255	
134	X79	152	
135	X80	50	
136	X81	–52	
137	X82	–154	
138	X83	–257	
139	X84	–359	
140	X85	–462	
141	X86	–564	
142	X87	–567	
143	X88	–769	
144	X89	–872	
145	X90	–974	
146	X91	–1077	
147	X92	–1179	
148	X93	–1282	
149	X94	–1385	
150	X95	–1487	
151	X96	–1590	
152	X97	–1692	
153	X98	–1795	
154	X99	–1897	
155	X100	–2000	
156	X101	–2102	
157	X102	–2205	
158	X103	–2307	
159	X104	–2410	
160	X105	–2512	
161	X106	–2615	
162	X107	–2717	
163	X108	–2820	
164	X109	–2922	
165	X110	–3025	
166	X111	–3127	
167	X112	–3230	
168	X113	–3332	
169	X114	–3435	
170	X115	–3537	
171	X116	–3640	
172	X117	–3742	
173	X118	–3845	
174	X119	–3947	
175	X120	–4050	
176	X121	–4152	
177	X122	–4255	
178	X123	–4357	
179	X124	–4460	
180	X125	–4562	
181	X126	–4655	
182	X127	–4767	
183	X128	–4870	
184	X129	–4972	
185	X130	–5075	
186	X131	–5177	

Units: µm

Pin	Name	X	Y
187	X132	–5280	1246
188	X133	–5382	
189	X134	–5485	
190	X135	–5587	
191	X136	–5690	
192	X137	–5792	
193	X138	–5895	
194	X139	–5997	
195	X140	–6100	
196	X141	–6303	1009

Pin	Name	X	Y
197	X142	–6303	903
198	X143		797
199	X144		690
200	X145		584
201	X146		478
202	X147		372
203	X148		265
204	X149		159
205	X150		53
206	X151		–53

Pin	Name	X	Y
207	X152	–6303	–159
208	X153		–265
209	X154		–371
210	X155		–478
211	X156		–584
212	X157		–690
213	X158		–797
214	X159		–903
215	X160		–1009

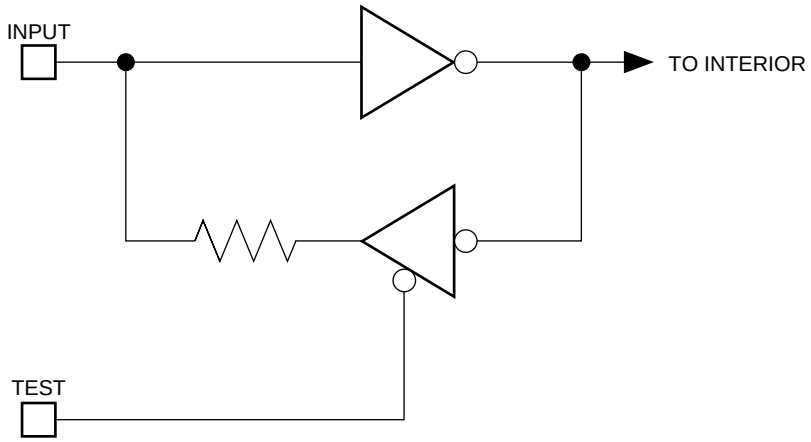
Pin Functions

Pin Functions Table

Pin Name	I/O	Function	# of Pins
X1 to X160	O	Segment (column) output to drive the LC. Output transition occurs on falling edge of LP.	160
BSEL	I	Display data input bit number select input. “L”: 4 bit input. “H”: 8 bit input.	1
LSEL	I	1/2 H operation select input. “L”: Normal operation. “H”: 1/2 H operation.	1
D0 to D7	I	Display data input. When 4 bit input is used, D0 to D3 is used, and D4 to D7 can be left NC.	8
XSCL	I	Display data shift clock input. Display data (D0 to D7) is read sequentially into the data register on the falling edge.	1
LP	I	Display data latch clock input * Accepts into the LCD driver the control signal from the LC driver selected by the MLS decoder, doing so at the falling edge, and outputs the LC driver output. * Writes the contents of the data registers to the frame memory 4 LP at a time for the specified column address. * Resets the enable control circuit. * When 1/2 operation is selected, inputs the LP with twice the normal frequency.	1
EIO1 EIO2	I/O	Enable I/O * Is set to input or output depending on the SHL input level. * When output, the LP input is reset (in an “H” state), and when the 160 bit of display data has been read in, the signal automatically falls to L. * When connected in cascade, is connected to the next stage EIO input.	1 1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th># of Pins</th></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and EIO terminal I/O control input.
<u>WHEN BSEL = “L” (i.e. 4-bit input):</u>
When the display data has been input to terminals (D3, D2, D1, D0) in the order (a, b, c, d) (e, f, g, h)... (w, x, y, z), the relationship between the data and the segment is as shown in the table below:
<table>
<tr><td rowspan="2">SHL</td><td colspan="20">Xn (Segment Output)</td><td colspan="2">EIO</td></tr>
<tr><td>160</td><td>159</td><td>158</td><td>157</td><td>156</td><td>155</td><td>154</td><td>153</td><td>...</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>...</td><td>s</td><td>t</td><td>u</td><td>v</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>...</td><td>h</td><td>g</td><td>f</td><td>e</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
<u>WHEN BSEL = “H” (i.e., 8-bit input):</u>
When the display data has been input to terminals (D7, D6, D5, D4, D3, D2, D1, D0) in the order (a, b, c, d, e, f, g, h) ... (s, t, u, v, w, x, y, z), the relationship between the data and the segment is as shown in the table below:
<table>
<tr><td rowspan="2">SHL</td><td colspan="20">Xn (Segment Output)</td><td colspan="2">EIO</td></tr>
<tr><td>160</td><td>159</td><td>158</td><td>157</td><td>156</td><td>155</td><td>154</td><td>153</td><td>...</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>...</td><td>s</td><td>t</td><td>u</td><td>v</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>...</td><td>h</td><td>g</td><td>f</td><td>e</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input.
When at “L” level, segment output is forced to Vc. The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1).</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Frame running start input
* Resets the column address for writing or reading.
* The number of running lines for writing (column address number) relating to frame memory is determined based on the number of LP pulses input during a single YD cycle.</td><td>1</td></tr>
<tr><td>CA</td><td>I</td><td>Field delimiter signal input. With terminator (*1).
This signal is input at the start of each new field, and is output by the SED1751.</td><td>1</td></tr>
<tr><td>F1S
F2S</td><td>I</td><td>Drive pattern cutover gap set input
(F2S, F1S) = (0,0), (0,1), (1,0), (1,1)
Cutover gap Field, 8H, 2H, 4H</td><td>1
1</td></tr>
<tr><td>F1O
F2O</td><td>O</td><td>Driver pattern select output for the Y driver. Connects to the common (row) driver.</td><td>1
1</td></tr>
<tr><td>TEST</td><td>I</td><td>Test input. Normally fixed at “L”.</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power</td><td>Power supply for logic.</td><td>1 each</td></tr>
<tr><td>V_3, V_2, V_C, $-V_2$, $-V_3$</td><td>Power</td><td>Power supply for LC driver. $V_3 > V_2 > V_C > -V_2 > -V_3$</td><td>5 each</td></tr>
</table>

Note: *1 Regarding the terminator


INPUT
TO INTERIOR
TEST

FUNCTIONS

The Functional Blocks

Enable Control

When the enable signal is in a disable state (EIO = "H"), the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.
When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to "VSS".
The enable control circuit automatically senses when 160 bits worth of data have been received, and automatically sends the enable signal, thus eliminating the need for a control signal from the control LSI.

Bi-directional Shift Register

This sends the control signal for writing the display data D0 – D7 to the data register. The order in which the display data is latched into the data register by the SHL input is returned (SIC? Reversed?).

Data Register

This is a 160 dot register which controls writing to the display RAM. It has 4 lines. At each falling edge of the LP signal it accepts display data from one line, and writes to the frame memory after it has stored 4 lines of data.

Frame Memory

This is static RAM (with peripheral circuits) that stores LC display data. It has a capacity of 160 segments by 240 lines.

MLS Decoder

This outputs the drive control signals necessary for the 4 MLS driving. The control signal is set by field information provided by the four lines of display data, FR, DOFF, and the control circuit.

LCD Driver

The LCD driver outputs the LC drive voltage. The driver voltage is selected by the control signal from the 5 levels V3, V2, VC, –V2 and –V3, determined by the MLS decoder.

Column Address Generating Circuit

When writing to or reading from frame memory, this outputs the column address corresponding to the location of the RAM in frame memory.

Level Shifter

This is a level interface circuit used to convert signal levels when signals are propagated from low-voltage parts to high-voltage parts.

Data Control

This accepts display data input when enabled, and sends it to the data register.

Control Circuit

This determines the self refresh rate, enables the data register to write to the display RAM, controls the output of the column address generator, and performs field control on the MLS decoder.

The Self Refresh Function

Setting the Self Refresh Mode

"Self refresh mode" refers to a situation where the transmission of display data from the display controller to the SED1580 is suspended when the content of the display does not change, and where the SED1580 automatically senses this and enters a power down display mode.
To place the SED1580 in the self refresh mode maintain the shift clock XSCL at the "L" level during four horizontal display periods (4x the LP signal period) after the completion of the input of the display data of an n + 3 line.
When the XSCL is suspended, the power is reduced, so display data inputs D0 – D7 are suspended, as is transmission from the display controller, being set to "H" or "L". At this time the display controller must send LP, YD, or FR signals periodically to the SED1580 as it does when data is being sent. The SED1580 receives these signals, periodically reads display data from its internal RAM, and refreshes the display. The display off function is operational even when in the self refresh mode.

Getting Out of the Self Refresh Mode

In order to get out of the self refresh mode, the display controller inputs the shift clock XSCL to the SED1580 for four or more horizontal display periods with the timing of the data transmission from the falling edge of the LP signal at the time of an n + 3 line. With the falling edge of the LP signal after the fourth horizontal period after getting out of this mode, the display data transmitted during the four horizontal display intervals is written to frame memory.
When SED1580s are cascade connected, if the number of XSCL clocks input does not correspond to the cascade connections, then not all of the SED1580s will be released from self refresh mode.

Note: When the number of lines is 240:

n lines	1, 5, 9, ...233, 237 (1 + multiples of 4)
n + 1 lines	2, 6, 10,...234, 238 (2 + multiples of 4)
n + 2 lines	3, 7, 11,...235, 239 (3 + multiples of 4)
n + 3 lines	4, 8, 12,...236, 240 (Multiples of 4)

The Relationship Between Drive Output Voltages and Display Data

F20, F10, and the common drive voltage have the following relationships:

FR	**L**				**H**			
F1O **F2O**	**1** **1**	**0** **1**	**1** **0**	**0** **0**	**1** **1**	**0** **1**	**1** **0**	**0** **0**
n line	V1	V1	–V1	V1	–V1	–V1	V1	–V1
n + 1 line	–V1	V1	V1	V1	V1	–V1	–V1	–V1
n + 2 line	V1	–V1	V1	V1	–V1	V1	–V1	–V1
n + 3 line	V1	V1	V1	–V1	–V1	–V1	–V1	V1

Note: Voltage relationships: V1 > VC > –V1 (VC is the middle voltage level)

The transitions in (F2O, F1O) within each field when the drive pattern changes:

First field	In the order (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0)
Second field	In the order (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1)
Third field	In the order (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0)
Fourth field	In the order (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1)

This is determined by the values of the inputs (F2S, F1S) during the changeover interval. The relationship between F2S and F1S and the changeover interval is as follows:

When the changeover interval is selected for each field, the value stored in the field is the first value shown in the shown in the (F2O, F1O) change table above (the value on the left).

F2S	F1S	Changeover Interval
0	0	Field
0	1	8-line interval
1	0	2-line interval
1	1	4-line interval

The relationship between the display data, the LC AC signal FR, and the segment output voltage is as shown below. The output voltage changes in conjunction with the F20, F10 values that determine the common drive voltage.

Display data: 0= not lit, 1 = lit

When FR = "L"

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O) = (1,1)	V_2	V_C	V_C	$-V_2$	V_3	V_2	V_2	V_C	V_C	$-V_2$	$-V_2$	$-V_3$	V_2	V_C	V_C	$-V_2$
	(F2O, F1O) = (1,0)	V_2	V_C	V_3	V_2	V_C	$-V_2$	V_2	V_C	V_C	$-V_2$	V_2	V_C	$-V_2$	$-V_3$	V_C	$-V_2$
	(F2O, F1O) = (0,1)	V_2	V_C	V_C	$-V_2$	V_C	$-V_2$	$-V_2$	$-V_3$	V_3	V_2	V_2	V_C	V_2	V_C	V_C	$-V_2$
	(F2O, F1O) = (0,0)	V_2	V_3	V_C	V_2	V_C	V_2	$-V_2$	V_C	V_C	V_2	$-V_2$	V_C	$-V_2$	V_C	$-V_3$	$-V_2$

When FR = "H"

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O) = (1,1)	$-V_2$	V_C	V_C	V_2	$-V_3$	$-V_2$	$-V_2$	V_C	V_C	V_2	V_2	V_3	$-V_2$	V_C	V_C	V_2
	(F2O, F1O) = (1,0)	$-V_2$	V_C	$-V_3$	$-V_2$	V_C	V_2	$-V_2$	V_C	V_C	V_2	$-V_2$	V_C	V_2	V_3	V_C	V_2
	(F2O, F1O) = (0,1)	$-V_2$	V_C	V_C	V_2	V_C	V_2	V_2	V_3	$-V_3$	$-V_2$	$-V_2$	V_C	$-V_2$	V_C	V_C	V_2
	(F2O, F1O) = (0,0)	$-V_2$	$-V_3$	V_C	$-V_2$	V_C	$-V_2$	V_2	V_C	V_C	$-V_2$	V_2	V_C	V_2	V_C	V_3	V_2

When $\overline{DOFF}$ = "L", all drive outputs are tied to the V_C level.

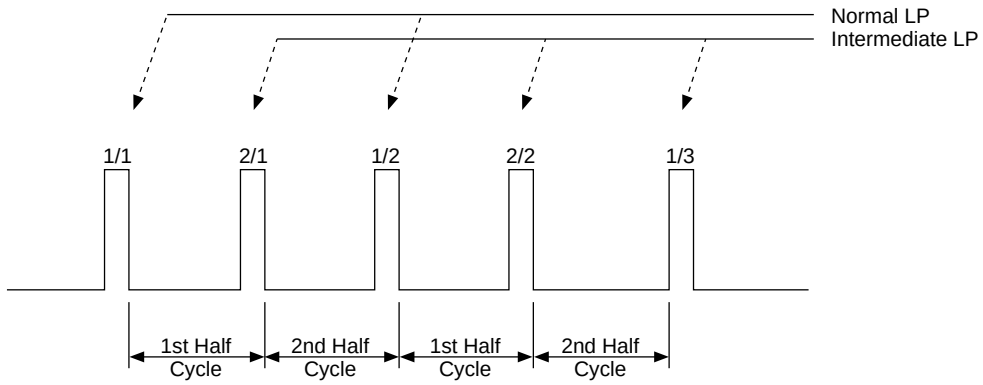
LC Drive Output Voltages During 1/2 H Operation

When LSEL is set to "H" and twice the normal frequency is applied to the LP input terminal, then the chip functions in 1/2 mode. Each time LP is input the field data changes, thus the output changes at the center point of the 1H interval. However, the input of display data to the D1580, writing of display data to the frame memory, and read in display data from the frame memory is the same as in the normal drive.
The Y driver output changes according to the field data output by the X driver with each LP input, causing a transition at the center point of the 1H interval; however, the transition of the drive line occurs each 1H, just as in the normal drive.
During 1/2 H operation, the changes of the F20, F10 in each field are as shown in the table below. In this table the statuses of the F20 and F10 are represented as given below:

(F2O, F1O) = (1,1)	(1)
(F2O, F1O) = (1,0)	(2)
(F2O, F1O) = (0,1)	(3)
(F2O, F1O) = (0,0)	(4)

	First Half Cycle	Second Half Cycle	First Half Cycle	Second Half Cycle	
Field #1	(4)	(1)	(1)	(4)	
Field #2	(1)	(4)	(4)	(1)	This pattern is
Field #3	(3)	(2)	(2)	(3)	repeated hereafter.
Field #4	(2)	(3)	(3)	(2)	

During 1/2H operation, the values of F2S and F1S are ignored.

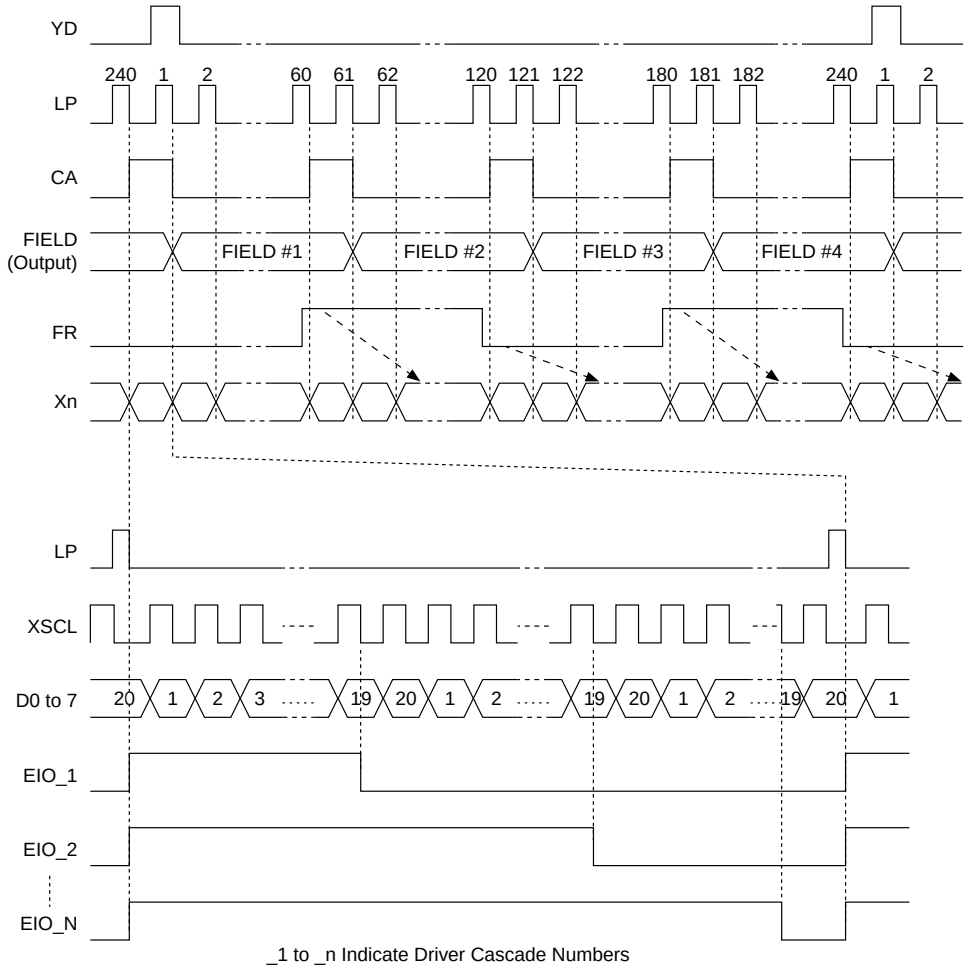


The segment output voltage during 1/2 H operation also follows the display data of 4.3 and the diagram showing the relationship between the LC AC signal FR and the segment output voltage. In the signal B/A that indicates the number of the LP, the “A” in the figure indicates LP during a normal drive, and “B” differentiates between the normal LP and the intermediate LP (where B = 1 is normal and B = 2 is intermediate).

Timing diagram (assuming 1/240 duty)

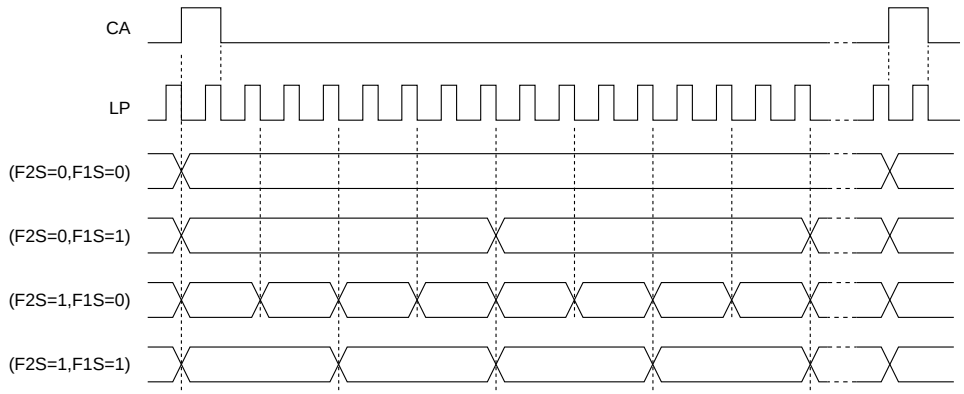
(This diagram provided only as a reference.)

Normal Drive Timing

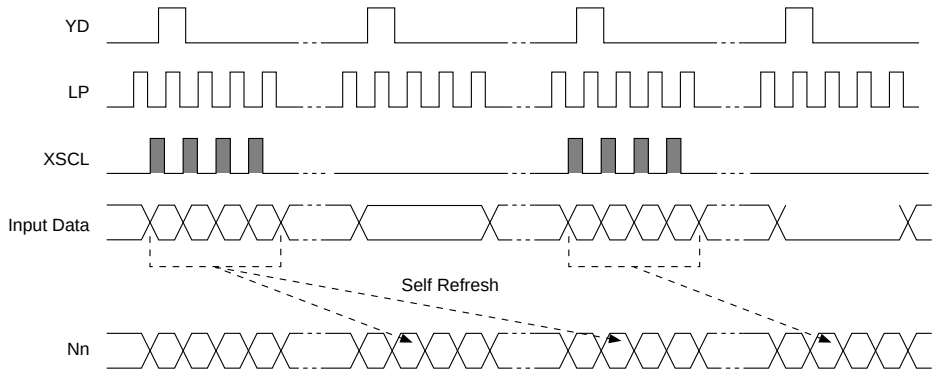


_1 to _n Indicate Driver Cascade Numbers

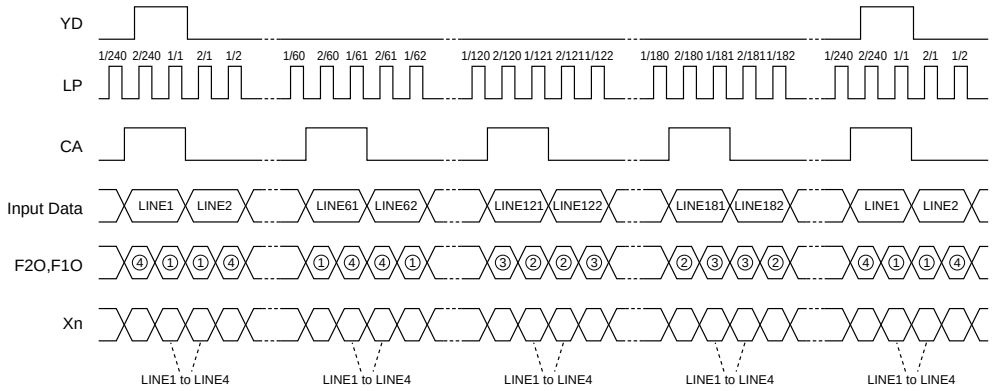
F2O, F1O Change Timing



Setting and Releasing Self Refresh



1/2 H Drive Timing



ELECTRICAL CHARACTERISTICS

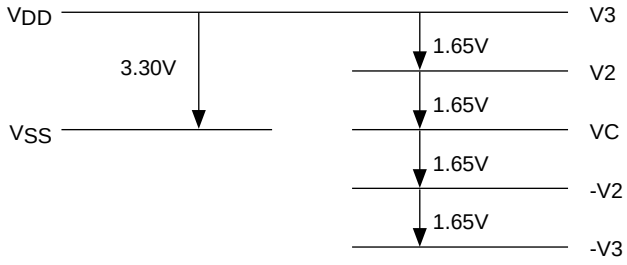
Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	$–V_3$	–8.0 to +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I_{O1}	20	mA
Operating temperature	Topr	–20 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

Note 1: The voltages are all relative to V_{DD} = 0V.

Note 2: Storage temperature 1 is the recommendation for the chip itself or for the chip and a plastic package, and storage temperature 2 is the recommendation for the chip mounted on TCP.

Note 3: Ensure that the relationship between V_3, V_2, V_C, $–V_2$ and $–V_3$ is always as follows:
$V_{DD} \geq V_3 > V_2 > V_C > –V_2 > –V_3$



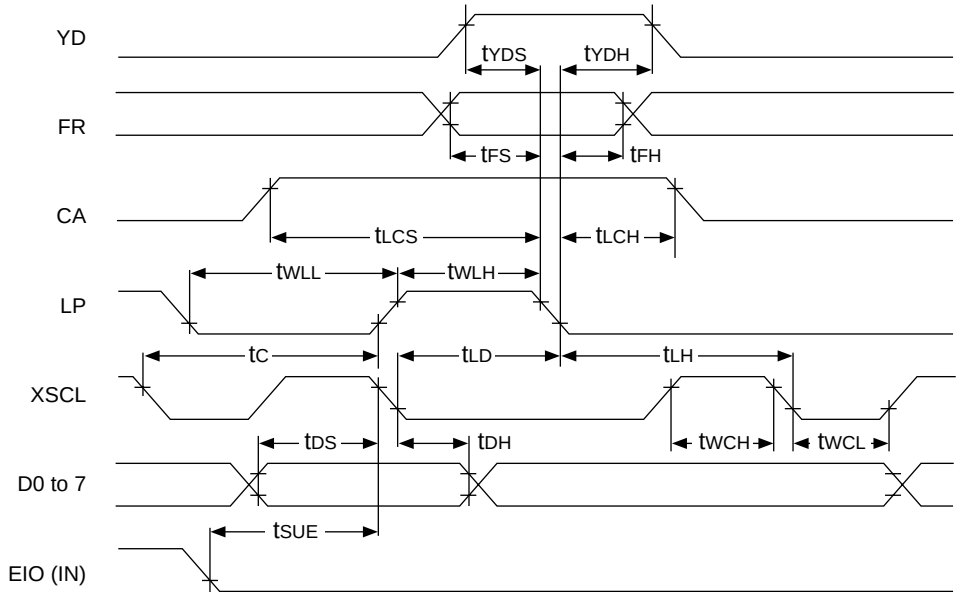
DC Characteristics

Unless otherwise specified, V_{DD} = V3 = 0V, V_{SS} = –3.3V ± 0.3V, Ta = –20 to 85°C

Parameter	Symbol	Conditions	Applicable terminals	Min	Typ	Max	Units
Power voltage (1)	V_{SS}		V_{SS}	–3.6	–3.3	–3.0	V
Power voltage (2)	$–V_3$	V_{SS} = –3.0V to –3.6V	$–V_3$	–7.2	–6.4	–6.0	V
Power voltage (3)	$–V_2$	V_{SS} = –3.0V to –3.6V	$–V_2$		$(–V_3)$* 3/4		V
Power voltage (4)	V_C	V_{SS} = –3.0V to –3.6V	V_C		$(–V_3)$* 2/4		V
Power voltage (5)	V_2	V_{SS} = –3.0V to –3.6V	V_2		$(–V_3)$* 1/4		V
High-level input voltage	V_{IH}	V_{SS} = –3.3V to –3.6V	EIO1, EIO2, SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$	0.2* V_{SS}			V
Low-level input voltage	V_{IL}					0.8* V_{SS}	V
High-level output voltage	V_{OH}	V_{SS} = –3.3V to –3.6V	I_{OH} = –0.6mA; EIO1, EIO2 F1O, F2O	V_{DD} – 0.4			V
Low-level output voltage	V_{OL}		I_{OL} = 0.6mA; EIO1, EIO2 F1O, F2O			V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$			5.0	µA
I/O leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$	EIO1, EIO2			5.0	µA
Static current (1)	Issq	V_{IN} = V_{DD} or V_{SS}	V_{SS}			10	µA
Static current (2)	$–I_{3T}$	$–V_3$ = –6.6V	$–V_3$			5	µA
Output resistance	R_{SEG}	ΔV_{ON} = 0.5V, V_{SS} = –3.30V, V_3 = V_{DD} = 0V, V_2 = –1.65V, V_C = –3.30V, $–V_2$ = –4.95V, V_3 = 6.60V	X1 to X160		0.8	1.5	KΩ
Average operating consumption current (1) Data Transfer Mode	Isst	V_{SS} = –3.30V, V_3 = V_{DD} = 0V, V_2 = –1.65V, V_C = –3.30V, $–V_2$ = –4.95V, $–V_3$ = –6.60V, V_{IN} = V_{DD} or V_{SS}, f_{XSCL} = 480 kHz, f_{LP} = 12kHz, f_{FR} = 30Hz, Input Data: checker pattern, 8-bit, 320 × 200, no load	V_{SS}		70	100	µA
Average operating consumption current (1) Self Refresh Mode	Isss	XSCL = V_{SS} Other parameters are the same as for Isst			50	70	µA
Average operating consumption current (2)	$–I_{3T}$	Parameters are the same as for Isst	$–V_3$		10	20	µA
Input terminal capacitance	CI	Freq = 1 MHz, Ta = 25°C, Chip alone	SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, $\overline{DOFF}$			8	pF
I/O terminal capacitance	CI/O		EIO1, EIO2			15	pF
Output terminal capacitance	CO		F1O, F2O			7	pF

AC Characteristics

Input Timing Characteristics

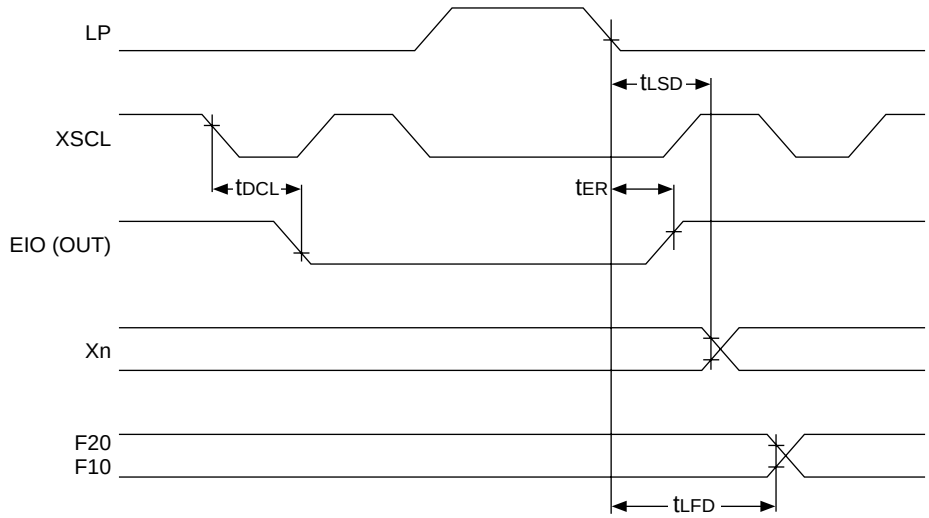


V_{SS} = –3.3 V ± 0.3 V, V_{IH} = 0.2 V_{SS}, V_{IL} = 0.8 V_{SS}

Parameter	Symbol	Conditions	Min	Max	Units
XSCL period	t_C		150		ns
XSCL high level pulse width	t_{WCH}		20		ns
XSCL low level pulse width	t_{WCL}		20		ns
Data setup time	t_{DS}		10		ns
Data hold time	t_{DH}		10		ns
Time between XSCL and LP fall	t_{LD}		10		ns
Time between LP and XSCL fall	t_{LH}		150		ns
LP high level pulse width	t_{WLH}		100		ns
LP low level pulse width	t_{WLL}		100		ns
FR setup time	t_{FS}		25		ns
FR hold time	t_{FH}		10		ns
EIO setup time	t_{SUE}		30		ns
YD setup time	t_{YDS}		50		ns
YD hold time	t_{YDH}		50		ns
CA setup time	t_{LCS}		10		µs
CA hold time	t_{LCH}		–200	200	ns
Input signal rise time and fall time	tr, tf			30	ns

Note: CA is only effective at the first LP in the field. Assuming 1/N duty, the “first LP” refers to 1 and 1+ (multiples of (N/4).
FR is accepted at the falling edge of LP, and its state is reflected into the output that changes at the falling edge the following 1H.

Output Timing Characteristics

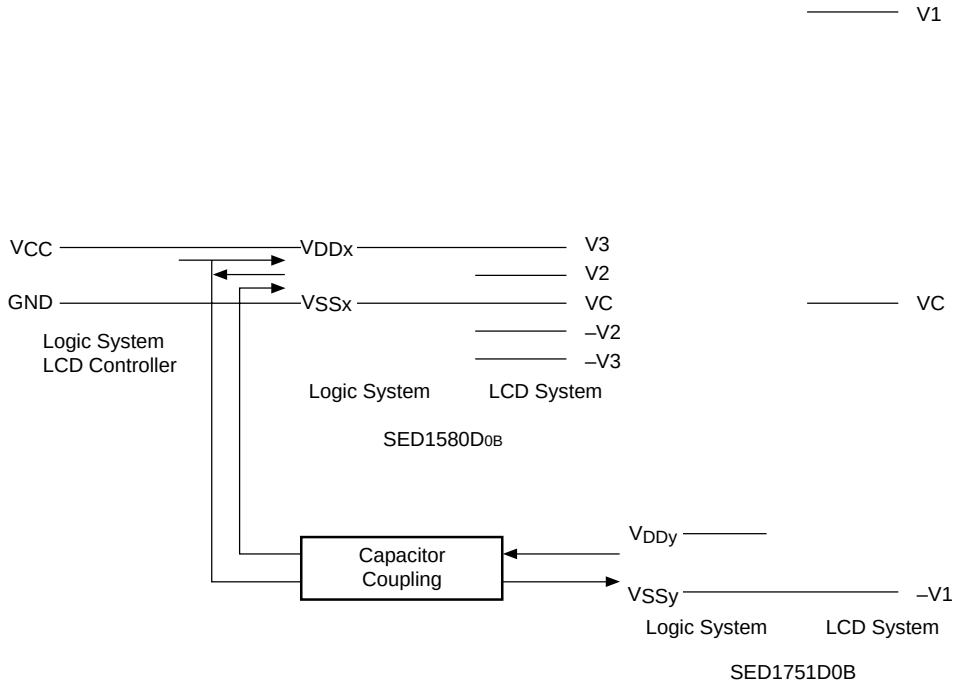


V_{SS} = –3.3V ± 0.3V, V_{IH} = 0.2 V_{SS}, V_{IL} = 0.8 V_{SS}, –V_3 = –6.6V ± 0.6V

Parameter	Symbol	Conditions	Min	Max	Units
EIO reset time	t_{ER}	C_L = 15 pF (EI0)		80	ns
EIO output delay time	t_{DCL}			90	ns
LP → Xn output delay time	t_{LSD}	CL = 100 pF		400	ns
LP → F2O, F1O output delay time	t_{LFD}			3000	ns

POWER SOURCE

The Relationship Between Voltage Levels



When the SED1580 and SED1751 are used to structure an extremely low-power module system, the power supplies for the SED1580 logic systems and LCD systems, and the power supplies for the LCD controller should have the voltage relationships shown in the figure above.
In this case, caution is required when sending signals to the logic system. Specifically, use caution with the following:

LCD Controller	→	SED1580	Direct connection
LCD Controller	→	SED1751	Requires a capacitor coupling
SED1580	→	SED1751	Requires a capacitor coupling
SED1751	→	SED1580	Requires a capacitor coupling

Cautions During Power Up and Power Down

This LSI requires special attention to be paid to the sequence in which the power supplies are turned on. Ensure that the power supply ON sequence is always one of the sequences below:

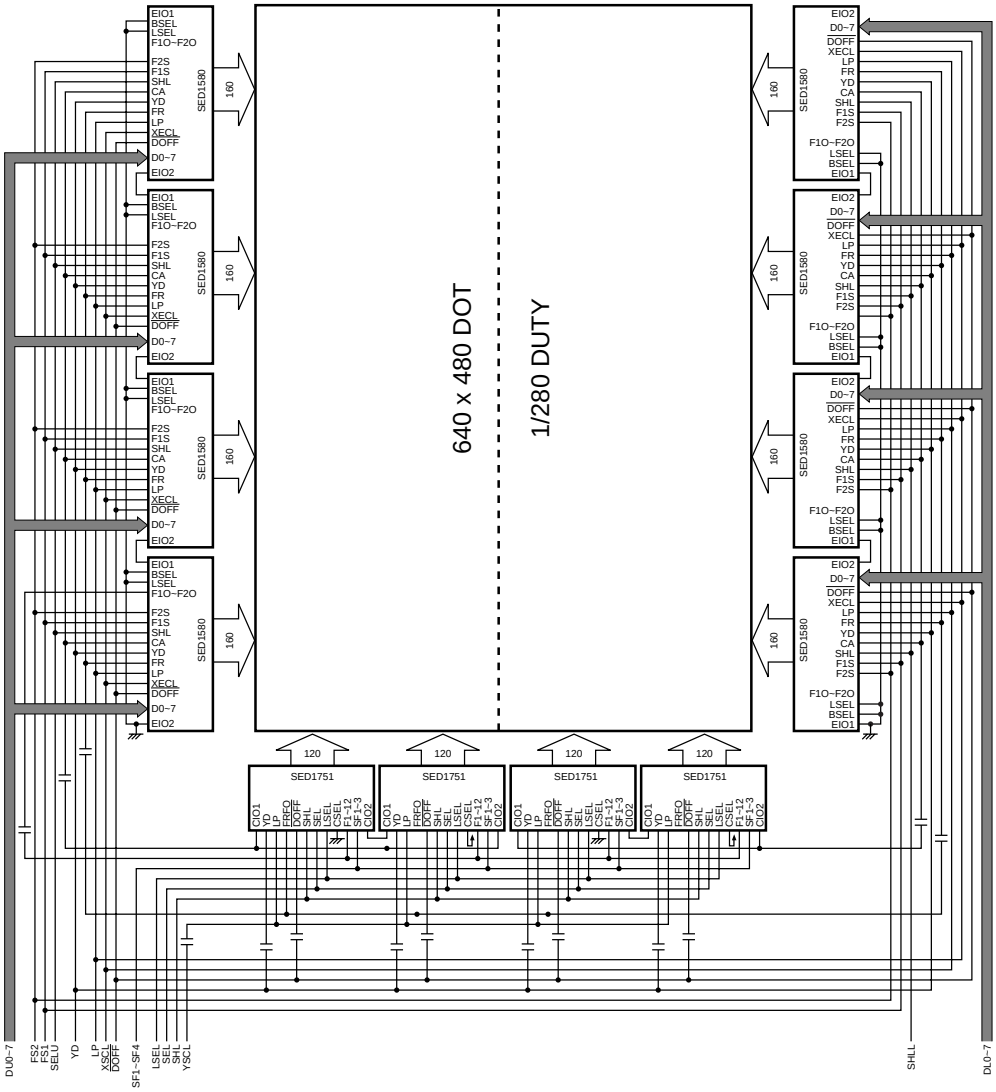
Logic system ON → First LP cycle → LCD system ON

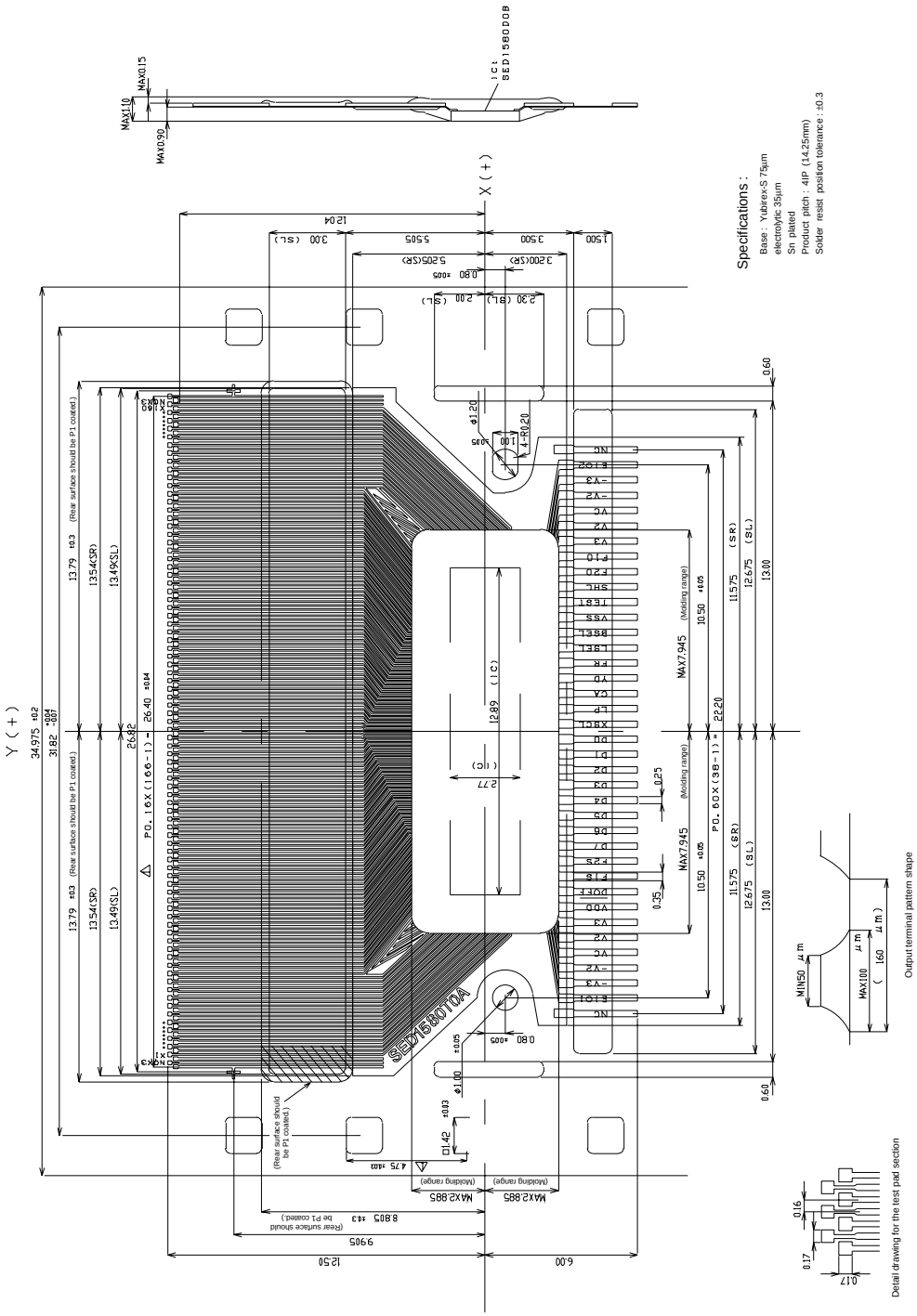
or

Logic system ON → $\overline{\text{DOFF}}$ = "L" → LCD system ON → First LP cycle (*2) → $\overline{\text{DOFF}}$ = "H"

After applying power to the SED1580, the 2 frame interval is not displayed correctly because the number of LP cycles input in the first frame is counted and used to determine an address in the frame memory. This requires the use of $\overline{\text{DOFF}}$. Consequently, display data should be transmitted at the point marked with (*2). For power down, use the LCD system OFF → Logic system OFF sequence, or power both down at the same time.

EXAMPLE OF EXTERNAL CONNECTIONS




Specifications :
Base : Yubirex-S 75µm
electrolytic 35µm
Sn plated
Product pitch : 4IP (14.25mm)
Solder resist position tolerance : ±0.3
X (+)
Y (+)
SED1580T0A
Output terminal pattern shape
Detail drawing for the test pad section

Notes

Regarding this development specification, take the followings into consideration.

1. The contents of this development specification may be revised without prior notice.
2. This development specification does not guarantee or grant the industrial property rights or any other rights.
   The application examples contained in this development manual are given in order to help customers understand the product. Note that we shall not take any responsibility regarding problems on circuits.
   Regarding the use of semiconductor elements, take the followings into consideration.

[Precautions on Handling Optical Parts]

Following the solar cell theory, the characteristics of a semiconductor element changes as it is exposed to the light. Therefore, if this IC is exposed to the light, malfunction may occur.

(1) Design and mount the IC so that it won't be exposed to the light when in use.
(2) Design and mount the IC so that it won't be exposed to the light in the inspection process.
(3) Be concerned about shading of all the surfaces (front, back and side) of the IC.

SED1590

Contents

OVERVIEW

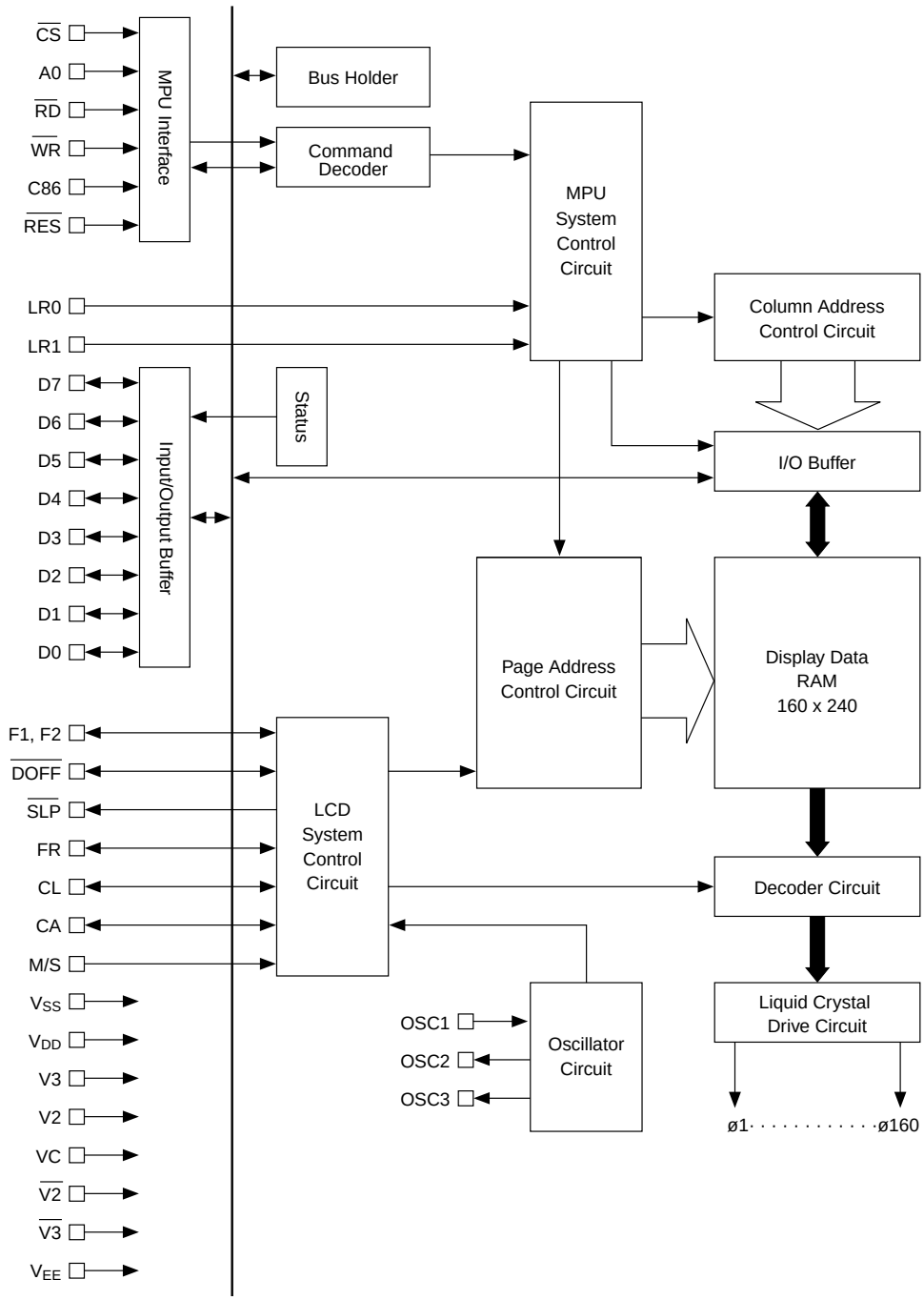
Description

The SED 1590 is a high image quality mid-display-size-compatible RAM-integrated segment (column) driver that boasts the low power consumption required by portable devices. It is used in a set with the SED 1751 common (row) driver and the SCI 7500 power supply IC.
The SED 1590 can be connected directly to the MPU bus. It stores in its internal display RAM memory the 8-bit parallel display data sent to it from the MPU and then issues the LCD drive signals independent of the MPU. The chip has 160 LCD drive outputs and is equipped with 160 out × 240 line internal display RAM. Furthermore, because there is a one-to-one correspondence between picture elements on the LCD display and internal RAM dots, displays can be created with a high degree of flexibility.
Because it is not necessary to supply an external clock when writing to the SED 1590 internal RAM from the MPU side, these operations can be performed with an absolute minimum power consumption. Moreover, even when multiple SED 1590 chips are used, single chip select is supported; thus it is not necessary for the MPU to distinguish between the multiple chips.
The SED 1590 has a slim form that is useful in creating thinner LCD panels. It can operate using a low-voltage logic power supply system, and is thus suited to a broad range of applications.

Features

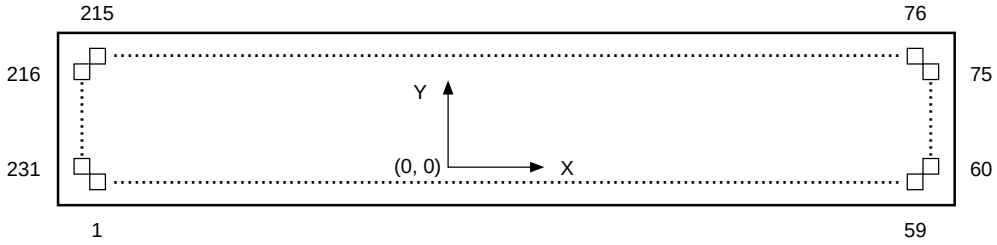
- Number of LCD drive outputs: 1 ..... 0 out
- Drive duty ratio (MAX): ..... 1/240 duty
- RAM data displayed directly using the display data RAM.
- RAM bit data (when in normal display mode): ..... "0" - Off
  "1" - On
- Internal RAM capacity: ..... 160 × 240 bit
- High speed 8-bit MPU interface
- Compatible with both 80x86 series and 68000 series MPUs.
- Single chip select when multiple chips are used.
- Rich command functions.
- Extremely low consumption current.
- Power supply
- Logic system: ..... 2.7 to 3.6 V
- LCD system: ..... 5.4 to 7.2 V
- Non-biased display off function
- Slim chip shape
- Package: DIE D0B
  TCP ..... TXX
- This product is not designed for resistance to radiation or exposure to light.

Block Diagram



TERMINAL FUNCTIONS

Terminal Layout Diagram D0B



DIE: D0B
Chip size: 14.82 mm × 2.50 mm
Bump size: 67 μm × 80 μm (min.)
Bump pitch: 100 μm (min.)
Bump height: 22.5 ± 5.5 μm

Terminal Coordinates D0B

Pin	Name	X	Y
1	$\overline{V2}$	–6692	–1130
2	VC	–6548	
3	V2	–6404	
4	V3	–6260	
5	V_{SS}	–6025	
6	OSC1	–5846	
7	OSC2	–5588	
8	OSC3	–5292	
9	V_{SS}	–5016	
10	NC	–4847	
11	NC	–4703	
12	$\overline{CS}$	–4507	
13	A0	–4344	
14	$\overline{RD}$	–4181	
15	$\overline{WR}$	–4019	
16	$\overline{RES}$	–3856	
17	V_{SS}	–3703	
18	C86	–3508	
19	V_{DD}	–3355	
20	LR0	–3160	
21	V_{SS}	–3001	
22	LR1	–2805	
23	V_{DD}	–2652	
24	MS	–2453	
25	V_{SS}	–2295	
26	D0	–1926	
27	D1	–1609	
28	V_{DD}	–1309	
29	D2	–1055	
30	D3	–728	
31	D4	–432	
32	D5	–104	
33	D6	191	
34	D7	518	
35	FR	858	
36	CL	1154	
37	V_{SS}	1413	
38	F1	1882	
39	F2	2178	
40	$\overline{DOF}$	2506	
41	CA	2802	
42	$\overline{SLP}$	3191	
43	COD0	3519	
44	COD1	3815	
45	COD2	4142	
46	COD3	4438	
47	COD4	4766	
48	NC	5002	
49	NC	5146	
50	NC	5290	
51	NC	5434	
52	NC	5578	
53	NC	5722	
54	NC	5866	
55	NC	6010	
56	V3	6260	
57	V2	6404	
58	VC	6548	

Pin	Name	X	Y
59	$\overline{V2}$	6692	–1130
60	$\overline{V3}$	7290	–837
61	V_{EE}		–693
62	NC		–549
63	NC		–369
64	O160		–268
65	O159		–167
66	O158		–66
67	O157		33
68	O156		134
69	O155		235
70	O154		336
71	O153		437
72	O152		537
73	O151		638
74	O150		739
75	NC		840
76	NC	7007	1130
77	O149	6904	
78	O148	6804	
79	O147	6703	
80	O146	6602	
81	O145	6501	
82	O144	6400	
83	O143	6300	
84	O142	6199	
85	O141	6098	
86	O140	5997	
87	O139	5896	
88	O138	5796	
89	O137	5695	
90	O136	5594	
91	O135	5493	
92	O134	5392	
93	O133	5292	
94	O132	5191	
95	O131	5090	
96	O130	4989	
97	O129	4888	
98	O128	4788	
99	O127	4687	
100	O126	4586	
101	O125	4485	
102	O124	4384	
103	O123	4284	
104	O122	4183	
105	O121	4082	
106	O120	3981	
107	O119	3880	
108	O118	3780	
109	O117	3679	
110	O116	3578	
111	O115	3477	
112	O114	3376	
113	O113	3276	
114	O112	3175	
115	O111	3074	
116	O110	2973	

Pin	Name	X	Y
117	O109	2872	1130
118	O108	2772	
119	O107	2671	
120	O106	2570	
121	O105	2469	
122	O104	2368	
123	O103	2268	
124	O102	2167	
125	O101	2066	
126	O100	1965	
127	O99	1864	
128	O98	1764	
129	O97	1663	
130	O96	1562	
131	O95	1461	
132	O94	1360	
133	O93	1260	
134	O92	1159	
135	O91	1058	
136	O90	957	
137	O89	856	
138	O88	756	
139	O87	655	
140	O86	554	
141	O85	453	
142	O84	352	
143	O83	252	
144	O82	151	
145	O81	50	
146	O80	–50	
147	O79	–151	
148	O78	–252	
149	O77	–352	
150	O76	–453	
151	O75	–554	
152	O74	–655	
153	O73	–756	
154	O72	–856	
155	O71	–957	
156	O70	–1058	
157	O69	–1159	
158	O68	–1260	
159	O67	–1360	
160	O66	–1461	
161	O65	–1562	
162	O64	–1663	
163	O63	–1764	
164	O62	–1864	
165	O61	–1965	
166	O60	–2066	
167	O59	–2167	
168	O58	–2268	
169	O57	–2368	
170	O56	–2469	
171	O55	–2570	
172	O54	–2671	
173	O53	–2772	
174	O52	–2872	

Pin	Name	X	Y
175	O51	–2973	1130
176	O50	–3074	
177	O49	–3175	
178	O48	–3276	
179	O47	–3376	
180	O46	–3477	
181	O45	–3578	
182	O44	–3679	
183	O43	–3780	
184	O42	–3880	
185	O41	–3981	
186	O40	–4082	
187	O39	–4183	
188	O38	–4284	
189	O37	–4384	
190	O36	–4485	
191	O35	–4586	
192	O34	–4687	
193	O33	–4788	
194	O32	–4888	
195	O31	–4989	
196	O30	–5090	
197	O29	–5191	
198	O28	–5292	
199	O27	–5392	
200	O26	–5493	
201	O25	–5594	
202	O24	–5695	
203	O23	–5796	
204	O22	–5896	
205	O21	–5997	
206	O20	–6098	
207	O19	–6199	
208	O18	–6300	
209	O17	–6400	
210	O16	–6501	
211	O15	–6602	
212	O14	–6703	
213	O13	–6804	
214	O12	–6904	
215	NC	–7007	
216	NC	–7290	840
217	O11		739
218	O10		638
219	O9		537
220	O8		437
221	O7		336
222	O6		235
223	O5		134
224	O4		33
225	O3		–66
226	O2		–167
227	O1		–268
228	NC		–369
229	NC		–549
230	V_{EE}		–693
231	$\overline{V3}$		–837

Explanation of Terminals

Power Supply Terminals

Terminal Name	I/O	Explanation	No. of Terminals
V_{DD}	Power Supply	These are connected to V_{CC} (the system power supply).	3
V_{SS}	Power Supply	These are connected to the system GND.	6
V_{EE}	Power Supply	These are the liquid crystal drive system load-side power supplies. V_{DD}–V_{EE}.	2
V3, V2, VC, –V2, –V3	Power Supply	These are the liquid crystal drive multi-level power supplies. The relationships between the various levels must be: $V_{DD} \geq V3 \geq V2 \geq VC > -V2 > -V3 \geq V_{EE}$	2 Each

Terminals Pertaining to the MPU

Terminal Name	I/O	Explanation	No. of Terminals
D7 to D0	I	These comprise the 8–bit bi-directional data bus, and are connected to a standard 8–bit or 16–bit MPU data bus.	8
A0	I	The least significant bit of the address bus of a normal MPU is connected to discern between data and commands. H: Inidcates that D7 to D0 are control data. L: Indicates that D7 to D0 are display data.	1
$\overline{RES}$	I	When initial settings are restored by placing $\overline{RES}$ to “L”. The reset operation is performed based on the $\overline{RES}$ level. Schmidt trigger.	1
$\overline{CS}$	I	This is the chip select signal. In the SED 1590, even if multiple chips are used, the $\overline{CS}$ is a shared line. When $\overline{CS}$ is in a non-active state, D7 to D0 enter a high-impedance state.	1
$\overline{RD}$ (E)	I	• When connected to an 80x86 series MPU Active “L” This terminal connects to the $\overline{RD}$ signal of the 80x86 MPU, and while this signal is low, the data bus is in an output state. • When connected to a 68000 series MPU Active “H” This serves as the 68000 MPU-enabled clock input terminal.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 80x86 system MPU Active “L” This terminal is connected to the $\overline{WR}$ signal of the 80x86 series MPU. The data bus signals are latched on the rising edge of the $\overline{WR}$ signal. • When connected to a 68000 series MPU This is the read/write control input terminal. R/W = “H”: Read R/W = “L”: Write	1
C86	I	This is the MPU interface switch terminal. C86 = “H”: The 68000 MPU interface. C86 = “L”: The 80x86 series MPU interface.	1

Liquid Crystal Drive Circuit Signals

Terminal Name	I/O	Explanation	No. of Terminals
OSC1	I	This is for the oscillator circuit. When an external input is used, it is input to this terminal. Connect to "H" or "L" in case of slave operations.	1
OSC2	O	This is a terminal for the oscillator circuit. When the internal oscillator circuit is used, connect to OSC1 through a capacitor. Make this terminal open in case of slave operations.	1
OSC3	O	This is a terminal for the oscillator circuit. When the internal oscillator circuit is used, connect to OSC1 through a resistor. Make this terminal open in case of slave operations.	1
M/S	I/O	This terminal selects master/slave operation. In master mode, signals required for the liquid crystal display are output, while during slave operation signals that are required to the liquid crystal display are input, thereby synchronizing the liquid crystal display system. M/S = "H": Master operation M/S = "L": Slave operation	1
CL	I/O	This is the display clock input/output terminal. When using master/slave mode, this is connected to the various CL terminals. This is also connected to the common driver YSCL terminals. When M/S = "H": Output When M/S = "L": Input	1
FR	I/O	This is the liquid crystal alternating current input/output terminal. When using master/slave mode, this is connected to the various FR terminals. This is also connected to the common driver FR terminals. When M/S = "H": Output When M/S = "L": Input	1
CA	I/O	This is the field start signal. When using master/slave mode, this is connected to the various CA terminals. This is also connected to the common driver CA terminals. When M/S = "H": Output When M/S = "L": Input	1
$\overline{DOF}$	I/O	This is the liquid crystal display blanking control terminal. When using master/slave mode, this is connected to the various $\overline{DOFF}$ terminals. This is also connected to the common driver $\overline{DOFF}$ terminals. When M/S = "H": Output When M/S = "L": Input	1
$\overline{SLP}$	O	This is the sleep control terminal. When set to a sleep status by the MCU, both the master and the slave circuits enter the sleep mode. This terminal is not connected between the master and the slave. Connect to the SCI 7500 $\overline{SLP}$ terminal for the master only.	1
F1, F2	I/O	These are the drive pattern signal input/output terminals. When in master/slave mode, these are connected to the F1 and F2 terminals respectively. These are connected to the common driver F1 and F2 terminals. When M/S = "H": Output When M/S = "L": Input	1 each
On	O	Liquid crystal segment drive outputs	160

Control Terminals

Terminal Name	I/O	Explanation	No. of Terminals
LR0, LR1	I	When multiple SED1590 chips are used, these terminals specify the various segment driver layout positions. Using this information, the SED1590 determines the relationships between the various segments and the position in internal RAM.	1 each
COD0 COD1 COD2 COD3 COD4	O	These comprise the 5–bit output port. The status of this port can be controlled by commands from the MPU. They can be used for controls of the electronic volume control knobs and other applications.	1 each

EXPLANATION OF FUNCTIONS

The MPU Interface

The SED1590 exchanges data with the MPU through an 8–bit bi-directional data bus (D7 to D0).
By setting the C86 terminal to "H" or "L" the SED1590 can be connected directly to the MPU bus for either the 80x86 system MPUs or the 68000 system MPUs, as shown in Table 1.

Table 1

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
H	68000 MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7
L	80×86 MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

The SED1590 identifies data bus signals using combinations of the A0, E, R/W and ($\overline{RD}$, $\overline{WR}$) signals as shown in Table 2.

Table 2

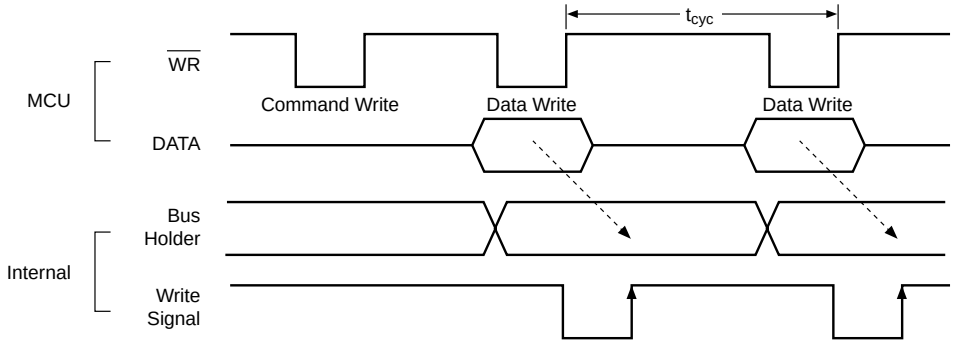
Common	68 System	80 System		
A0	R/W	$\overline{RD}$	$\overline{WR}$	Function
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

The SED1590 possesses a function that automatically identifies the segment driver position by the LR0 and LR1 terminals even when multiple SED1590 chips are used, so from the perspective of the MPU, there is no need for the MPU to identify the individual segment drivers. As a result, the $\overline{CS}$ chip select terminals can share a common line from the outside. The LR will be discussed below.
When the chips are not selected, D0 to D7 enter a high impedance state and terminals A0, $\overline{RD}$, and $\overline{WR}$ inputs are disabled.

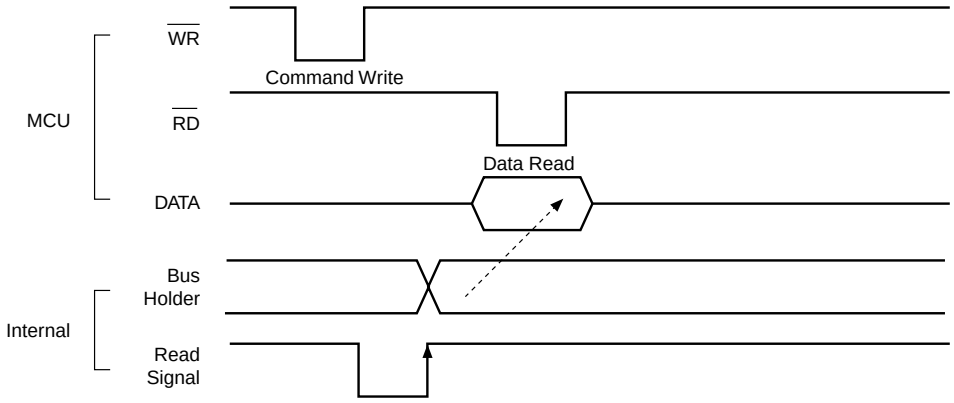
Accessing the Display Data RAM and the Internal Registers.

The SED1590 uses a type of pipeline process between LSIs through the bus holders in the internal data bus in order to match the operating frequencies between the MPU and the display data RAM and internal registers. Consequently, when viewed from the MPU side, there are no constraints on accessing the SED1590 in terms of the display data RAM access time (t_{ACC}), but rather the cycle time is dominant. When the cycle time is not adequate, then the MPU may insert an NOP command, which is equivalent to executing a dummy wait.

• Writing



• Reading



Busy Flag

When the busy flag is "L", the SED1569 is making internal operations. The busy flag is being output through the terminal D7 by the status read command. Although commands from the MPU are being accepted even while the busy flag is appearing, it is necessary to secure due cycle time (tcyc) in order to make proper writing of the indication data. Meanwhile, in case the cycle time is being satisfied, it is not necessary to check this flag.

Page Address Control Circuit

Page direction address control is performed when the display RAM is accessed by the MPU and when contents of the display data RAM are read for the liquid crystal display.
When the page direction scan is designated by the scan direction select command, the page address will increment each time the MPU makes the writing operation. While the internal RAM contains 240 lines worth of data, because the MPU access processes in 8 dot units in the common direction, the number of pages is 240/8 = 30 pages.
Consequently, the count is locked when address value 29 is reached, and there is no incrementation beyond this level. The count lock is cleared next time the page address is set. Moreover, the counter within the page address control circuit is independent of the column address control circuit counter.
When there is a read operation for the liquid crystal display, incrementation is synchronized with the CL signal, and the count is reset when the display line that is set by a control command from the MPU has been reached.

The Column Address Control Circuit

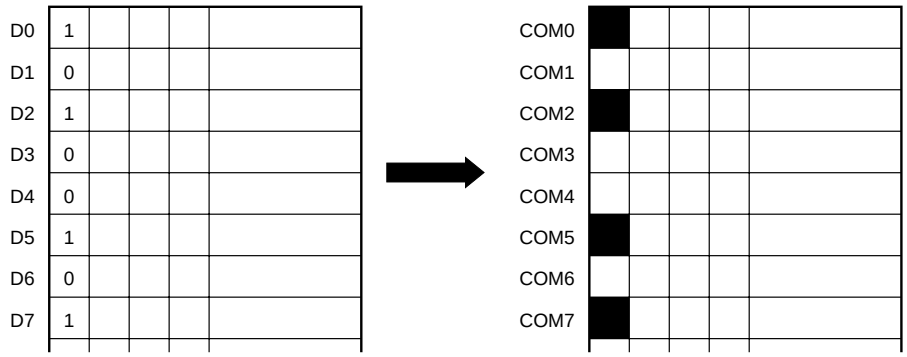
Address control in the column direction is performed when the display RAM is accessed from the MPU. The SED1590 unit has only 160 columns; however, using multiple chips the SED1590 can handle continuous column addressing even when using four chips in the column direction (640 columns). Consequently, from the MPU perspective, the MPU need not be aware of the multiple chips.
The address value is incremented or decremented when a write or read operation is performed by the MPU. In the increment mode, the count is locked at 279H (639), while in the decrement mode the count is locked at 000H (0). Incrementing/decrementing will not proceed past that count. The count lock is cleared the next time that a column address set is performed. Moreover, the counter within the column address control circuit operates independently of the page address control circuit counter.

The I/O Buffer

The I/O buffer is a bi-directional buffer for cases where the MPU accesses the display data RAM via the SED1590 internal bus.

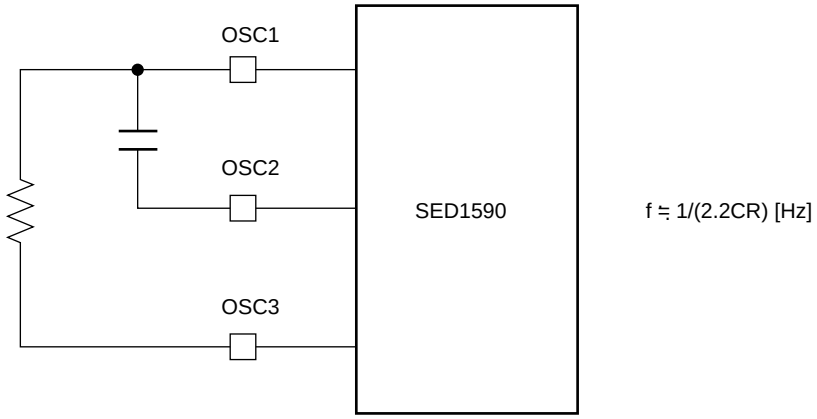
The Display Data RAM

The display data RAM is RAM in which is stored the dot data for the display. It has a 160×240 bit structure. The data can be selected by specifying the page address and the column address. The display data D0 to D7 from the MPU corresponds to 8 dots in the common direction of the liquid crystal display, and thus when multiple SED1590 chips are used, there are few constraints when the display data is sent, allowing the display to be structured freely.
MPU-side display RAM reading and writing is done through the I/O buffer, which operates to prevent timing overlaps with the display RAM reads for driving the liquid crystal. Consequently, there is absolutely no negative effect on the display such as flickering even if operations that write data to the RAM or read data from the RAM are performed completely asynchronously with the liquid crystal drive timing during the dipslay.



The Oscillator Circuit

The oscillator circuit generates the synch circuit for the liquid crystal drive. When the internal oscillator circuit of the SED1590 is used, then a capacitor must be placed between OSC1 and OSC2, and a resistor must be placed between OSC1 and OSC3, as shown in the figure below. Determine the C and R values based on the oscillation frequency formula given below.



When the internal oscillator circuit is not used (i.e. when an external clock input is used instead), input the external clock into OSC1. Leave OSC2 and OSC3 open.

M/S		OSC1	OSC2	OSC3
"H"	Master operation (using the internal oscillation circuit)	Refer to Fig. 3 indicated above.		
"H"	Master operation (using external signal inputs)	Input terminal.	Open	Open
"L"	Slave operation	Connect to "H" or "L".	Open	Open

The Decoder

The decoder outputs the segment driver control signal that is required for the liquid crystal drive. This control signal is determined by the display data, the drive pattern signals F1 and F2, and by the liquid crystal alternating current signal FR.

The Liquid Crystal Drive Circuit

This outputs the liquid crystal drive voltage. The liquid crystal drive voltage can be of one of five values: V3, V2, VC, $\overline{V2}$, $\overline{V3}$. These values are selected by the drive control signal determined by the decoder.

The Internal Timing Generator Circuit

The internal timing generator circuit controls the internal write operations when the display data RAM is accessed by the MPU. Moreover, in this case the column address counter and page address counter incrementation/decrementation is also controlled by the internal timing generator circuit.

When a module is structured from multiple chips, the SED1590 automatically determines from LR0 and LR1 which chip corresponds to which segments on the panel so that only the address relating to the corresponding segment responds. Consequently, from the perspective of the MPU, there is no need to identify each individual SED1590 chip, but rather when accessing in the column direction, continuous addresses can be handled in so far as the addresses are in the same page. As a result, the CS line can be shared. In this case, the relationship between the actual segment output and the column address is as shown in the following figure.

When there is an access race where both the MPU system and the display system are attempting to access the display data RAM simultaneously, the conflict between both accesses is mediated by the display control circuit. Consequently, there is no need for the MPU to perform a busy check in so far as the accesses ensure the cycle time that is set by the AC timing.

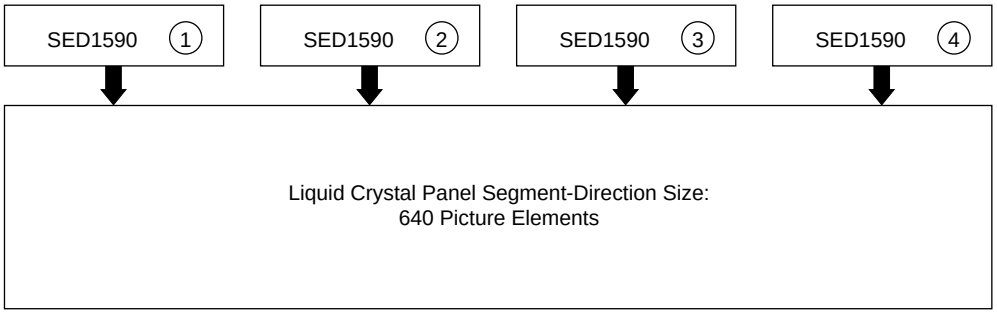


Table 3

	LR1	LR0	Corresponding Picture Elements	Column Address (10–bit binary display)
SED1590 1	"L"	"L"	1 to 160	0000000000B to 0010011111B
SED1590 2	"L"	"H"	161 to 320	0010100000B to 0100111111B
SED1590 3	"H"	"L"	321 to 480	0101000000B to 0111011111B
SED1590 4	"H"	"H"	481 to 640	0111100000B to 1001111111B

The Display Control Circuit

The display control circuit generates the timing signals CL, CA, FR, along with the drive pattern signals F1 and F2, for the display based on the oscillator output from the oscillator circuit. Moreover, depending on the commands from the MPU, this circuit generates the $\overline{\text{DOFF}}$ display On/Off control signal and the $\overline{\text{SLP}}$ sleep signal as well.
When multiple SED1590 chips are used, the input and output statuses of these signals are as given in Table 4.

Table 4

Operating Mode	CL	CA	F1, F2	FR	$\overline{\text{DOFF}}$	$\overline{\text{SLP}}$
Master	Output	Output	Output	Output	Output	Output
Slave	Input	Input	Input	Input	Input	Output

The Relationship Between the Display Drive Output Voltage and the Display Data

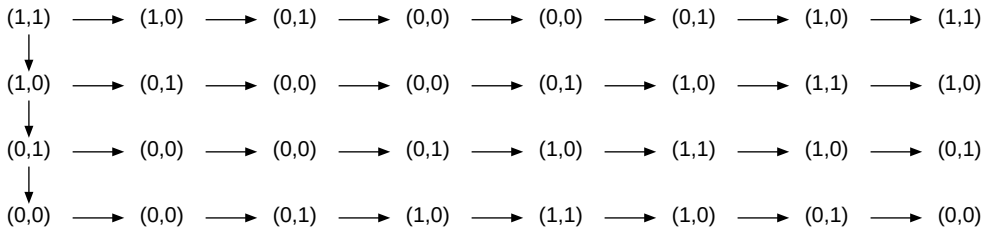
Table 5 shows the relationships between F1, F2 and the common drive voltage.

Table 5

FR	L				H			
F1	H	L	H	L	H	L	H	L
F2	H	H	L	L	H	H	L	L
n Line	V1	V1	–V1	V1	–V1	–V1	V1	–V1
n + 1 Line	–V1	V1	V1	V1	V1	–V1	–V1	–V1
n + 2 Lines	V1	–V1	V1	V1	–V1	V1	–V1	–V1
n + 3 Lines	V1	V1	V1	–V1	–V1	–V1	–V1	V1

Note: The voltage relationships are as follows: V1 > VC > –V1 (where VC is the central voltage).

The values of F1 and F2 change for each horizontal interval (as described below) and for each CA set by the commands. The changes are as shown below. Moreover, in this display the numbers are described as (F2, F2).



Changes in the horizontal direction indicate changes that happen each horizontal interval, where the horizontal interval was set by using commands. The changes in the vertical direction, shown on the column on the left, show the value change that starts with each CA.
The relationships between the display data, the liquid crystal alternating current signal FR, and the segment drive voltage are as shown in Table 6. These drive voltages change according to the combination of F1 and F2. In this table, “0” indicates “Off” and “1” indicates “On”.

Table 6

FR = “L”

Display Picture Element	n	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	1	V2	VC	VC	–V2	V3	V2	V2	VC	VC	V2	–V2	–V3	V2	VC	VC	–V2
	2	V2	VC	V3	V2	VC	–V2	V2	VC	VC	–V2	V2	VC	–V2	–V3	VC	–V2
	3	V2	VC	VC	–V2	VC	–V2	–V2	–V3	V3	V2	V2	VC	V2	VC	VC	–V2
	4	V2	V3	VC	V2	VC	V2	–V2	VC	VC	V2	–V2	VC	–V2	VC	–V3	–V2

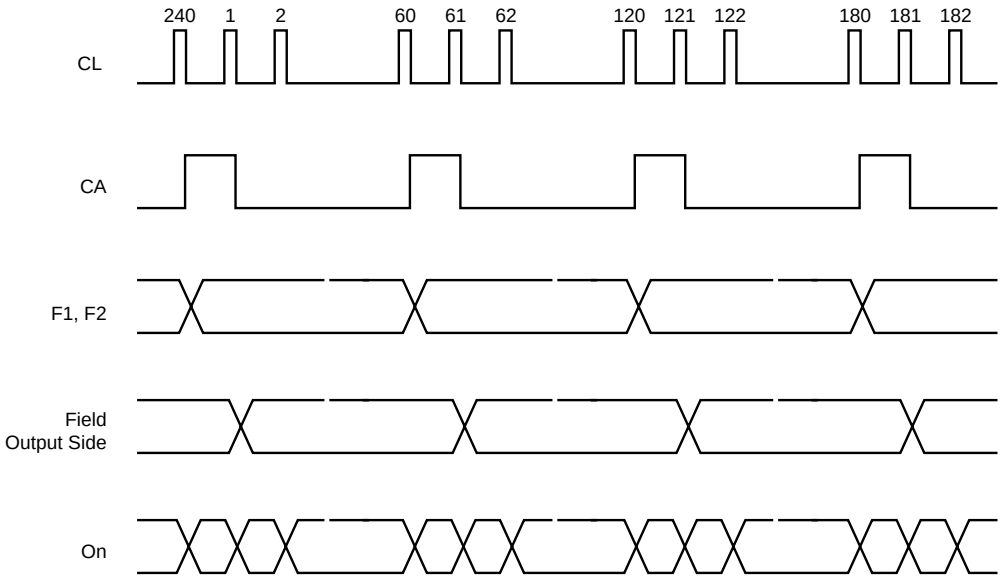
FR = “H”

Display Picture Element	n	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	1	–V2	VC	VC	V2	–V3	–V2	–V2	VC	VC	V2	V2	V3	–V2	VC	VC	V2
	2	–V2	VC	–V3	–V2	VC	V2	–V2	VC	VC	V2	–V2	VC	V2	V3	VC	V2
	3	–V2	VC	VC	V2	VC	V2	V2	V3	–V3	–V2	–V2	VC	–V2	VC	VC	V2
	4	–V2	–V3	VC	–V2	VC	–V2	V2	VC	VC	–V2	V2	VC	V2	VC	V3	V2

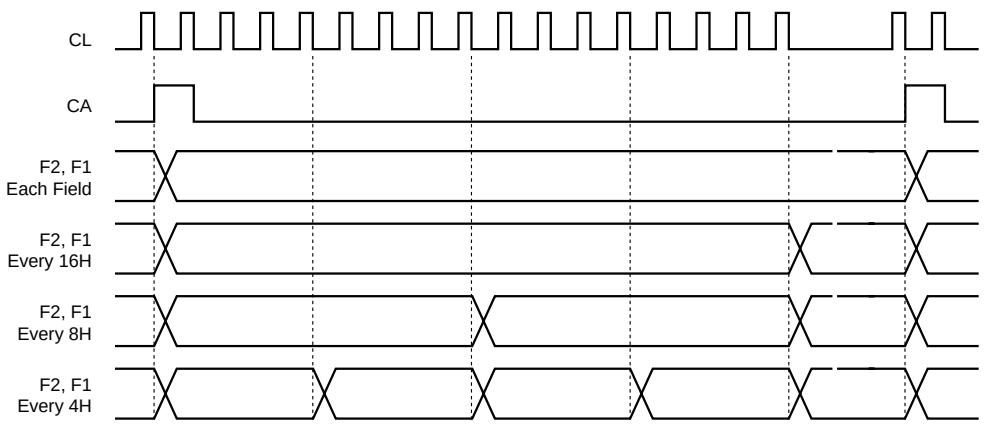
Notes: (1), (2), (3) and (4) correspond to the following drive pattern:
(1): (F2, F1) = (H, H)
(2): (F2, F1) = (H, L)
(3): (F2, F1) = (L, H)
(4): (F2, F1) = (L, L)

Timing Diagram

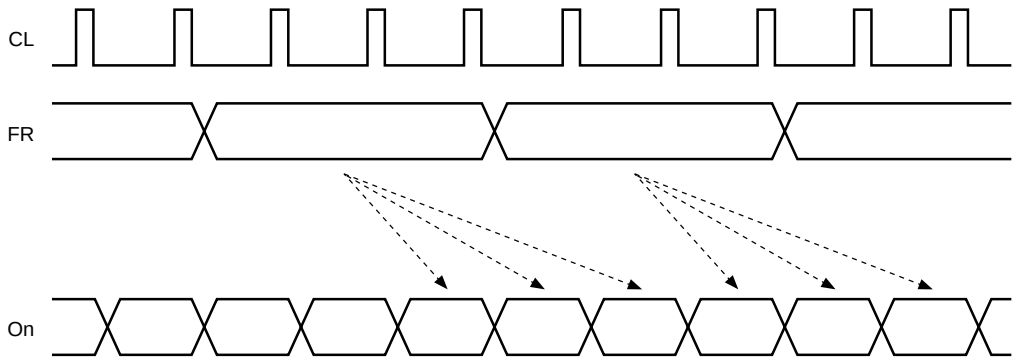
The timing diagram for the liquid crystal display is as shown in the following figure.
Example: The example shows the fields used in a 1/240 duty, where the liquid crystal drive pattern (F2, F1) switches for each field.



The figure below shows an example where the drive pattern (F2, F1) is different. The drive pattern is changed with the falling edge of CL and the status is reflected to the driver output that changes at the next falling edge of CL.



The figure below shows the timing with which FR changes. FR changes on the falling edge of CL, and the changes are reflected to the driver which changes on the next falling edge of CL (master mode). Moreover, in the case of slave mode, the FR status is accepted with the falling edge of CL, and is reflected to the driver output that changes on the next falling edge of CL.



COMMANDS

Table of Commands

Table 7 shows a table of SED1590 commands

Table 7

Command Name		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameters
1	DON	0	1	0	1	0	1	0	1	1	1	1	Display ON	None
2	DOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal display	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse display	None
5	DTYSET	0	1	0	1	0	1	0	1	0	0	0	Duty set	1 byte
6	LINSET	0	1	0	1	1	0	0	1	0	1	0	FR interval set	1 byte
7	PATSET	0	1	0	1	1	0	0	1	1	0	0	Drive pattern set	1 byte
8	VOLCTL	0	1	0	1	1	0	0	0	1	1	0	Output port control	1 byte
9	SLPON	0	1	0	1	0	0	1	0	1	0	1	Sleep on	None
10	SLPOFF	0	1	0	1	0	0	1	0	1	0	0	Sleep off	None
11	DVDSET	0	1	0	1	0	1	1	0	1	0	0	Divide offset	1 byte
12	PASET	0	1	0	0	1	1	1	0	1	0	1	Page address set	1 byte
13	PDNOR	0	1	0	0	1	1	0	1	0	1	0	Page direction normal	None
14	PDINV	0	1	0	0	1	1	0	1	0	1	1	Page direction inverse	None
15	CASET	0	1	0	0	0	0	1	0	1	0	1	Column address set	2 byte
16	CAINC	0	1	0	0	1	0	1	1	0	1	0	Column address increment	None
17	CADEC	0	1	0	0	1	0	1	1	0	1	1	Column address decrement	None
18	PDIR	0	1	0	0	1	0	0	1	0	1	0	Page direction scan	None
19	CDIR	0	1	0	0	1	0	0	1	0	1	1	Column direction scan	None
20	MWRITE	0	1	0	0	1	0	1	1	1	0	0	Memory write	Data
21	CNTCLR	0	1	0	0	1	0	1	0	1	1	0	Counter clear	None
22	PCCLR	0	1	0	0	0	0	0	1	0	1	0	Page counter clear	None
23	CCCLR	0	1	0	0	0	0	0	0	1	0	1	Column counter clear	None
24	CKSET	0	1	0	1	0	1	1	1	1	1	1	Clock divide set	1 byte
25	RETURN	0	1	0	1	0	1	1	1	1	1	0	Return	None
26	VOLRD	0	1	0	1	0	1	1	0	1	1	0	Output port set read	1 byte
27	STREAD	0	0	1									Status read	

Command Details

The SED1590 identifies the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$). The command interpretation and execution is performed based entirely on internal timing without relying on any external clock.
In the 80×86 MPU interface, a low pulse is sent to the $\overline{WR}$ terminal to launch the command when writing. In the 68000 series MPU interface, a "L" input to the R/$\overline{W}$ terminal causes a write state, and then the commands are launched when a high pulse input is sent to the E terminal. Consequently, the 68000 series MPU interface is different from the 80x86 MPU interface in the command details and command tables, and in that the $\overline{RD}$ (E) terminal is "1" ("H") when performing status reads and when reading display data. The commands will be explained below using the 80×86 MPU interface in the examples.

Display ON/OFF Command: 1, Parameter:0

This command forces the entire display ON or OFF. When the display is OFF, all outputs are fixed at VC. Because the display is not possible when in sleep mode, make sure that this command is used after the sleep mode is turned OFF.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DON	0	1	0	1	0	1	0	1	1	1	1	Display ON
DOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF

Page Address Set Command: 1, Parameter: 1

This command and its following parameters makes it possible to set the page address corresponding to the low address when accessing the display data RAM from the MPU side. The desired bit of the display data RAM can be accessed by specifying the page address and the column address. The page addresses are 5 bits, corresponding to 30 pages (pages 0 to 29). Even if the page address changes, there is no change to the display status.
This command is input into the registers and loaded in the counters). That which is input is stored within the register, and can be reloaded by the PACLR command.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PASET	0	1	0	0	1	1	1	0	1	0	1	Page address set
Parameter	1	1	0				D	D	D	D	D	

Page Address Direction Command: 1, Parameter: 0

This command makes it possible to reverse the position of page 0 in the page address of the display RAM data. Consequently, it is possible to reverse the page address scan direction when the MPU uses the display data in the page direction. The relationship between the physical position in internal RAM and the page address is inverted:
Normal: 0 → 29
Reversed: 24 ← 0
When reversed, the final page address becomes 24. Consequently, the number of lines which can be indicated becomes upto 200.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PDNOR	0	1	0	0	1	1	0	1	0	1	0	Page direction normal
PDINV	0	1	0	0	1	1	0	1	0	1	1	Page direction inverted

Column Address Set Command: 1, Parameter: 2

This command and its following parameters make it possible to specify the column address when the MPU accesses display data RAM in the column direction. The desired bit of display data RAM can be accessed by specifying the page address and the column address. The column address has 10 bits, and when four of the chips are used in the column direction, up to 640 dots (pixels) are supported. Even when the address changes, the state of the display does not change. There are 640 columns (columns 0 to 639).
The address value is input with the less significant address 5 bit first and then the more significant 5 bit. With the less significant alone, when another command is entered, only the less significant is entered into the register, however, the counter is not loaded. When the less significant is followed by the more significant, they are loaded into the counter and the input is stored in the register. When the less significant address is followed by some other command, the counter will not be loaded and the command will be cancelled. With this command, the set values can be reloaded by the CCCLR command.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CASET	0	1	0	0	0	0	1	0	1	0	1	Column address set
Parameter 1	1	1	0				D	D	D	D	D	Lower 5 bits
Parameter 2	1	1	0				D	D	D	D	D	Upper 5 bits

Column Address Direction Command: 1, Parameters: 0

This command specifies the behavior of the column address counter (increment vs. decrement).
The address increments or decrements each time RAM accesses the display data. In the increment mode, the count operation stops when the value reaches 279H (639), or when the value reaches 000H (0) in the decrement mode.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CAINC	0	1	0	0	1	0	1	1	0	1	0	Column address increment
CADEC	0	1	0	0	1	0	1	1	0	1	1	Column address decrement

Scan Direction Select Command: 1, Parameter: 0

When the MPU continuously accesses display memory, this determines whether the scanning will be done in the page direction or in the column direction.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PDIR	0	1	0	0	1	0	0	1	0	1	0	Page direction scan
CDIR	0	1	0	0	1	0	0	1	0	1	1	Column direction scan

Display Data Write Command: 1, Parameter: Number of data to be written

When the MPU writes data to the memory, this command places the chip in a data entry mode. By writing data again after this command, the display data RAM contents can be changed. The data write mode is cleared automatically when another command is entered.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
MWRITE	0	1	0	0	1	0	1	1	1	0	0	Memory write
Parameter	1	1	0	D	D	D	D	D	D	D	D	Write data

Status Read

This read operation makes it possible to monitor the internal operating status of the SED1590.
No other command except for the status read command will be accepted with a RAM busy state (1). If the cycle time is followed, then there is no need to check for the RAM busy state under normal use.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
STREAD	0	0	1	O	O	O	O	O	O	O	O	Status

D7: Busy/Ready — Busy: 1, Ready: 0
D6: Page Address Direction — Normal: 1, Inverted: 0
D5: Column Address Direction — Normal: 1, Inverted:0
D4: Increment Direction — Column: 0, Page: 1
D3: Display ON/OFF — Off: 1, On: 0
D2: SLEEP ON/OFF — Off: 0, On: 1
D1: INVERT — Normal Display: 1, Invert Display: 0
D0: Reserved terminal

Display Normal/Inverted Command: 1, Parameter:0

This command makes it possible to inert the ON/OFF status of each point on the display without having to rewrite the contents of the display data RAM. Because all points in the display are either set to the normal display or reverse, partial inversions are not supported.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Display normal
DISINV	0	1	0	1	0	1	0	0	1	1	1	Display inverted

Duty Set Command: 1, Parameter: 1

This command combined with the following paramenter sets the duty.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DTYSET	0	1	0	1	0	1	0	1	0	0	0	Duty set
Parameter	1	1	0			D	D	D	D	D	D	(Number of display lines)/ 4/1
Example: 1/200 duty	1	1	0	0	0	1	1	0	0	0	1	
Example: 1/240 duty	1	1	0	0	0	1	1	1	0	1	1	

Sleep Mode On/Off Command: 1, Parameter:0

This command controls the sleep mode of the LCD module. Before launching this command, be sure that the Display OFF command has been entered and that the display is in an OFF state. Moreover, after issuing the Sleep OFF command, be sure to maintain the logic power supply for 40 ms to discharge the load of the power supply IC.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
SLPON	0	1	0	1	0	0	1	0	1	0	1	Sleep ON
SLPOFF	0	1	0	1	0	0	1	0	1	0	0	Sleep OFF

Line Inverse Number Set Tab Command: 1, Parameter: 1

This command controls the number of lines inverted in the LCD module.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
LINSET	0	1	0	1	1	0	0	1	0	1	0	FR inverse set
Parameter	1	1	0					D	D	D	D	FR inverse set value

The default value is being set to 11H inverse. (D3 to D0 = 1010)

Pattern Set Command: 1, Parameter: 1

This command controls the MLS pattern switching interval.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PATSET	0	1	0	1	1	0	0	1	1	0	0	Drive pattern set
Parameter	1	1	0							D	D	Drive pattern set value

The correspondence between the input data and the switching interval is as follows:
(The default value will be set to 8H.)

	8H	4H	16H	Field
D0:	0	1	0	1
D1:	0	0	1	1

Output Port Control Command: 1, Parameter: 1

This command sets 5 bit data to control the LCD power supply.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
VOLCTL	0	1	0	1	1	0	0	0	1	1	0	Output port control
Parameter	1	1	0				D	D	D	D	D	Output port control value

D0: COD 0 D1: COD 1
D2: COD 2 D3: COD 3
D4: COD 4

Partition DOFF Set Command: 1, Parameter: 1

This command controls the LCD module display on/off for each driver.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DVDSET	0	1	0	1	0	1	1	0	1	0	0	Partition offset
Parameter	1	1	0					D	D	D	D	Partition offset set value

D= “1”: Display ON D = “0”: Display OFF
(LR1, LR0): (0, 0) → D0; (0,1) → D1; (1, 0) → D2; (1,1) → D3

Initialize Command: 1, Parameter: 0

These commands clear the contents of the page counter, the page register, the column counter, and the column register to 0.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CNTCLR	0	1	0	0	1	0	1	0	1	1	0	Counter clear
PCCLR	0	1	0	0	0	0	0	1	0	1	0	Page counter clear
CCCLR	0	1	0	0	0	0	0	0	1	0	1	Column counter clear

CNTCLR: Resets the page counter and register to 0, and the column counter and register to 0.

PACLR: Loads the register value to the page counter.

CACLR: Loads the register value to the column counter.

Clock Divide Set Command: 1, Parameter: 1

This command sets the CL division ratio that serves as the basis for the timing signal for the liquid crystal display.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CKSET	0	1	0	1	0	1	1	1	1	1	1	Clock division set
Parameter	1	1	0							D	D	Clock division set value

Correspondence of Divider Ratios

		2	1	4	8
Data	D1:	0	0	1	1
	D0:	0	1	0	1

Return Command: 1, Parameter: 0

This command sets the scan direction counter to the set value, and increments (+1) the counter in the fixed direction.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RETURN	0	1	0	1	0	1	1	1	1	1	0	Address return

Output Port Setting Read Command: 1

This command reads the output port set bit to the data bus. Perform a read operation after this command is input. Only the master chip gives an output.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
VOLRD	0	1	0	1	0	1	1	0	1	1	0	Output port set read
Parameter	1	0	1				O	O	O	O	O	

NOP (Non-operating) Command: 1, Parameter: 0

This command has no effect on operations.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP1	0	1	0	0	0	1	0	0	1	0	1	NOP
NOP2	0	1	0	0	1	0	0	0	1	0	0	NOP

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Signal	Rated Value	Units
Power supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Power supply voltage (2)	V_{EE}	–8.0 to +0.3	V
Power supply voltage (3)	V3, V2, VC, –V2, –V3	V_{EE} to +0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to +0.3	V
Operating temperature	Topr	–20 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

Note 1: The voltages are all relative to V_{DD} = 0V.

Note 2: Storage temperature 1 is the storage temperature for the bare chip or the plastic chip package products, and storage temperature 2 is the specification for the TCP packaged product.

Note 3: Be sure that the relationships between voltages V3, V2, VC, –V2, –V3 are always such that $V_{DD} \geq V3 > V2 > VC > -V2 > -V3 \geq V_{EE}$.

Note 4: This LSI chip may be permanently damaged if the LSI chip is used in conditions exceeding the absolute maximum ratings. Furthermore, it is desirable to always operate the LSI chip within these electrical characteristic conditions, not only may the LSI chip malfunction if these conditions are exceeded, but there will be adverse effects on the reliability of the LSI chip.

DC Characteristics

Unless otherwise stated, V_{DD} = V3 = 0V, V_{SS} = –3.0V, V_{EE} = –V3 = –6.0V, V2 = –1.5V, V_C = –3.0, –V2 = –4.5V

Item	Symbol	Parameter	Min	Typ	Max	Units	Corresponding Terminal
Power supply voltage (1)	V_{SS}		–3.6	–3.0	–2.7	V	V_{SS}
Power supply voltage (2)	V_{EE}		–7.2	–6.0	–5.4	V	V_{EE}
Power supply voltage (3)	V3				V_{DD}	V	V3
Power supply voltage (4)	V2			0.25 V_{EE}		V	V2
Power supply voltage (5)	VC			0.50 V_{EE}		V	VC
Power supply voltage (6)	–V2			0.75 V_{EE}		V	–V2
Power supply voltage (7)	–V3		V_{EE}			V	–V3
High-level input voltage	V_{IHC}		0.3V_{SS}	—	V_{DD}	V	*1
Low-level input voltage	V_{ILC}		V_{SS}	—	0.7 V_{SS}	V	*1
High-level output voltage	V_{OH}	I_{OH} = –0.6mA	V_{DD}–0.4	—	V_{DD}	V	*2
Low-level output voltage	V_{OL}	I_{OL} = +0.6mA	V_{SS}	—	V_{SS}+0.4	V	*2
Schmidt high-level input voltage	V_{IHS}		0.3V_{SS}	—	V_{DD}	V	$\overline{RES}$
Schmidt low-level input voltage	V_{ILS}		V_{SS}	—	0.7V_{SS}	V	$\overline{RES}$
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	5.0	µA	*3
Input/output leakage current	$I_{LI/O}$	V_{IN}=V_{DD}, V_{SS}	—	—	5.0	µA	*4
Driver output resistance	R_{ON}	V_{SS} = –3.0V, V_{EE} = –6.0V V3 = 0V, V2 = –1.5V VC = –3.0V –V2 = –4.5V –V3 = –6.0V, ∆ V = 0.5V	—	0.6	1.0	kΩ	O1~ O160
Static consumption current	I_{SSQ}	V_{IN} = V_{DD} or V_{SS}	—	—	5	µA	V_{SS}
Static consumption current	I_{EEQ}	V_{EE} = –6.0V	—	—	5	µA	V_{EE}
Dynamic consumption current	I_{SSOP1}	MPU access *6	—	1.5	2.0	µA	V_{SS}
Dynamic consumption current	I_{SSOP2}	MPU no access *6	—	90	130	µA	V_{SS}
Dynamic consumption current	I_{EEOP}	V_{EE} = –6.0V	—	12	20	µA	V_{EE}
Input terminal capacitance	CI	Freq. = 1MHz Ta = 25°C IC alone	—	—	8	pF	*3
Input/output terminal capacitance	CI/O		—	—	15	pF	*4
Output terminal capacitance	CO		—	—	7	pF	$\overline{SLP}$
Oscillator frequency	Ifosc	Ta = 25°C	—	24	—	kHz	*5

DC Characteristics: Supplemental Explanation for Corresponding Terminals

*1 •Input terminals: A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0, and LR1.
•Input/output terminals (Input mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1 and F2.

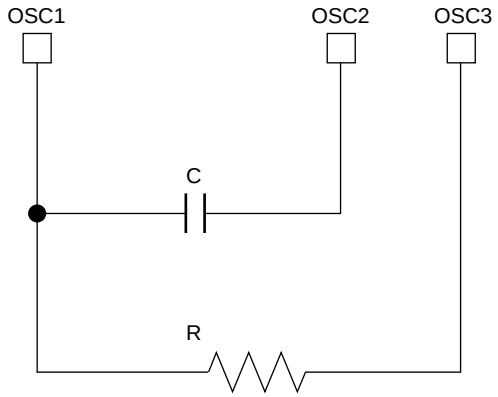
*2 •Input/output terminals (Output mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, F1, and F2.
•Output terminals: OSC2, OSC3, and $\overline{SLP}$

*3 •Input terminals: A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0, and LR1.

*4 •Input/Output terminals (Input mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1, and F2.

*5 •Local oscillator circuit depending on CR.

*6 •Frame frequency = 60 Hz, Duty = 1/200 and CR oscillation 24 kHz should be split into two-divisions when used.
•Adjust the "C" to C = 100 pF and adjust the R to 24 kHz, using a variable resistor.
•Access of the MPU will be made by continuous writing of the indicated data within the cycle time of 1,333 ns (750 kHz).
•The indicated data will appear in black or white in units of 4 lines each, repetitively.

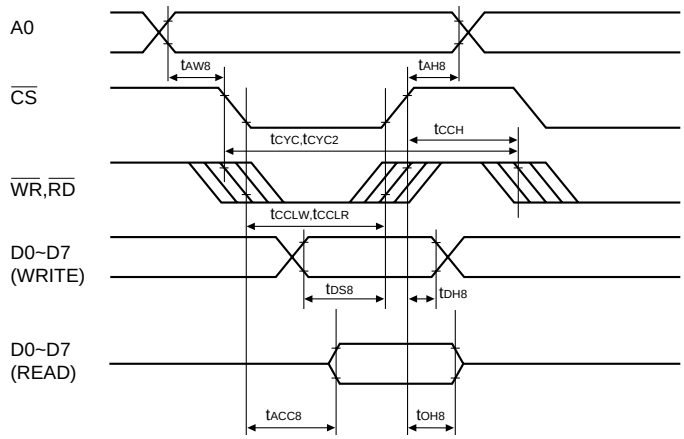


Oscillating frequency: $f \fallingdotseq 1/(2.2\ CR)$

AC Characteristics

The System Bus

Read/Write Characteristics I (80×86 Series MPUs)



[Ta = –20 to 85°C, VSS = –3.0 to –3.6V]

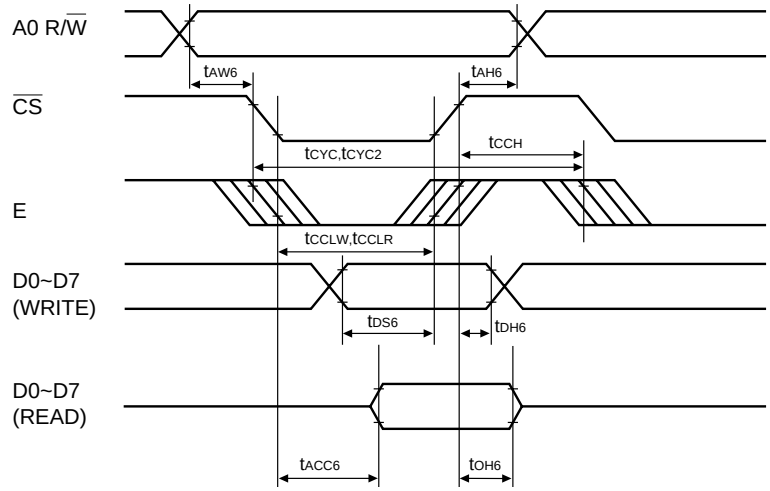
Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0	t_{AH8}	Address hold time	5	—	ns	
	t_{AW8}	Address setup time	5	—	ns	
WR, RD	t_{CYC}	Write cycle	1300	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	300	—	ns	
	t_{CCH}	Duration of the control pulse “H”	600	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	50	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	35	—	ns	CL = 100 pF
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	140	ns	
	t_{OH8}	Output disable time	30	90	ns	

[Ta = –20 to 85°C, VSS = –2.7 to –3.0V]

Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0	t_{AH8}	Address hold time	5	—	ns	
	t_{AW8}	Address setup time	5	—	ns	
WR, RD	t_{CYC}	Write cycle	1600	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	350	—	ns	
	t_{CCH}	Duration of the control pulse “H”	900	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	70	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	160	—	ns	
D0 to D7	t_{DS8}	Data setup time	50	—	ns	CL = 100 pF
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	160	ns	
	t_{OH8}	Output disable time	40	110	ns	

- The timing for the input signal rising edge and the input signal falling edge (t_r, t_f) is specified at 15 ns or less.
- All timings are specified based on 20% or 80% $V_{DD} – V_{SS}$.
- The “t_{CCLW}” and “t_{CCLR}” are being specified depending on the overlap period where the $\overline{CS}$ is being on the “L” level and the $\overline{WR}$, $\overline{RD}$ are being on the “L” level.
- These specifications guarantee writing into the RAM of the indicated data, output port reading and status reading only.

Read/Write Characteristics II (68000 Series MPUs)



[Ta = –20 to 85°C, V_{SS} = –3.0 to –3.6V]

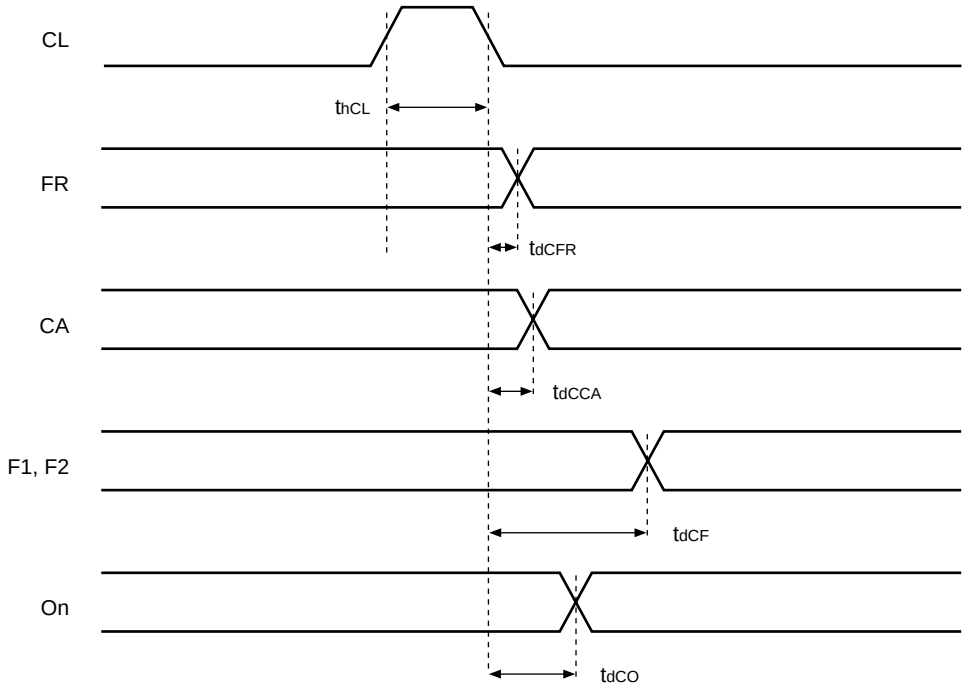
Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0, R/W	t_{AH6}	Address hold time	5	—	ns	
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1300	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	300	—	ns	
	t_{CCH}	Duration of the control pulse “H”	600	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	50	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	140	—	ns	
D0 to D7	t_{DS6}	Data setup time	35	—	ns	CL = 100 pF
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	140	ns	
	t_{OH6}	Output disable time	30	90	ns	

[Ta = –20 to 85°C, V_{SS} = –2.7 to –3.0V]

Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0, R/W	t_{AH6}	Address hold time	5	—	ns	
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1600	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	350	—	ns	
	t_{CCH}	Duration of the control pulse “H”	900	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	70	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	160	—	ns	
D0 to D7	t_{DS6}	Data setup time	50	—	ns	CL = 100 pF
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	160	ns	
	t_{OH6}	Output disable time	40	110	ns	

- The timing for the input signal rising edge and the input signal falling edge (t_r, t_f) is specified at 15 ns or less.
- All timings are specified based on 20% or 80% V_{DD} – V_{SS}.
- The “t_{CCLW}” and “t_{CCLR}” are being specified depending on the overlap period where the $\overline{CS}$ is being on the “L” level and the $\overline{WR}$, $\overline{RD}$ are being on the “L” level.
- These specifications guarantee writing into the RAM of the indicated data, output port reading and status reading only.

Output Timing Characteristics



[Ta = –20 to 85°C, V_{SS} = –2.7 to –3.6V]

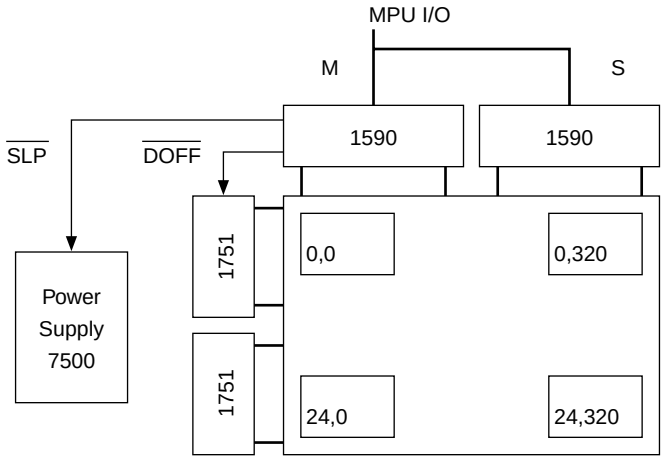
Signal	Symbol	Parameter	Min	Typ	Max	Units	Measurement Conditions
CL	t_{dCL}	CL pulse width	100	—	1000	ns	CL = 100 pF
FR	t_{dCFR}	FR output delay	10	—	1000	ns	
CA	t_{dCCA}	CA output delay	10	—	1000	ns	
F1, F2	t_{dCF}	F1, F2 output delay	10	—	1000	ns	
On	t_{dCO}	ON output delay	—	—	500	ns	

EXAMPLE OF USE

The use of the commands will be explained based on actual examples of use.

Assuming 1/200 Duty (200-line Display)

X driver: SED 1590, Y Driver: SED 1751
Power supply: $\overline{SLP}$ is input to the $\overline{SLP}$ terminal of the SCI7500



Address (24, 320) is written with the page address first followed by the column address. The page is 24, and because processing is performed in 1 byte units, $30 \times 8 = 200$ line displays.

Example of Actual Use

The Power-up Process

Turn on the system power supply (V_{CC}).
↓
Do not neglect the power-on reset.
At the time of reset the default values will be as follows:

Sleep status:	Sleep status
DON/DOFF status:	DOFF Status
(The divider OFF has not been applied.)	
Display normal/reversed:	Normal
Duty:	1/240 (set to 240 lines)
Non-display interval:	0 selected intervals
FR period:	Each 11 selected intervals
Page address register:	00.H
Column address register:	000.H
Page address direction:	Forward direction
Column address direction:	Increment
Scanning direction:	Column direction
MLS pattern:	Changes at each 8 selected intervals
Power supply control bit:	00.H
Clock 2 divider:	0.H

↓
Input commands for the settings to be changed
Example: Change the duty
Reverse the scan direction
Set the scaning direction to the page direction
Set the non-display interval
↓
Sleep off
↓
Display Data input
Example: Write Start
Write data input
↓ 1 line's worth
Return command
Repeat for the number of lines to be displayed.
↓
Display ON (at least 40 ms after the sleep was released).
↓
Rewrite only a portion of the display contents.
Example: Page address set
Column address set
Write start
Write data input
↓ The amount to be rewritten
Return command
Repeat for the number of lines to be displayed.
↓
Read the part where there is content displayed.
Example: Page address set
Column address set
Read start
Data read
↓ The amount to be read
Return command
Repeat for the number of lines to be displayed.
↓

Reverse the display contents
Example: Page address set
Column address set
Read-modify-write start
↓ The amount to be rewritten
Return command
Repeat for the number of times to modify lines
↓
Display off.
↓
Change settings
Rewrite all display data
Example: Initialize command (CNTCLR) input
Write start
Write data input
↓ The amount to be rewritten
Return command
Repeat for the number of lines to be rewritten.
↓
Display ON
↓
Display OFF
↓
Sleep on
↓ Hold the power supply for 10 ms
Power supply OFF (V_{DD}, V_{SS})

Notes and Cautions:
1) When rewriting all data, do it with the display OFF.
2) Even when partial data is rewritten, do not continually rewrite the same area many times within a single frame interval (i.e. if the display is at 60 Hz, 16.6 mS).
3) Follow the specified sequences when turning the display ON and OFF.
4) Only the following three commands will affect the display because of noise:
   1. Display ON/OFF
   2. Display normal/inverted
   3. Sleep ON/OFF

If there is noise regardless of efforts, periodically insert the above three commands.
When entering data, set the address to start the data entry without using the return command.

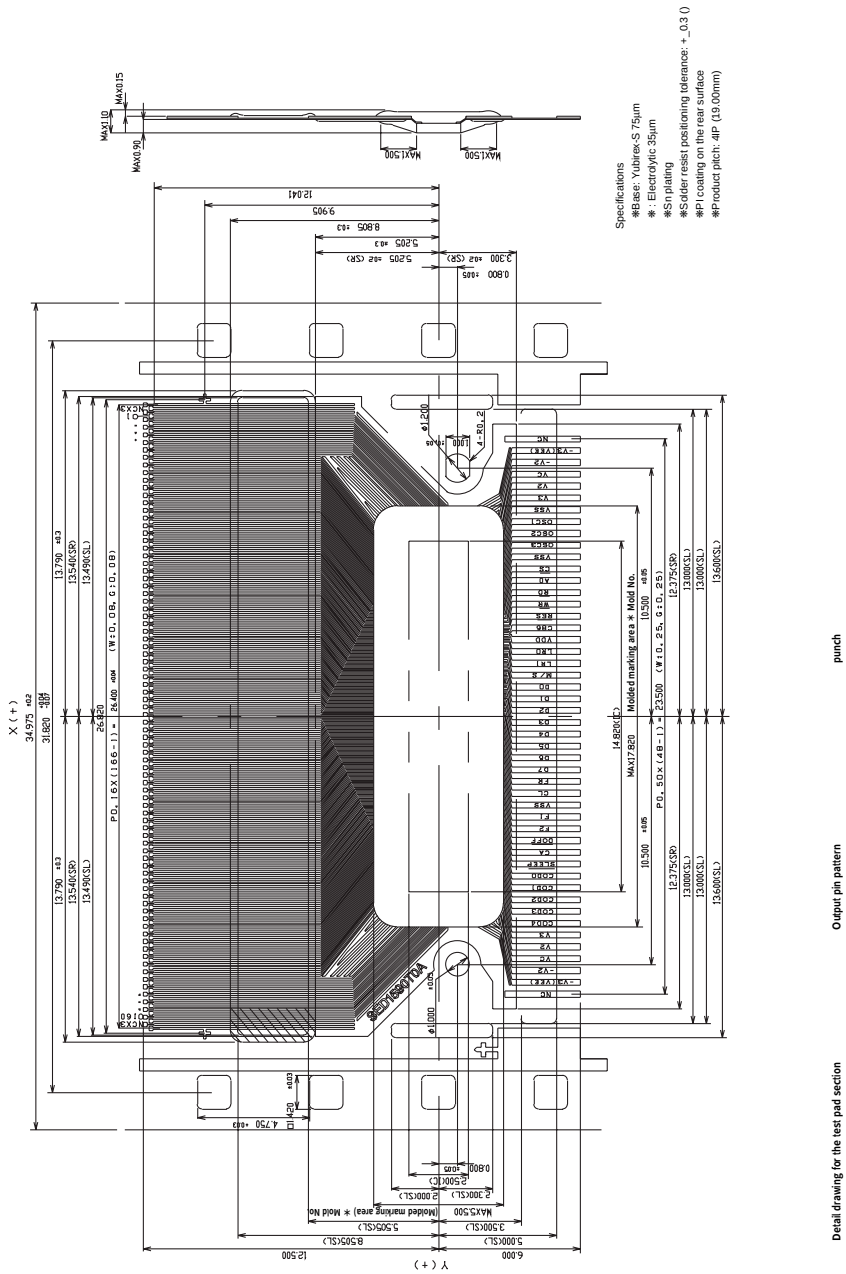
Notes

Be aware of the following when using these development specifications:
1. To facilitate improvements, the contents of these development specifications are subject to change without notice.
2. These development specifications neither guarantee the execution of industrial property rights or other authorities, nor grant execution authorities.

The examples of application found in these development specifications are strictly to assist in the understanding of this product; be aware that we assume absolutely no responsibility for problems in circuits wherein these examples are used.
Pay attention to the following precautions when using the SED1590 Series devices.

[Use When Exposed to Light]
The properties of semiconducting elements change when exposed to light because of the same principle used in everyday solar cells. Thus, exposure to light may cause this IC to malfunction.
(1) Design and package the actual application of the IC in a structure eliminates light.
(2) In test processes, design and package this IC in a structure that eliminates light.
(3) When eliminating light from the IC, eliminate light from the front surface, side surfaces, and back surface of the IC.

[Precautions against external noise, etc.]
(1) Although the SED1590 Series devices can preserve and store the operation status and the indicated data, excessive external noise may force to change the internal status. Consequently, take necessary measures to suppress noise or to avoid influences of the noise when designing their package or when designing a system using them.
(2) We recommend you to program a software which works to refresh the operation statuses (such as re-setting of the commands and re-transference of the indicated data) periodically to deal with occurrences of the sudden noise.


Specifications
*Base: Yubirex-S 75µm
*: Electrolytic 35µm
*Sn plating
*Solder resist positioning tolerance: +_0.3 ()
*PI coating on the rear surface
*Product pitch: 4IP (19.00mm)
Molded marking area * Mod No.
Output pin pattern
punch
Detail drawing for the test pad section
SED1590D0A
X (+)
Y (+)

SED1750

Contents

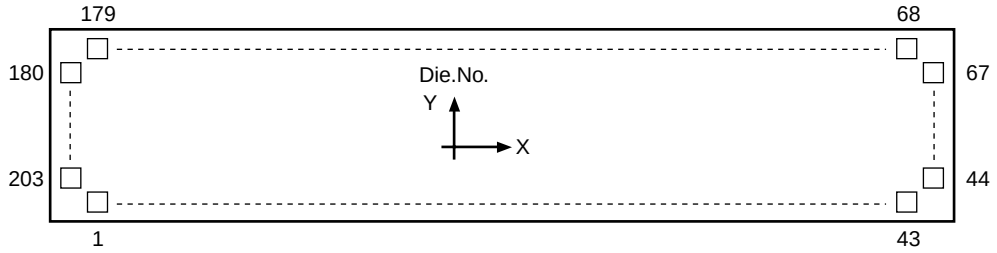
OVERVIEW

The SED1750 is an MLS (Multi Line Selection) driving, 160 output, triple-value low resistance common (low) driver which can realize high picture quality and high speed responses.
Receiving signals from an LCD controller such as the SED1335 or SED1351, it works to make 4-line MLS drives in combination with the SED1580 or in combination with the SED1590 receiving signals direct from the MPU. Employing the SCI7500 as the power IC, the power to use for the MLS drive liquid crystal display system can be prepared easily.
Adopting a slim chip shape which is more advantageous to realize narrower borders with the LCD panels, the SED1750 is capable of making low voltage logic power operations and is applicable to a wide range of applications.
Owing to its pad layout designed to facilitate its installation to the substrate and thanks to its two-way choices of the driver output sequence, the highest working efficiency can be acquired with a 1/160 or 1/320 duty panel.

Features

- LCD driver outputs 160
- Low output ON resistance
- High duty drive supported ..... 1/320 (Reference value)
- Broad range of LC drive voltages ..... + 14 to + 42 V (V_{CC} = 2.7 to 5.5 V)
- Output shift direction pin select is possible
- Can be switched between 140 and 160 outputs
- Non-biased display OFF function
- Logic system power source ..... 2.7 V to 5.5 V
- LC power source offset bias can be adjusted relative to the V_{DDH} and GND levels
- Slim chip shape
- D_{0B} ..... Au Bump die
- T_{0A} ..... TCP

Pad Layout



Chip size	15.62 mm × 2.47 mm
Pad pitch	80 μm (Min.)
Chip thickness	525 μm ± 25 μm

1) Au Bump Specifications (SED1750D_{0B}) Reference Values Only
Au vertical bump
Parallel to Scribe × Perpendicular to Scribe ± Tolerance

Bump Size A	60 μm × 75 μm ± 4 mm (Pad No. 1 to 43, 68 to 179)
Bump Size B	80 μm × 50 μm ± 4 mm (Pad No. 44 to 67, 180 to 203)
Bump height	17 to 28 μm (The details specified in the acceptance specifications.)

Pad Coordinates

Units: µm

Pin	Name	X	Y
1	V_{DDH}	-7522	-1045
2	+V1	-7427	
3	VC	-7332	
4	-V1	-7237	
5	V_{SS}	-7142	
6	SHL	-6804	
7	SEL	-6579	
8	V_{CC}	-6241	
9	LSEL	-5902	
10	DOFF	-5538	
11	FR	-4791	
12	DM	-4323	
13	DM	-3943	
14	DM	-3563	
15	DM	-3183	
16	DM	-2803	
17	CSEL	-2336	
18	LP	-1998	
19	DM	-1162	
20	CIO2	-755	
21	DM	-347	
22	DM	0	
23	DM	347	
24	CIO1	755	
25	DM	1162	
26	YD	1998	
27	DM	2336	
28	DM	2803	
29	DM	3183	
30	DM	3563	
31	DM	3943	
32	DM	4323	
33	DM	4791	
34	DM	5538	
35	F1	5902	
36	DM	6241	
37	F2	6579	
38	TEST1	6804	
39	V_{SS}	7142	
40	-V1	7237	
41	VC	7332	
42	+V1	7427	
43	V_{DDH}	7522	
44	COM1	7655	-935
45	COM2		-855
46	COM3		-775
47	COM4		-695
48	COM5		-615
49	COM6		-535
50	COM7		-455
51	COM8	7655	-375
52	COM9		-295
53	COM10		-215
54	COM11		-135
55	COM12		-55
56	COM13		25
57	COM14		105
58	COM15		185
59	COM16		265
60	COM17		345
61	COM18		425
62	COM19		505
63	COM20		585
64	COM21		665
65	COM22		745
66	COM23		825
67	COM24		905
68	COM25	7419.3	1083
69	COM26	7285.6	
70	COM27	7152	
71	COM28	7018.3	
72	COM29	6884.7	
73	COM30	6751	
74	COM31	6617.3	
75	COM32	6483.7	
76	COM33	6350	
77	COM34	6216.3	
78	COM35	6082.7	
79	COM36	5949	
80	COM37	5815.3	
81	COM38	5681.7	
82	COM39	5548	
83	COM40	5414.3	
84	COM41	5280.7	
85	COM42	5147	
86	COM43	5013.3	
87	COM44	4879.7	
88	COM45	4746	
89	COM46	4612.3	
90	COM47	4478.7	
91	COM48	4345	
92	COM49	4211.4	
93	COM50	4077.7	
94	COM51	3944	
95	COM52	3810.4	
96	COM53	3676.7	
97	COM54	3543	
98	COM55	3409.4	
99	COM56	3275.7	
100	COM57	3142	
101	COM58	3008.4	1083
102	COM59	2874.7	
103	COM60	2741	
104	COM61	2607.4	
105	COM62	2473.7	
106	COM63	2340	
107	COM64	2206.4	
108	COM65	2072.7	
109	COM66	1939	
110	COM67	1805.4	
111	COM68	1671.7	
112	COM69	1538.1	
113	COM70	1404.4	
114	COM71	1270.7	
115	COM72	1137.1	
116	COM73	1003.4	
117	COM74	869.7	
118	COM75	736.1	
119	COM76	602.4	
120	COM77	468.7	
121	COM78	335.1	
122	COM79	201.4	
123	COM80	67.7	
124	COM81	-67.7	
125	COM82	-201.4	
126	COM83	-335.1	
127	COM84	-468.7	
128	COM85	-602.4	
129	COM86	-736.1	
130	COM87	-869.7	
131	COM88	-1003.4	
132	COM89	-1137.1	
133	COM90	-1270.7	
134	COM91	-1404.4	
135	COM92	-1538.1	
136	COM93	-1671.7	
137	COM94	-1805.4	
138	COM95	-1939	
139	COM96	-2072.7	
140	COM97	-2206.4	
141	COM98	-2340	
142	COM99	-2473.7	
143	COM100	-2607.4	
144	COM101	-2741	
145	COM102	-2874.7	
146	COM103	-3008.4	
147	COM104	-3142	
148	COM105	-3275.7	
149	COM106	-3409.4	
150	COM107	-3543	

Pin	Name	X	Y
151	COM108	-3676.7	1083
152	COM109	-3810.4	
153	COM110	-3944	
154	COM111	-4077.7	
155	COM112	-4211.4	
156	COM113	-4345	
157	COM114	-4478.7	
158	COM115	-4612.3	
159	COM116	-4746	
160	COM117	-4879.7	
161	COM118	-5013.3	
162	COM119	-5147	
163	COM120	-5280.7	
164	COM121	-5414.3	
165	COM122	-5548	
166	COM123	-5681.7	
167	COM124	-5815.3	
168	COM125	-5949	

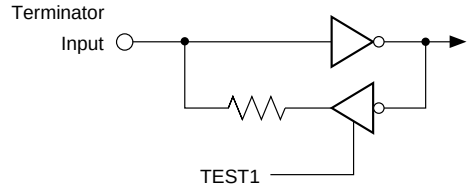
Pin	Name	X	Y
169	COM126	-6082.7	1083
170	COM127	-6216.3	
171	COM128	-6350	
172	COM129	-6483.7	
173	COM130	-6617.3	
174	COM131	-6751	
175	COM132	-6884.7	
176	COM133	-7018.3	
177	COM134	-7152	
178	COM135	-7285.6	
179	COM136	-7419.3	
180	COM137	-7655	905
181	COM138		825
182	COM139		745
183	COM140		665
184	COM141		585
185	COM142		505
186	COM143		425

Pin	Name	X	Y
187	COM144	-7655	345
188	COM145		265
189	COM146		185
190	COM147		105
191	COM148		25
192	COM149		-55
193	COM150		-135
194	COM151		-215
195	COM152		-295
196	COM153		-375
197	COM154		-455
198	COM155		-535
199	COM156		-615
200	COM157		-695
201	COM158		-775
202	COM159		-855
203	COM160		-935

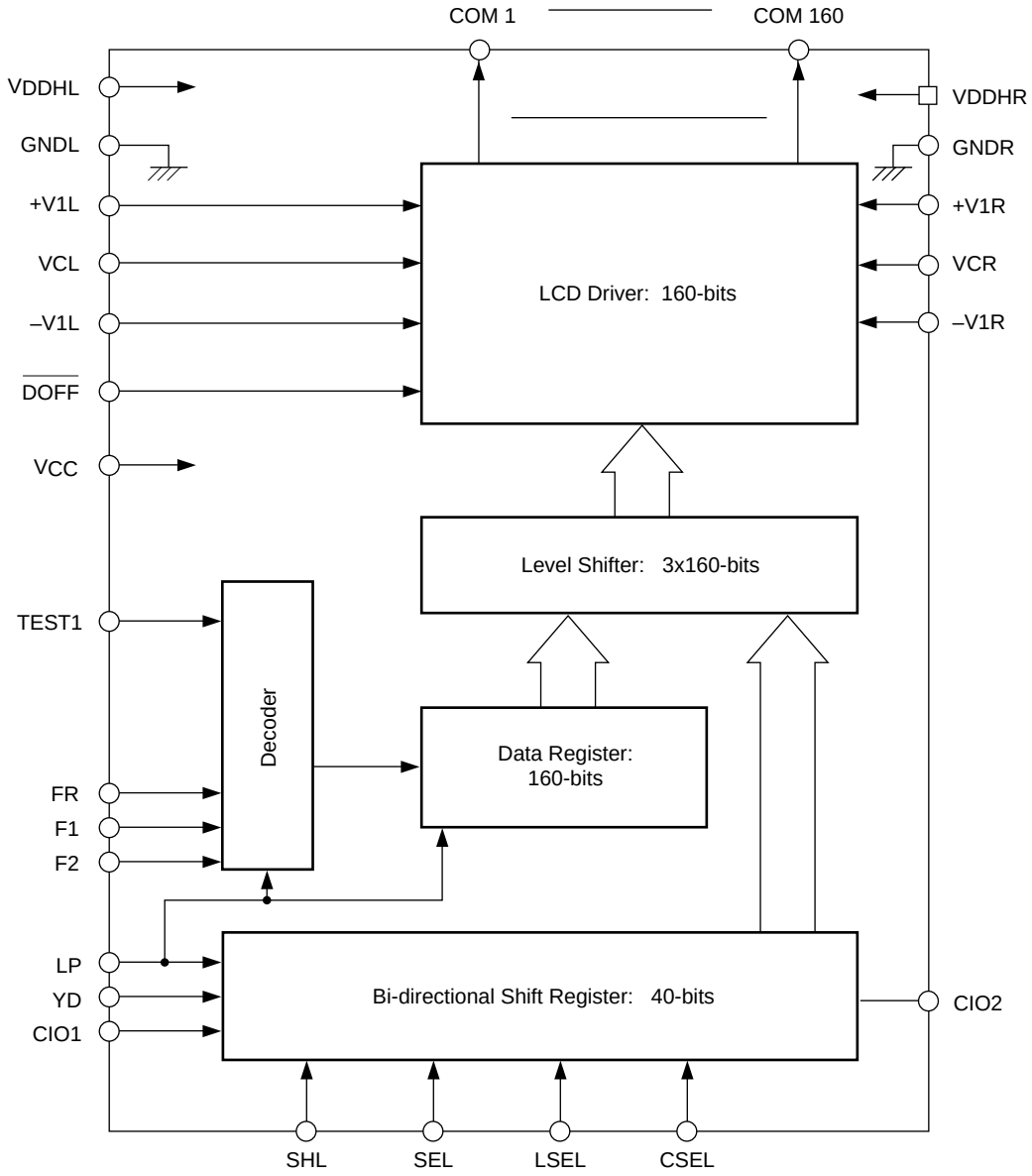
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Number of Terminals</th></tr>
<tr><td>COM1 to
COM160</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>160</td></tr>
<tr><td>CIO1
CIO2</td><td>I/O</td><td>Carry signal I/O.
This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of LP.</td><td>2</td></tr>
<tr><td>YD</td><td>I</td><td>Frame start/pulse input, with terminator. (*1)</td><td>1</td></tr>
<tr><td>F1, F2</td><td>I</td><td>Drive pattern select signal input, with terminator. (*1)</td><td>2</td></tr>
<tr><td>LP</td><td>I</td><td>Shift clock input for display data.
(Triggers on falling edge.) With terminator. (*1)</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and CIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th></th></tr>
<tr><th>CIO1</th><th>CIO2</th></tr>
<tr><td>L</td><td>1(9) → 160(148)</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>160(148) → 1(9)</td><td>Output</td><td>Input</td></tr>
</table>
The numbers in parentheses are for 140 output mode.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Select input for the number of COM output terminals:
160 outputs ←→ 140 outputs
L: COM1 to COM160
H: COM9 to COM148</td><td>1</td></tr>
<tr><td>LSEL</td><td>I</td><td>1/2 H operation select signal input.
L: Normal operation. H: 1/2 operation.</td><td>1</td></tr>
<tr><td>CSEL</td><td>I</td><td>Chip select signal input for when a cascade connection is used.
L: Leading chip
H: Other chips</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1)</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LC display blanking control input. With a low level input, all common outputs are temporarily set to the V_C level. The contents of the latches are maintained. With terminator (*1)</td><td>1</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test1 signal input. Normally tied at L.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL, GNDR</td><td>Power</td><td>Power source for logic:
GND: 0 V , V_{CC}: +2.7 to 5.5 V</td><td>3</td></tr>
<tr><td>V_{CL}, V_{CR}, $+V_{1L}$, $+V_{1R}$, $-V_{1L}$, $-V_{1R}$, V_{DDHL}, V_{DDHR}</td><td>Power</td><td>LC Drive Power:
GND: 0 V,
V_{DDH}: + 14.0 to 42.0 V, $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq$ GND</td><td>8</td></tr>
<tr><td>DM</td><td></td><td>Dummy pad</td><td>19</td></tr>
<tr><td></td><td></td><td>Total</td><td>203</td></tr>
</table>

Note: *1



Block Diagram



Explanation of Each Block

Shift Register

This is a bi-directional shift register used for transmitting common data. The display data shifts on the falling edge of LP.

Level Shifter

The level shifter is a voltage level converter circuit which converts the signal voltage level from a logic system level to the LC driver system voltage level.

LCD Driver

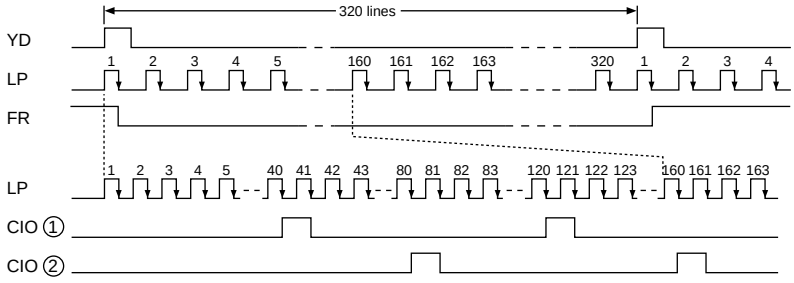
The LCD driver outputs the LC drive voltage.
The relationship between the display blanking signal $\overline{DOFF}$, the field recognition signals F1 & F2, the AC signal FR, and the common output voltage is as follows:

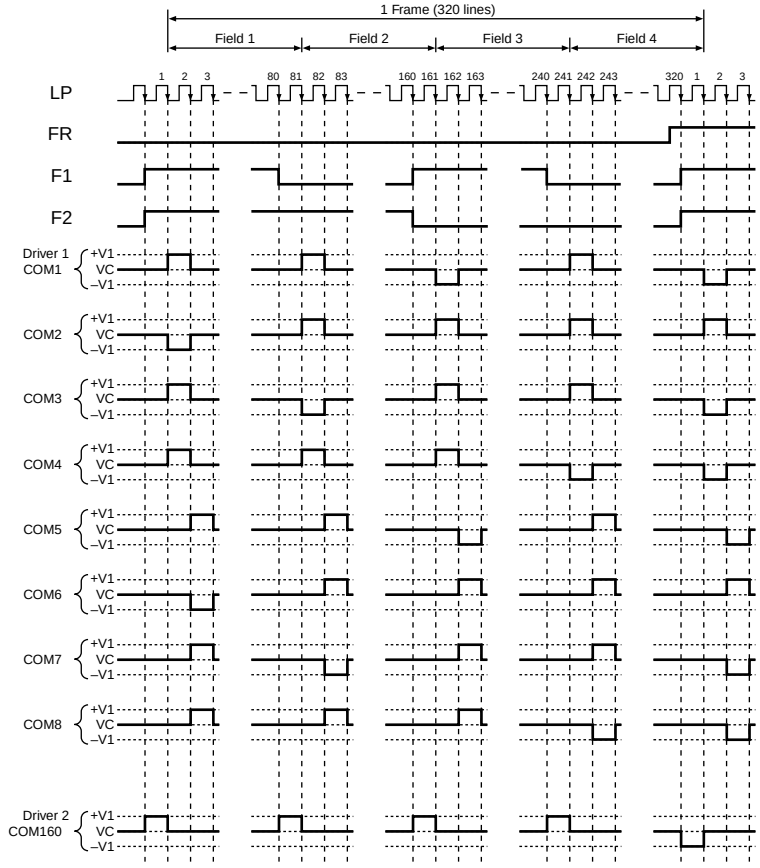
$\overline{DOFF}$	H								L
FR	L				H				—
F1,F2	1,1	0,1	1,0	0,0	1,1	0,1	1,0	0,0	—
Line 1	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	$+V_1$	$-V_1$	V_C
Line 2	$-V_1$	$+V_1$	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	V_C
Line 3	$+V_1$	$-V_1$	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	V_C
Line 4	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	$-V_1$	$+V_1$	V_C

Voltage level relationships: $+V_1 > V_C > -V_1$ (V_C is the center voltage level)

Timing Diagram (1)

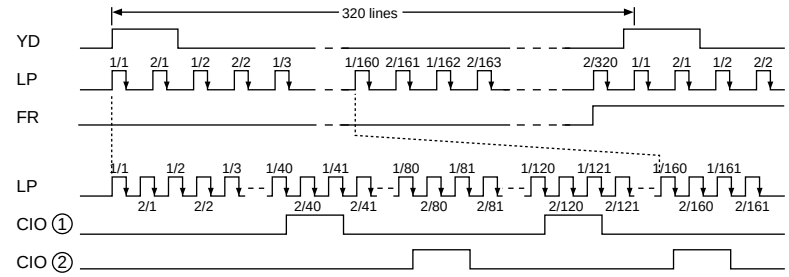
1/320 duty, normal operation.
SHL = L, SEL = L, LSEL = L, CSEL = L (This diagram provided only as a reference.)

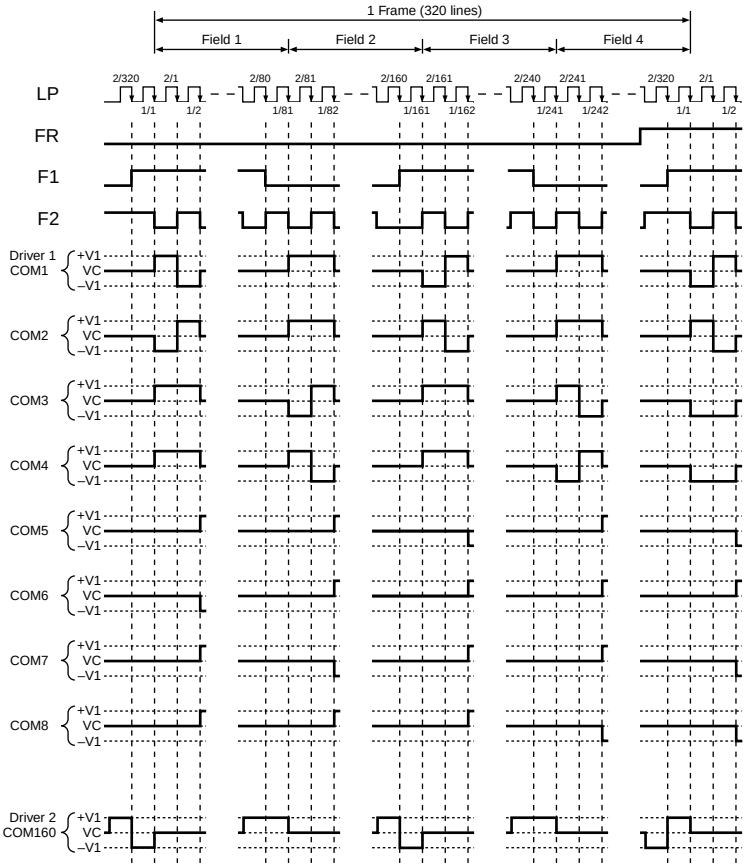




Timing Diagram (2)

1/320 duty, 1/2 H operation.
SHL = L, SEL = L, LSEL = H, CSEL = L (This diagram provided only as a reference.)

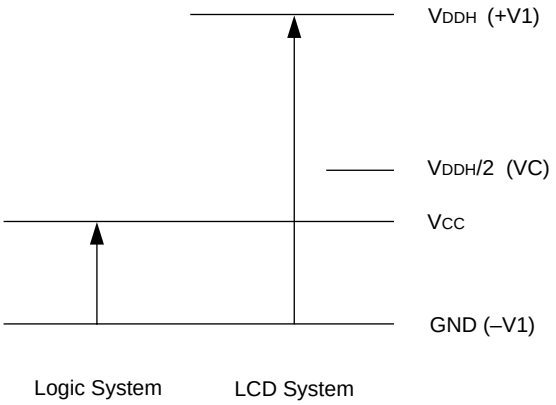




ABSOLUTE MAXIMUM RATINGS

Item	Signal	Rated Value	Units
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to + 45.0	V
Power voltage (3)	± V_1, V_C	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
CIO output current	I_{O1}	20	mA
Operating temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

NOTE 1: The voltages are all relative to GND = 0 V.
NOTE 2: Storage temperature 1 is for the chip alone, and storage temperature 2 is for the TCP product.
NOTE 3: Ensure that the relationship between $+V_1$, V_C, and $-V_1$ is always as follows: $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq GND$.



NOTE 4: The LSI may be permanently damaged if the logic system power is floating or V_{CC} is less than or equal to 2.6 V when power is applied to the LC drive system. Special caution must be paid to the power sequences during power up and power down.

Electrical Characteristics

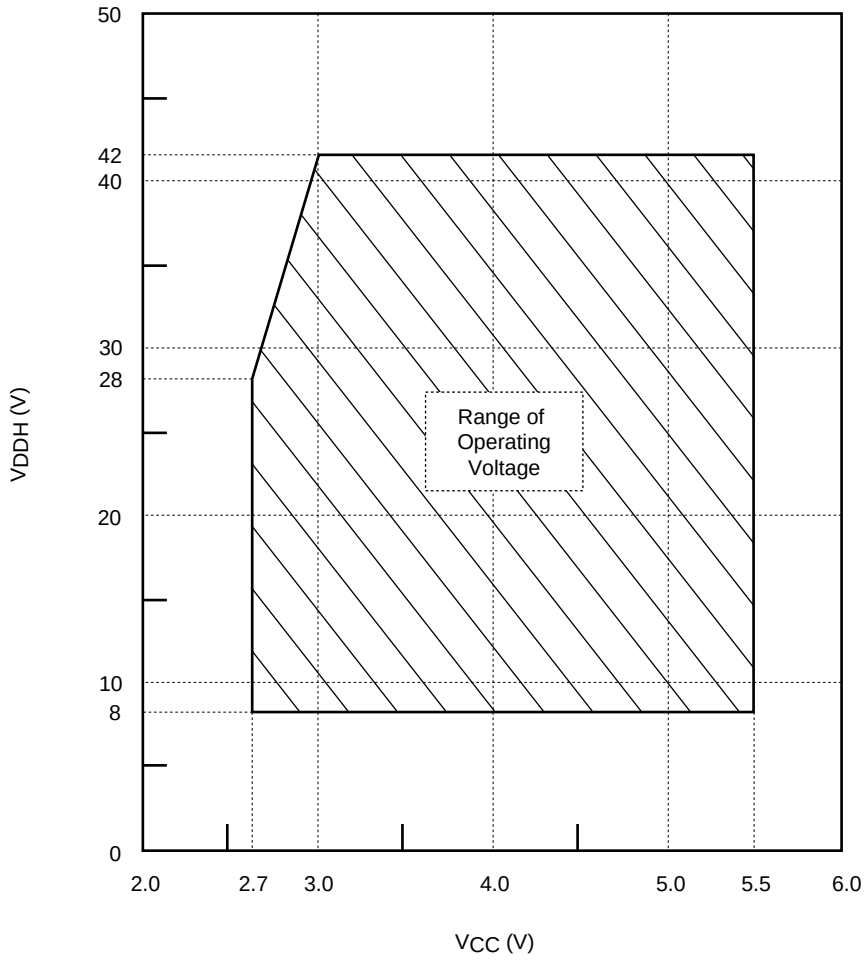
DC Characteristics

Unless otherwise noted, GND = 0 V, V_{CC} = + 5.0 V ± 10%, Ta = –30 to 85°C

Item	Signal	Parameter		Applicable Terminals	Min	Typ	Max	Unit
Power Supply Voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Range Operating Voltages	V_{DDH}	Function		V_{DDH}	8.0		42.0	V
Power Supply Voltage (2)	$+V_1$	Recommended Value		$+V_1$			V_{DDH}	V
Power Supply Voltage (3)	V_C	Recommended Value		V_C		$V_{DDH}/2$		V
Power Supply Voltage (4)	$–V_1$	Recommended Value		$–V_1$	GND			V
High-level Input Voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		CIO1,CIO2,FR, YD,LP,SHL,SEL, LSEL,CSEL, $\overline{DOFF}$,F1,F2, TEST1	0.8V_{CC}			V
Low-level Input Voltage	V_{IL}						0.2V_{CC}	V
High-level Output Voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	CIO1,CIO2	V_{CC}–0.4			V
Low-level Output Voltage	V_{OL}		I_{OL} = 0.3mA				0.4	V
Input Leakage Current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		LP,YD,SHL,SEL, LSEL,CSEL,F1, F2,$\overline{DOFF}$,TEST1, FR			2.0	µA
Input/Output Leakage Current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		CIO1,CIO2			5.0	µA
Static Current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND			25	µA
Output Resistance	R_{COM}	ΔVON = 0.5 V Recommended parameter	V_{DDH} = +30.0V	COM1 to COM120		0.55	0.7	kΩ
			V_{DDH} = +40.0V			0.5	0.7	
Average Operating Consumption Current (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC} V_{IL} = GND, f_{LP} = 22.4 kHz f_{FR} = 70 Hz, Input data: 1/320 No load		V_{CC}		12	25	µA
		V_{CC} = 3.0 V All other parameters the same as V_{CC} = 5.0 V.				8	17	
Average Operating Consumption Current (2)	I_{DDH}	V_{DDH} = $+V_1$ = +30.0 V, V_C = $V_{DDH}/2$, $–V_1$ = 0.0 V, V_{CC} = 5.0 V All other parameters the same as the I_{CC} item.		V_{DDH}		7	13	µA
Input Terminal Capacity	C_I	Freq. = 1 MHz Chip alone Ta = 25°C		LP,YD,SHL,SEL, LSEL,CSEL,F1,F2, $\overline{DOFF}$,TEST1,FR			10	pF
Input/Output Terminal Capacity	$C_{I/O}$			CIO1,CIO2			18	pF

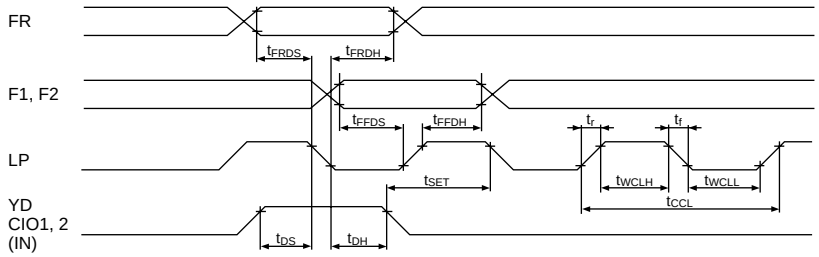
Range of Operating Voltages: V_{CC} – V_{DDH}

It is necessary to set the voltage for V_{DDH} within the V_{CC} – V_{DDH} operating voltage range shown in the diagram below.



AC Characteristics

Input Timing Characteristics



The FR latched at the nth LP is reflected in the output at the n+1th LP.

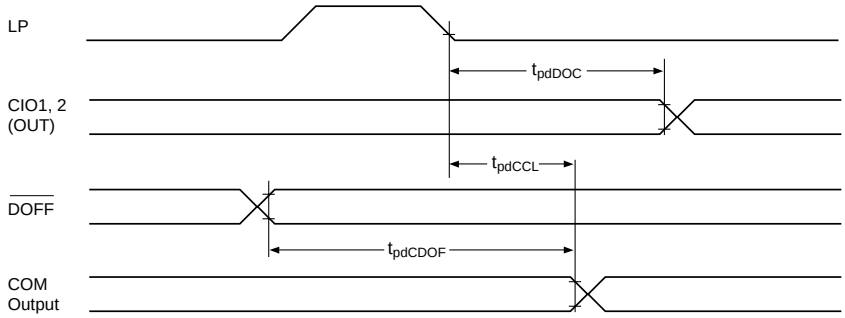
(V_{CC} = +5.0 V ± 10%, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		500		ns
LP "H" Pulse Width	t_{WCLH}		55		ns
LP "L" Pulse Width	t_{WCLL}		330		ns
FR Setup Time	t_{FRDS}		100		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		100		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			50	ns
Input Signal Fall Time	tf			50	ns
CIO Setup Time	t_{DS}		100		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		80		ns

(V_{CC} = +2.7 V to 4.5 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		800		ns
LP "H" Pulse Width	t_{WCLH}		100		ns
LP "L" Pulse Width	t_{WCLL}		660		ns
FR Setup Time	t_{FRDS}		200		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		200		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			100	ns
Input Signal Fall Time	tf			100	ns
CIO Setup Time	t_{DS}		200		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		150		ns

Output Timing Characteristics



(V_{CC} = 5.0 V ± 10%, V_{DDH} = +14.0 to +42.0 V, Ta = –30 to +85°C)

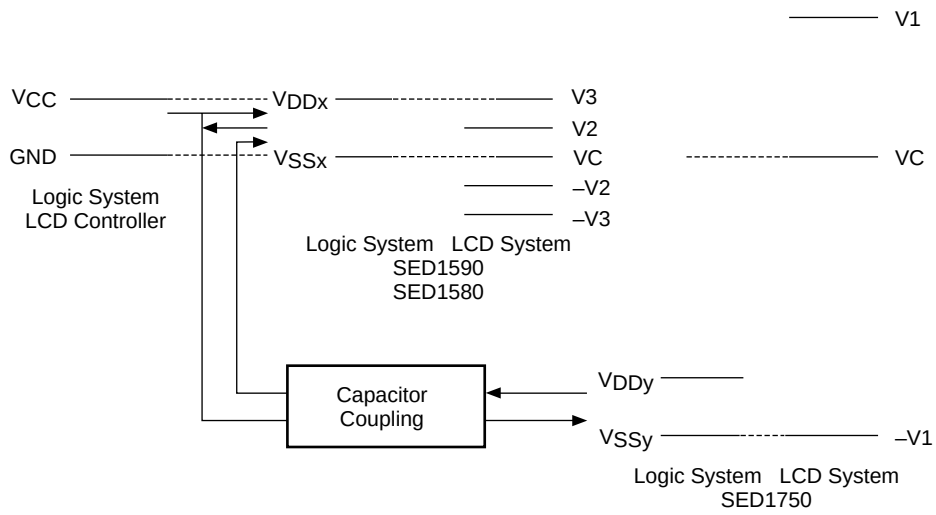
Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		300	ns
Delay time from LP to COM output	t_{pdCCL}			350	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			700	ns

(V_{CC} = +2.7 V to 4.5 V, V_{DDH} = +14.0 to +28.0 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		600	ns
Delay time from LP to COM output	t_{pdCCL}			500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

The Power Supply

Method of Forming Each Voltage Level



When the SED1590 (SED1580) and the SED1750 are used to form an extremely low power module system, the power relationships as shown in the figure above between the SED1590 (SED1580) and SED1750 logic systems, and the LCD system power supply, and the LCD controller power supply are optimal.

In this case, care is required when it comes to signal propagation in the logic system.

LCD Controller	→	SED1580, SED1590	Direct
LCD Controller	→	SED1750	Capacitor coupling is required
SED1580, SED1590	→	SED1750	Capacitor coupling is required
SED1750	→	SED1580, SED1590	Capacitor coupling is required

Cautions at Power Up and Power Down

Because the voltage level in the LCD system is high voltage, if the logic system power supply of this LSI is floating or if V_{CC} is 2.6 V or less when the LCD system high voltage (30 V or above) is applied, or if the LCD drive signal is output before the voltage level that is applied to the LCD system has stabilized, then there is the risk that there will be an over current condition in this LSI, resulting in permanent damage to this LSI.

It is recommended that the display OFF function (DOFF) is used until the LCD system voltage stabilizes to insure that the LCD drive output power level is at the VC level.

Be sure to follow the sequences below when turning the power supplies ON and OFF:

When turning the power supply ON:

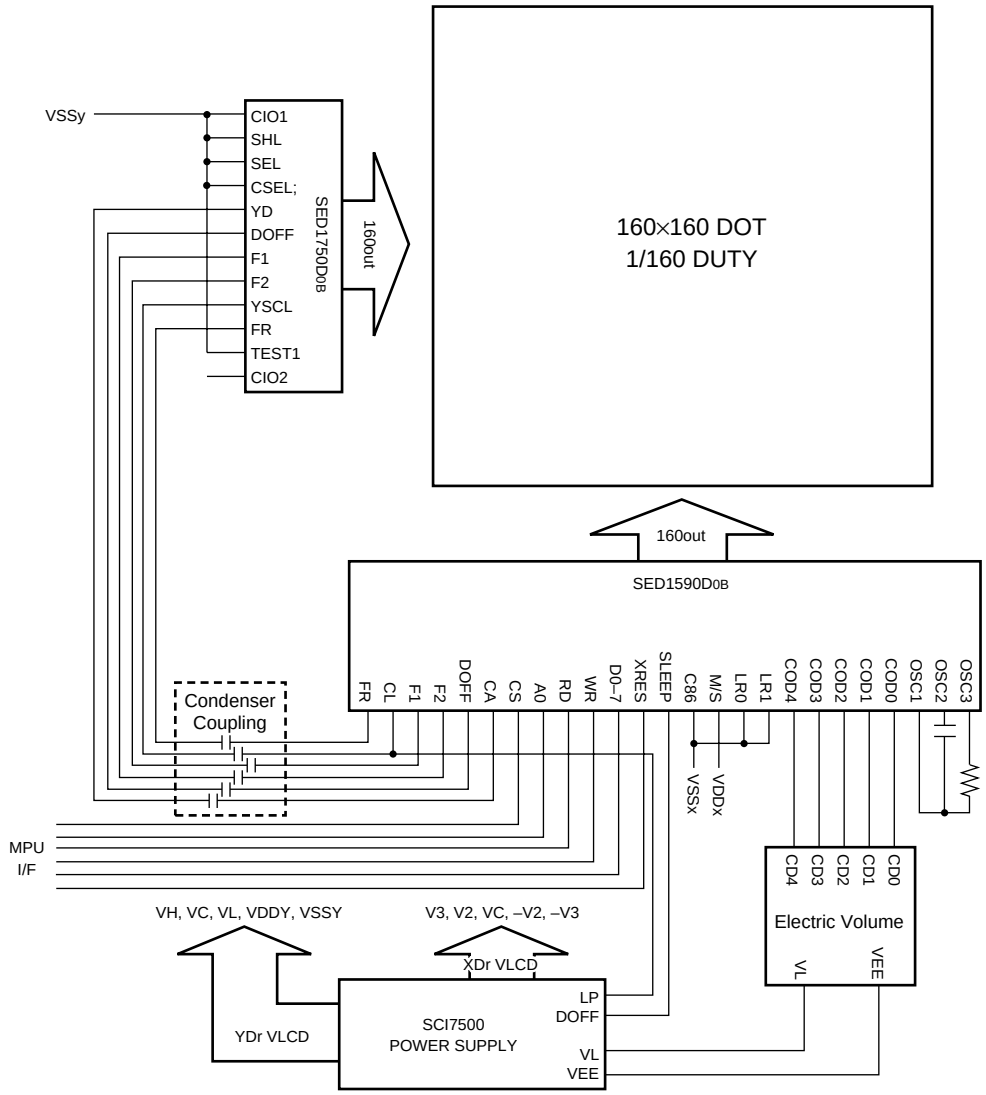
Logic system ON → LCD drive system ON, or simultaneously ON.

When turning the power supply OFF:

LCD drive system OFF → Logic system OFF, or simultaneously OFF.

As a countermeasure to guard against over current conditions, it is effective to insert a high-speed fuse or a guard resistance in series with the LC power supply. The guard resistance value must be optimized depending on the capacity of the LC cell.

Example of Connection



SED1751

Contents

OVERVIEW

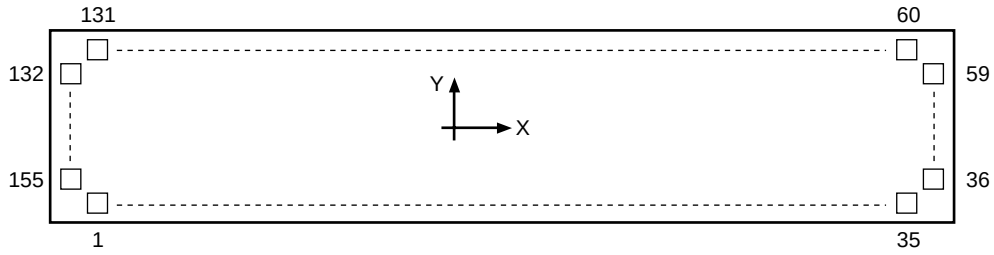
Description

The SED1751 is an 120 output, 3-level low-resistance common (row) driver suitable for high-quality, high-response-speed MLS (Multi Line Selection) driving.
The SED1751 receives signals from LCD controllers such as the SED1335, and when used is used in conjunction with the SED1580, can be used to structure a 4-line MLS drive.
The SED1751 uses a slim-chip form that is useful for making LCD panels slimmer. It also supports reduced logic system voltage operation, making it suitable for a broad range of applications.
The SED1751 has a pad layout supporting easy mounting, and supports bi-directional selection of driver output order, and has the highest use efficiency for 1/240 and 1/480 duty panels.

Features

- LCD driver outputs 120
- Low output ON resistance
- High duty drive supported ..... 1/480 (Reference value)
- Broad range of LC drive voltages ..... + 14 to + 42 V (V_{CC} = 2.7 to 5.5 V)
- Output shift direction pin select is possible
- Can be switched between 100 and 120 outputs
- Non-biased display OFF function
- Logic system power source ..... 2.7 V to 5.5 V
- LC power source offset bias can be adjusted relative to the V_{DDH} and GND levels
- Slim chip shape
- D_{0B} ..... Au Bump die
- T_{0A} ..... TCP

Pad Layout



Chip size 12.19 mm × 2.38 mm
Pad pitch 80 µm (Min.)
Chip thickness 525 µm ± 25 µm

1) Au Bump Specifications (SED1751D_{0B}) Reference Values Only
Au vertical bump
Parallel to Scribe × Perpendicular to Scribe ± Tolerance
Bump Size A 60 µm × 75 µm ± 4 µm (Pad No. 1 to 35, 60 to 131)
Bump Size B 80 µm × 50 µm ± 4 µm (Pad No. 36 to 59, 132 to 155)
Bump height 17 to 28 µm (The details specified in the acceptance specifications.)

Pad Coordinates

Units: µm

Pin	Name	X	Y
1	V_{DDHL}	–5812	–1012
2	$+V_{1L}$	–5717	
3	V_{CL}	–5622	
4	$–V_{1L}$	–5527	
5	GNDL	–5432	
6	SHL	–5094	
7	SEL	–4869	
8	V_{CC}	–4531	
9	LSEL	–4192	
10	$\overline{DOFF}$	–3828	
11	FR	–3081	
12	CSEL	–2336	
13	LP	–1998	
14	DM	–1162	
15	CIO2	–755	
16	DM	–347	
17	DM	0	
18	DM	347	
19	CIO1	755	
20	DM	1162	
21	YD	1998	
22	DM	2336	
23	DM	2674	
24	DM	3081	
25	DM	3489	
26	DM	3828	
27	F1	4192	
28	DM	4531	
29	F2	4869	
30	TEST1	5094	
31	GNDR	5432	
32	$–V_{1R}$	5527	
33	V_{CR}	5622	
34	$+V_{1R}$	5717	
35	V_{DDHR}	5812	

Pin	Name	X	Y
36	COM1	5945	–902
37	COM2		–822
38	COM3		–742
39	COM4		–662
↓	↓	↓	↓
57	COM22	5945	778
58	COM23	5945	858
59	COM24	5945	938
60	COM25	5709	1034
61	COM26	5549	1034
62	COM27	5389	1034
↓	↓	↓	↓
93	COM58	429	1034
94	COM59	269	
95	COM60	109	
96	COM61	–109	
97	COM62	–269	
98	COM63	–429	
↓	↓	↓	↓
129	COM94	–5389	1034
130	COM95	–5549	1034
131	COM96	–5709	1034
132	COM97	–5945	938
133	COM98	–5945	858
134	COM99	–5945	778
↓	↓	↓	↓
152	COM117	–5945	–662
153	COM118		–742
154	COM119		–822
155	COM120		–902

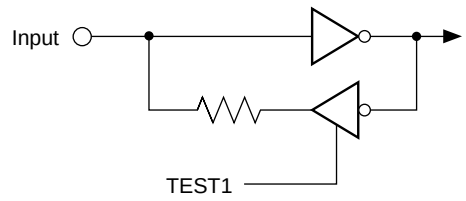
COMn XY coordinates:

COM1 to COM24: (5945, –902 + [80 × (n–1)])
COM25 to COM60: (5709 – [160 × (n–25)], 1034)
COM61 to COM96: (–109 – [160 × (n–61)], 1034)
COM97 to COM120: (–5945, 938 – [80 × (n–97)])

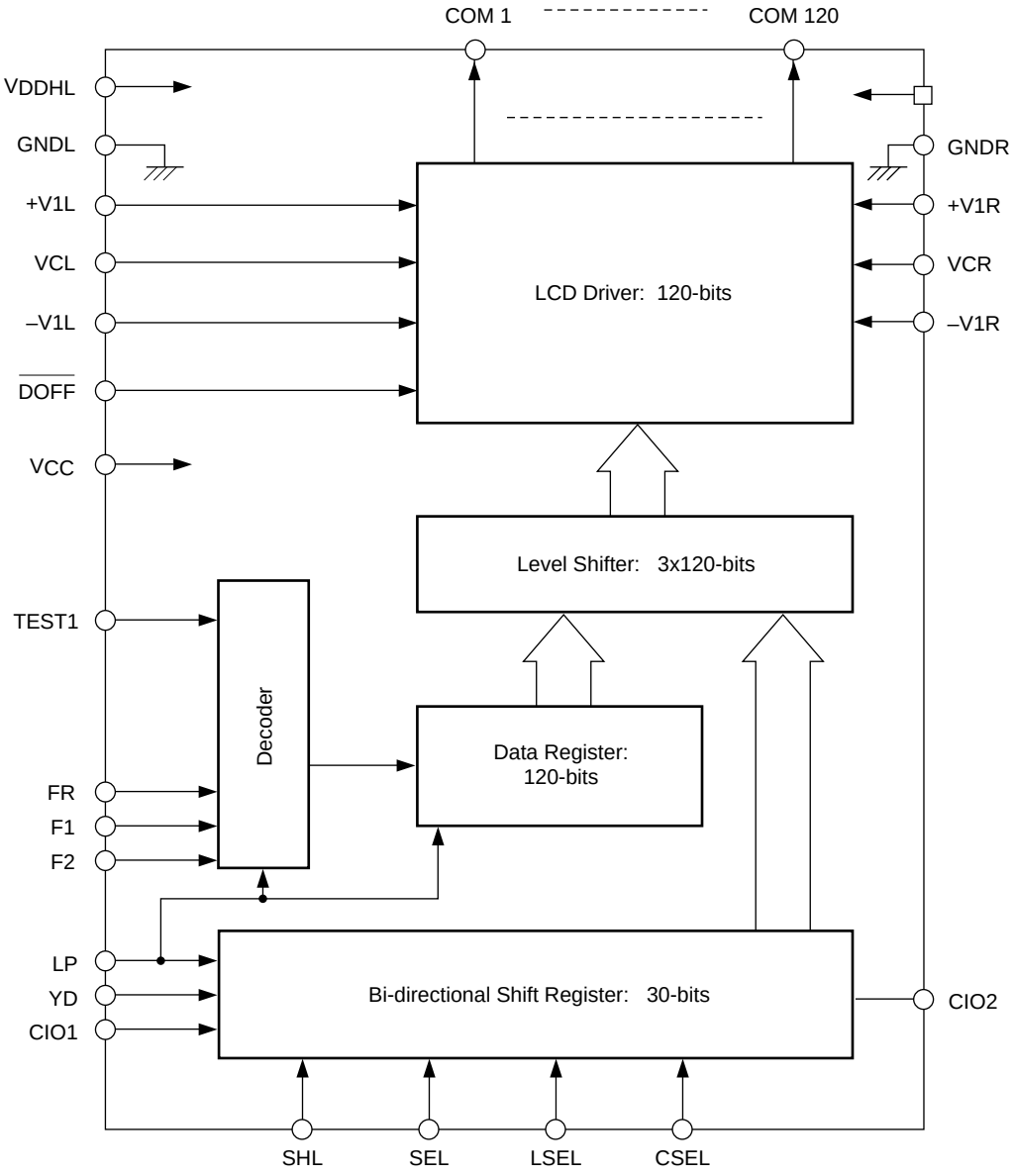
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Number of Terminals</th></tr>
<tr><td>COM1 to COM120</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>120</td></tr>
<tr><td>CIO1
CIO2</td><td>I/O</td><td>Carry signal I/O.
This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of LP.</td><td>2</td></tr>
<tr><td>YD</td><td>I</td><td>Frame start/pulse input, with terminator. (*1)</td><td>1</td></tr>
<tr><td>F1, F2</td><td>I</td><td>Drive pattern select signal input, with terminator. (*1)</td><td>2</td></tr>
<tr><td>LP</td><td>I</td><td>Shift clock input for display data.
(Triggers on falling edge.) With terminator. (*1)</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and CIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th colspan="2">CIO</th></tr>
<tr><th>CIO1</th><th>CIO2</th></tr>
<tr><td>L</td><td>1(9) → 120(108)</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>120(108) → 1(9)</td><td>Output</td><td>Input</td></tr>
</table>
The numbers in parentheses are for 100 output mode.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Select input for the number of COM output terminals:
120 outputs ←→ 100 outputs
L: COM1 to COM120
H: COM9 to COM108</td><td>1</td></tr>
<tr><td>LSEL</td><td>I</td><td>1/2 H operation select signal input.
L: Normal operation. H: 1/2 operation.</td><td>1</td></tr>
<tr><td>CSEL</td><td>I</td><td>Chip select signal input for when a cascade connection is used.
L: Leading chip
H: Other chips</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1)</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LC display blanking control input. With a low level input, all common outputs are temporarily set to the V_C level. The contents of the latches are maintained. With terminator (*1)</td><td>1</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test1 signal input. Normally tied at L.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL, GNDR</td><td>Power</td><td>Power source for logic:
GND: 0 V , V_{CC}: +2.7 to 5.5 V</td><td>3</td></tr>
<tr><td>V_{CL}, V_{CR}, $+V_{1L}$, $+V_{1R}$, $-V_{1L}$, $-V_{1R}$, V_{DDHL}, V_{DDHR}</td><td>Power</td><td>LC Drive Power:
GND: 0 V,
V_{DDH}: + 14.0 to 42.0 V, $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq$ GND</td><td>8</td></tr>
<tr><td>DM</td><td></td><td>Dummy pad</td><td>11</td></tr>
<tr><td></td><td></td><td>Total</td><td>155</td></tr>
</table>

Note: *1



Block Diagram



Explanation of Each Block

Shift Register

This is a bi-directional shift register used for transmitting common data. The display data shifts on the falling edge of LP.

Level Shifter

The level shifter is a voltage level converter circuit which converts the signal voltage level from a logic system level to the LC driver system voltage level.

LCD Driver

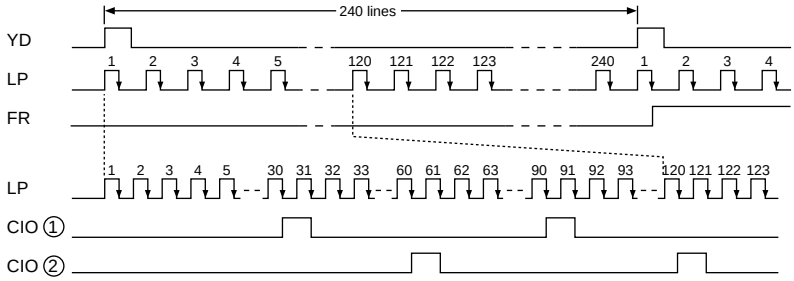
The LCD driver outputs the LC drive voltage.
The relationship between the display blanking signal $\overline{DOFF}$, the field recognition signals F1 & F2, the AC signal FR, and the common output voltage is as follows:

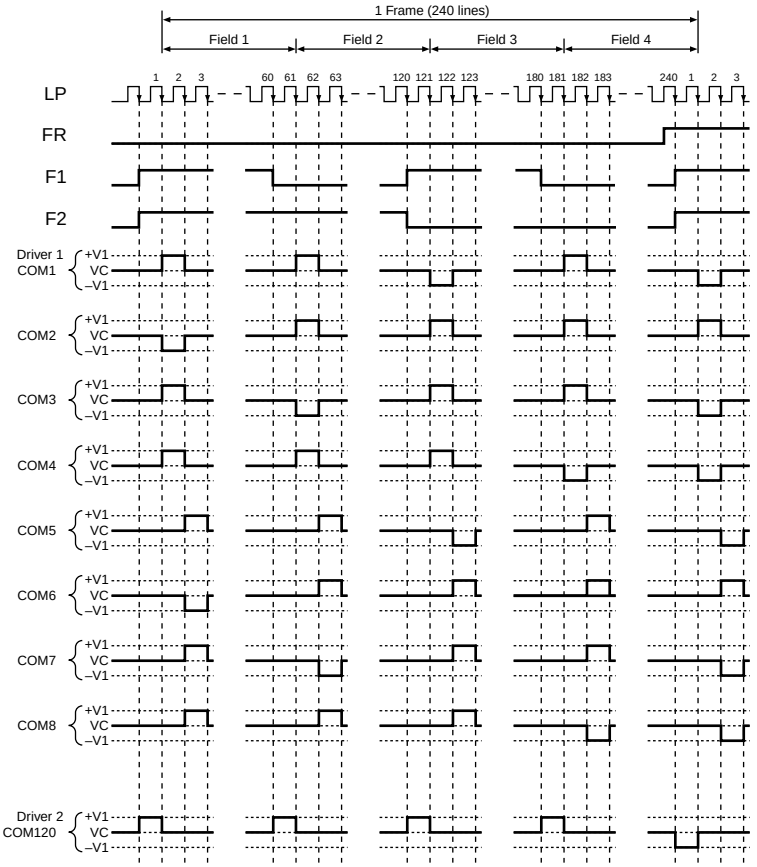
$\overline{DOFF}$	H								L
FR	L				H				—
F1,F2	1,1	0,1	1,0	0,0	1,1	0,1	1,0	0,0	—
Line 1	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	$+V_1$	$-V_1$	V_C
Line 2	$-V_1$	$+V_1$	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	V_C
Line 3	$+V_1$	$-V_1$	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	V_C
Line 4	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	$-V_1$	$+V_1$	V_C

Voltage level relationships: $+V_1 > V_C > -V_1$ (V_C is the center voltage level)

Timing Diagram (1)

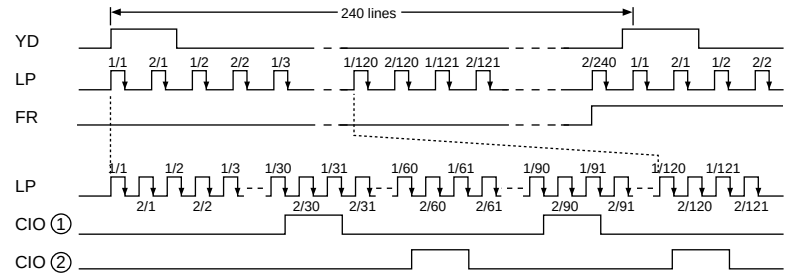
1/240 duty, normal operation.
SHL = L, SEL = L, LSEL = L, CSEL = L (This diagram provided only as a reference.)

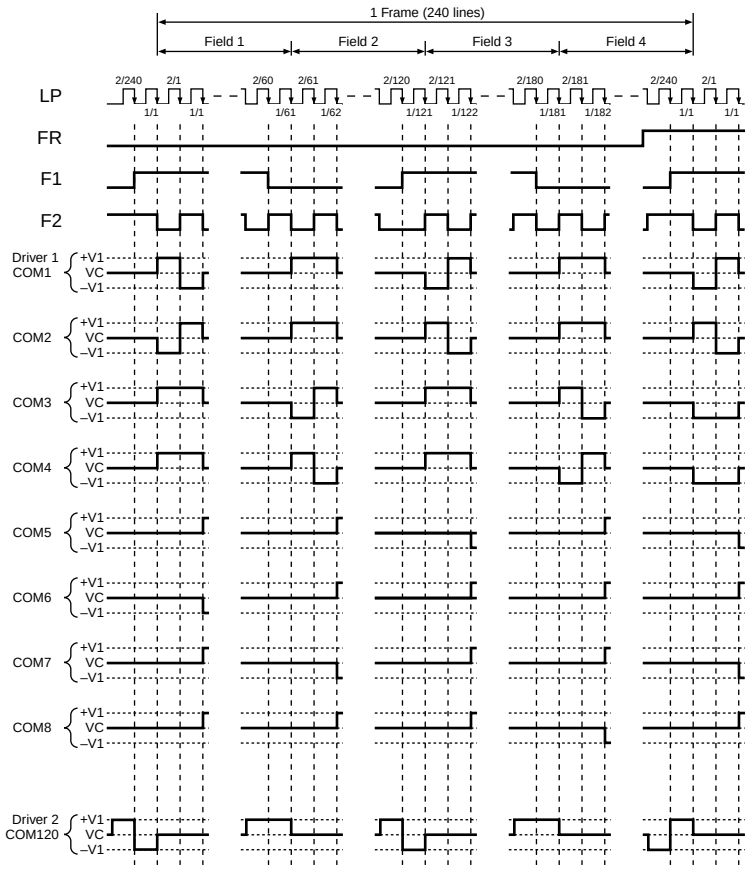




Timing Diagram (2)

1/240 duty, 1/2 H operation.
SHL = L, SEL = L, LSEL = H, CSEL = L (This diagram provided only as a reference.)

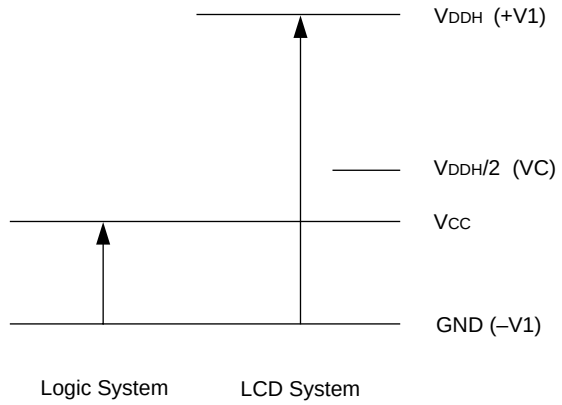




ABSOLUTE MAXIMUM RATINGS

Item	Signal	Rated Value	Units
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to + 45.0	V
Power voltage (3)	± V_1, V_C	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
CIO output current	I_{O1}	20	mA
Operating temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

NOTE 1: The voltages are all relative to GND = 0 V.
NOTE 2: Storage temperature 1 is for the chip alone, and storage temperature 2 is for the TCP product.
NOTE 3: Ensure that the relationship between $+V_1$, V_C, and $-V_1$ is always as follows: $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq GND$.



NOTE 4: The LSI may be permanently damaged if the logic system power is floating or V_{CC} is less than or equal to 2.6 V when power is applied to the LC drive system. Special caution must be paid to the power sequences during power up and power down.

Electrical Characteristics

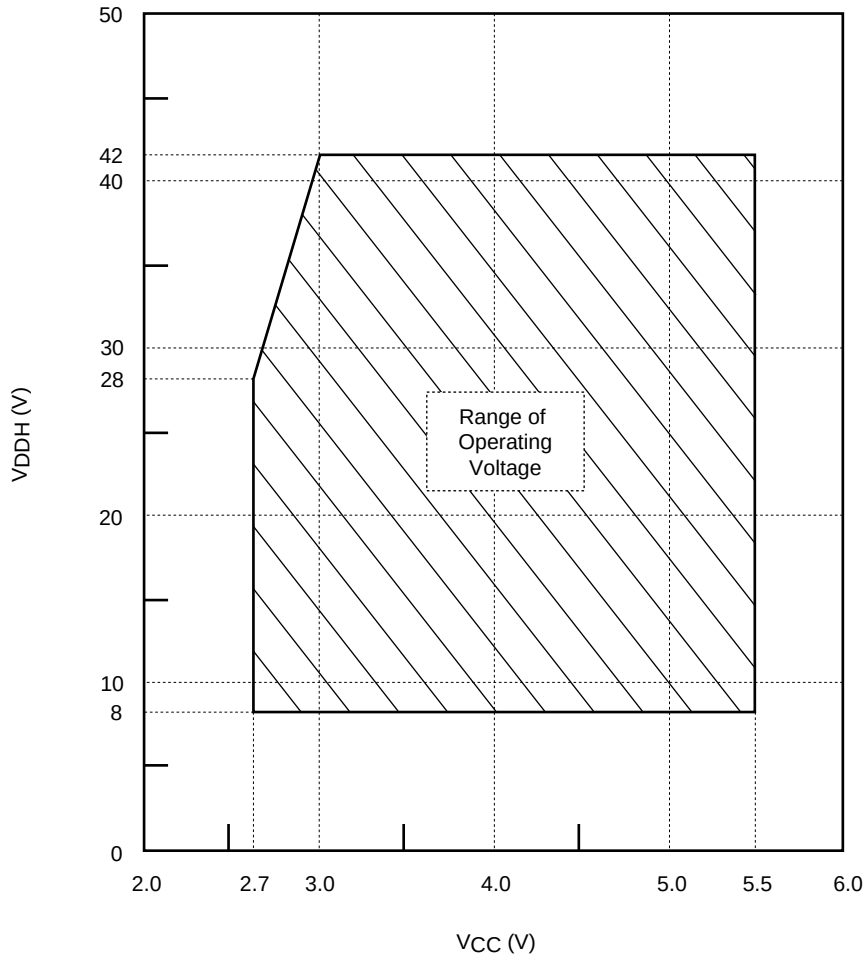
DC Characteristics

Unless otherwise noted, GND = 0 V, V_{CC} = + 5.0 V ± 10%, Ta = –30 to 85°C

Item	Signal	Parameter		Applicable Terminals	Min	Typ	Max	Unit
Power Supply Voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Range Operating Voltages	V_{DDH}	Function		V_{DDH}	8.0		42.0	V
Power Supply Voltage (2)	$+V_1$	Recommended Value		$+V_1$			V_{DDH}	V
Power Supply Voltage (3)	V_C	Recommended Value		V_C		$V_{DDH}/2$		V
Power Supply Voltage (4)	$–V_1$	Recommended Value		$–V_1$	GND			V
High-level Input Voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		CIO1,CIO2,FR, YD,LP,SHL,SEL, LSEL,CSEL, $\overline{DOFF}$,F1,F2, TEST1	0.8V_{CC}			V
Low-level Input Voltage	V_{IL}						0.2V_{CC}	V
High-level Output Voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	CIO1,CIO2	V_{CC}–0.4			V
Low-level Output Voltage	V_{OL}		I_{OL} = 0.3mA				0.4	V
Input Leakage Current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		LP,YD,SHL,SEL, LSEL,CSEL,F1, F2,$\overline{DOFF}$,TEST1, FR			2.0	µA
Input/Output Leakage Current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		CIO1,CIO2			5.0	µA
Static Current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND			25	µA
Output Resistance	R_{COM}	ΔVON = 0.5 V Recommended parameter	V_{DDH} = +30.0V	COM1 to COM120		0.55	0.7	kΩ
			V_{DDH} = +40.0V			0.5	0.7	
Average Operating Consumption Current (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC} V_{IL} = GND, f_{LP} = 16.8 kHz f_{FR} = 70 Hz, Input data: 1/240 No load		V_{CC}		10	25	µA
		V_{CC} = 3.0 V All other parameters the same as V_{CC} = 5.0 V.				7	17	
Average Operating Consumption Current (2)	I_{DDH}	V_{DDH} = $+V_1$ = +30.0 V, V_C = $V_{DDH}/2$, $–V_1$ = 0.0 V, V_{CC} = 5.0 V All other parameters the same as the I_{CC} item.		V_{DDH}		6	13	µA
Input Terminal Capacity	C_I	Freq. = 1 MHz Chip alone Ta = 25°C		LP,YD,SHL,SEL, LSEL,CSEL,F1,F2, $\overline{DOFF}$,TEST1,FR			10	pF
Input/Output Terminal Capacity	$C_{I/O}$			CIO1,CIO2			18	pF

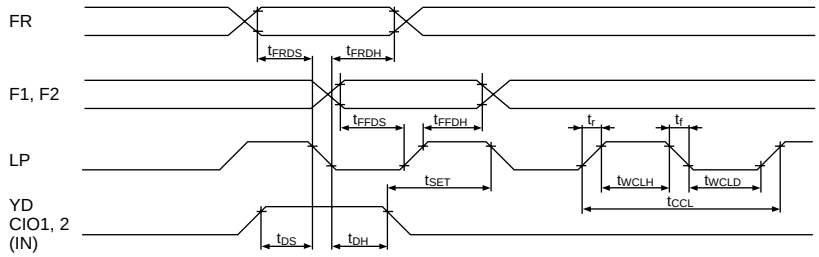
Range of Operating Voltages: $V_{CC} – V_{DDH}$

It is necessary to set the voltage for V_{DDH} within the $V_{CC} – V_{DDH}$ operating voltage range shown in the diagram below.



AC Characteristics

Input Timing Characteristics



The FR latched at the nth LP is reflected in the output at the n+1th LP.

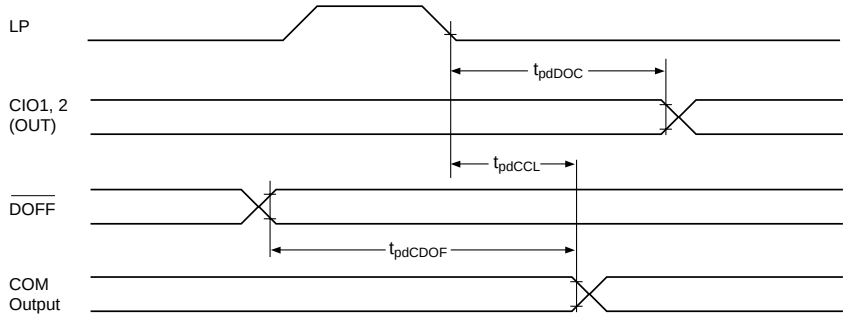
(V_{CC} = +5.0 V ± 10%, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		500		ns
LP "H" Pulse Width	t_{WCLH}		55		ns
LP "L" Pulse Width	t_{WCLL}		330		ns
FR Setup Time	t_{FRDS}		100		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		100		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			50	ns
Input Signal Fall Time	tf			50	ns
CIO Setup Time	t_{DS}		100		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		80		ns

(V_{CC} = +2.7 V to 4.5 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		800		ns
LP "H" Pulse Width	t_{WCLH}		100		ns
LP "L" Pulse Width	t_{WCLL}		660		ns
FR Setup Time	t_{FRDS}		200		ns
FR Hold Time	t_{FRDH}		80		
F1, F2 Setup Time	t_{FFDS}		200		
F1, F2 Hold Time	t_{FFDH}		80		
Input Signal Rise Time	tr			100	ns
Input Signal Fall Time	tf			100	ns
CIO Setup Time	t_{DS}		200		ns
CIO Hold Time	t_{DH}		80		ns
YD → LP Allowable Time	t_{SET}		150		ns

Output Timing Characteristics



(V_{CC} = 5.0 V ± 10%, V_{DDH} = +14.0 to +42.0 V, Ta = –30 to +85°C)

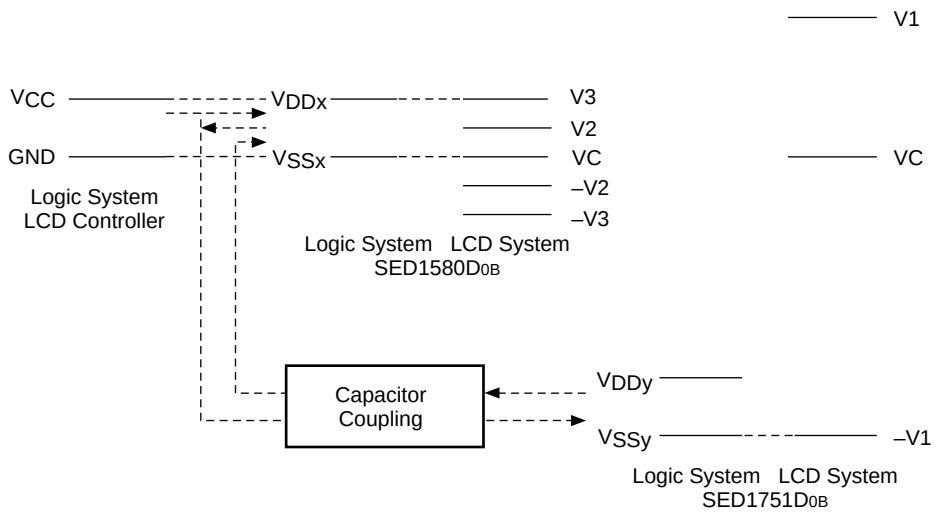
Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		300	ns
Delay time from LP to COM output	t_{pdCCL}			350	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			700	ns

(V_{CC} = +2.7 V to 4.5 V, V_{DDH} = +14.0 to +28.0 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		600	ns
Delay time from LP to COM output	t_{pdCCL}			500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

The Power Supply

Method of Forming Each Voltage Level



When the SED1580 and the SED1751 are used to form an extremely low power module system, the power relationships as shown in the figure above between the SED1580 and SED1751 logic systems, and the LCD system power supply, and the LCD controller power supply are optimal.
In this case, care is required when it comes to signal propagation in the logic system.

LCD Controller	→	SED1580	Direct
LCD Controller	→	SED1751	Capacitor coupling is required
SED1580	→	SED1751	Capacitor coupling is required
SED1751	→	SED1580	Capacitor coupling is required

Cautions at Power Up and Power Down

Because the voltage level in the LCD system is high voltage, if the logic system power supply of this LSI is floating or if V_{CC} is 2.6 V or less when the LCD system high voltage (30 V or above) is applied, or if the LCD drive signal is output before the voltage level that is applied to the LCD system has stabilized, then there is the risk that there will be an over current condition in this LSI, resulting in permanent damage to this LSI.
It is recommended that the display OFF function (DOFF) is used until the LCD system voltage stabilizes to insure that the LCD drive output power level is at the VC level.
Be sure to follow the sequences below when turning the power supplies ON and OFF:

When turning the power supply ON:

Logic system ON → LCD drive system ON, or simultaneously ON.

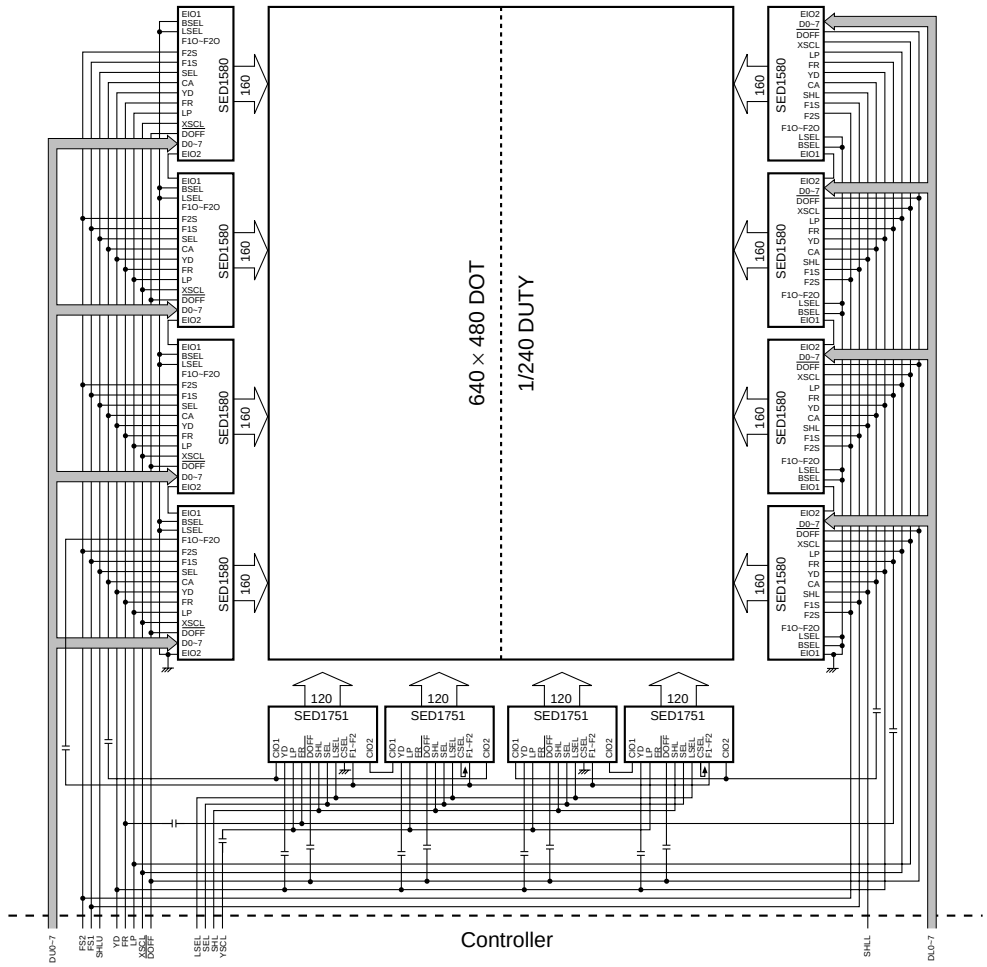
When turning the power supply OFF:

LCD drive system OFF → Logic system OFF, or simultaneously OFF.

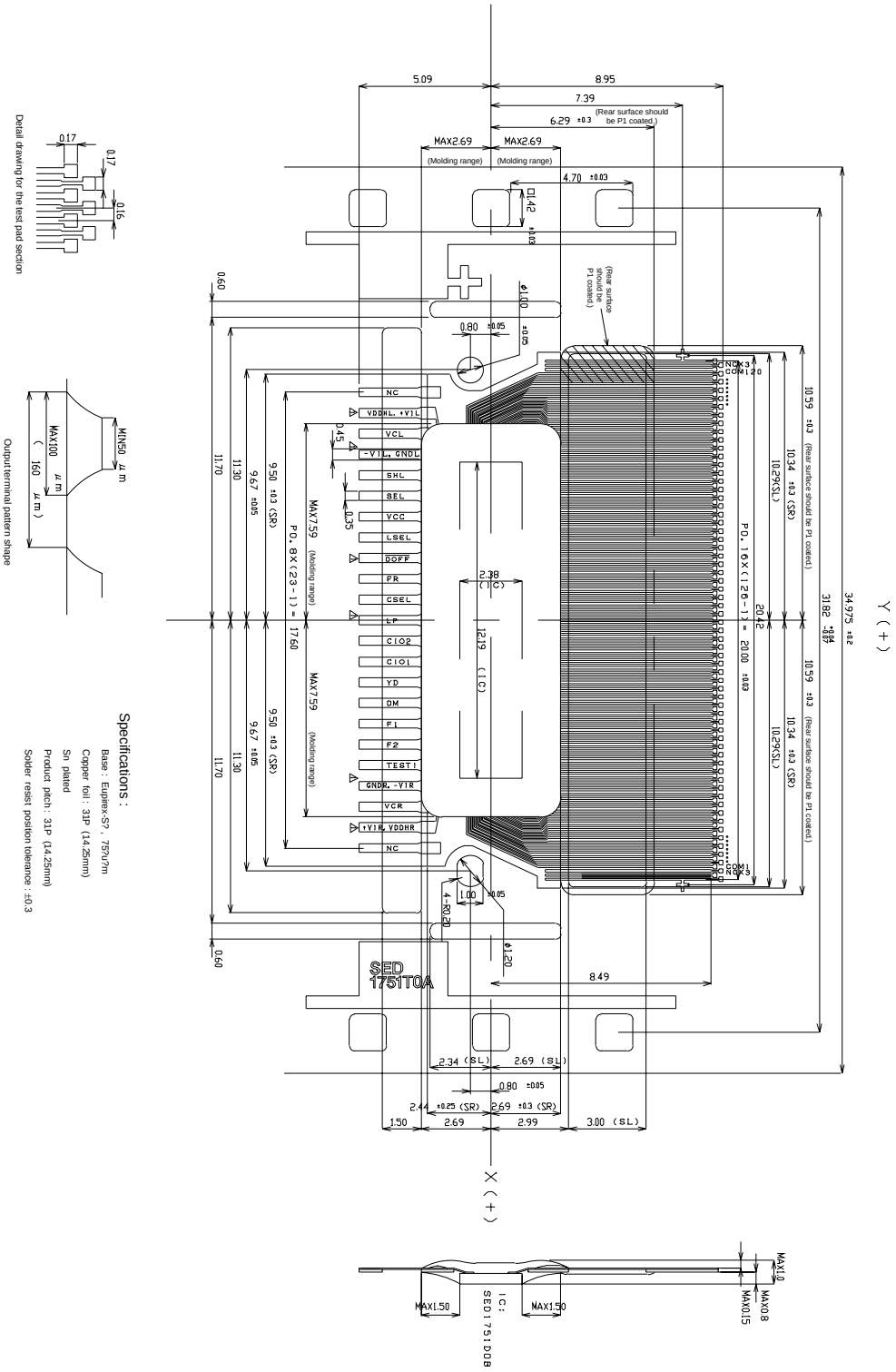
As a countermeasure to guard against over current conditions, it is effective to insert a high-speed fuse or a guard resistance in series with the LC power supply. The guard resistance value must be optimized depending on the capacity of the LC cell.

Example of Connection

Large Screen LCD Structure Diagram



Example of External Connections



SCI7500F0A

Contents

OVERVIEW

Description

The SCI7500F0A is a four-line simultaneous selection method MLS (Multi Line Selection) drive power supply IC for driving liquid crystal displays. Using its CMOS charge pump-type high-efficiency voltage converter circuit, the chip is able to generate all the bias voltages required for the four-line MLS drive based on a single 3.0 V power supply input.
When a system is structured from column (segment) drivers such as the SED1580, row (common) drivers such as the SED1751, and this IC, this structure is able to produce a module with extremely low power consumption when compared to a conventional drive method.
Moreover, even greater power conservation is possible when combined with an LCD controller that can pause data transmission (a controller such as the SED1360).

Features

- Power Supply Voltage: 2.4 V to 3.6 V single-input power supply
- Low Consumption Current: 340 μA (in 6 × step-up mode, TYP)
- Standby Current: 5 μA (MAX)
- High Voltage Conversion Efficiency: 88% (6 × step-up mode, TYP)
- Generates all bias voltages required for 4-line MLS driving.
  An external contrast adjustment function can also be attached.
- Equipped with an internal charge pump-type DC/DC voltage converter circuit.
  Depending on the terminal settings, the chip can be switched between 5 × step-up (compatible with 1/200 duty) and 6 × step-up (compatible with 1/240 duty).
- Built-in electric charge discharging circuit for the liquid crystal drive current (VL).
- Internal “power off” function using an external signal (XSLP).
- Equipped internally with a liquid crystal drive polarity reverse signal generator circuit.
- The terminal settings can be used to set the range of time for the polarity reversal to 2H to 17H.
- Recommended panel size: VGA, 6.3" or less
- Product being shipped in QFP form ..... (QFP12-48 pin) SCI7500F0A
  Product being shipped in chip form SCI7500D0A
- This product not designed for resistance to radiation.

Block Diagram

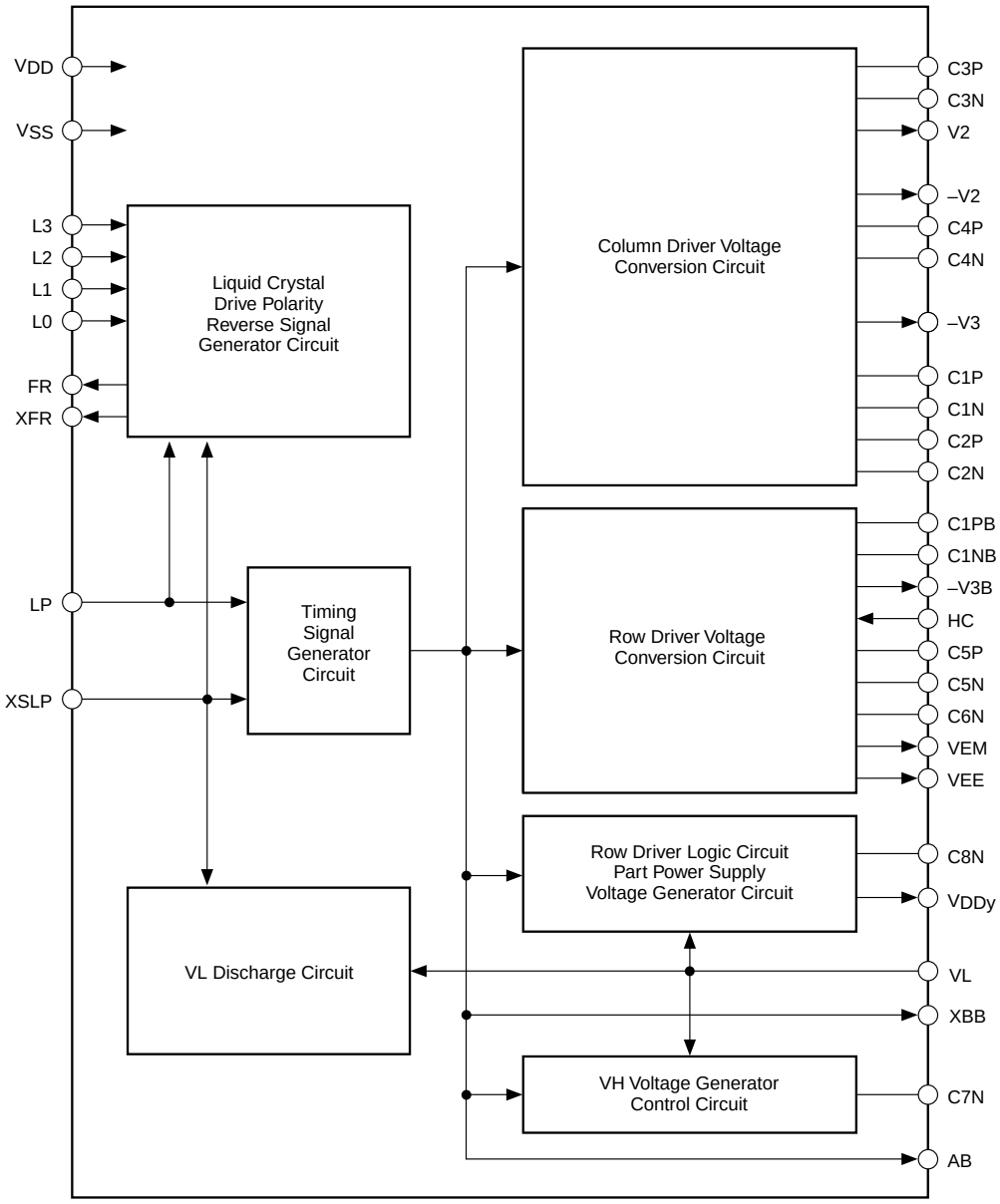


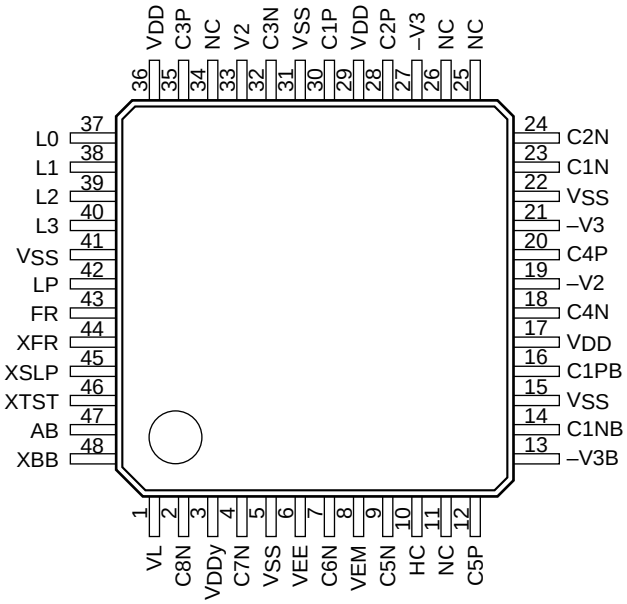
Figure 1: Block Diagram

Explanation of Block Diagram

- Liquid Crystal Drive Polarity Reverse Signal Generator Circuit
  This circuit generates the reverse polarity signal FR from the 1H period pulse signal LP. Pins L0 to L3 can be used to set the polarity reversal interval to 2H to 17H. Moreover, so that it will be possible to drive the top and bottom screens in a 2-screen drive panel in opposite phases, this IC outputs two signals with opposite polarities of each other (FR, XFR).
- Timing Signal Generator Circuit
  This circuit generates the clock for the charge pump from the 1H period pulse signal LP. When the display off control signal XSLP is set to the V_{SS} level, the clock stops and the voltage converter operation stops.
- Column Driver Voltage Conversion Circuit
  This circuit generates the V_2, $-V_2$, and $-V_3$ voltage levels required for column driving.
- Row Driver Voltage Conversion Circuit
  This generates the voltage (V_{EE}) required for generating the power supply voltages (V_H, V_L) required for the row drivers. Using V_{DD} as the reference, this generates either a $5\times$ or $6\times$ voltage level in the negative direction relative to the input power supply voltage. A terminal can be used to switch between the step-up modes. The contrast adjustment function is performed through the use of an external emitter follower circuit to adjust V_{EE} to generate VL.
- Row Driver Logic Circuit Part Power Supply Voltage Generator Circuit
  This generates the power supply voltage (V_{DDy}) required by the row driver logic circuit part. This generates a voltage that is higher than the voltage level V_L by an amount equal to V_{DD}–V_{SS}.
- V_H Voltage Generator Control Circuit
  This is a circuit for generating the power supply voltage (V_H) required for the row driver. The V_H voltage can be generated by an external MOS transistor and this circuit.
- V_L Discharge Circuit
  At power off or display off, this circuit discharges the charge remaining on the row driver negative voltage level-side power supply voltage terminal (V_L).

TERMINAL FUNCTIONS

Terminal Layout Diagram



Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name	Terminal No.	Terminal Name
1	V_L	13	$-V_{3B}$	25	—	37	L0
2	C8N	14	C1NB	26	—	38	L1
3	V_{DDy}	15	V_{SS}	27	$-V_3$	39	L2
4	C7N	16	C1PB	28	C2P	40	L3
5	V_{SS}	17	V_{DD}	29	V_{DD}	41	V_{SS}
6	V_{EE}	18	C4N	30	C1P	42	LP
7	C6N	19	$-V_2$	31	V_{SS}	43	FR
8	VEM	20	C4P	32	C3N	44	XFR
9	C5N	21	$-V_3$	33	V_2	45	XSLP
10	HC	22	V_{SS}	34	—	46	XTST
11	—	23	C1N	35	C3P	47	AB
12	C5P	24	C2N	36	V_{DD}	48	XBB

Explanation of Terminals

Liquid Crystal Drive Polarity Reverse Signal Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
L0 to L3	I	37 to 40	1 to 4	Polarity reverse time setting terminals. These are the input terminals for setting the polarity reverse time. The time can be set in the range of 2H to 17H.
FR	O	43	7	Polarity reverse forward phase signal terminal. This terminal outputs the signal that is generated by the polarity reverse signal generating circuit.
XFR	O	44	8	Polarity reverse signal reverse phase terminal. This outputs the signal that is in the reverse phase from the polarity reverse forward phase signal terminal.

Timing Signal Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
LP	I	42	6	Display data latch pulse input terminal. This is the input terminal for generating the charge pump clock and the polarity reverse signal. It is necessary to input into this terminal a pulse signal with a period of 1H.
XSLP	I	45	9	The display off control signal terminal. Setting this terminal to the VSS level stops the clock and stops the operations of the voltage converter.

Column Driver Voltage Conversion Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C3P	(O)	35	43	The positive-side connection terminal for the flying capacitor CP3 for generating the V_2 output voltage.
C3N	(O)	32	41	The negative-side connection terminal for the flying capacitor CP3 for generating the V_2 output voltage.
V_2	O	33	42	V_2 output voltage terminal.
C4P	(O)	20	31	The positive-side connection terminal for the flying capacitor CP4 for generating the $-V_2$ output voltage.
C4N	(O)	18	29	The negative-side connection terminal for the flying capacitor CP4 for generating the $-V_2$ output voltage.
$-V_2$	O	19	30	$-V_2$ output voltage terminal.
C1P	(O)	30	39	The positive-side connection terminal for the flying capacitor CP1 for generating the $-V_3$ output voltage.
C1N	(O)	23	34	The negative-side connection terminal for the flying capacitor CP1 for generating the $-V_3$ output voltage.
C2P	(O)	28	37	The positive-side connection terminal for the flying capacitor CP2 for generating the $-V_3$ output voltage.
C2N	(O)	24	35	The negative-side connection terminal for the flying capacitor CP2 for generating the $-V_3$ output voltage.
$-V_3$	O	21, 27	32, 36	$-V_3$ output voltage terminal.

Row Driver Voltage Conversion Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C1PB	(O)	16	27	The positive-side connection terminal for the flying capacitor CP1B and CP8 for generating the $-V_{3B}$ output voltage.
C1NB	(O)	14	25	The negative-side connection terminal for the flying capacitor CP1B for generating the $-V_{3B}$ output voltage.
$-V_{3B}$	O	13	24	The negative V_{3B} output voltage terminal. This is an output terminal equipped as the middle voltage level for generating the V_{EE} output voltage.
HC	I	10	22	The step-up mode select terminal. When this terminal is tied V_{SS}, then the chip is put into 5 X step-up mode. However, when it is connected to –3B, the chip is set to 6 X step-up mode.
C5P	(O)	12	23	The positive-side connection terminal for the flying capacitor CP5 and CP6 for generating the V_{EM} output voltage.
C5N	(O)	9	21	The negative-side connection terminal for the flying capacitor CP5 for generating the V_{EM} output voltage.
VEM	O	8	20	The V_{EM} output voltage terminal. This is an output terminal equipped as the middle voltage level for generating the V_{EE} output voltage.
C6N	(O)	7	19	The negative-side connection terminal for the flying capacitor CP6 for generating the V_{EE} output voltage. (The positive-side of CP6 is C5P.)
V_{EE}	O	6	18	The V_{EE} output voltage terminal. By changing the HC terminal interconnection method, it is possible to switch between the 5-level step-up mode and the 6-level step-up mode.

Common Driver Logic Circuit Part Power Supply Voltage Generator Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
C8N	(O)	2	14	The negative-side connection terminal for the flying capacitor CP8 for generating the V_{DDy} output voltage. The positive connection terminal for CP8 is the same as C1PB.
V_{DDy}	O	3	15	The row driver logic circuit part power supply output terminal. This generates the power supply voltage required for the row driver logic circuit part. The output is higher than the V_L level in the positive direction by an amount equal to the difference between V_{DD} and V_{SS}.

VH Voltage Generator Control Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
AB	O	47	11	The V_H output voltage generator clock terminal A. This is the clock output terminal for the external N-channel MOS transistor control.
XBB	O	48	12	The V_H output voltage generator clock terminal B. This is the clock output terminal for the external P-channel MOS transistor control.
C7N	(O)	4	16	The negative-side connection terminal for the flying capacitor CP7 for generating the V_H output voltage. The positive-side connection terminal corresponds to the external transistor.

VL Discharge Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
VL	I	1	13	This is the row driver negative voltage level power supply voltage terminal. The V_L signal that is used to adjust the contrast is input to this terminal. This serves as the power supply for the V_H voltage generator control circuit. XSLP operates the discharge circuit at the VSS level.

The Test Circuit

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
XTST	I	46	10	This is a test terminal. Insure that this terminal is always tied to the V_{DD} level.

Power Supply Terminals <Note 1>

Terminal Name	I/O	SCI7500F0A Terminal Number	SCI7500D0A PAD Number	Function
V_{DD}	I	17, 29, 36 *1	28, 38 44 *1	Input power supply terminals (positive).
V_{SS}	I	5, 15, 22, 31, 41 *1	5, 17, 26 33, 40 *1	Input power supply terminals (negative).

Note: *1 Please connect these power supply terminals externally.

EXPLANATIONS OF FUNCTIONS

Overview of Operation

The SCI7500F0A is a power supply IC for operating the 4-line simultaneous selection method MLS (Multi Line Selection) driver LCDs. Using its CMOS charge pump-type high-efficiency voltage converter circuit, this chip can produce all of the bias voltages necessary for a 4-line MLS driving based on a single 3.0 V power supply.

The voltage levels produced are as follows:

- The liquid crystal drive power supply voltages required for the column drivers ($V_3 = V_{DD}$, V_2, $V_C = V_{SS}$, $-V_2$, $-V_3$).
- The liquid crystal drive power supply voltages required for the row drivers (V_H, $V_C = V_{SS}$, V_L).
- The power supply voltages for the logic circuits of the row driver (V_{DDy}).

However, the row driver low voltage-side power supply voltage (V_L) requires an external bipolar transistor for adjusting the contrast. Moreover, external MOS transistors (2SK***, 2SJ***) are required for generating the row driver high-level power supply voltage (V_H).

Depending on a terminal setting, the chip can switch between 6 X step-up mode and 5 X step-up mode, with 1/240 duty and 1/200 duty, respectively. Consequently, it is possible to obtain the required voltages with maximum efficiency.

An example of a system structure diagram for the power supply interconnections is given below:

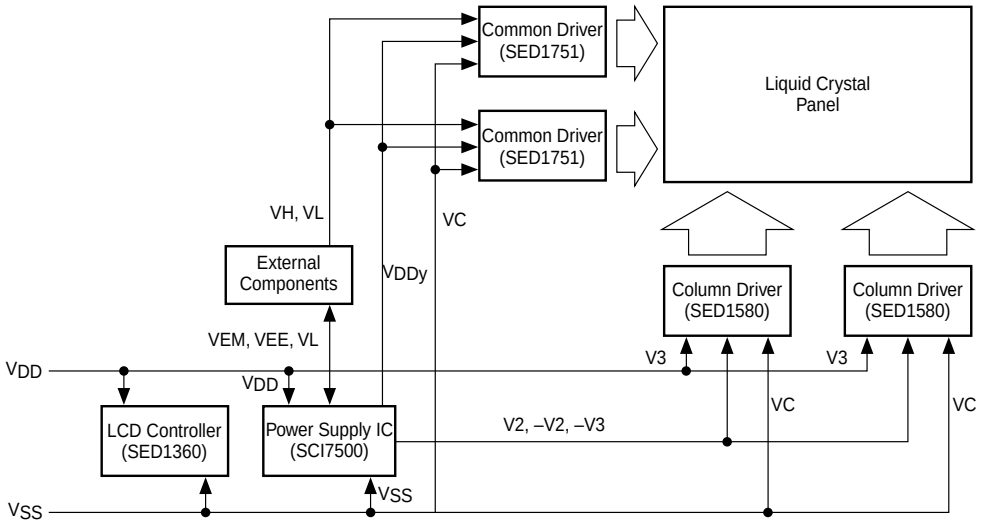


Figure 2: The System Configuration

The relationships between voltage levels in the system shown in Figure 2 are given in the table below.

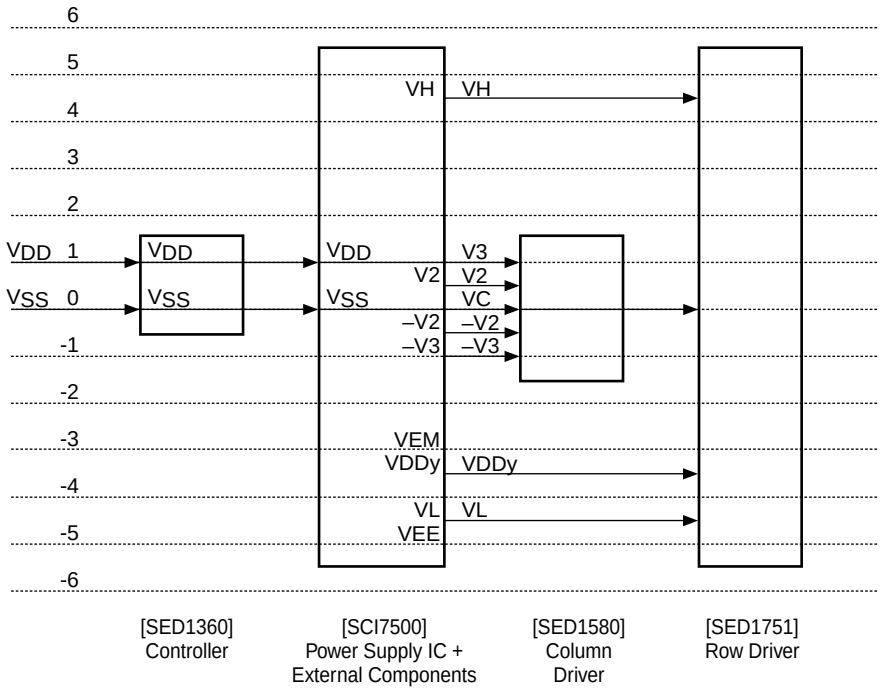


Figure 3: The Relationships Between Voltages Within the System (in 6 × step-up mode)

The logical formulas for each of the voltage levels is as given below:

When in 6 × step-up mode (when HC is connected to –V_{3B}).		**When in 5 × step-up mode (when HC is connected to V_{SS}).**	
Logical Formula	**Voltage level when V_{DD} = 3.0V and V_{SS} = 0V**	**Logical Formula**	**Voltage level when V_{DD} = 3.0V and V_{SS} = 0V**
$V_H = -V_L = 5 (V_{DD}-V_{SS})-\alpha$	15.0–α	$V_H = -V_L = 4 (V_{DD}-V_{SS})-\alpha$	12.0–α
$V_3 = V_{DD}-V_{SS}$	3.0	$V_3 = V_{DD}-V_{SS}$	3.0
$V_2 = 1/2 (V_{DD}-V_{SS})$	1.5	$V_2 = 1/2 (V_{DD}-V_{SS})$	1.5
$V_C = V_{SS}$	0	$V_C = V_{SS}$	0
$-V_2 = -1/2 (V_{DD}-V_{SS})$	–1.5	$-V_2 = -1/2 (V_{DD}-V_{SS})$	–1.5
$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0	$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0
$V_{EM} = -3 (V_{DD}-V_{SS})$	–9.0	$V_{EM} = -2 (V_{DD}-V_{SS})$	–6.0
$V_{DDy} = -4 (V_{DD}-V_{SS}) + \alpha$	–12.0 + α	$V_{DDy} = -3 (V_{DD}-V_{SS}) + \alpha$	–9.0 + α
$V_L = -5 (V_{DD}-V_{SS}) + \alpha$	–15.0 + α	$V_L = -4 (V_{DD}-V_{SS}) + \alpha$	–12.0 + α
$V_{EE} = -5 (V_{DD}-V_{SS})$	–15.0	$V_{EE} = -4 (V_{DD}-V_{SS})$	–12.0

Where α = variable ≥ 0 (contrast adjustment)

The Liquid Crystal Drive Polarity Reverse Signal Generator Circuit

This circuit produces the polarity reverse signal from the 1H period pulse signal LP. Terminals L0 to L3 can be used to set the polarity reversed period in the range of 2H to 17H. So that the upper and lower screens can be driven in mutually opposite phases when a 2-screen drive panel is used, this IC outputs two signals with mutually opposing polarities (i.e. with opposite phases) from the FR and the XFR terminals. The timing of the output transitions is synchronized with the falling edge of the LP signal.

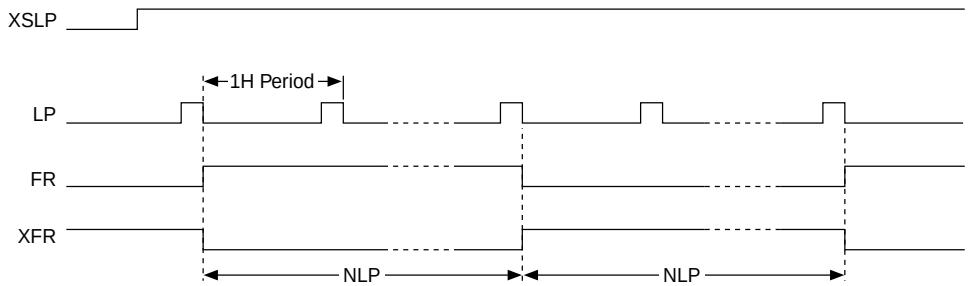


Figure 4: LP and FR Signal Timing Diagram

The relationship between the NLP during the polarity reversed interval and the settings of terminals L0 to L3 is as shown below:

Terminal Settings While Polarity is Reversed				Function		
L3	L2	L1	L0	Time	NLP	
0	0	0	0	17H	LP Signal	17th pulse
			1	2H	LP Signal	2nd pulse
		1	0	3H	LP Signal	3rd pulse
			1	4H	LP Signal	4th pulse
	1	0	0	5H	LP Signal	5th pulse
			1	6H	LP Signal	6th pulse
		1	0	7H	LP Signal	7th pulse
			1	8H	LP Signal	8th pulse
1	0	0	0	9H	LP Signal	9th pulse
			1	10H	LP Signal	10th pulse
		1	0	11H	LP Signal	11th pulse
			1	12H	LP Signal	12th pulse
	1	0	0	13H	LP Signal	13th pulse
			1	14H	LP Signal	14th pulse
		1	0	15H	LP Signal	15th pulse
			1	16H	LP Signal	16th pulse

The Timing Signal Generator Circuit

This generates the clock for the charge pump from the 1H period pulse signal LP. When the display off control signal XSLP is set to Vss, this clock stops and the IC voltage converter operation halts. The VH output voltage generator clocks AB and XBB are also produced by this circuit.

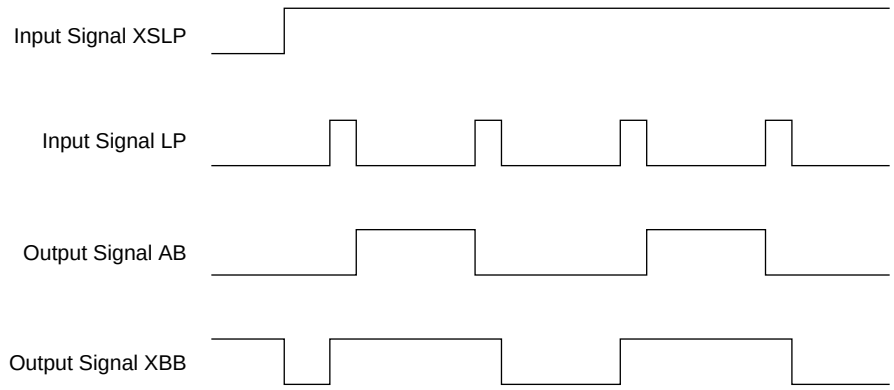


Figure 5: The AB and XBB Signal Output Timing

The Voltage Converter Circuit

The voltage converter circuit comprises a CMOS charge pump-type DC/DC converter. The relational diagram of the voltage converter circuits within this IC is as shown below. The numbers within parentheses in the diagram correspond to the number in "Figure 1: Block Diagram."

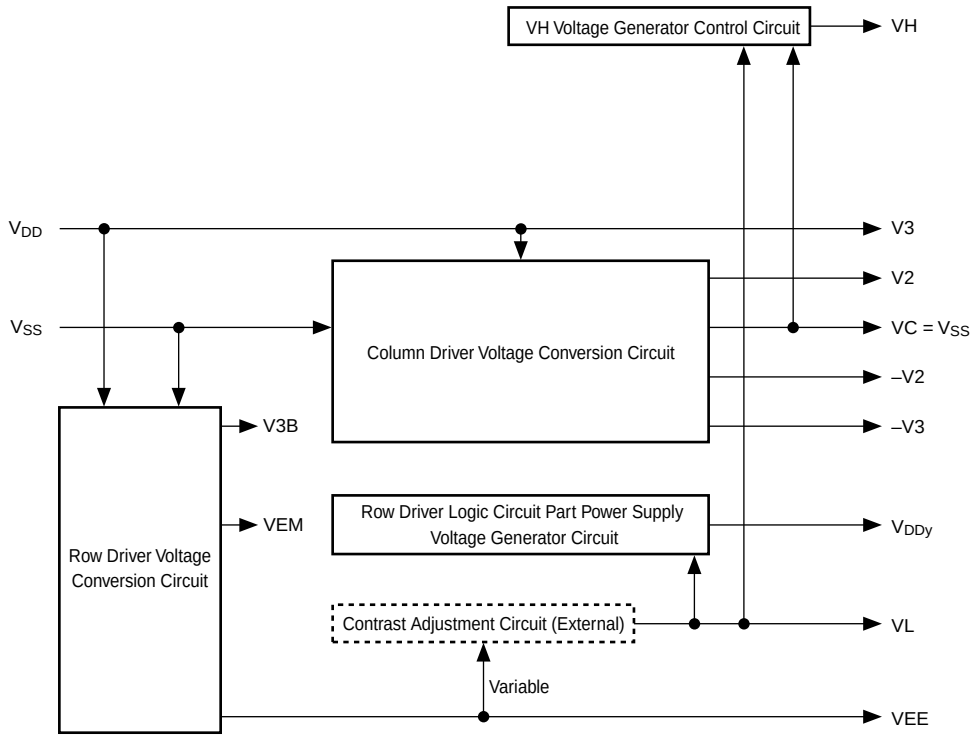


Figure 6: A Relational Diagram of the Voltage Converter Circuits

Logical Formulas for the Various Voltage Levels

When in 6 × step-up mode (when HC is connected to –V3B).		When in 5 × step-up mode (when HC is connected to VSS).	
Logical Formula	**Voltage level when VDD = 3.0V and VSS = 0V**	**Logical Formula**	**Voltage level when VDD = 3.0V and VSS = 0V**
$V_H = -V_L = 5\ (V_{DD}-V_{SS})-a$	15.0–α	$V_H = -V_L = 4\ (V_{DD}-V_{SS})-\alpha$	12.0–α
$V_3 = V_{DD}-V_{SS}$	3.0	$V_3 = V_{DD}-V_{SS}$	3.0
$V_2 = 1/2\ (V_{DD}-V_{SS})$	1.5	$V_2 = 1/2\ (V_{DD}-V_{SS})$	1.5
$V_C = V_{SS}$	0	$V_C = V_{SS}$	0
$-V_2 = -1/2\ (V_{DD}-V_{SS})$	–1.5	$-V_2 = -1/2\ (V_{DD}-V_{SS})$	–1.5
$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0	$-V_3 = -V_{3B} = -(V_{DD}-V_{SS})$	–3.0
$V_{EM} = -3\ (V_{DD}-V_{SS})$	–9.0	$V_{EM} = -2\ (V_{DD}-V_{SS})$	–6.0
$V_{DDy} = -4\ (V_{DD}-V_{SS}) + \alpha$	–12.0+ α	$V_{DDy} = -3\ (V_{DD}-V_{SS}) + \alpha$	–9.0 + α
$V_L = -5\ (V_{DD}-V_{SS}) + \alpha$	–15.0+ α	$V_L = -4\ (V_{DD}-V_{SS}) + \alpha$	–12.0 + α
$V_{EE} = -5\ (V_{DD}-V_{SS})$	–15.0	$V_{EE} = -4\ (V_{DD}-V_{SS})$	–12.0

Where α = variable ≥ 0 (contrast adjustment)

The capacitors for the charge pump can be of two different types: the flying capacitors which transition between a charged state and a discharged state, and the storage capacitor that stores charge. The clock that controls the state changes in the flying capacitors is generated by the timing signal generator circuit from the display data latch pulse input terminal LP. The operating frequency f sw of the flying capacitor is calculated as follows:

$f_{SW} = 1/(2 \times t_{CLP})$
Where t CLP is the LP frequency.

The voltage logic that is biased by both ends of the flying capacitors and storage capacitors is as shown below: (Reference “10. Example of Connections (Reference)” regarding recommended capacitance values and connection methods for the capacitors.)

Flying Capacitors and Storage Capacitors

Capacitor Name		Voltage logic formula biased by both ends of the capacitors		Column side/ Row side
		6 × step-up mode	5 × step-up mode	
Flying Capacitor	CP1	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Column Side
	CP2	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	
	CP3	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CP4	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CP1B	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Row side
	CP5	$2\ (V_{DD}-V_{SS})$	$V_{DD}-V_{SS}$	
	CP6	$2\ (V_{DD}-V_{SS})$	$2\ (V_{DD}-V_{SS})$	
	CP7	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
	CP8	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
Storage Capacitor	CB1	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Column side
	CB3	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CB4	$1/2\ (V_{DD}-V_{SS})$	$1/2\ (V_{DD}-V_{SS})$	
	CB1B	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	Row side
	CB5	$2\ (V_{DD}-V_{SS})$	$V_{DD}-V_{SS}$	
	CB6	$2\ (V_{DD}-V_{SS})$	$2\ (V_{DD}-V_{SS})$	
	CB7	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	
	CB8	$V_{DD}-V_{SS}$	$V_{DD}-V_{SS}$	
	CVL	$5\ (V_{DD}-V_{SS}) -\alpha$	$4\ (V_{DD}-V_{SS}) -\alpha$	

Where α = variable ≥ 0 (contrast adjustment)

In the column driver voltage converter circuit either flying capacitor CP1 or CP2 can be omitted. When the panel is smaller than a 6.3 inch VGA panel, or if one wishes to sacrifice image quality to save cost, one may consider this omission; however, the output impedance will increase and will be outside of what is indicated in "Electrical Characteristics," and thus we recommend that you experimentally confirm the structure for each application.
Switching between the step-up modes in the row driver voltage converter circuits can be done by setting the HC terminal. When the HC terminal is connected to –V3B, then the system will be in 6 × step-up mode, but when the HC terminal is connected to the VSS terminal, then the system will be in 5 × step-up mode. Furthermore, by connecting the –V3 terminal to the –V3B terminal, it is possible to omit the flying capacitor CP1B and storage capacitor CP1B. However, when these capacitors are omitted, the output impedance will increase and will be outside of what is indicated in "Electrical Characteristics," and thus we recommend that you experimentally confirm the structure for each application.

The Contrast Adjustment Circuit

The row driver negative voltage-side power supply voltage VL can be adjusted and generated by an external emitter follower circuit using VEE. The contrast adjustment function is shown in the circuit connection example below:

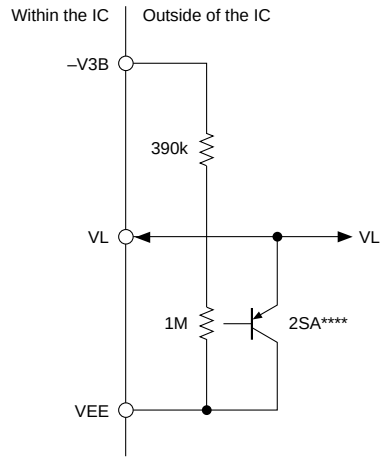


Figure 7: Contrast Adjustment Circuit

The VH Voltage Generator Control Circuit

The row driver positive voltage-side power supply voltage VH can be generated from this circuit and the VH output voltage generator clocks AB, XBB, and external components. This is shown in the circuit connection example below.

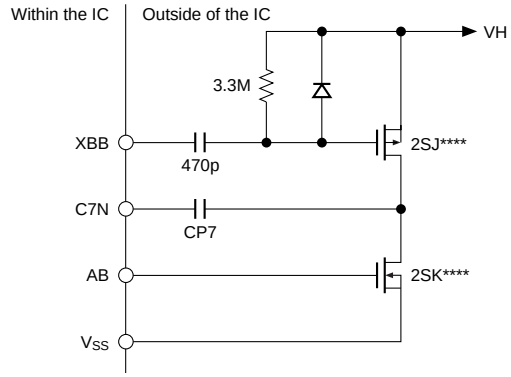


Figure 8: Example of Circuit Connections for Generating the VH Voltage

The VL Discharge Circuit

When XSLP is put to the VSS level, the VL discharge circuit within the IC is triggered, and residual charge at the row driver negative voltage-side power supply voltage terminal VL is discharged to the VSS level. The VL voltage adjusted for the contrast must be input to the VL terminal. (See "The Contrast Adjustment Circuit.")

The VH Discharge Circuit

When XSLP is put to the VSS level, the residual charge at the row driver positive voltage-side power supply terminal VH can be discharged to the VSS level through an external MOS transistor. An example circuit connection is shown below.

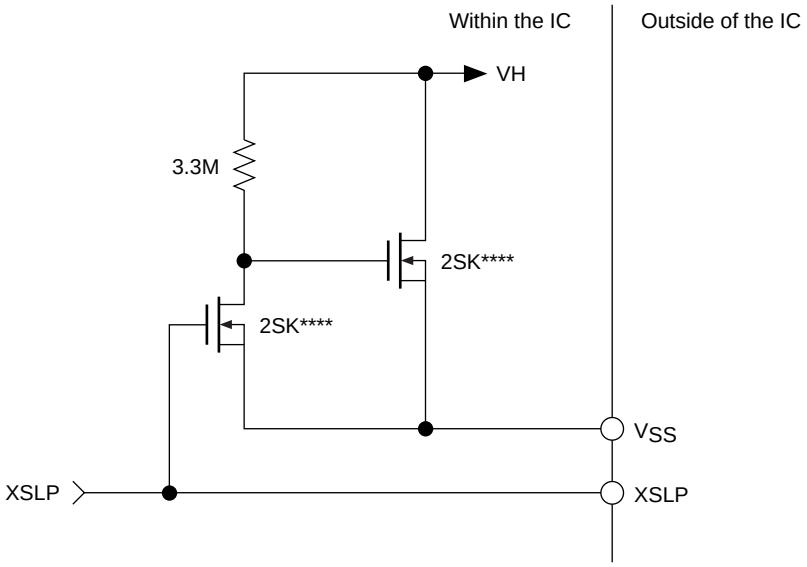


Figure 9: The VH Discharge Circuit

ELECTRICAL CHARACTERISTICS

The Absolute Maximum Ratings

V_{SS} = 0V

Item	Signal	Rated Value		Units	Notes
		Minimum	Maximum		
Input power supply voltage 1	V_{DD}	—	3.7	V	V_{DD} terminal
Input power supply voltage 2	V_L	V_{EE}-0.3	0.3	V	V_L terminal
Input terminal voltage	V_I	–0.3	V_{DD} + 3.0	V	The L3 to L0, LP, XSLP, and XTST terminals
Input current	I_{DD}	—	10	mA	V_{DD}, V_L
Output current 1	I_{V2}	—	6	mA	V_2 terminal
Output current 2	I-V_2	—	6	mA	-V_2 terminal
Output current 3	I-V_3	—	5	mA	-V_3 terminal
Output current 4	I V_{EE}	—	1	mA	V_{EE} terminal
Output current 5	I V_{DDy}	—	0.1	mA	V_{DDy} terminal
Allowable loss	Pd	—	100	mW	Ta ≤ 55 °C
Operating temperature	Topr	–30	85	°C	—
Storage temperature	Tstg	–55	150	°C	—
Soldering temperature and time	Tsol	—	260 × 10	°C × S	At the lead

Notes: *1 Do not apply a voltage from the outside to the output terminals nor to the capacitor connection terminals.

Notes: *2 Operating failures and/or permanent damage may occur if this chip is used under conditions exceeding the absolute maximum ratings listed above. Moreover, the reliability of this chip may be dramatically compromised even if the chip continues to function normally for a time.

DC Characteristics

When not otherwise specified: Ta = –30°C to +85°C, V_{SS} = 0V, 6 × step-up, $V_L = V_{EE} + 0.6V$, Standard connections <Note 1>, LP period = 69µs, LP width = 1µs.

Item	Symbol	Parameters		Standards Min	Standards Typ	Standards Max	Units	Notes
Input power supply voltage	V_{DD}	—		2.4	3.0	3.6	V	—
Input power supply voltage	V_L	—		V_{EE}+0.6	—	$–V_3$	V	—
High level input voltage	V_{IH}	Applicable terminals: LP, XSLP, L0 to L3, XTST V_{DD} = 2.4 to 3.6V		0.8V_{DD}	—	V_{DD}	V	—
Low level input voltage	V_{IL}			0	—	0.2V_{DD}	V	—
Input leakage current	I_{LIN}	$V_{SS} \le V_I \le V_{DD}$, V_{DD} = 2.4 to 3.6V		–0.5	—	0.5	µA	—
V_2 output voltage	V_2	I_O = 2mA (to V_{SS})	V_{DD} = 2.4V	1.148	—	1.2	V	—
			V_{DD} = 2.7V	1.298	—	1.35		
$–V_2$ output voltage	$–V_2$	I_O = 2mA (from V_{SS})	V_{DD} = 2.4V	–1.2	—	–1.120	V	2
			V_{DD} = 2.7V	–1.35	—	–1.272		
$–V_3$ output voltage	$–V_3$	I_O = 1mA (from V_{SS})	V_{DD} = 2.4V	–2.4	—	–2.340	V	2
			V_{DD} = 2.7V	–2.7	—	–2.644		
V_{EE} output voltage	V_{EE}	I_O = 0.4mA (from V_{SS})	V_{DD} = 2.4V	–12.0	—	–11.2	V	—
			V_{DD} = 2.7V	–13.5	—	–12.7		
V_{DDy} output voltage	V_{DDy}	I_O = 0.02mA (to V_L)	V_{DD} = 2.4V	V_L + 2.33	—	V_L + 2.40	V	—
			V_{DD} = 2.7V	V_L + 2.63	—	V_L + 2.70		
Output resistor 1	R_{ON1}	Applicable terminal: C7N I_{OH} = –0.2mA	V_{DD} = 2.4V	—	—	16	Ω	3
			V_{DD} = 2.7V	—	—	15		
Output resistor 1	R_{ON2}	Applicable terminal: C7N I_{OH} = 0.2mA	V_{DD} = 2.4V	—	—	21	Ω	3
			V_{DD} = 2.7V	—	—	20		
High level output voltage	V_{OH}	Applicable terminals: XBB, AB, FR, XFR V_{DD} = 2.4 to 3.6V	I_{OH} = –20µA	V_{DD}–0.1	—	V_{DD}	V	—
Low level output voltage	V_{OL}		I_{OL} = 20µA	0	—	0.1	V	—
Consumption	I_{OPR5}	5 × step-up, no load V_{DD} = 3.0V		—	250	330	µA	—
Current	I_{OPR6}	6 × step-up, no load V_{DD} = 3.0V		—	340	470	µA	—
Static current	I_Q	V_{DD} = 2.4 to 3.6V, XSLP = 0V		—	—	5	µA	—
Step-up power converter efficiency	Peff	6 × step-up, V_{DD} = 3.0V The load conditions were as follows: V_2: I_O = 2mA $–V_2$: I_O = 2mA $–V_3$: I_O = 1mA V_L: I_O = 0.4mA V_{DDy}: I_O = 0.02mA		—	88	—	%	—

Notes
1. For standard connections, see “Example of Connections (Reference).”
2. Measured in a state where negative charges were not applied to -V_2 and -V_3 simultaneously.
3. The measurement circuits and timing of the output resistance 1 R_{ON1}, and output resistance 2 R_{ON2} are as shown below.

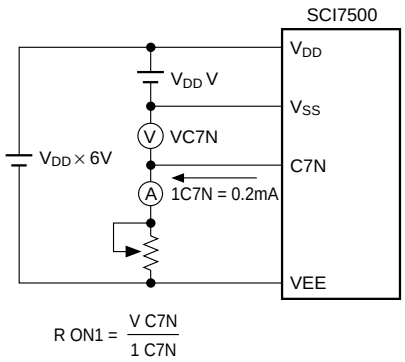


Figure 10: The RON1 Measurement Circuit Figure

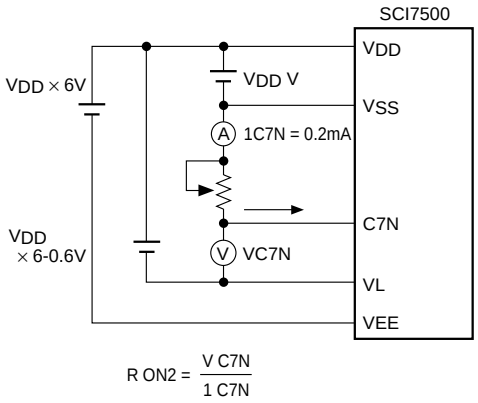


Figure 11: The RON2 Measurement Circuit

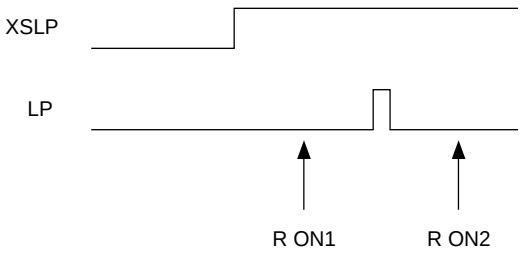


Figure 12: The Measurement Timing using RON1 and RON2

AC Characteristics

The AC test parameters:

- Input voltage level: V_{IH} = 0.8 V_{DD} V
  V_{IL} = 0.2 V_{DD} V
- Input signal rise time: Tr = max 10 ns
- Input signal fall time: Tf = max 10 ns
  V_{DD} = 2.4 to 3.6 V
  V_{SS} = 0 V
  Ta = –30 to 85 °C

Input Timing Characteristics

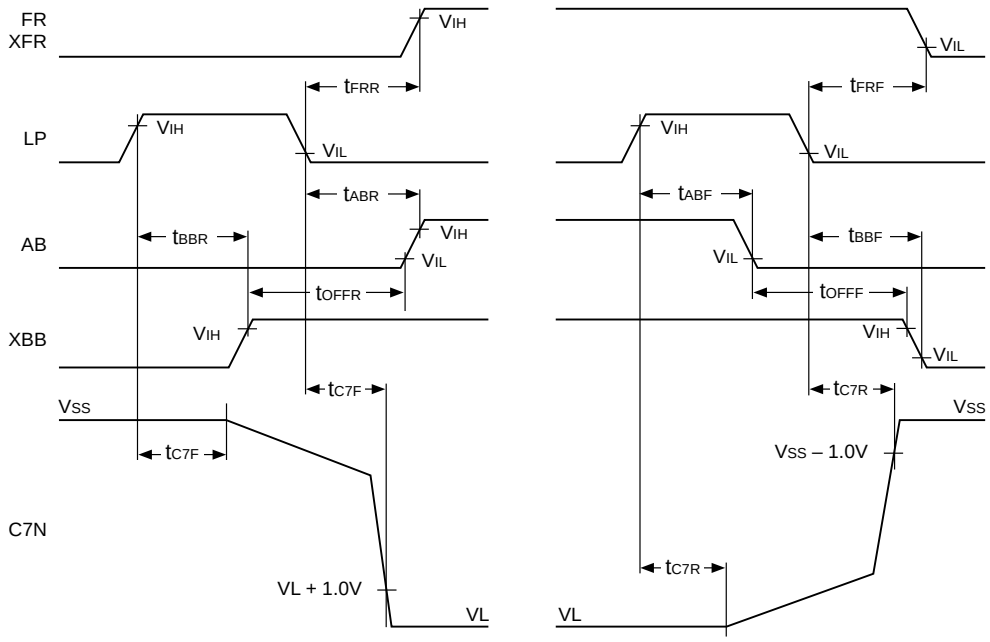
Item	Symbol	Ratings			Units	Notes
		Min	Typ	Max		
LP Period	t_{CLP}	50	65 to 90	125	µs	*1
LP Pulse Width	t_{WLP}	70	—	2000	ns	

Note *1 While the chip continues to function with LP pulse widths in excess of 2000 ns, the wider the LP pulse width, the higher the output impedance of the various output voltages. For this IC, although we are recommending inputting of LP signals through the LP pin as the basic clock, inputting of other signals through the LP pin will also provide the same characteristics as far as the signals being input can satisfy the above specifications.

(Reference) LP Period

Frame Frequency	Duty	LP Period
40	1/200	125 µs
60	1/200	83 µs
60	1/240	69 µs
80	1/240	52 µs

Output Timing Characteristics



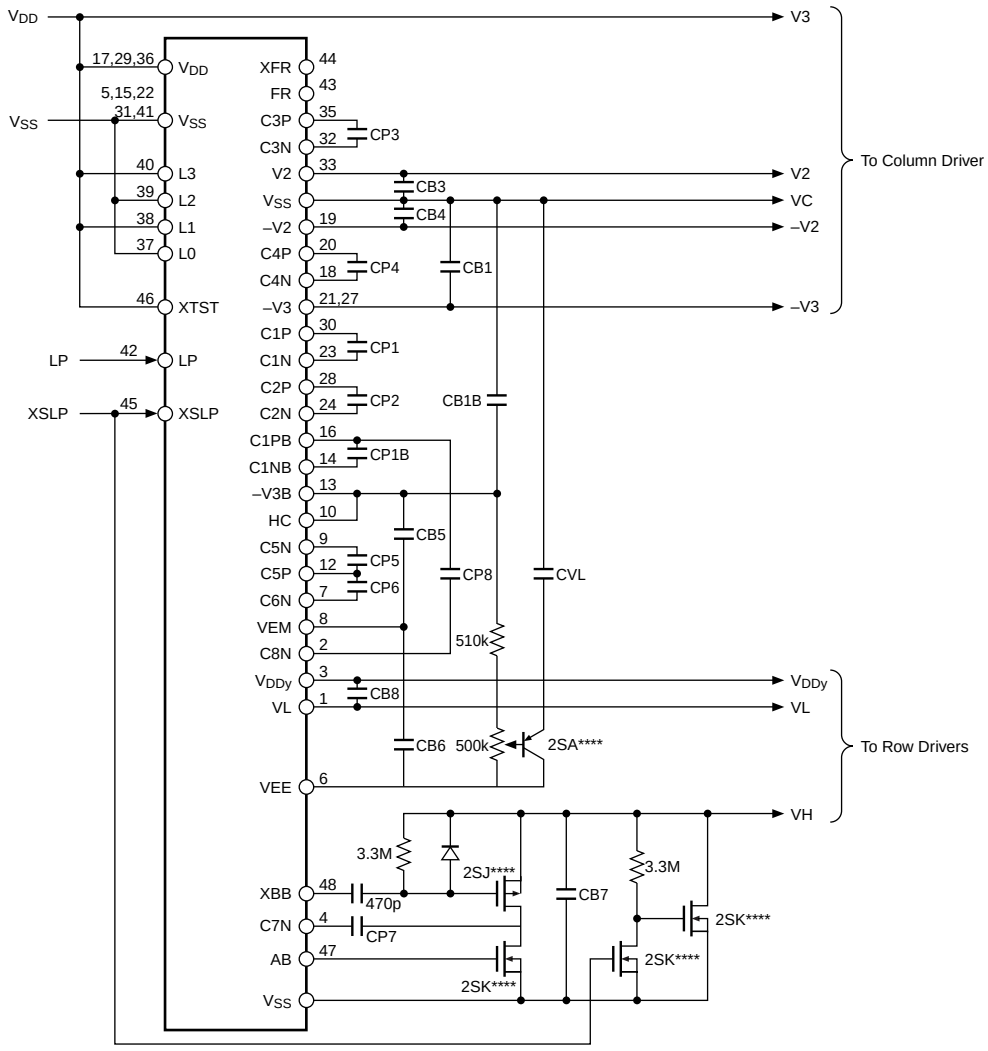
LP pulse width = 1µs, 6 X step-up voltage, VL = VEE + 0.6V, Standard Connections

Item	Signal	Applicable Terminals	Load Conditions	Rated Values		Units
				Min	Max	
FR signal rise delay time	t_{FRR}	FR, XFR	C_L = 50pF	330	3300	ns
FR signal fall delay time	t_{FRF}	FR, XFR		330	3300	ns
AB signal rise delay time	t_{ABR}	AB	*2	230	2000	ns
AB signal fall delay time	t_{ABF}	AB		180	1900	ns
XBB signal rise delay time	t_{BBR}	XBB		130	1100	ns
XBB signal fall delay time	t_{BBF}	XBB		280	3200	ns
Rising edge output phase differential time	t_{OFFR}	AB, XBB		1000	2400	ns
Falling edge output phase differential time	t_{OFFF}	AB, XBB		1000	2200	ns
C7N signal falling edge delay time	t_{C7F}	C7N	*3	270	2400	ns
C7N signal rising edge delay time	t_{C7R}	C7N		490	3800	ns

Note *2 When 2SJ185, 2SK1399 (manufactured by NEC) are used.
Note *3 With a load with standard connections.

EXAMPLE OF CONNECTIONS (REFERENCE)

Standard Connections for the 6 × step-up mode.

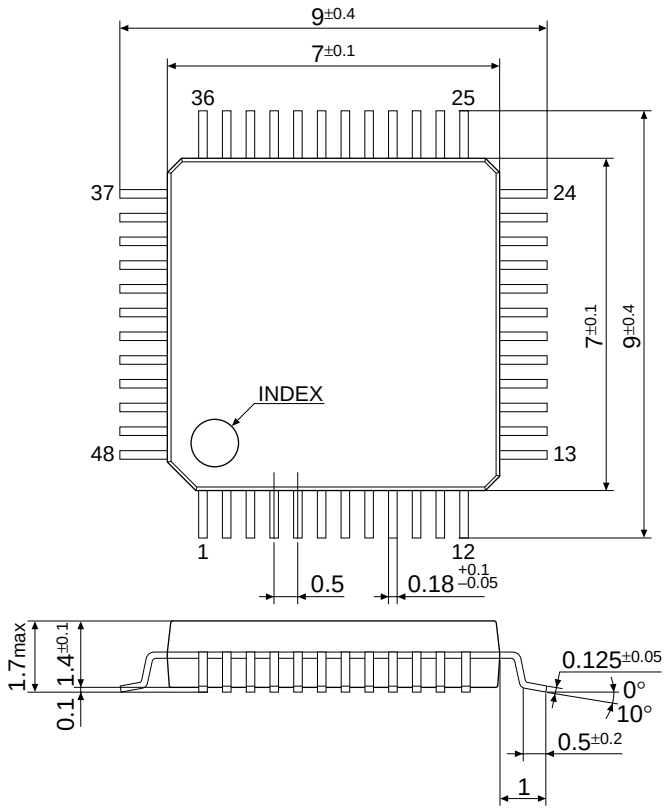


Capacitor Name	Capacitance Value (μF)	Capacitor Name	Capacitance Value (μF)
CP1	4.7	CB1	4.7
CP2	4.7	CB3	4.7
CP3	4.7	CB4	4.7
CP4	4.7	CB5	1.0
CP5	1.0	CB6	1.0
CP6	1.0	CB7	1.0
CP7	1.0	CB8	0.1
CP8	0.1	CB1B	4.7
CP1B	4.7	CVL	1.0

The capacitance values for the capacitors are the recommended value for a 6.3 inch VGA liquid crystal panel. The characteristics shown in “Electrical Characteristics” are the characteristics obtained when capacitors with the values shown above are used. Consequently, while one may consider reducing the capacitance values of these capacitors when a liquid crystal panel smaller than a 6.3-inch VGA screen is used, in such a case the output impedance would increase, and thus we recommend experimental verification for each product type, and that the capacitance values be set such that the liquid crystal drive voltages are stable.

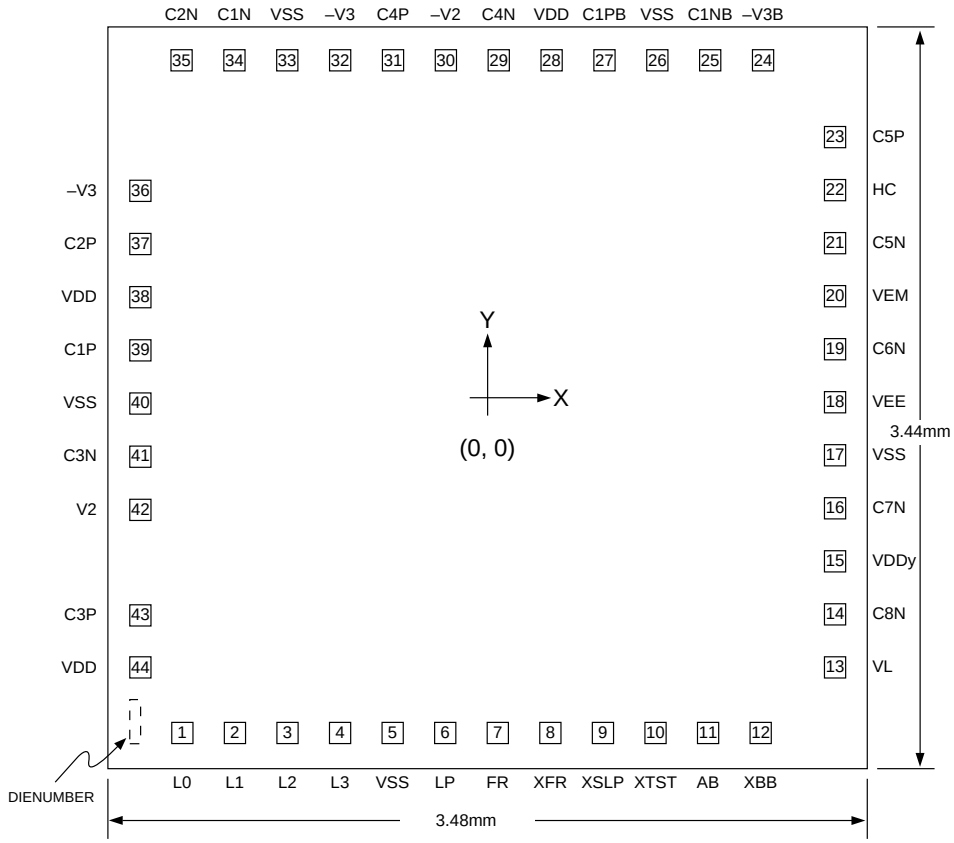
EXTERNAL DIMENSIONS (REFERENCE)

Note: These dimensions are subject to change without notice.



Plastic QFP12-48 pin

EXTERNAL SHAPE OF THE CHIP (SCI7500D0A)



PAD layout

Chip size:	3.48mm × 3.44mm
Chip thickness:	400μm ± 30μm
PAD hole size:	100μm × 100μm
Substrate potential:	V_{DD}
DIE number:	F7500D0A

COORDINATES OF RESPECTIVE PAD CENTERS

Unit: µm

PAD No.	PAD name	X	Y
1	L0	–1431.2	–1554.4
2	L1	–1191.2	
3	L2	–951.2	
4	L3	–711.2	
5	VSS	–471.2	
6	LP	–280.8	
7	FR	–40.8	
8	XFR	199.2	
9	XSLP	439.2	
10	XTST	679.2	
11	AB	919.2	
12	XBB	1159.2	
13	VL	1574.4	–1264.8
14	C8N		–1024.8
15	VDDy		–784.8
16	C7N		–544.8
17	VSS		–304.8
18	VEE		–64.8
19	C6N		175.2
20	VEM		415.2
21	C5N		655.2
22	HC		895.2

PAD No.	PAD name	X	Y
23	C5P	1574.4	1135.2
24	–V3B	1235.2	1554.4
25	C1NB	995.2	
26	VSS	755.2	
27	C1PB	475.2	
28	VDD	235.2	
29	C4N	–4.8	
30	–V2	–244.8	
31	C4P	–484.8	
32	–V3	–724.8	
33	VSS	–964.8	
34	C1N	–1204.8	
35	C2N	–1444.8	
36	–V3	–1574.4	935.2
37	C2P		655.2
38	VDD		415.2
39	C1P		175.2
40	VSS		–64.8
41	C3N		–304.8
42	V2		–544.8
43	C3P		–1024.8
44	VDD		–1264.8

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