SED1360 Series

Contents

INTRODUCTION

Scope

This is the Functional Specification for SED1360 3.3 V Ultra Low Power LCD Controller Chip.

Objectives

(1) To specify functions and interface requirements of the chip.
(2) To allow review of the functions of the chip, as a preliminary specification.

FEATURES

Technology

- ultra low power CMOS process
- 3.3 volt operation
- chip supply with aluminum pad
- 64 pin QFP6 surface mount package

System

- Direct connection to the 68 family CPUs.
- minimum CPU Interface pin count.
- no buffers are required in a 3.3 V-System.
- internal oscillator with external Capacitance and Resistance, or external oscillator for a low frequency input source.
- interfaces to 64 kb and, or 256 kb SRAMs.
- controls Seiko Epson's RAM integrated Segment Drivers.
- self-controlled Doze Mode.
- optimized Hardware for low to medium resolution LCDs.
- ultra low power consumption.

OVERVIEW DESCRIPTION

SED1360 is an ultra low power 3.3 V LCD controller which is optimized to drive low to medium resolution LCD panels. SED1360 can interface to the 68 family CPUs in the Port Peripheral Timing.

Typical System Block Diagram

The following figure shows typical system implementation with SED1360.

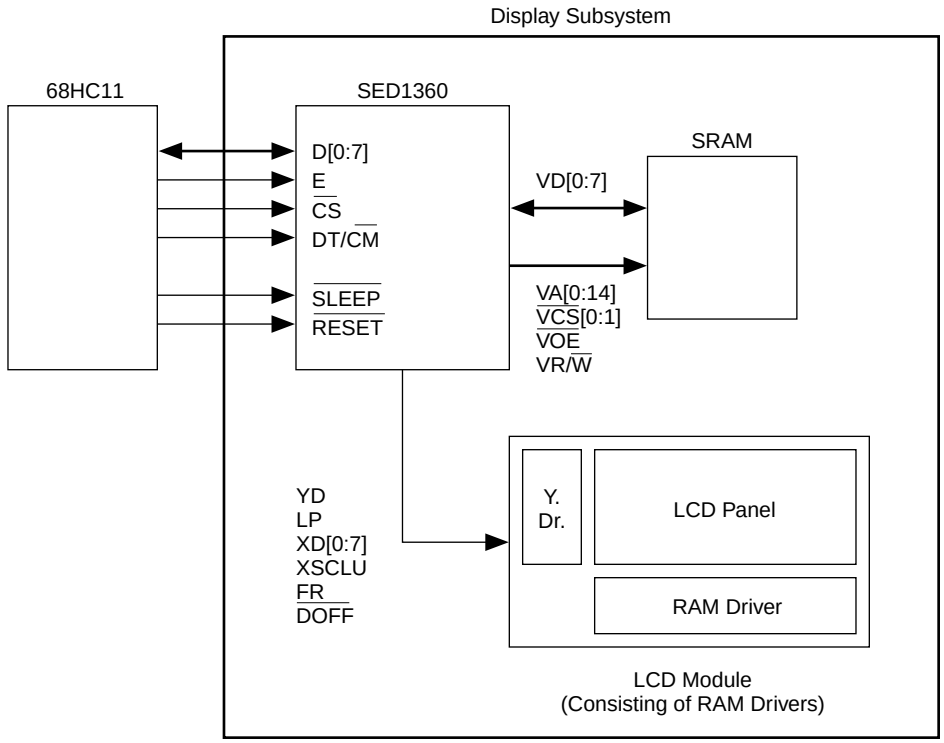

Figure 1. Typical System Block Diagram

SED1360

(1) 3.3 V operational low power LCD Controller Chip.
(2) receives Data from CPU.
(3) stores the Display Data into SRAM.
(4) reads the Data written in the SRAM to update LCD Display.
(5) transfers the read Data to LCD Module automatically.
(6) controls entering to Doze Mode and returning to Active Mode automatically.
(7) supports local oscillation or low frequency input to realize the Ultra Low Power LCD Display Subsystem.
(8) supports Hardware Suspend Mode.

LCD Module

(1) 3.3 V operational low power LCD Module.
(2) consists of Seiko Epson's RAM integrated Segment Drivers, Common Drivers and an LCD panel.
(3) The LCD Module enters into Power Save Mode automatically, if "XSCLU" is not provided.

SRAM

(1) SED1360 uses the SRAM to store the Display Data written by CPU in order to arbitrate between CPU access and LCD Display refresh.
(2) has to be 3.3 V operational.

SED1360 Internal Block Diagram

The following figure shows an overview of the LCD Controller chip SED1360.

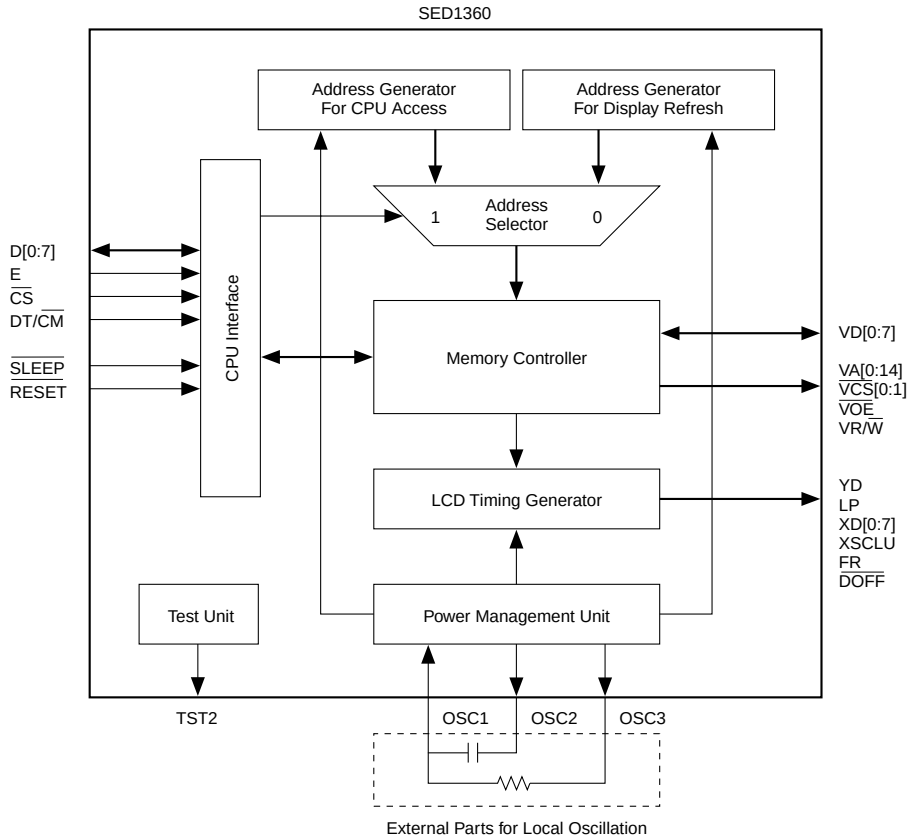

Figure 2. SED1360 Internal Block Diagram

CPU Interface

(1) 3.3 V 68XX dedicated CPU Interface.
(2) 8 bit Data are used to transfer Data or Commands.
(3) The rising edge of "$\overline{CS}$" signal is used to execute the Data Transfer.
(4) "DT/$\overline{CM}$" is used for CPU to indicate either Data or Command is on the bus.
(5) "$\overline{SLEEP}$" signal is used to set the chip in Sleep Mode.
(6) No other signals are required for the normal operation.
(7) "$\overline{RESET}$" is used to initialize the chip.

Address Generator for CPU Access

(1) The internal CPU Write Start Address can be set by the command.
(2) After every single CPU Display Data Write Access, the internal CPU Write Address Counter is increased by one.

Address Generator for Display Refresh

(1) "E" is used to generate the Display Refresh Address.
(2) Address Generator begins when the immediate Frame comes after the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) Address Generation stops if no CPU Display Data Write Access occurs for two LCD Frame period.

Address Selector

When CPU Display Data Write Access occurs, the internal CPU Write Address is selected to generate the address for SRAM.

Memory Controller

(1) When CPU Display Data Write Access occurs, Memory Controller stores the data into SRAM.
(2) The Memory Controller begins reading the data stored in the SRAM to transfer to the LCD Module when the immediate Frame comes after the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) The Memory Controller stops reading the data from the SRAM if no CPU Display Data Write Access occurs for two LCD Frame period.

LCD Timing Generator

(1) Local oscillation is directly used to generate "LP" (Horizontal Sync. Pulse), "YD" (Vertical Sync. Pulse) and "FR" (LCD voltage alternation signal).
(2) The updated data stored in the SRAM is transferred through the Memory Controller and the LCD Timing Generator to the LCD Module, if the CPU Display Data Write Access occurs or when CPU sets the "Display Data Transfer" command.
(3) The LCD Timing Generator uses "E" to generate "XSCLU".
(4) "XSCLU" is automatically controlled by the CPU Display Data Write Access or setting the "Display Data Transfer" command.

Power Management Unit

(1) Power Management Unit monitors the occurrence of CPU Display Data Write Access, the execution of the "Display Data Transfer" command, the internal state of LCD Frame period and the "$\overline{SLEEP}$" signal in order to determine entering to Doze Mode and returning to Active Mode. And this unit also controls local oscillation.

Test Unit

Test Unit controls test functions of the chip if the chip is in Test Mode.

PINOUT DIAGRAM

SED1360D0A

The following figure shows a pinout placement.

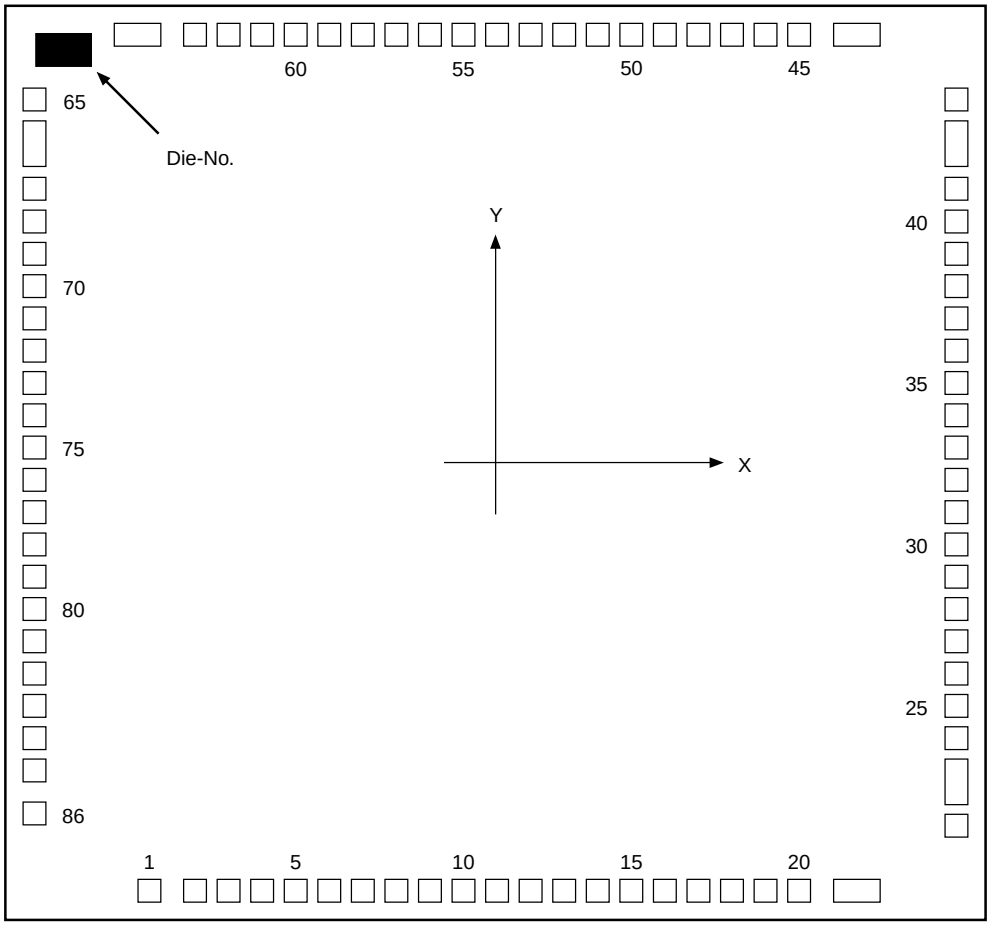

Figure 3. SED1360D0A Pinout Diagram

chip size	4.21 mm × 4.11 mm
chip thickness	400 µm
pad pich (min.)	136 µm
pad size (min.)	100 µm × 100 µm

Table 1. SED1360D0A Pin Coordinates

Pin No.	X (μm)	Y (μm)
1	–1425	–1913
2	–1221	
3	–1085	
4	–949	
5	–813	
6	–677	
7	–541	
8	–405	
9	–269	
10	–133	
11	3	
12	139	
13	275	
14	411	
15	547	
16	683	
17	819	
18	955	
19	1091	
20	1227	
21	1506	
22	1964	–1560
23		–1359
24		–1159
25		–1023
26		–887
27		–751
28		–615
29		–479
30		–343
31		–207
32		–71
33		65
34		201
35		337
36		473
37		609
38		745
39		881
40		1017
41		1153
42		1359
43		1564

Pin No.	X (μm)	Y (μm)
44	1506	1913
45	1227	
46	1091	
47	955	
48	819	
49	683	
50	547	
51	411	
52	275	
53	139	
54	3	
55	–133	
56	–269	
57	–405	
58	–541	
59	–677	
60	–813	
61	–949	
62	–1085	
63	–1221	
64	–1476	
65	–1964	1547
66		1350
67		1153
68		1017
69		881
70		745
71		609
72		473
73		337
74		201
75		65
76		–71
77		–207
78		–343
79		–479
80		–615
81		–751
82		–887
83		–1023
84		–1159
85		–1295
86		–1499

SED1360F0A

The following figure shows a pinout placement.

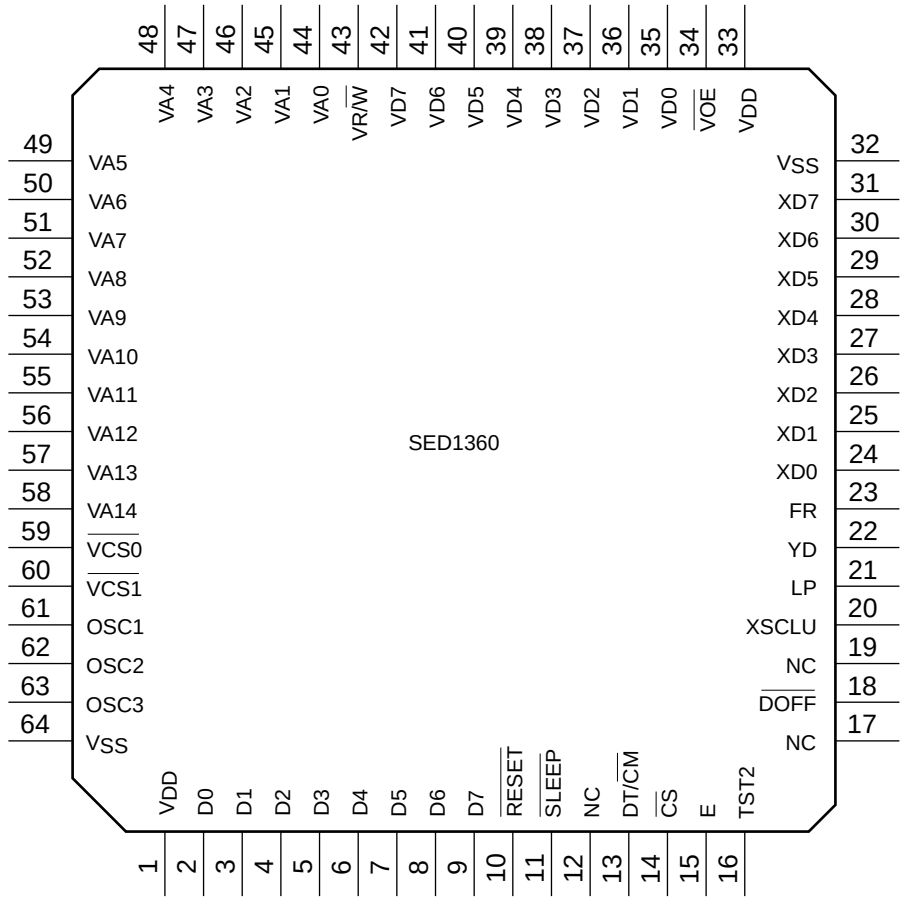

Figure 4. SED1360F0A Pinout Diagram

Note: Pinout placement subject to change.
Package type: 64 pin surface mount QFP6 NC pins are left unconnected.

PIN DESCRIPTION

Key
C = CMOS level input
CS = CMOS level input with hysteresis
COSC = CMOS level input for an internal oscillation inverter
T = TTL level input
OX = CMOS output, x denotes output driver type.
OOSC = CMOS output for an internal oscillation inverter
PU = integrated pull-up resistor
PD = integrated pull-down resistor

CPU Interface

The CPU interface signals are placed on one side of the chip for easy connection to CPU. And the input levels of all CPU Interface pins are unified with CMOS level to allow easy connection to 3.3 V 68 family CPUs.

Table 2. CPU Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
D [0:7]	I	2…9	C	Data inputs. The data is captured into an SED1360's input data register by the rising edge of "$\overline{CS}$".
E	I	15	C	In Active Mode, "E" is used to write or read the CPU data to from SRAM and transfer the data written in the SRAM to the LCD Module.
$\overline{CS}$	I	14	C	The rising edge of this signal is used to capture the state of "D [0:7] and "DT/$\overline{CM}$" into SED1360. When "$\overline{CS}$" is high, no data captures occur.
DT/$\overline{CM}$	I	13	C	If this signal is high, Data is on the bus. If this signal is low, Command is on the bus.
$\overline{SLEEP}$	I	11	C	If this signal is pulled low, the chip enters Sleep Mode. In the Sleep Mode, internal oscillation is disabled, all of the input signals are masked and all of the output signals are controlled to inactive state.
$\overline{RESET}$	I	10	CS	The active low "$\overline{RESET}$" signal from the system clears all internal registers.

SRAM Interface

The SRAM Interface signals are basically placed on two sides of the chip. The input level of "VD [0:7]" is met with TTL level to connect with generic 3.3 V SRAMs. And also "VD [0:7]" have integrated pull-up resistors to eliminate current consumption at the input buffers in Doze Mode.

Table 3. SRAM Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
VD [0:7]	I/O	35…42	T O2 PU	The "VD [0:7]" signals are connected to SRAM's 8 bit data. The captured display data in SED1360 are stored in the SRAM through "VD [0:7]" by the "VR/$\overline{W}$" signal.
VA [0:14]	O	44…58	O2	The "VA [0:14]" signals are connected to SRAM's address lines. "VA [0:14]" generate either CPU Display Data Write Address or Display Refresh Address depending upon operation modes.
$\overline{VCS}$ [0:1]	O	59, 60	O2	SED1360 manages up to 64 kb of SRAM as a frame buffer memory. SED1360 is configured to primarily use two 256 kb SRAMs. "$\overline{VCS0}$" is active when 1st 32 kb is selected. "$\overline{VCS1}$" is active when the rest 32 kb is selected. "$\overline{VCS}$ [0:1]" are connected to SRAM's chip select inputs (active low). Those signals are inactie (high), if the chip is in Sleep Mode.
$\overline{VOE}$	O	34	O2	The "$\overline{VOE}$" signal is connected to SRAM's data output enable input.
VR/$\overline{W}$	O	43	O2	The "VR/$\overline{W}$" signal is connected to SRAM's write strobe input.

LCD Interface

The LCD interface signals are placed on the rest one side of the chip. The output type of all signals is optimized to drive the Ultra Low Power LCD Module properly.

Table 4. LCD Interface Pin Description

Pin Name	Type	Pin No.	Drv	Description
XD [0:7]	O	24…31	O1	The "XD [0:7]" signals are connected to the display data inputs of the LCD Module. During Doze Mode, the signals are driven low. "XD [0:7] are transferred to the LCD Module by the falling edge of "XSCLU".
XSCLU	O	20	O1	The "XSCLU" signal is connected to the display data shift clock of the LCD Module. During Doze Mode, the signal is driven low to force the RAM integrated Segment Drivers to be in Power Save Mode.
LP	O	21	O1	The "LP" signal is connected to te input, which drives the data latching pulse of the segment drivers and the scanning clock of the common drivers, of the LCD Module. The "LP" period is directly generated by the signal which is input through "OSC1".
YD	O	22	O1	The "YD" is connected to the frame start pulse signal of the LCD Module.
FR	O	23	O1	The "FR" signal is connected to the signal which alternates the LCD voltage in the LCD Module.
$\overline{DOFF}$	O	18	O1	This signal outputs low if the chip is in Sleep Mode.

Oscillation

The oscillation pins are used to generate the low frequency which directly generates the “LP” signal.

Table 5. Oscillation Pin Description

Pin Name	Type	Pin No.	Drv	Description
OSC1	I	61	COSC	The pin is connected to the one node of the capacitance and the one node of the resistance. If an external oscillator is used as a clock source, then this pin is the clock input.
OSC2	O	62	OOSC	This pin is connected to the other node of the capacitance. If an external oscillator is used as a clock source, then this pin should be left unconnected.
OSC3	O	63	OOSC	This pin is connected to the other node of the resistance. If an external oscillator is used as a clock source, then this pin should be left unconnected.

Test

The test signals are prepared for testing the chip itself.

Table 6. Test Pin Description

Pin Name	Type	Pin No.	Drv	Description
NC	—	12, 17, 19	—	NC pins are not connected to the chip. These pins should be left unconnected.
TST2	O	16	O1	This pin should be left unconnected.

Power Supply

Table 7. Power Supply Pin Description

Pin Name	Type	Pin No.	Drv	Description
VDD	P	1, 33		VDD supply for the chip. Normally 3.3 volt.
VSS	P	32, 64		VSS supply for the chip. Normally 0 volt.

D.C. CHARACTERISTICS

Conditions: V_{DD} = 3.0 V ~ 3.6 V, Ta = –10°C to 70°C unless otherwise specified

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	V_{SS} – 0.3 to 5.0	Volts
Input Voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	Volts
Output Voltage	V_{OUT}	V_{SS} to V_{DD}	Volts
Operating Temperature	T_{OPR}	–10 to +70	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Soldering Temperature/Time	T_{SOL}	260 for 10 sec max. at lead	°C

Recommended Operating Conditions

Table 9. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	V_{DD}	V_{SS} = 0 V	3.0	3.3	3.6	V
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V

Input Specification

Table 10. Input Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low Level Input Voltage for type C input pins	V_{IL1} (C)	V_{DD} = MIN			0.6	V
High Level Input Voltage for type C input pins	V_{IH1} (C)	V_{DD} = MAX	2.5			V
High Level Input Voltage for type CS input pins	V_{IL2} (CS)	V_{DD} = 3.3 V			0.5	V
High Level Input Voltage for type CS input pins	V_{IH2} (CS)	V_{DD} = 3.3 V	2.9			V
Hysteresis Voltage for type CS input pins	V_{HYS} (CS)	V_{DD} = 3.3 V		0.1		V
High Level Input Voltage for type T input pins	V_{IL3} (T)	V_{DD} = MIN			0.5	V
High Level Input Voltage for type T input pins	V_{IH3} (T)	V_{DD} = MAX	1.7			V
Low Level Input Voltage for type COSC input pins	V_{IL4} (COSC)	V_{DD} = MIN			0.6	V
Low Level Input Voltage for type COSC input pins	V_{IH4} (COSC)	V_{DD} = MAX	2.5			V
Input Leakage Current	I_{IZ}	V_{DD} = MAX $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$	–1.0		1.0	µA
Input Pin Capacitance	C_{IN}			10		pF
Pull Down Resistance	R_{PD} (PU)	V_{DD} = 3.3 V	90		1100	kΩ
Pull Up Resistance	R_{PU} (PU)	V_{DD} = 3.3 V	90		1100	kΩ

Output Specifications

Table 11. Output Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low Level Output Voltage for type O1 output pins	V_{OL1} (O1)	V_{DD} = MIN I_{OL} = 1.0 mA	V_{SS} +0.3			V
Low Level Output Voltage for type O1 output pins	V_{OH1} (O1)	V_{DD} = MIN I_{OH} = –0.5 mA			V_{DD} –0.3	V
Low Level Output Voltage for type O2 output pins	V_{OL2} (O2)	V_{DD} = MIN I_{OL} = 3.0 mA	V_{SS} +0.3			V
Low Level Output Voltage for type O2 output pins	V_{OH2} (O2)	V_{DD} = MIN I_{OH} = –1.5 mA			V_{DD} –0.3	V
Low Level Output Voltage for type OOSC output pins	V_{OL3} (OOSC)	V_{DD} = MIN I_{OL} = 100 µA	V_{SS} +0.3			V
Low Level Output Voltage for type OOSC output pins	V_{OH3} (OOSC)	V_{DD} = MIN I_{OH} = –100 µA			V_{DD} –0.3	V
Output Leakage Current	I_{OZ}	V_{DD} = MAX $V_{OH} = V_{DD}$, $V_{OL} = V_{SS}$	–1.0		1.0	µA
Output Pin Capacitance	C_{OUT}			10		pF

Power Consumption

Table 12. Power Consumption

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Consumption in Active Mode with CPU write access	I_{OP1}	V_{DD} = 3.3 V t_{CYCE} = 500 ns f_{OSC} = 24 kHz		5		mA
Current Consumption in Active Mode with no CPU write access	I_{OP2}	V_{DD} = 3.3 V t_{CYCE} = 500 ns "$\overline{CS}$" = high f_{OSC} = 24 kHz		1		mA
Current Consumption in Doze Mode with CPU write access	I_{OP3}	V_{DD} = 3.3 V t_{CYCE} = 500 ns f_{OSC} = 24 kHz		4		mA
Current Consumption in Doze Mode with no CPU write access	I_{OP4}	V_{DD} = 3.3 V t_{CYCE} = 500 ns "$\overline{CS}$" = high f_{OSC} = 24 kHz		150		µA
Current Consumption in Sleep Mode	I_{OP5}	V_{DD} = 3.3 V No input signals toggle.		1		µA

Note: The above table shows the target power consumption.

A.C. CHARACTERISTICS

Conditions: V_{DD} = 3.3 V, Ta = 0°C to 70°C unless otherwise specified
Tr, Tf for all inputs must be –10 ns (10% to 90%)
C_L = 10 pF (SRAM Interface)
C_L = 20 pF (LCD Interface)

A single 1.5 V threshold voltage is used for the A.C. measurements.

CPU Interface Timing

Table 13. CPU Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"$\overline{CS}$" period	t_{cycCS}	t_{cycE}			ns
"$\overline{CS}$" low pulse width	t_{lCS}	170			ns
"$\overline{CS}$" high pulse width	t_{hCS}	100			ns
"DT/$\overline{CM}$" setup to "$\overline{CS}$"	t_{dsu1}	20			ns
"DT/$\overline{CM}$" hold from "$\overline{CS}$"	t_{dh1}	0			ns
"D [0:7]" setup to "$\overline{CS}$"	t_{dsu2}	70			ns
"D [0:7]" hold from "$\overline{CS}$"	t_{dh2}	0			ns

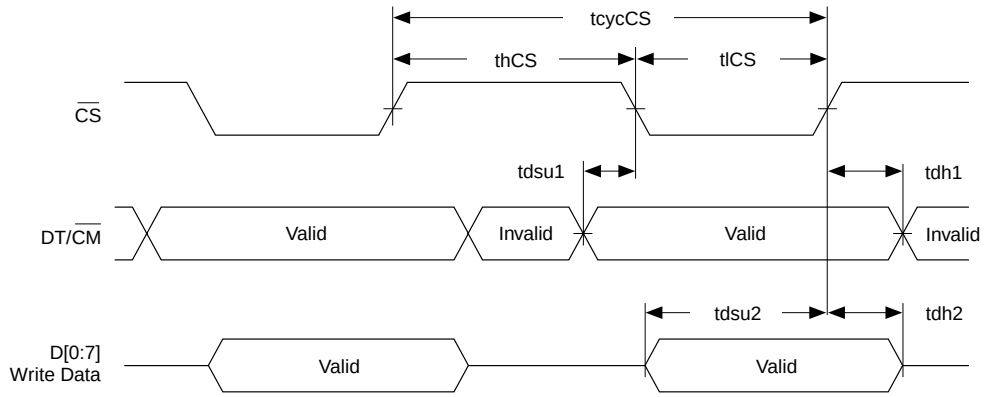

Figure 5. CPU Interface Timing

SRAM Interface Timing

Table 14. SRAM Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"E" period	t_{cycE}	333			ns
"E" low pulse width	t_{lE}	142			ns
"E" high pulse width	t_{hE}	137			ns
"VR/$\overline{W}$" period	t_{cycVW}	t_{cycE}			ns
"VR/$\overline{W}$" low pulse width	t_{lVW}		t_{hE}-40		ns
"VR/$\overline{W}$" high pulse width	t_{hVW}		t_{lE}		ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" setup to "VR/$\overline{W}$"	t_{asuVW}	0			ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" hold from "VR/$\overline{W}$"	t_{ahVW}	0			ns
"VD [0:7]" setup to "VR/$\overline{W}$"	t_{dsuVW}	t_{lVW}-20	t_{lVW}-10		ns
"VD [0:7]" hold from "VR/$\overline{W}$"	t_{dhVW}	0			ns
valid address period for the Display Refresh	t_{aVR}	t_{lE}-15	t_{lE}		ns
valid address period for the CPU data write	t_{aVW}	t_{hE}-15	t_{hE}		ns
SRAM read data access from the valid address	t_{accV}			t_{aVR}-25	ns
SRAM read data hold time from the valid address	t_{pdhV}	0			ns
"VA [0:14]", "$\overline{VCS}$ [0:1]" setup to "$\overline{VOE}$"	t_{asuOE}	0			ns
"$\overline{VOE}$" hold from "VA [0:14]", "$\overline{VCS}$ [0:1]"	t_{ahOE}	0			ns
"$\overline{VOE}$" low pulse width	t_{lOE}		t_{lE}		ns
"$\overline{VOE}$" high pulse width	t_{hOE}		t_{hE}		ns
"VR/$\overline{W}$" delay from "$\overline{VOE}$"	t_{pdOW}	0			ns
"$\overline{VOE}$" delay from "VR/$\overline{OW}$"	t_{pdWO}	0			ns

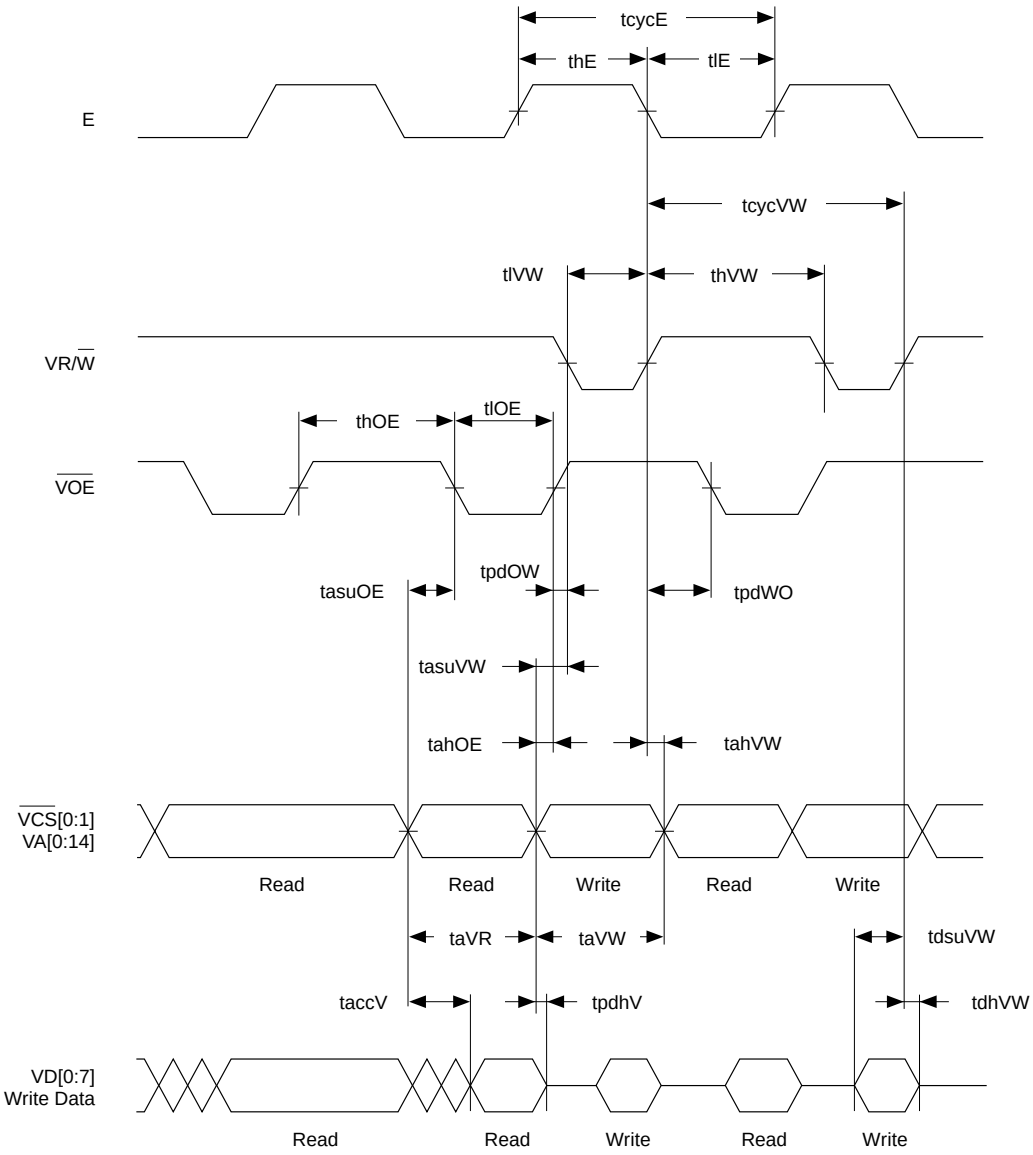

Figure 6. SRAM Interface Timing

LCD Interface Timing

Table 15. LCD Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"XSCLU" period	t_{cycXC}	t_{cycE}			ns
"XSCLU" low pulse width	t_{lXC}		t_{lE}		ns
"XSCLU" high pulse width	t_{hXC}		t_{hE}		ns
"XD [0:7]" setup to "XSCL"	t_{dsuXC}		t_{hE}		ns
"XD [0:7]" hold from "XSCL"	t_{dhXC}		t_{lE}		ns
"YD" delay from "LP"	t_{pdLY}	0			ns
"LP" period	t_{cycLP}	t_{cycOSC}	$2t_{cycOSC}$	$4t_{cycOSC}$	ns
"LP" high pulse width	t_{hLP}	500	700	1200	ns
"XSCL" delay from "LP"	t_{pdLXC}	$3t_{cycE}$ $+t_{hE}$-50	$4t_{cycE}$	$4t_{cycE}$ $+t_{hE+50}$	ns
"LP" delay from "XSCL"	t_{pdXCL}				ns
"XSCL" enabled	t_{XSCL}		[(Hor. size/8)-1] $\times t_{cyE}+t_{hE}$		ns
"YD" period	t_{cycYD}		(Ver.size) $\times t_{cycLP}$		ns
"FR" high or Low time	t_{cycFR}		t_{cycYD}		ns
"FR" delay from "LP"	t_{pdLF}	10	0	200	ns

Notes: 1. t_{cycOSC} is a period of frequency given to or generated at "OSC1".
2. Hor.size is described in the section Display Size.
3. Ver.size is described in the section Display Size.

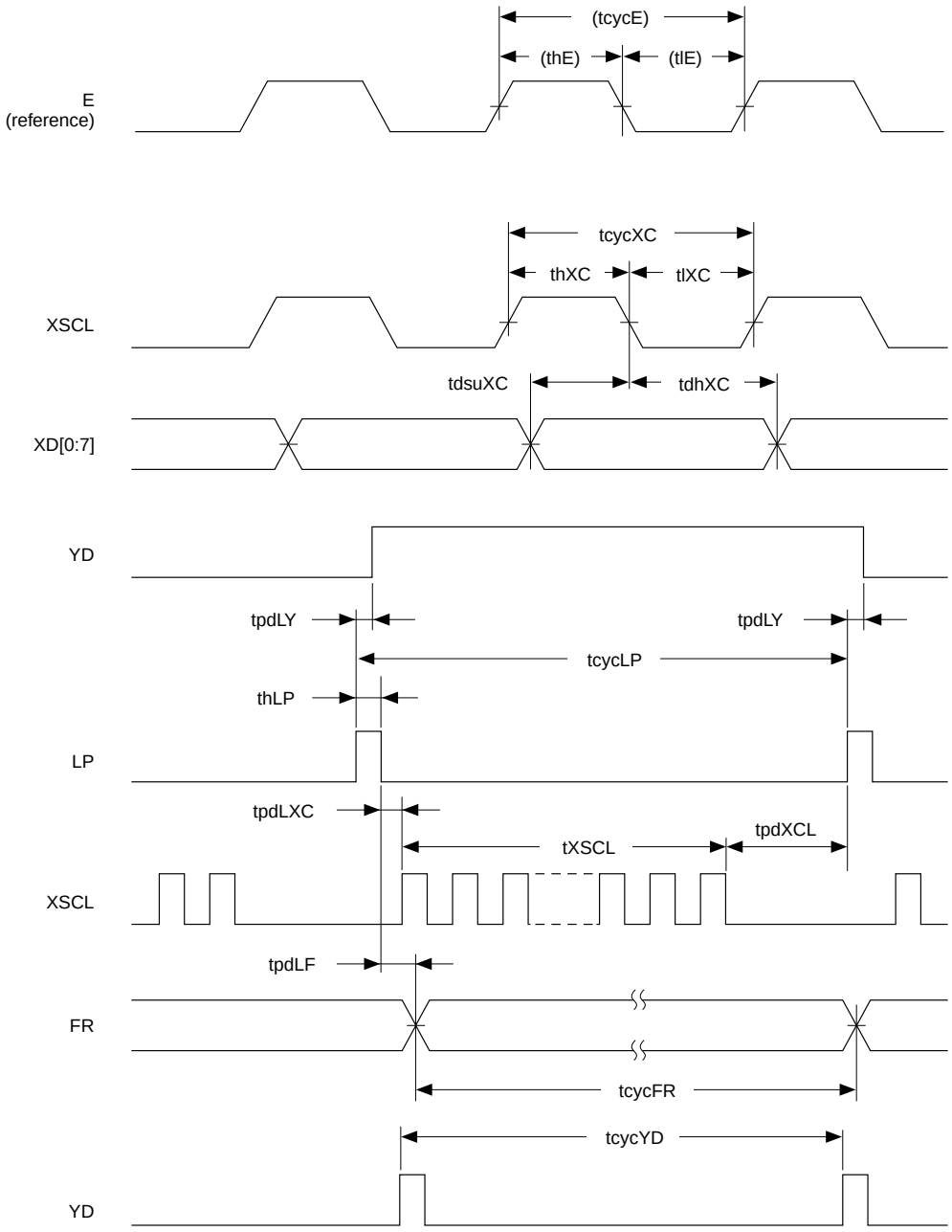

Figure 7. LCD Interface Timing

Oscillation Timing

Table 16. LCD Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
"OSC1" period	t_{cycOSC}	20 t_{OSC} = 50 kHz	41.7 f_{OSC} = 24 kHz	50 f_{OSC} = 20 kHz	µs
"OSC1" low width if external oscillation is used.	t_{lOSC}		$0.5t_{cycOSC}$		µs
"OSC1" high width if external oscillation is used.	t_{hOSC}		$0.5t_{cycOSC}$		µs

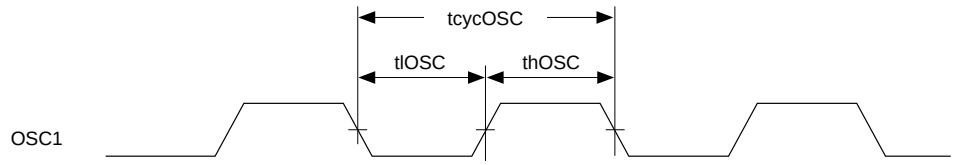

Figure 8. LCD Interface Timing

OPERATION DESCRIPTION

CPU Write Data Transfer

The following figure gives a basic timing for SED1360 to receive the CPU Write Data and relationship between CPU Data and pixels on the LCD panel. It is assumed that both CPU Write Start Address and Display Refresh Start Address are the same and the 320 × 200 dot LCD is used in the following figure.

(1) The rising edge of "$\overline{CS}$" is used for SED1360 to latch the CPU data.
(2) The CPU Data Write, after the "Display Data Write" command is executed, will be stored in the SRAM according to the internal CPU Write Address.
(3) The first 40 Byte data will be stored in SRAM and displayed continuously on the same line.
(4) The data will be displayed at the most left position on the next line on the panel every 40 Byte data.

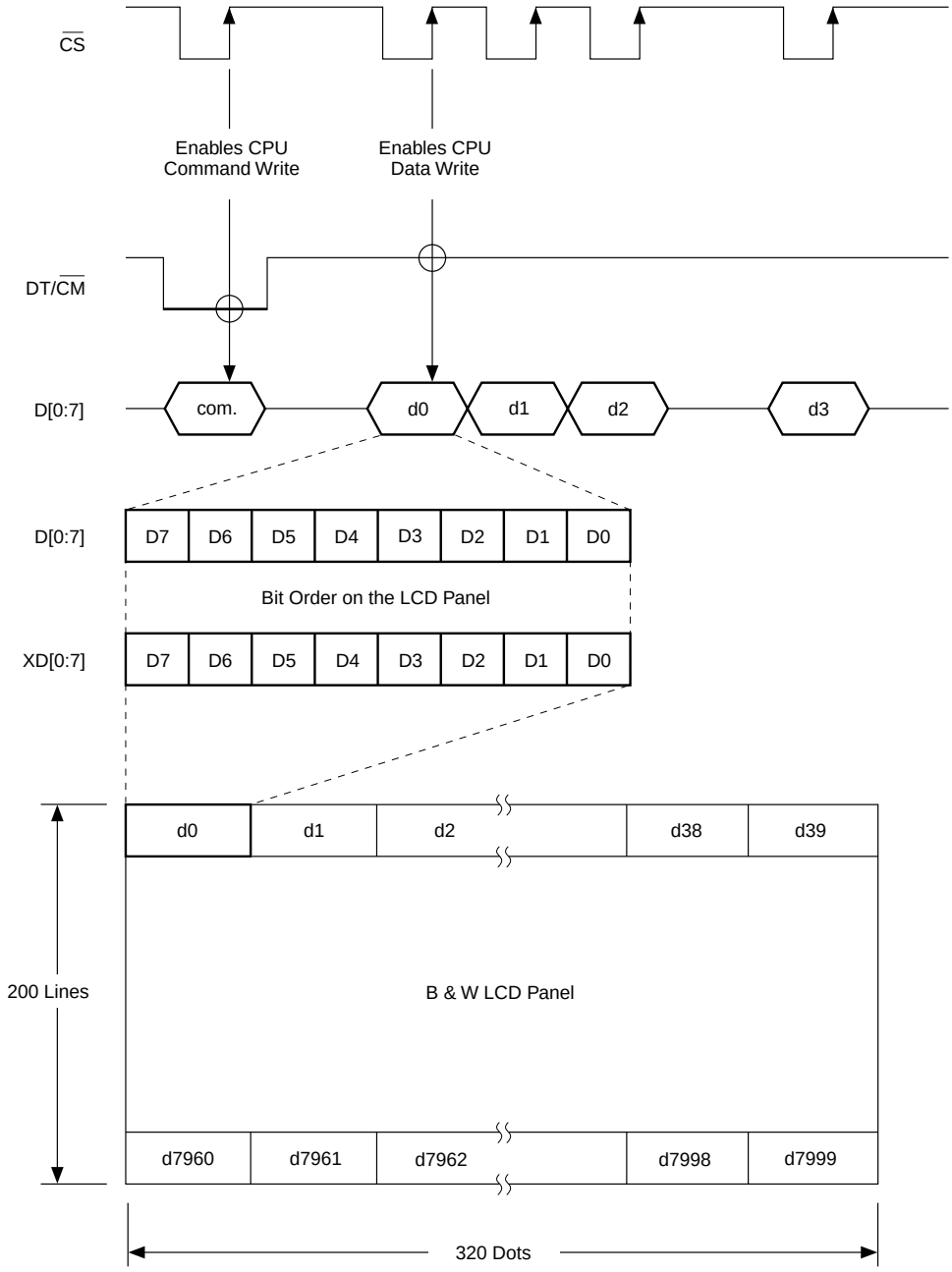

Figure 9. CPU Write Data Transfer

Display Data Transfer Modes

Display Data Auto Transfer Mode

The following figure gives a basic operation mode which SED1360 switches automatically. The figure assumes that the chip is configured in Display Data Auto Transfer Mode.

(1) If CPU Display Data Write Access occurs, then the next Frame period will be Active Mode. That is the Active Mode is initiated by the CPU Display Data Write Access, if the chip is configured in Display Data Auto Transfer Mode.
(2) If no CPU Display Data Write Access occurs in one Frame period, then the next Frame period will be Doze Mode.
(3) SED1360 switches the whole LCD Display Subsystem between Doze Mode and Active Mode.
(4) In the Active Mode, SED1360 reads the data from the SRAM, enables “XSCLU” in order to transfer the data stored in the SRAM to the LCD Module, then the RAM integrated Segment Drivers wake up from the power save mode.
(5) In the Doze Mode, SED1360 stops reading the data from the SRAM, disables “XSCLU” in order for the RAM integrated Segment Drivers to enter into the Power Save Mode.

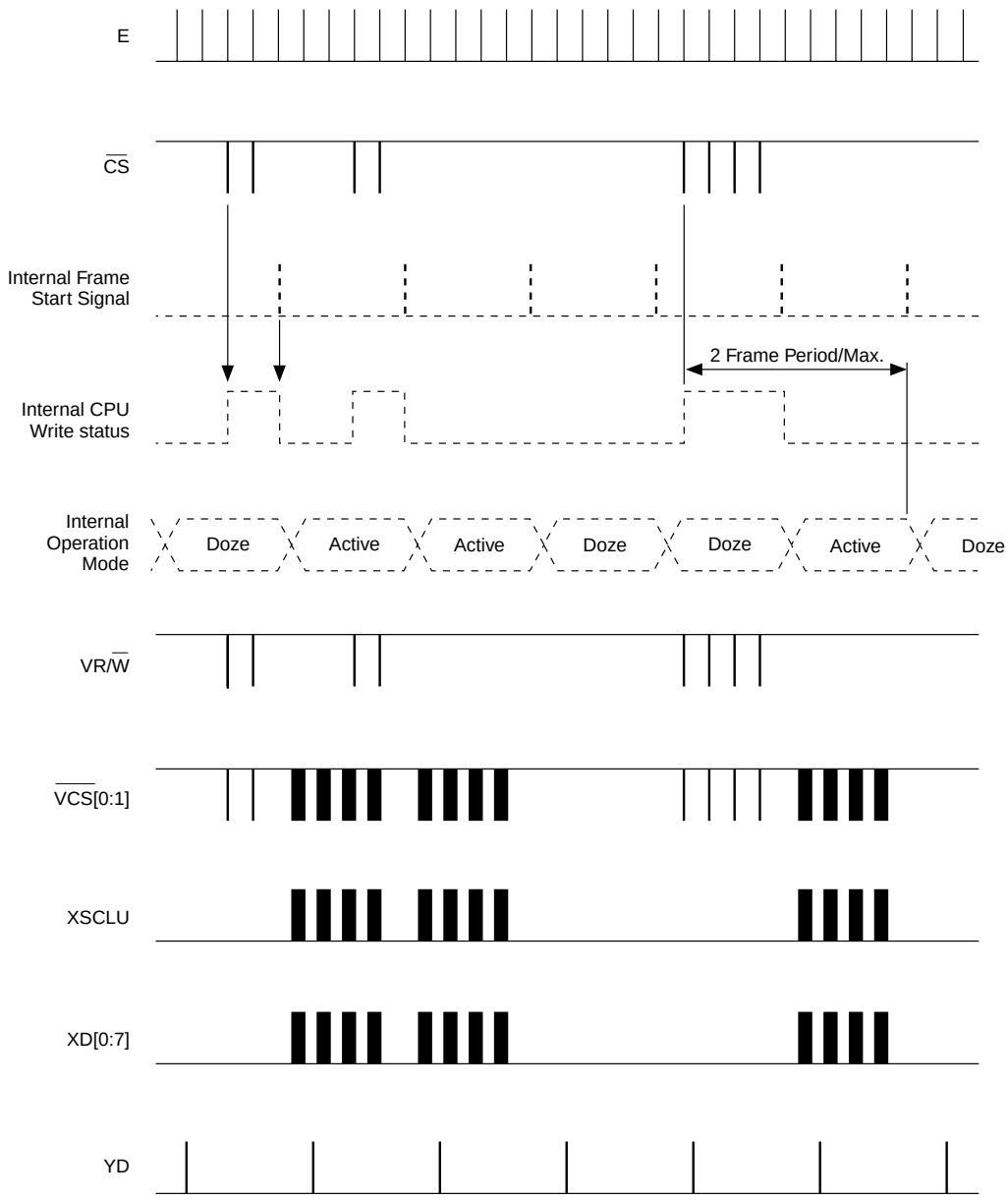

Figure 10. Display Data Auto Transfer Mode

Display Data Manual Transfer Mode

The following figure gives another basic operation mode which SED1360 controls Active Mode with the "Display Data Transfer" command. The figure assumes that the chip is configured in Display Data Manual Transfer Mode.

(1) If the "Display Data Transfer" command is set to the chip, then the next Frame period will be Active Mode. That is the Active Mode is initiated by the Display Data Transfer" command, if the chip is configured in Display Data Manual Transfer Mode.
(2) Once one Frame of display data, which are in the SRAM, are transferred to the LCD Module, the chip switches to Doze Mode and it keeps the Doze Mode until next "Display Data Transfer" command is executed. But if the next "Display Data Transfer" command is set without having any other commands between these two "Display Data Transfer" commands, the next "Display Data Transfer" command is ignored. That is in this case the next "Display Data Transfer" command does not set the chip in the Active Mode.
(3) SED1360 switches the whole LCD Display Subsystem between Doze Mode and Active Mode.
(4) In the Active Mode, SED1360 reads the data from the SRAM, enables "XSCLU" in order to transfer the data stored in the SRAM to the LCD Module, then the RAM integrated Segment Drivers wake up from the power save mode.
(5) In the Doze Mode, SED1360 stops reading the data from the SRAM, disables "XSCLU" in order for the RAM integrated Segment Drivers to enter into the Power Save Mode.

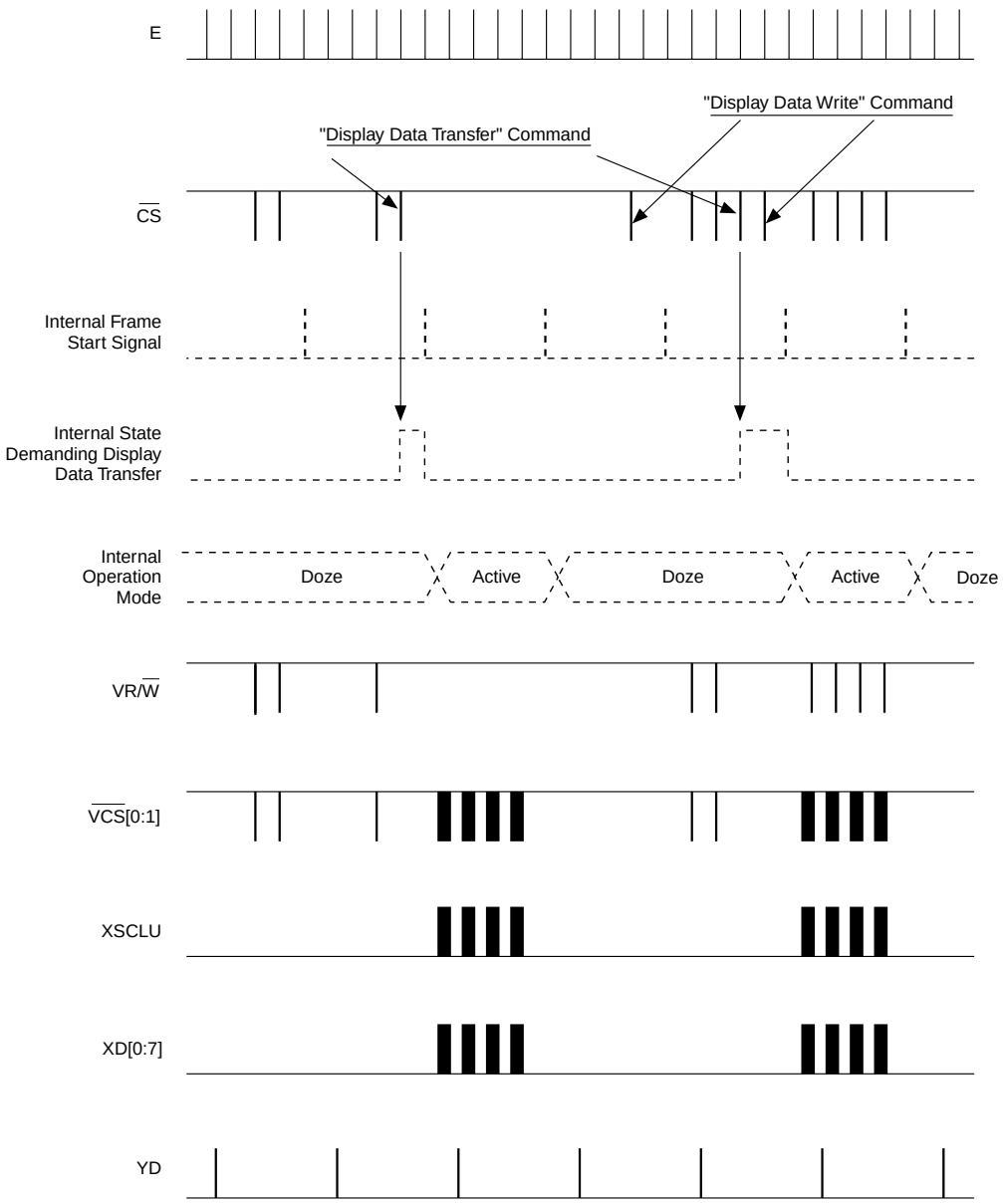

Figure 11. Display Data Manual Transfer Mode

Sleep Mode

SED1360 can enter into the Sleep Mode by setting the "$\overline{\text{SLEEP}}$" signal low. This mode is prepared to shut the whole LCD Display Subsystem off with keeping the data in the SRAM. In the Sleep Mode, the chip will be in the following state.

(1) The internal oscillation is displayed.
(2) VA [0:14] output low, $\overline{\text{VCS}}$ [0:1] output high, VD [0:7] will be high impedance (pins are pulled high by the integrated pull-up resisters).
(3) "FR", "YD", "LP", "XSCLU", "XD [0:7]" and "$\overline{\text{DOFF}}$" output low. $\overline{\text{VOE}}$, VR/$\overline{\text{W}}$ output high.
(4) "D [0:7]", "E" "$\overline{\text{CS}}$", "DT/$\overline{\text{CM}}$" and "$\overline{\text{RESET}}$" are internally masked but they also should be kept in invalid state.

OSCILLATION DESCRIPTION

SED1360's Hardware is optimized to display 320 × 200 LCD panel driven by RAM integrated Segment Drivers as a default chip configuraiton. This section describes how to determine the frequency which is input to OSC1 and how to generate the frequency by using the internal oscillation function.

OSC1 Frequency Determination

Conditions: 320 × 200 single scan LCD panel assumes 60 Hz as an LCD frame frequency

(1) "LP" period is obtained by the following calculation.
$60 \times 200 = 12$ kHz
(2) If an external oscillator is used, the OSC1 frequency can be the same as "LP". Then 12 kHz is the required frequency for OSC1.
(3) If an internal oscillator is used, the oscillation frequency has to be doubled to be 24 kHz. The internal oscillation might be unstable below 24 kHz. So if the required frequency is below 20 kHz, it is recommended to generate doubled frequency. There is a register which divides the internal oscillation frequency by two, four or eight.

Internal Oscillation

The following figure shows how to connect a capacitance and a resistance to the oscillation pins. The values of C and R have to be determined on the actual system.

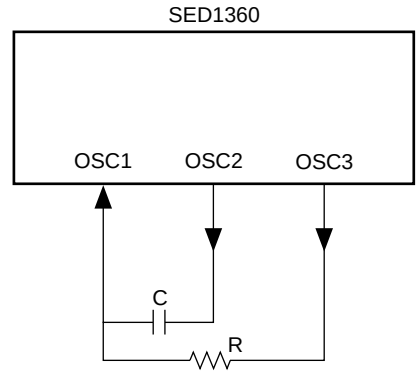

Figure 12. Internal Oscillation Implementation

COMMAND DESCRIPTION

SED1360 has several commands which can manipulate the data transfer procedure between CPU, SRAM, LCD Module and SED1360.

Display Size

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	1	01H

data; DT/$\overline{CM}$ = 1

0	0	HC5	HC4	HC3	HC2	HC1	HC0	data1
VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	data2

(1) This command sets the size of the display.
(2) This command requires two bytes of data which follow this command.
(3) The first data defines a horizontal size of the display in byte unit, and the second data defines a vertical size of the display in line unit.
(4) The horizontal size is set 320 dots and the vertical size is set 200 lines when the "$\overline{RESET}$" signal is set low.

Table 17. Horizontal Size

Hor. size	HC [5:0]
8	00h
16	01h
24	02h
240	1Dh
320	27h
512	3Fh

Table 18. Vertical Size

Ver. size	VC [7:0]
1	00h
2	01h
3	02h
200	C7h
240	Efh
256	Ffh

Display Data Auto Transfer Mode

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	02H

(1) This command configures the chip in the Display Data Auto Transfer Mode. Detailed functional explanation is described in "Display Data Auto Transfer Mode".

Display Data Manual Transfer Mode

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	1	03H

(1) This command configures the chip in the Display Data Manual Transfer Mode. Detailed functional explanation is described in “Display Manual Transfer Mode”.

Display Data Transfer

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	0	04H

(1) This command force the chip to go into the Active Mode so that the chip can start transferring the display data to the LCD Module. Detailed functional explanation is described in “Display Data Manual Transfer Mode”. This command is executable in not only Display Data Manual Transfer Mode but also Display Data Auto Transfer Mode.

Display Data Write

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	0	1	05H

data; DT/$\overline{CM}$ = 1

*	*	*	*	*	*	*	*	data1
*	*	*	*	*	*	*	*	data2
*	*	*	*	*	*	*	*	datan

(1) This command enables the chip to receive the data as the display data which are stored in SRAM.
(2) Data (data1,…datan) which follow this command are stored in SRAM until other commands are executed. If any other command breaks Display Data Write Access to the SRAM through the chip, this command has to be set again before starting Display Data Write Access.

CPU Write Start Address

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	1	0	06H

data; DT/$\overline{CM}$ = 1

WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA1	data1
WA15	WA14	WA13	WA12	WA11	WA10	WA9	WA8	data2

(1) This command sets the SRAM address which CPU Display Data can be stored.
(2) This command requires two bytes of data which follow this command.
(3) The order of two byte data is that the first data is lower byte and second data is higher byte.
(4) The two bytes of data are temporarily set to the internal CPU Write Address Counter by this command. And the CPU Write Address Counter is increased by one, when CPU Display Data Write Access occurs.

Display Refresh Start Address

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	1	1	1	07H

data; DT/$\overline{CM}$ = 1

RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA1	data1
RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	data2

(1) This command sets the SRAM address which SED1360 starts reading the data from, to transfer the display data to the LCD Module in Active Mode.
(2) This command requires two bytes of data which follow this command.
(3) The order of two byte data is that the first data is lower byte and second data is higher byte.
(4) The two bytes of data are set to the internal Display Data Refresh Address Counter by this command.

Display ON/$\overline{OFF}$

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	0	0	0	0	ON/$\overline{OFF}$	81H 80H

(1) This command controls "$\overline{DOFF}$" output.
(2) If the ON/$\overline{OFF}$ is set to high "$\overline{DOFF}$" outputs high. If the ON/$\overline{OFF}$ is set to low "$\overline{DOFF}$" outputs low.
(3) The ON/$\overline{OFF}$ is set to low at the reset.

LP Configuration

command; DT/$\overline{CM}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	1	0	0	0	08H

data; DT/$\overline{CM}$ = 1

0	0	0	0	0	0	FS1	FS0	data1

(1) This command selects "LP" period.
(2) FS1,0 select the period of the signal "LP". The following table shows how to select the required frequency for the signal "LP".
(3) FS [1,0] = [0,0] is set when the "$\overline{RESET}$" signal is set low.

Table 19. LP Frequency

FS1	FS0	LP frequency
0	0	fosc
0	1	fosc/2
1	0	fosc/4
1	1	fosc/8

ERRORTA

This version has one error. About CPU Write Start Address, Values which CPU wrote is increased by one. So, you should set values which is decreased by one.

NOTICE