SED1590

Contents

OVERVIEW

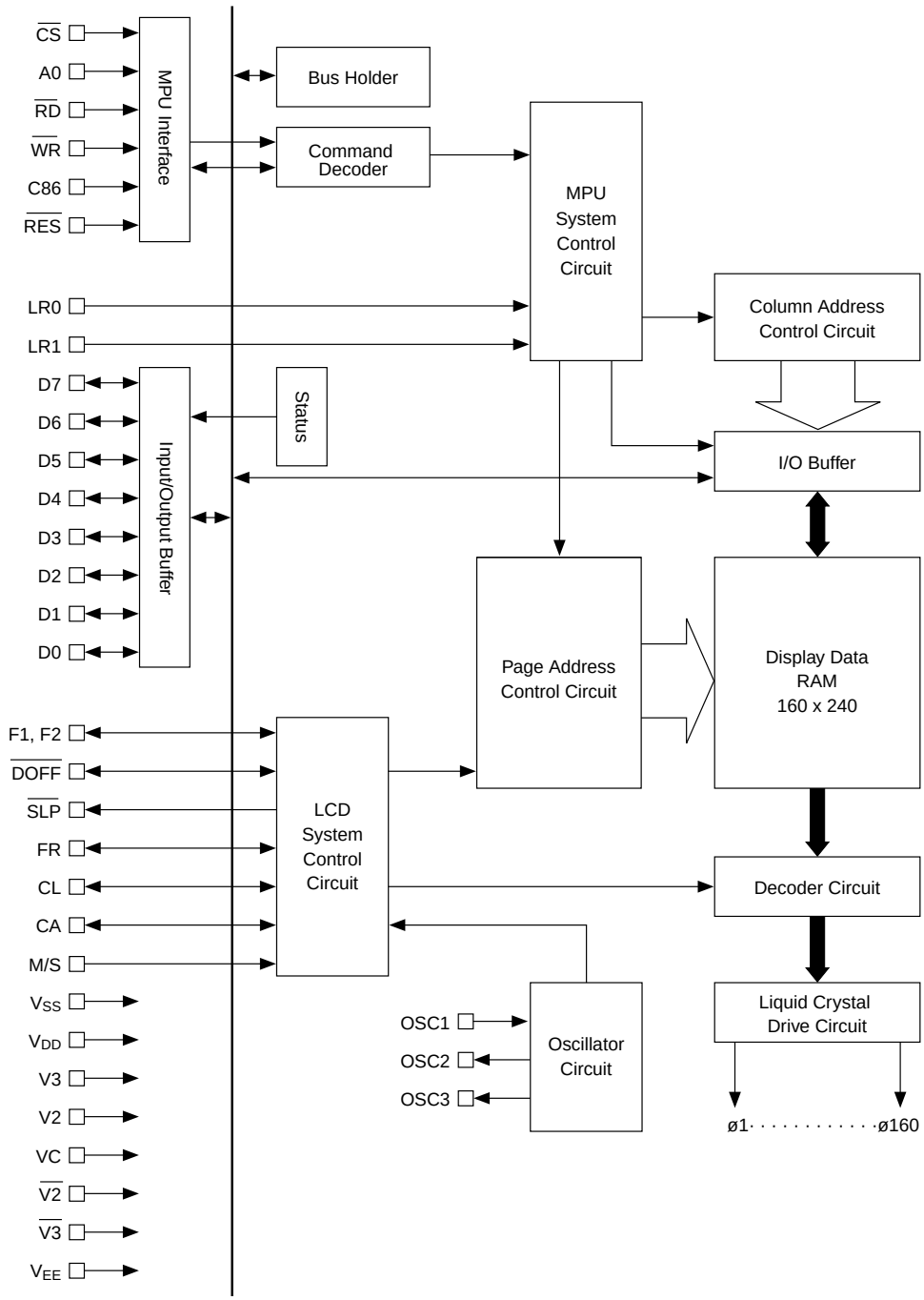
Description

The SED 1590 is a high image quality mid-display-size-compatible RAM-integrated segment (column) driver that boasts the low power consumption required by portable devices. It is used in a set with the SED 1751 common (row) driver and the SCI 7500 power supply IC.
The SED 1590 can be connected directly to the MPU bus. It stores in its internal display RAM memory the 8-bit parallel display data sent to it from the MPU and then issues the LCD drive signals independent of the MPU. The chip has 160 LCD drive outputs and is equipped with 160 out × 240 line internal display RAM. Furthermore, because there is a one-to-one correspondence between picture elements on the LCD display and internal RAM dots, displays can be created with a high degree of flexibility.
Because it is not necessary to supply an external clock when writing to the SED 1590 internal RAM from the MPU side, these operations can be performed with an absolute minimum power consumption. Moreover, even when multiple SED 1590 chips are used, single chip select is supported; thus it is not necessary for the MPU to distinguish between the multiple chips.
The SED 1590 has a slim form that is useful in creating thinner LCD panels. It can operate using a low-voltage logic power supply system, and is thus suited to a broad range of applications.

Features

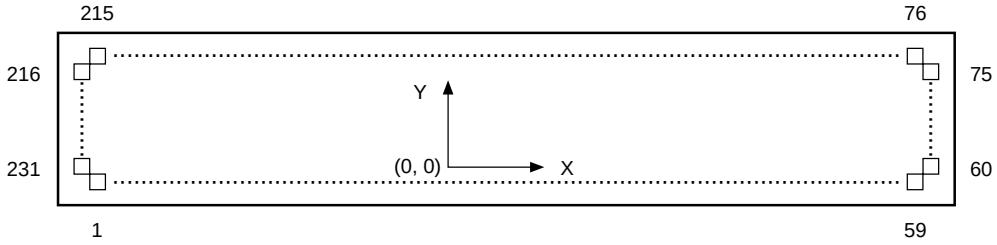
- Number of LCD drive outputs: 1 ..... 0 out
- Drive duty ratio (MAX): ..... 1/240 duty
- RAM data displayed directly using the display data RAM.
- RAM bit data (when in normal display mode): ..... "0" - Off
  "1" - On
- Internal RAM capacity: ..... 160 × 240 bit
- High speed 8-bit MPU interface
- Compatible with both 80x86 series and 68000 series MPUs.
- Single chip select when multiple chips are used.
- Rich command functions.
- Extremely low consumption current.
- Power supply
- Logic system: ..... 2.7 to 3.6 V
- LCD system: ..... 5.4 to 7.2 V
- Non-biased display off function
- Slim chip shape
- Package: DIE D0B
  TCP ..... TXX
- This product is not designed for resistance to radiation or exposure to light.

Block Diagram



TERMINAL FUNCTIONS

Terminal Layout Diagram D0B



DIE: D0B
Chip size: 14.82 mm × 2.50 mm
Bump size: 67 μm × 80 μm (min.)
Bump pitch: 100 μm (min.)
Bump height: 22.5 ± 5.5 μm

Terminal Coordinates D0B

Pin	Name	X	Y
1	$\overline{V2}$	–6692	–1130
2	VC	–6548	
3	V2	–6404	
4	V3	–6260	
5	V_{SS}	–6025	
6	OSC1	–5846	
7	OSC2	–5588	
8	OSC3	–5292	
9	V_{SS}	–5016	
10	NC	–4847	
11	NC	–4703	
12	$\overline{CS}$	–4507	
13	A0	–4344	
14	$\overline{RD}$	–4181	
15	$\overline{WR}$	–4019	
16	$\overline{RES}$	–3856	
17	V_{SS}	–3703	
18	C86	–3508	
19	V_{DD}	–3355	
20	LR0	–3160	
21	V_{SS}	–3001	
22	LR1	–2805	
23	V_{DD}	–2652	
24	MS	–2453	
25	V_{SS}	–2295	
26	D0	–1926	
27	D1	–1609	
28	V_{DD}	–1309	
29	D2	–1055	
30	D3	–728	
31	D4	–432	
32	D5	–104	
33	D6	191	
34	D7	518	
35	FR	858	
36	CL	1154	
37	V_{SS}	1413	
38	F1	1882	
39	F2	2178	
40	$\overline{DOF}$	2506	
41	CA	2802	
42	$\overline{SLP}$	3191	
43	COD0	3519	
44	COD1	3815	
45	COD2	4142	
46	COD3	4438	
47	COD4	4766	
48	NC	5002	
49	NC	5146	
50	NC	5290	
51	NC	5434	
52	NC	5578	
53	NC	5722	
54	NC	5866	
55	NC	6010	
56	V3	6260	
57	V2	6404	
58	VC	6548	

Pin	Name	X	Y
59	$\overline{V2}$	6692	–1130
60	$\overline{V3}$	7290	–837
61	V_{EE}		–693
62	NC		–549
63	NC		–369
64	O160		–268
65	O159		–167
66	O158		–66
67	O157		33
68	O156		134
69	O155		235
70	O154		336
71	O153		437
72	O152		537
73	O151		638
74	O150		739
75	NC		840
76	NC	7007	1130
77	O149	6904	
78	O148	6804	
79	O147	6703	
80	O146	6602	
81	O145	6501	
82	O144	6400	
83	O143	6300	
84	O142	6199	
85	O141	6098	
86	O140	5997	
87	O139	5896	
88	O138	5796	
89	O137	5695	
90	O136	5594	
91	O135	5493	
92	O134	5392	
93	O133	5292	
94	O132	5191	
95	O131	5090	
96	O130	4989	
97	O129	4888	
98	O128	4788	
99	O127	4687	
100	O126	4586	
101	O125	4485	
102	O124	4384	
103	O123	4284	
104	O122	4183	
105	O121	4082	
106	O120	3981	
107	O119	3880	
108	O118	3780	
109	O117	3679	
110	O116	3578	
111	O115	3477	
112	O114	3376	
113	O113	3276	
114	O112	3175	
115	O111	3074	
116	O110	2973	

Pin	Name	X	Y
117	O109	2872	1130
118	O108	2772	
119	O107	2671	
120	O106	2570	
121	O105	2469	
122	O104	2368	
123	O103	2268	
124	O102	2167	
125	O101	2066	
126	O100	1965	
127	O99	1864	
128	O98	1764	
129	O97	1663	
130	O96	1562	
131	O95	1461	
132	O94	1360	
133	O93	1260	
134	O92	1159	
135	O91	1058	
136	O90	957	
137	O89	856	
138	O88	756	
139	O87	655	
140	O86	554	
141	O85	453	
142	O84	352	
143	O83	252	
144	O82	151	
145	O81	50	
146	O80	–50	
147	O79	–151	
148	O78	–252	
149	O77	–352	
150	O76	–453	
151	O75	–554	
152	O74	–655	
153	O73	–756	
154	O72	–856	
155	O71	–957	
156	O70	–1058	
157	O69	–1159	
158	O68	–1260	
159	O67	–1360	
160	O66	–1461	
161	O65	–1562	
162	O64	–1663	
163	O63	–1764	
164	O62	–1864	
165	O61	–1965	
166	O60	–2066	
167	O59	–2167	
168	O58	–2268	
169	O57	–2368	
170	O56	–2469	
171	O55	–2570	
172	O54	–2671	
173	O53	–2772	
174	O52	–2872	

Pin	Name	X	Y
175	O51	–2973	1130
176	O50	–3074	
177	O49	–3175	
178	O48	–3276	
179	O47	–3376	
180	O46	–3477	
181	O45	–3578	
182	O44	–3679	
183	O43	–3780	
184	O42	–3880	
185	O41	–3981	
186	O40	–4082	
187	O39	–4183	
188	O38	–4284	
189	O37	–4384	
190	O36	–4485	
191	O35	–4586	
192	O34	–4687	
193	O33	–4788	
194	O32	–4888	
195	O31	–4989	
196	O30	–5090	
197	O29	–5191	
198	O28	–5292	
199	O27	–5392	
200	O26	–5493	
201	O25	–5594	
202	O24	–5695	
203	O23	–5796	
204	O22	–5896	
205	O21	–5997	
206	O20	–6098	
207	O19	–6199	
208	O18	–6300	
209	O17	–6400	
210	O16	–6501	
211	O15	–6602	
212	O14	–6703	
213	O13	–6804	
214	O12	–6904	
215	NC	–7007	
216	NC	–7290	840
217	O11		739
218	O10		638
219	O9		537
220	O8		437
221	O7		336
222	O6		235
223	O5		134
224	O4		33
225	O3		–66
226	O2		–167
227	O1		–268
228	NC		–369
229	NC		–549
230	V_{EE}		–693
231	$\overline{V3}$		–837

Explanation of Terminals

Power Supply Terminals

Terminal Name	I/O	Explanation	No. of Terminals
V_{DD}	Power Supply	These are connected to V_{CC} (the system power supply).	3
V_{SS}	Power Supply	These are connected to the system GND.	6
V_{EE}	Power Supply	These are the liquid crystal drive system load-side power supplies. V_{DD}–V_{EE}.	2
V3, V2, VC, –V2, –V3	Power Supply	These are the liquid crystal drive multi-level power supplies. The relationships between the various levels must be: $V_{DD} \geq V3 \geq V2 \geq VC > -V2 > -V3 \geq V_{EE}$	2 Each

Terminals Pertaining to the MPU

Terminal Name	I/O	Explanation	No. of Terminals
D7 to D0	I	These comprise the 8–bit bi-directional data bus, and are connected to a standard 8–bit or 16–bit MPU data bus.	8
A0	I	The least significant bit of the address bus of a normal MPU is connected to discern between data and commands. H: Inidcates that D7 to D0 are control data. L: Indicates that D7 to D0 are display data.	1
$\overline{RES}$	I	When initial settings are restored by placing $\overline{RES}$ to “L”. The reset operation is performed based on the $\overline{RES}$ level. Schmidt trigger.	1
$\overline{CS}$	I	This is the chip select signal. In the SED 1590, even if multiple chips are used, the $\overline{CS}$ is a shared line. When $\overline{CS}$ is in a non-active state, D7 to D0 enter a high-impedance state.	1
$\overline{RD}$ (E)	I	• When connected to an 80x86 series MPU Active “L” This terminal connects to the $\overline{RD}$ signal of the 80x86 MPU, and while this signal is low, the data bus is in an output state. • When connected to a 68000 series MPU Active “H” This serves as the 68000 MPU-enabled clock input terminal.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 80x86 system MPU Active “L” This terminal is connected to the $\overline{WR}$ signal of the 80x86 series MPU. The data bus signals are latched on the rising edge of the $\overline{WR}$ signal. • When connected to a 68000 series MPU This is the read/write control input terminal. R/W = “H”: Read R/W = “L”: Write	1
C86	I	This is the MPU interface switch terminal. C86 = “H”: The 68000 MPU interface. C86 = “L”: The 80x86 series MPU interface.	1

Liquid Crystal Drive Circuit Signals

Terminal Name	I/O	Explanation	No. of Terminals
OSC1	I	This is for the oscillator circuit. When an external input is used, it is input to this terminal. Connect to "H" or "L" in case of slave operations.	1
OSC2	O	This is a terminal for the oscillator circuit. When the internal oscillator circuit is used, connect to OSC1 through a capacitor. Make this terminal open in case of slave operations.	1
OSC3	O	This is a terminal for the oscillator circuit. When the internal oscillator circuit is used, connect to OSC1 through a resistor. Make this terminal open in case of slave operations.	1
M/S	I/O	This terminal selects master/slave operation. In master mode, signals required for the liquid crystal display are output, while during slave operation signals that are required to the liquid crystal display are input, thereby synchronizing the liquid crystal display system. M/S = "H": Master operation M/S = "L": Slave operation	1
CL	I/O	This is the display clock input/output terminal. When using master/slave mode, this is connected to the various CL terminals. This is also connected to the common driver YSCL terminals. When M/S = "H": Output When M/S = "L": Input	1
FR	I/O	This is the liquid crystal alternating current input/output terminal. When using master/slave mode, this is connected to the various FR terminals. This is also connected to the common driver FR terminals. When M/S = "H": Output When M/S = "L": Input	1
CA	I/O	This is the field start signal. When using master/slave mode, this is connected to the various CA terminals. This is also connected to the common driver CA terminals. When M/S = "H": Output When M/S = "L": Input	1
$\overline{DOF}$	I/O	This is the liquid crystal display blanking control terminal. When using master/slave mode, this is connected to the various $\overline{DOFF}$ terminals. This is also connected to the common driver $\overline{DOFF}$ terminals. When M/S = "H": Output When M/S = "L": Input	1
$\overline{SLP}$	O	This is the sleep control terminal. When set to a sleep status by the MCU, both the master and the slave circuits enter the sleep mode. This terminal is not connected between the master and the slave. Connect to the SCI 7500 $\overline{SLP}$ terminal for the master only.	1
F1, F2	I/O	These are the drive pattern signal input/output terminals. When in master/slave mode, these are connected to the F1 and F2 terminals respectively. These are connected to the common driver F1 and F2 terminals. When M/S = "H": Output When M/S = "L": Input	1 each
On	O	Liquid crystal segment drive outputs	160

Control Terminals

Terminal Name	I/O	Explanation	No. of Terminals
LR0, LR1	I	When multiple SED1590 chips are used, these terminals specify the various segment driver layout positions. Using this information, the SED1590 determines the relationships between the various segments and the position in internal RAM.	1 each
COD0 COD1 COD2 COD3 COD4	O	These comprise the 5–bit output port. The status of this port can be controlled by commands from the MPU. They can be used for controls of the electronic volume control knobs and other applications.	1 each

EXPLANATION OF FUNCTIONS

The MPU Interface

The SED1590 exchanges data with the MPU through an 8–bit bi-directional data bus (D7 to D0).
By setting the C86 terminal to "H" or "L" the SED1590 can be connected directly to the MPU bus for either the 80x86 system MPUs or the 68000 system MPUs, as shown in Table 1.

Table 1

C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
H	68000 MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7
L	80×86 MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

The SED1590 identifies data bus signals using combinations of the A0, E, R/W and ($\overline{RD}$, $\overline{WR}$) signals as shown in Table 2.

Table 2

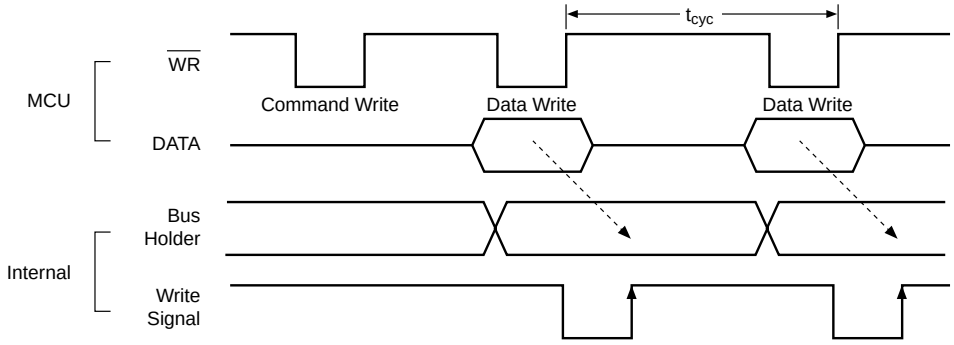
Common	68 System	80 System		
A0	R/W	$\overline{RD}$	$\overline{WR}$	Function
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

The SED1590 possesses a function that automatically identifies the segment driver position by the LR0 and LR1 terminals even when multiple SED1590 chips are used, so from the perspective of the MPU, there is no need for the MPU to identify the individual segment drivers. As a result, the $\overline{CS}$ chip select terminals can share a common line from the outside. The LR will be discussed below.
When the chips are not selected, D0 to D7 enter a high impedance state and terminals A0, $\overline{RD}$, and $\overline{WR}$ inputs are disabled.

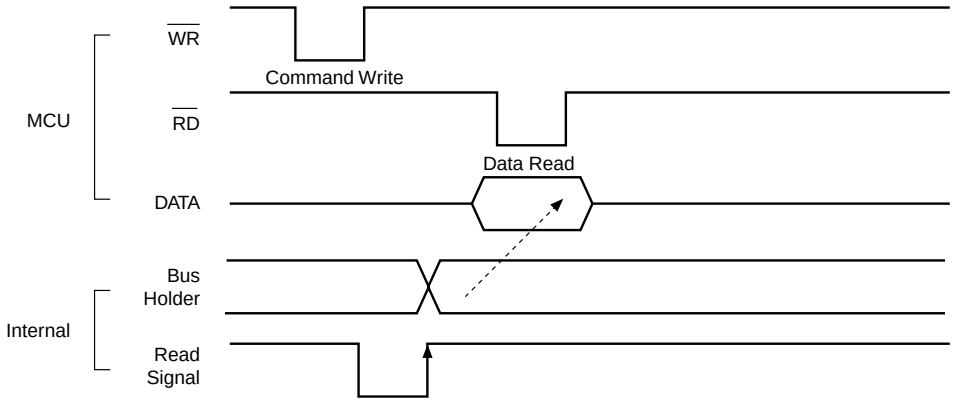
Accessing the Display Data RAM and the Internal Registers.

The SED1590 uses a type of pipeline process between LSIs through the bus holders in the internal data bus in order to match the operating frequencies between the MPU and the display data RAM and internal registers. Consequently, when viewed from the MPU side, there are no constraints on accessing the SED1590 in terms of the display data RAM access time (t_{ACC}), but rather the cycle time is dominant. When the cycle time is not adequate, then the MPU may insert an NOP command, which is equivalent to executing a dummy wait.

• Writing



• Reading



Busy Flag

When the busy flag is "L", the SED1569 is making internal operations. The busy flag is being output through the terminal D7 by the status read command. Although commands from the MPU are being accepted even while the busy flag is appearing, it is necessary to secure due cycle time (tcyc) in order to make proper writing of the indication data. Meanwhile, in case the cycle time is being satisfied, it is not necessary to check this flag.

Page Address Control Circuit

Page direction address control is performed when the display RAM is accessed by the MPU and when contents of the display data RAM are read for the liquid crystal display.
When the page direction scan is designated by the scan direction select command, the page address will increment each time the MPU makes the writing operation. While the internal RAM contains 240 lines worth of data, because the MPU access processes in 8 dot units in the common direction, the number of pages is 240/8 = 30 pages.
Consequently, the count is locked when address value 29 is reached, and there is no incrementation beyond this level. The count lock is cleared next time the page address is set. Moreover, the counter within the page address control circuit is independent of the column address control circuit counter.
When there is a read operation for the liquid crystal display, incrementation is synchronized with the CL signal, and the count is reset when the display line that is set by a control command from the MPU has been reached.

The Column Address Control Circuit

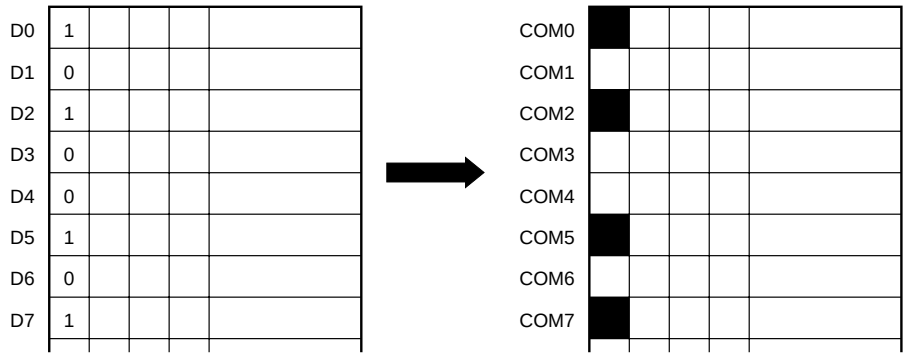
Address control in the column direction is performed when the display RAM is accessed from the MPU. The SED1590 unit has only 160 columns; however, using multiple chips the SED1590 can handle continuous column addressing even when using four chips in the column direction (640 columns). Consequently, from the MPU perspective, the MPU need not be aware of the multiple chips.
The address value is incremented or decremented when a write or read operation is performed by the MPU. In the increment mode, the count is locked at 279H (639), while in the decrement mode the count is locked at 000H (0). Incrementing/decrementing will not proceed past that count. The count lock is cleared the next time that a column address set is performed. Moreover, the counter within the column address control circuit operates independently of the page address control circuit counter.

The I/O Buffer

The I/O buffer is a bi-directional buffer for cases where the MPU accesses the display data RAM via the SED1590 internal bus.

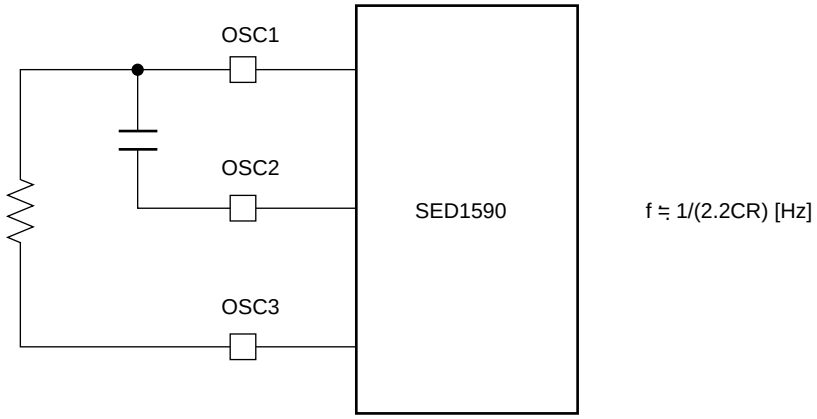
The Display Data RAM

The display data RAM is RAM in which is stored the dot data for the display. It has a 160×240 bit structure. The data can be selected by specifying the page address and the column address. The display data D0 to D7 from the MPU corresponds to 8 dots in the common direction of the liquid crystal display, and thus when multiple SED1590 chips are used, there are few constraints when the display data is sent, allowing the display to be structured freely.
MPU-side display RAM reading and writing is done through the I/O buffer, which operates to prevent timing overlaps with the display RAM reads for driving the liquid crystal. Consequently, there is absolutely no negative effect on the display such as flickering even if operations that write data to the RAM or read data from the RAM are performed completely asynchronously with the liquid crystal drive timing during the dipslay.



The Oscillator Circuit

The oscillator circuit generates the synch circuit for the liquid crystal drive. When the internal oscillator circuit of the SED1590 is used, then a capacitor must be placed between OSC1 and OSC2, and a resistor must be placed between OSC1 and OSC3, as shown in the figure below. Determine the C and R values based on the oscillation frequency formula given below.



When the internal oscillator circuit is not used (i.e. when an external clock input is used instead), input the external clock into OSC1. Leave OSC2 and OSC3 open.

M/S		OSC1	OSC2	OSC3
"H"	Master operation (using the internal oscillation circuit)	Refer to Fig. 3 indicated above.		
"H"	Master operation (using external signal inputs)	Input terminal.	Open	Open
"L"	Slave operation	Connect to "H" or "L".	Open	Open

The Decoder

The decoder outputs the segment driver control signal that is required for the liquid crystal drive. This control signal is determined by the display data, the drive pattern signals F1 and F2, and by the liquid crystal alternating current signal FR.

The Liquid Crystal Drive Circuit

This outputs the liquid crystal drive voltage. The liquid crystal drive voltage can be of one of five values: V3, V2, VC, $\overline{V2}$, $\overline{V3}$. These values are selected by the drive control signal determined by the decoder.

The Internal Timing Generator Circuit

The internal timing generator circuit controls the internal write operations when the display data RAM is accessed by the MPU. Moreover, in this case the column address counter and page address counter incrementation/decrementation is also controlled by the internal timing generator circuit.

When a module is structured from multiple chips, the SED1590 automatically determines from LR0 and LR1 which chip corresponds to which segments on the panel so that only the address relating to the corresponding segment responds. Consequently, from the perspective of the MPU, there is no need to identify each individual SED1590 chip, but rather when accessing in the column direction, continuous addresses can be handled in so far as the addresses are in the same page. As a result, the CS line can be shared. In this case, the relationship between the actual segment output and the column address is as shown in the following figure.

When there is an access race where both the MPU system and the display system are attempting to access the display data RAM simultaneously, the conflict between both accesses is mediated by the display control circuit. Consequently, there is no need for the MPU to perform a busy check in so far as the accesses ensure the cycle time that is set by the AC timing.

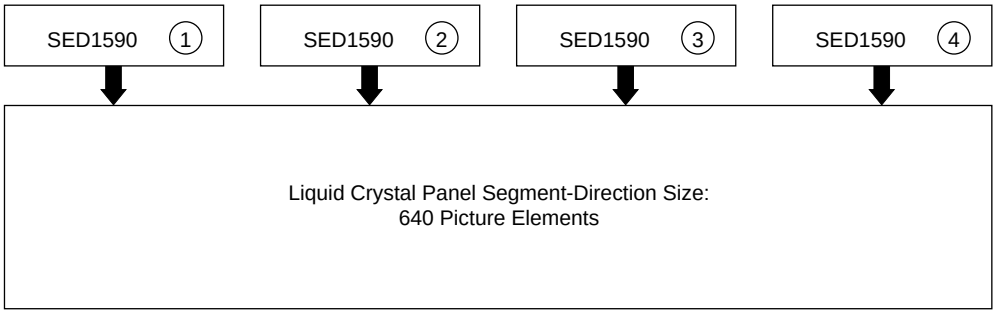


Table 3

	LR1	LR0	Corresponding Picture Elements	Column Address (10–bit binary display)
SED1590 1	"L"	"L"	1 to 160	0000000000B to 0010011111B
SED1590 2	"L"	"H"	161 to 320	0010100000B to 0100111111B
SED1590 3	"H"	"L"	321 to 480	0101000000B to 0111011111B
SED1590 4	"H"	"H"	481 to 640	0111100000B to 1001111111B

The Display Control Circuit

The display control circuit generates the timing signals CL, CA, FR, along with the drive pattern signals F1 and F2, for the display based on the oscillator output from the oscillator circuit. Moreover, depending on the commands from the MPU, this circuit generates the $\overline{\text{DOFF}}$ display On/Off control signal and the $\overline{\text{SLP}}$ sleep signal as well.
When multiple SED1590 chips are used, the input and output statuses of these signals are as given in Table 4.

Table 4

Operating Mode	CL	CA	F1, F2	FR	$\overline{\text{DOFF}}$	$\overline{\text{SLP}}$
Master	Output	Output	Output	Output	Output	Output
Slave	Input	Input	Input	Input	Input	Output

The Relationship Between the Display Drive Output Voltage and the Display Data

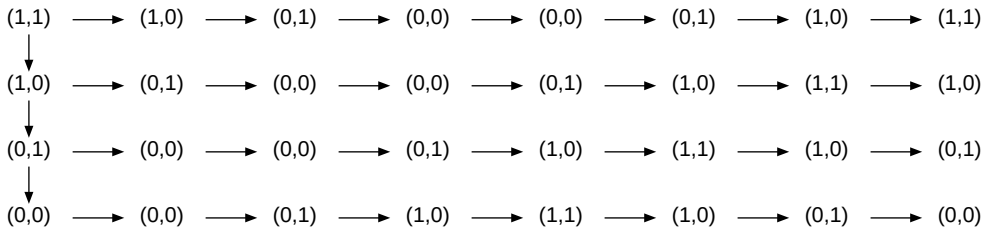
Table 5 shows the relationships between F1, F2 and the common drive voltage.

Table 5

FR	L				H			
F1	H	L	H	L	H	L	H	L
F2	H	H	L	L	H	H	L	L
n Line	V1	V1	–V1	V1	–V1	–V1	V1	–V1
n + 1 Line	–V1	V1	V1	V1	V1	–V1	–V1	–V1
n + 2 Lines	V1	–V1	V1	V1	–V1	V1	–V1	–V1
n + 3 Lines	V1	V1	V1	–V1	–V1	–V1	–V1	V1

Note: The voltage relationships are as follows: V1 > VC > –V1 (where VC is the central voltage).

The values of F1 and F2 change for each horizontal interval (as described below) and for each CA set by the commands. The changes are as shown below. Moreover, in this display the numbers are described as (F2, F2).



Changes in the horizontal direction indicate changes that happen each horizontal interval, where the horizontal interval was set by using commands. The changes in the vertical direction, shown on the column on the left, show the value change that starts with each CA.
The relationships between the display data, the liquid crystal alternating current signal FR, and the segment drive voltage are as shown in Table 6. These drive voltages change according to the combination of F1 and F2. In this table, “0” indicates “Off” and “1” indicates “On”.

Table 6

FR = “L”

Display Picture Element	n	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	1	V2	VC	VC	–V2	V3	V2	V2	VC	VC	V2	–V2	–V3	V2	VC	VC	–V2
	2	V2	VC	V3	V2	VC	–V2	V2	VC	VC	–V2	V2	VC	–V2	–V3	VC	–V2
	3	V2	VC	VC	–V2	VC	–V2	–V2	–V3	V3	V2	V2	VC	V2	VC	VC	–V2
	4	V2	V3	VC	V2	VC	V2	–V2	VC	VC	V2	–V2	VC	–V2	VC	–V3	–V2

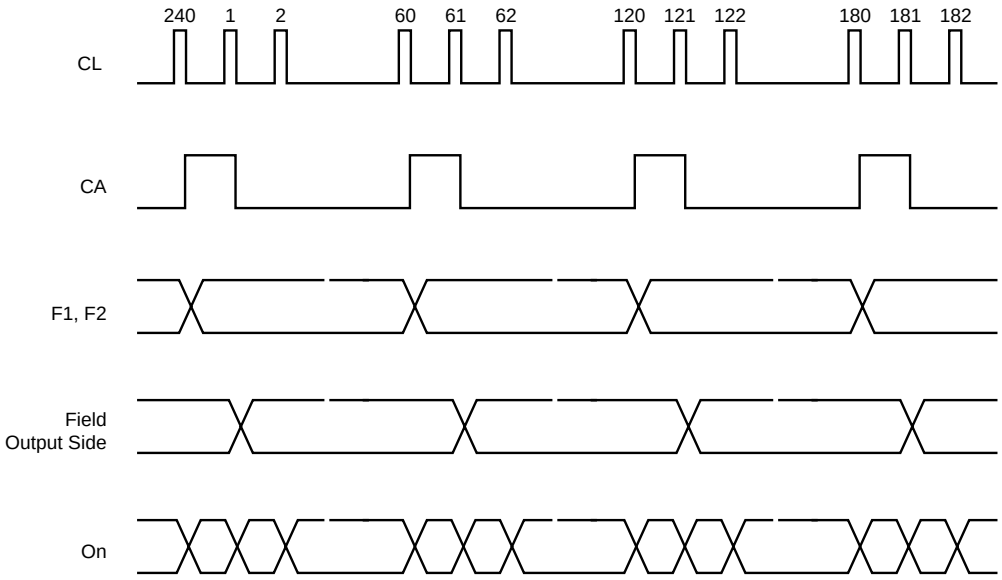
FR = “H”

Display Picture Element	n	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	1	–V2	VC	VC	V2	–V3	–V2	–V2	VC	VC	V2	V2	V3	–V2	VC	VC	V2
	2	–V2	VC	–V3	–V2	VC	V2	–V2	VC	VC	V2	–V2	VC	V2	V3	VC	V2
	3	–V2	VC	VC	V2	VC	V2	V2	V3	–V3	–V2	–V2	VC	–V2	VC	VC	V2
	4	–V2	–V3	VC	–V2	VC	–V2	V2	VC	VC	–V2	V2	VC	V2	VC	V3	V2

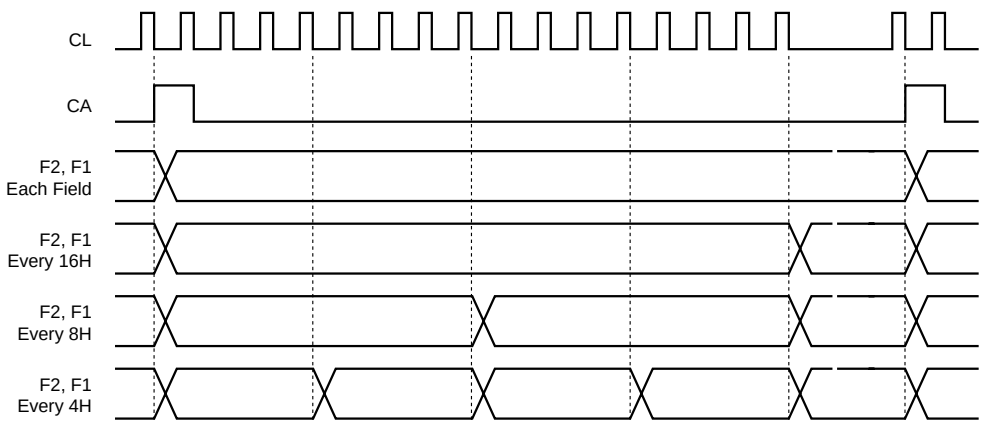
Notes: (1), (2), (3) and (4) correspond to the following drive pattern:
(1): (F2, F1) = (H, H)
(2): (F2, F1) = (H, L)
(3): (F2, F1) = (L, H)
(4): (F2, F1) = (L, L)

Timing Diagram

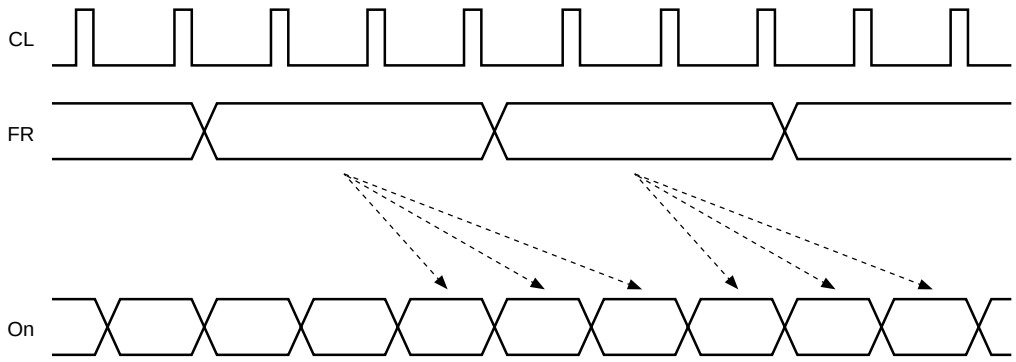
The timing diagram for the liquid crystal display is as shown in the following figure.
Example: The example shows the fields used in a 1/240 duty, where the liquid crystal drive pattern (F2, F1) switches for each field.



The figure below shows an example where the drive pattern (F2, F1) is different. The drive pattern is changed with the falling edge of CL and the status is reflected to the driver output that changes at the next falling edge of CL.



The figure below shows the timing with which FR changes. FR changes on the falling edge of CL, and the changes are reflected to the driver which changes on the next falling edge of CL (master mode). Moreover, in the case of slave mode, the FR status is accepted with the falling edge of CL, and is reflected to the driver output that changes on the next falling edge of CL.



COMMANDS

Table of Commands

Table 7 shows a table of SED1590 commands

Table 7

Command Name		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameters
1	DON	0	1	0	1	0	1	0	1	1	1	1	Display ON	None
2	DOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal display	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse display	None
5	DTYSET	0	1	0	1	0	1	0	1	0	0	0	Duty set	1 byte
6	LINSET	0	1	0	1	1	0	0	1	0	1	0	FR interval set	1 byte
7	PATSET	0	1	0	1	1	0	0	1	1	0	0	Drive pattern set	1 byte
8	VOLCTL	0	1	0	1	1	0	0	0	1	1	0	Output port control	1 byte
9	SLPON	0	1	0	1	0	0	1	0	1	0	1	Sleep on	None
10	SLPOFF	0	1	0	1	0	0	1	0	1	0	0	Sleep off	None
11	DVDSET	0	1	0	1	0	1	1	0	1	0	0	Divide offset	1 byte
12	PASET	0	1	0	0	1	1	1	0	1	0	1	Page address set	1 byte
13	PDNOR	0	1	0	0	1	1	0	1	0	1	0	Page direction normal	None
14	PDINV	0	1	0	0	1	1	0	1	0	1	1	Page direction inverse	None
15	CASET	0	1	0	0	0	0	1	0	1	0	1	Column address set	2 byte
16	CAINC	0	1	0	0	1	0	1	1	0	1	0	Column address increment	None
17	CADEC	0	1	0	0	1	0	1	1	0	1	1	Column address decrement	None
18	PDIR	0	1	0	0	1	0	0	1	0	1	0	Page direction scan	None
19	CDIR	0	1	0	0	1	0	0	1	0	1	1	Column direction scan	None
20	MWRITE	0	1	0	0	1	0	1	1	1	0	0	Memory write	Data
21	CNTCLR	0	1	0	0	1	0	1	0	1	1	0	Counter clear	None
22	PCCLR	0	1	0	0	0	0	0	1	0	1	0	Page counter clear	None
23	CCCLR	0	1	0	0	0	0	0	0	1	0	1	Column counter clear	None
24	CKSET	0	1	0	1	0	1	1	1	1	1	1	Clock divide set	1 byte
25	RETURN	0	1	0	1	0	1	1	1	1	1	0	Return	None
26	VOLRD	0	1	0	1	0	1	1	0	1	1	0	Output port set read	1 byte
27	STREAD	0	0	1									Status read	

Command Details

The SED1590 identifies the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$). The command interpretation and execution is performed based entirely on internal timing without relying on any external clock.
In the 80×86 MPU interface, a low pulse is sent to the $\overline{WR}$ terminal to launch the command when writing. In the 68000 series MPU interface, a "L" input to the R/$\overline{W}$ terminal causes a write state, and then the commands are launched when a high pulse input is sent to the E terminal. Consequently, the 68000 series MPU interface is different from the 80x86 MPU interface in the command details and command tables, and in that the $\overline{RD}$ (E) terminal is "1" ("H") when performing status reads and when reading display data. The commands will be explained below using the 80×86 MPU interface in the examples.

Display ON/OFF Command: 1, Parameter:0

This command forces the entire display ON or OFF. When the display is OFF, all outputs are fixed at VC. Because the display is not possible when in sleep mode, make sure that this command is used after the sleep mode is turned OFF.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DON	0	1	0	1	0	1	0	1	1	1	1	Display ON
DOFF	0	1	0	1	0	1	0	1	1	1	0	Display OFF

Page Address Set Command: 1, Parameter: 1

This command and its following parameters makes it possible to set the page address corresponding to the low address when accessing the display data RAM from the MPU side. The desired bit of the display data RAM can be accessed by specifying the page address and the column address. The page addresses are 5 bits, corresponding to 30 pages (pages 0 to 29). Even if the page address changes, there is no change to the display status.
This command is input into the registers and loaded in the counters). That which is input is stored within the register, and can be reloaded by the PACLR command.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PASET	0	1	0	0	1	1	1	0	1	0	1	Page address set
Parameter	1	1	0				D	D	D	D	D	

Page Address Direction Command: 1, Parameter: 0

This command makes it possible to reverse the position of page 0 in the page address of the display RAM data. Consequently, it is possible to reverse the page address scan direction when the MPU uses the display data in the page direction. The relationship between the physical position in internal RAM and the page address is inverted:
Normal: 0 → 29
Reversed: 24 ← 0
When reversed, the final page address becomes 24. Consequently, the number of lines which can be indicated becomes upto 200.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PDNOR	0	1	0	0	1	1	0	1	0	1	0	Page direction normal
PDINV	0	1	0	0	1	1	0	1	0	1	1	Page direction inverted

Column Address Set Command: 1, Parameter: 2

This command and its following parameters make it possible to specify the column address when the MPU accesses display data RAM in the column direction. The desired bit of display data RAM can be accessed by specifying the page address and the column address. The column address has 10 bits, and when four of the chips are used in the column direction, up to 640 dots (pixels) are supported. Even when the address changes, the state of the display does not change. There are 640 columns (columns 0 to 639).
The address value is input with the less significant address 5 bit first and then the more significant 5 bit. With the less significant alone, when another command is entered, only the less significant is entered into the register, however, the counter is not loaded. When the less significant is followed by the more significant, they are loaded into the counter and the input is stored in the register. When the less significant address is followed by some other command, the counter will not be loaded and the command will be cancelled. With this command, the set values can be reloaded by the CCCLR command.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CASET	0	1	0	0	0	0	1	0	1	0	1	Column address set
Parameter 1	1	1	0				D	D	D	D	D	Lower 5 bits
Parameter 2	1	1	0				D	D	D	D	D	Upper 5 bits

Column Address Direction Command: 1, Parameters: 0

This command specifies the behavior of the column address counter (increment vs. decrement).
The address increments or decrements each time RAM accesses the display data. In the increment mode, the count operation stops when the value reaches 279H (639), or when the value reaches 000H (0) in the decrement mode.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CAINC	0	1	0	0	1	0	1	1	0	1	0	Column address increment
CADEC	0	1	0	0	1	0	1	1	0	1	1	Column address decrement

Scan Direction Select Command: 1, Parameter: 0

When the MPU continuously accesses display memory, this determines whether the scanning will be done in the page direction or in the column direction.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PDIR	0	1	0	0	1	0	0	1	0	1	0	Page direction scan
CDIR	0	1	0	0	1	0	0	1	0	1	1	Column direction scan

Display Data Write Command: 1, Parameter: Number of data to be written

When the MPU writes data to the memory, this command places the chip in a data entry mode. By writing data again after this command, the display data RAM contents can be changed. The data write mode is cleared automatically when another command is entered.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
MWRITE	0	1	0	0	1	0	1	1	1	0	0	Memory write
Parameter	1	1	0	D	D	D	D	D	D	D	D	Write data

Status Read

This read operation makes it possible to monitor the internal operating status of the SED1590.
No other command except for the status read command will be accepted with a RAM busy state (1). If the cycle time is followed, then there is no need to check for the RAM busy state under normal use.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
STREAD	0	0	1	O	O	O	O	O	O	O	O	Status

D7: Busy/Ready — Busy: 1, Ready: 0
D6: Page Address Direction — Normal: 1, Inverted: 0
D5: Column Address Direction — Normal: 1, Inverted:0
D4: Increment Direction — Column: 0, Page: 1
D3: Display ON/OFF — Off: 1, On: 0
D2: SLEEP ON/OFF — Off: 0, On: 1
D1: INVERT — Normal Display: 1, Invert Display: 0
D0: Reserved terminal

Display Normal/Inverted Command: 1, Parameter:0

This command makes it possible to inert the ON/OFF status of each point on the display without having to rewrite the contents of the display data RAM. Because all points in the display are either set to the normal display or reverse, partial inversions are not supported.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Display normal
DISINV	0	1	0	1	0	1	0	0	1	1	1	Display inverted

Duty Set Command: 1, Parameter: 1

This command combined with the following paramenter sets the duty.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DTYSET	0	1	0	1	0	1	0	1	0	0	0	Duty set
Parameter	1	1	0			D	D	D	D	D	D	(Number of display lines)/ 4/1
Example: 1/200 duty	1	1	0	0	0	1	1	0	0	0	1	
Example: 1/240 duty	1	1	0	0	0	1	1	1	0	1	1	

Sleep Mode On/Off Command: 1, Parameter:0

This command controls the sleep mode of the LCD module. Before launching this command, be sure that the Display OFF command has been entered and that the display is in an OFF state. Moreover, after issuing the Sleep OFF command, be sure to maintain the logic power supply for 40 ms to discharge the load of the power supply IC.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
SLPON	0	1	0	1	0	0	1	0	1	0	1	Sleep ON
SLPOFF	0	1	0	1	0	0	1	0	1	0	0	Sleep OFF

Line Inverse Number Set Tab Command: 1, Parameter: 1

This command controls the number of lines inverted in the LCD module.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
LINSET	0	1	0	1	1	0	0	1	0	1	0	FR inverse set
Parameter	1	1	0					D	D	D	D	FR inverse set value

The default value is being set to 11H inverse. (D3 to D0 = 1010)

Pattern Set Command: 1, Parameter: 1

This command controls the MLS pattern switching interval.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
PATSET	0	1	0	1	1	0	0	1	1	0	0	Drive pattern set
Parameter	1	1	0							D	D	Drive pattern set value

The correspondence between the input data and the switching interval is as follows:
(The default value will be set to 8H.)

	8H	4H	16H	Field
D0:	0	1	0	1
D1:	0	0	1	1

Output Port Control Command: 1, Parameter: 1

This command sets 5 bit data to control the LCD power supply.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
VOLCTL	0	1	0	1	1	0	0	0	1	1	0	Output port control
Parameter	1	1	0				D	D	D	D	D	Output port control value

D0: COD 0 D1: COD 1
D2: COD 2 D3: COD 3
D4: COD 4

Partition DOFF Set Command: 1, Parameter: 1

This command controls the LCD module display on/off for each driver.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
DVDSET	0	1	0	1	0	1	1	0	1	0	0	Partition offset
Parameter	1	1	0					D	D	D	D	Partition offset set value

D= “1”: Display ON D = “0”: Display OFF
(LR1, LR0): (0, 0) → D0; (0,1) → D1; (1, 0) → D2; (1,1) → D3

Initialize Command: 1, Parameter: 0

These commands clear the contents of the page counter, the page register, the column counter, and the column register to 0.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CNTCLR	0	1	0	0	1	0	1	0	1	1	0	Counter clear
PCCLR	0	1	0	0	0	0	0	1	0	1	0	Page counter clear
CCCLR	0	1	0	0	0	0	0	0	1	0	1	Column counter clear

CNTCLR: Resets the page counter and register to 0, and the column counter and register to 0.

PACLR: Loads the register value to the page counter.

CACLR: Loads the register value to the column counter.

Clock Divide Set Command: 1, Parameter: 1

This command sets the CL division ratio that serves as the basis for the timing signal for the liquid crystal display.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
CKSET	0	1	0	1	0	1	1	1	1	1	1	Clock division set
Parameter	1	1	0							D	D	Clock division set value

Correspondence of Divider Ratios

		2	1	4	8
Data	D1:	0	0	1	1
	D0:	0	1	0	1

Return Command: 1, Parameter: 0

This command sets the scan direction counter to the set value, and increments (+1) the counter in the fixed direction.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
RETURN	0	1	0	1	0	1	1	1	1	1	0	Address return

Output Port Setting Read Command: 1

This command reads the output port set bit to the data bus. Perform a read operation after this command is input. Only the master chip gives an output.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
VOLRD	0	1	0	1	0	1	1	0	1	1	0	Output port set read
Parameter	1	0	1				O	O	O	O	O	

NOP (Non-operating) Command: 1, Parameter: 0

This command has no effect on operations.

Command Name	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP1	0	1	0	0	0	1	0	0	1	0	1	NOP
NOP2	0	1	0	0	1	0	0	0	1	0	0	NOP

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Signal	Rated Value	Units
Power supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Power supply voltage (2)	V_{EE}	–8.0 to +0.3	V
Power supply voltage (3)	V3, V2, VC, –V2, –V3	V_{EE} to +0.3	V
Input voltage	V_{IN}	V_{SS} –0.3 to +0.3	V
Output voltage	V_{OUT}	V_{SS} –0.3 to +0.3	V
Operating temperature	Topr	–20 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

Note 1: The voltages are all relative to V_{DD} = 0V.

Note 2: Storage temperature 1 is the storage temperature for the bare chip or the plastic chip package products, and storage temperature 2 is the specification for the TCP packaged product.

Note 3: Be sure that the relationships between voltages V3, V2, VC, –V2, –V3 are always such that $V_{DD} \geq V3 > V2 > VC > -V2 > -V3 \geq V_{EE}$.

Note 4: This LSI chip may be permanently damaged if the LSI chip is used in conditions exceeding the absolute maximum ratings. Furthermore, it is desirable to always operate the LSI chip within these electrical characteristic conditions, not only may the LSI chip malfunction if these conditions are exceeded, but there will be adverse effects on the reliability of the LSI chip.

DC Characteristics

Unless otherwise stated, V_{DD} = V3 = 0V, V_{SS} = –3.0V, V_{EE} = –V3 = –6.0V, V2 = –1.5V, V_C = –3.0, –V2 = –4.5V

Item	Symbol	Parameter	Min	Typ	Max	Units	Corresponding Terminal
Power supply voltage (1)	V_{SS}		–3.6	–3.0	–2.7	V	V_{SS}
Power supply voltage (2)	V_{EE}		–7.2	–6.0	–5.4	V	V_{EE}
Power supply voltage (3)	V3				V_{DD}	V	V3
Power supply voltage (4)	V2			0.25 V_{EE}		V	V2
Power supply voltage (5)	VC			0.50 V_{EE}		V	VC
Power supply voltage (6)	–V2			0.75 V_{EE}		V	–V2
Power supply voltage (7)	–V3		V_{EE}			V	–V3
High-level input voltage	V_{IHC}		0.3V_{SS}	—	V_{DD}	V	*1
Low-level input voltage	V_{ILC}		V_{SS}	—	0.7 V_{SS}	V	*1
High-level output voltage	V_{OH}	I_{OH} = –0.6mA	V_{DD}–0.4	—	V_{DD}	V	*2
Low-level output voltage	V_{OL}	I_{OL} = +0.6mA	V_{SS}	—	V_{SS}+0.4	V	*2
Schmidt high-level input voltage	V_{IHS}		0.3V_{SS}	—	V_{DD}	V	$\overline{RES}$
Schmidt low-level input voltage	V_{ILS}		V_{SS}	—	0.7V_{SS}	V	$\overline{RES}$
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	5.0	µA	*3
Input/output leakage current	$I_{LI/O}$	V_{IN}=V_{DD}, V_{SS}	—	—	5.0	µA	*4
Driver output resistance	R_{ON}	V_{SS} = –3.0V, V_{EE} = –6.0V V3 = 0V, V2 = –1.5V VC = –3.0V –V2 = –4.5V –V3 = –6.0V, ∆ V = 0.5V	—	0.6	1.0	kΩ	O1~ O160
Static consumption current	I_{SSQ}	V_{IN} = V_{DD} or V_{SS}	—	—	5	µA	V_{SS}
Static consumption current	I_{EEQ}	V_{EE} = –6.0V	—	—	5	µA	V_{EE}
Dynamic consumption current	I_{SSOP1}	MPU access *6	—	1.5	2.0	µA	V_{SS}
Dynamic consumption current	I_{SSOP2}	MPU no access *6	—	90	130	µA	V_{SS}
Dynamic consumption current	I_{EEOP}	V_{EE} = –6.0V	—	12	20	µA	V_{EE}
Input terminal capacitance	CI	Freq. = 1MHz Ta = 25°C IC alone	—	—	8	pF	*3
Input/output terminal capacitance	CI/O		—	—	15	pF	*4
Output terminal capacitance	CO		—	—	7	pF	$\overline{SLP}$
Oscillator frequency	Ifosc	Ta = 25°C	—	24	—	kHz	*5

DC Characteristics: Supplemental Explanation for Corresponding Terminals

*1 •Input terminals: A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0, and LR1.
•Input/output terminals (Input mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1 and F2.

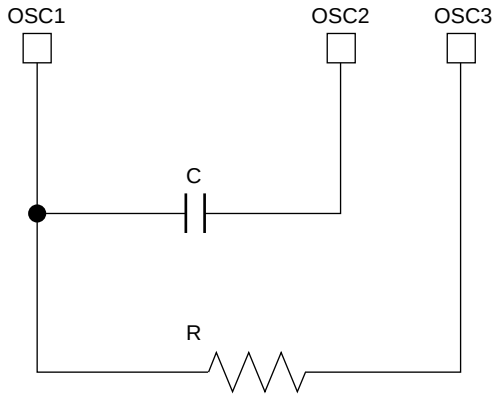
*2 •Input/output terminals (Output mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, F1, and F2.
•Output terminals: OSC2, OSC3, and $\overline{SLP}$

*3 •Input terminals: A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, C86, OSC1, M/S, LR0, and LR1.

*4 •Input/Output terminals (Input mode): D[0:7], CL, FR, CA, $\overline{DOFF}$, $\overline{SLP}$, F1, and F2.

*5 •Local oscillator circuit depending on CR.

*6 •Frame frequency = 60 Hz, Duty = 1/200 and CR oscillation 24 kHz should be split into two-divisions when used.
•Adjust the "C" to C = 100 pF and adjust the R to 24 kHz, using a variable resistor.
•Access of the MPU will be made by continuous writing of the indicated data within the cycle time of 1,333 ns (750 kHz).
•The indicated data will appear in black or white in units of 4 lines each, repetitively.

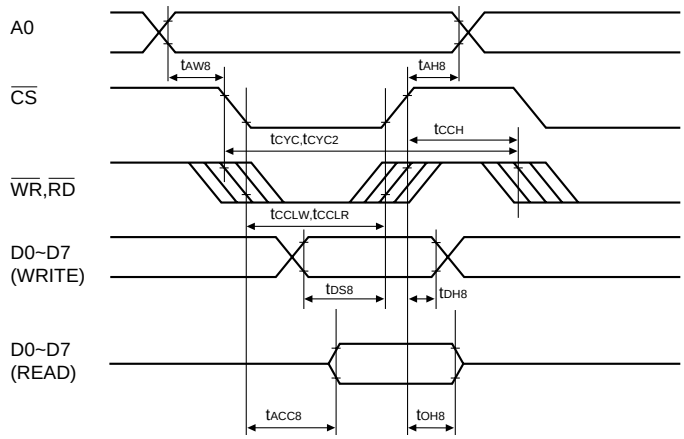


Oscillating frequency: $f \fallingdotseq 1/(2.2\ CR)$

AC Characteristics

The System Bus

Read/Write Characteristics I (80×86 Series MPUs)



[Ta = –20 to 85°C, VSS = –3.0 to –3.6V]

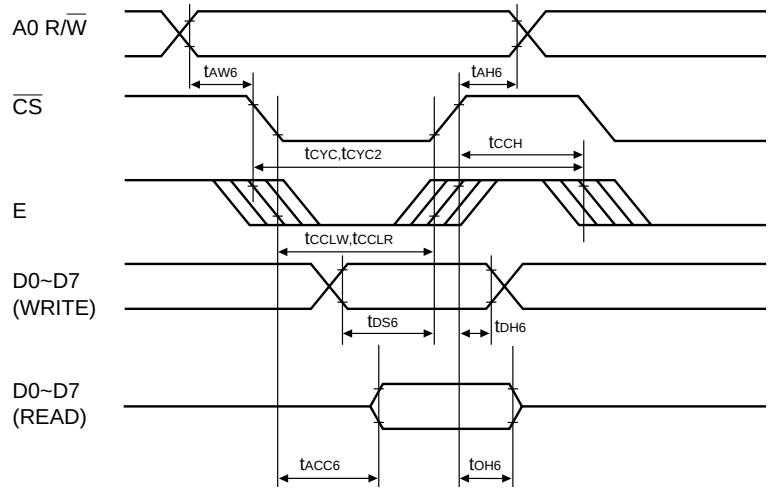
Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0	t_{AH8}	Address hold time	5	—	ns	
	t_{AW8}	Address setup time	5	—	ns	
WR, RD	t_{CYC}	Write cycle	1300	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	300	—	ns	
	t_{CCH}	Duration of the control pulse “H”	600	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	50	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	140	—	ns	
D0 to D7	t_{DS8}	Data setup time	35	—	ns	CL = 100 pF
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	140	ns	
	t_{OH8}	Output disable time	30	90	ns	

[Ta = –20 to 85°C, VSS = –2.7 to –3.0V]

Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0	t_{AH8}	Address hold time	5	—	ns	
	t_{AW8}	Address setup time	5	—	ns	
WR, RD	t_{CYC}	Write cycle	1600	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	350	—	ns	
	t_{CCH}	Duration of the control pulse “H”	900	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	70	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	160	—	ns	
D0 to D7	t_{DS8}	Data setup time	50	—	ns	CL = 100 pF
	t_{DH8}	Data hold time	5	—	ns	
	t_{ACC8}	Read access time	—	160	ns	
	t_{OH8}	Output disable time	40	110	ns	

- The timing for the input signal rising edge and the input signal falling edge (t_r, t_f) is specified at 15 ns or less.
- All timings are specified based on 20% or 80% $V_{DD} – V_{SS}$.
- The “t_{CCLW}” and “t_{CCLR}” are being specified depending on the overlap period where the $\overline{CS}$ is being on the “L” level and the $\overline{WR}$, $\overline{RD}$ are being on the “L” level.
- These specifications guarantee writing into the RAM of the indicated data, output port reading and status reading only.

Read/Write Characteristics II (68000 Series MPUs)



[Ta = –20 to 85°C, V_{SS} = –3.0 to –3.6V]

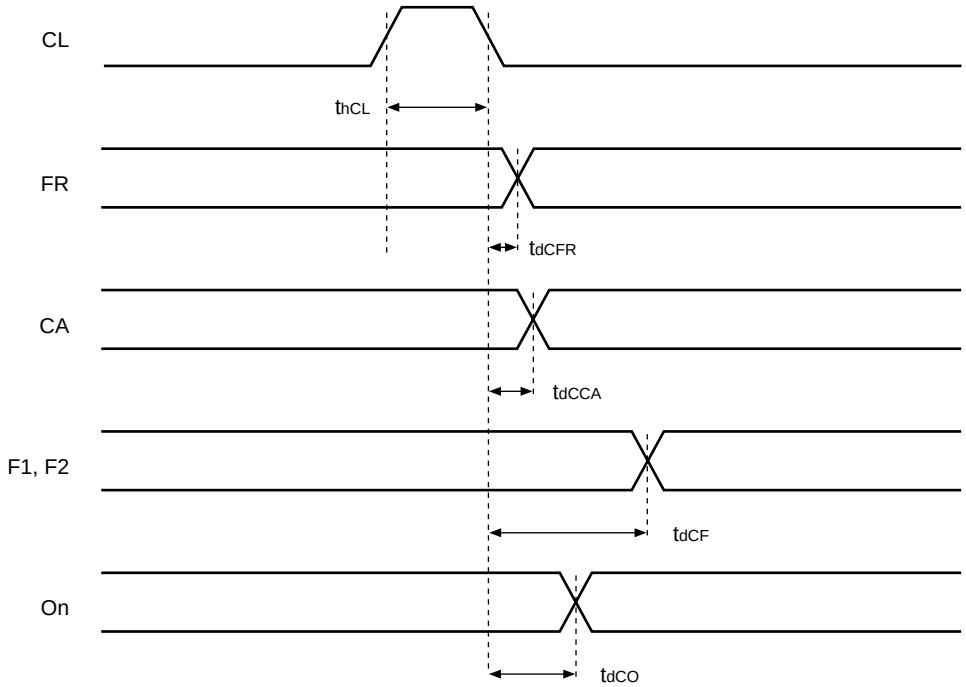
Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0, R/W	t_{AH6}	Address hold time	5	—	ns	
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1300	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	300	—	ns	
	t_{CCH}	Duration of the control pulse “H”	600	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	50	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	140	—	ns	
D0 to D7	t_{DS6}	Data setup time	35	—	ns	CL = 100 pF
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	140	ns	
	t_{OH6}	Output disable time	30	90	ns	

[Ta = –20 to 85°C, V_{SS} = –2.7 to –3.0V]

Signal	Symbol	Parameter	Min	Max	Units	Measurement Conditions
A0, R/W	t_{AH6}	Address hold time	5	—	ns	
	t_{AW6}	Address setup time	5	—	ns	
E	t_{CYC}	Write cycle	1600	—	ns	
	t_{CYC2}	Read cycle (Status read, output port read)	350	—	ns	
	t_{CCH}	Duration of the control pulse “H”	900	—	ns	
	t_{CCLW}	Duration of the control pulse “L” (WR)	70	—	ns	
	t_{CCLR}	Duration of the control pulse “L” (RD)	160	—	ns	
D0 to D7	t_{DS6}	Data setup time	50	—	ns	CL = 100 pF
	t_{DH6}	Data hold time	5	—	ns	
	t_{ACC6}	Read access time	—	160	ns	
	t_{OH6}	Output disable time	40	110	ns	

- The timing for the input signal rising edge and the input signal falling edge (t_r, t_f) is specified at 15 ns or less.
- All timings are specified based on 20% or 80% V_{DD} – V_{SS}.
- The “t_{CCLW}” and “t_{CCLR}” are being specified depending on the overlap period where the $\overline{CS}$ is being on the “L” level and the $\overline{WR}$, $\overline{RD}$ are being on the “L” level.
- These specifications guarantee writing into the RAM of the indicated data, output port reading and status reading only.

Output Timing Characteristics



[Ta = –20 to 85°C, V_{SS} = –2.7 to –3.6V]

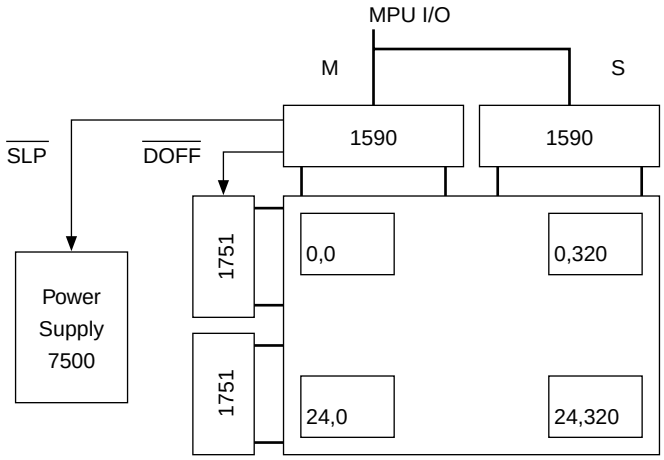
Signal	Symbol	Parameter	Min	Typ	Max	Units	Measurement Conditions
CL	t_{dCL}	CL pulse width	100	—	1000	ns	CL = 100 pF
FR	t_{dCFR}	FR output delay	10	—	1000	ns	
CA	t_{dCCA}	CA output delay	10	—	1000	ns	
F1, F2	t_{dCF}	F1, F2 output delay	10	—	1000	ns	
On	t_{dCO}	ON output delay	—	—	500	ns	

EXAMPLE OF USE

The use of the commands will be explained based on actual examples of use.

Assuming 1/200 Duty (200-line Display)

X driver: SED 1590, Y Driver: SED 1751
Power supply: $\overline{SLP}$ is input to the $\overline{SLP}$ terminal of the SCI7500



Address (24, 320) is written with the page address first followed by the column address. The page is 24, and because processing is performed in 1 byte units, $30 \times 8 = 200$ line displays.

Example of Actual Use

The Power-up Process

Turn on the system power supply (V_{CC}).
↓
Do not neglect the power-on reset.
At the time of reset the default values will be as follows:

Sleep status:	Sleep status
DON/DOFF status:	DOFF Status
(The divider OFF has not been applied.)	
Display normal/reversed:	Normal
Duty:	1/240 (set to 240 lines)
Non-display interval:	0 selected intervals
FR period:	Each 11 selected intervals
Page address register:	00.H
Column address register:	000.H
Page address direction:	Forward direction
Column address direction:	Increment
Scanning direction:	Column direction
MLS pattern:	Changes at each 8 selected intervals
Power supply control bit:	00.H
Clock 2 divider:	0.H

↓
Input commands for the settings to be changed
Example: Change the duty
Reverse the scan direction
Set the scaning direction to the page direction
Set the non-display interval
↓
Sleep off
↓
Display Data input
Example: Write Start
Write data input
↓ 1 line's worth
Return command
Repeat for the number of lines to be displayed.
↓
Display ON (at least 40 ms after the sleep was released).
↓
Rewrite only a portion of the display contents.
Example: Page address set
Column address set
Write start
Write data input
↓ The amount to be rewritten
Return command
Repeat for the number of lines to be displayed.
↓
Read the part where there is content displayed.
Example: Page address set
Column address set
Read start
Data read
↓ The amount to be read
Return command
Repeat for the number of lines to be displayed.
↓

Reverse the display contents
Example: Page address set
Column address set
Read-modify-write start
↓ The amount to be rewritten
Return command
Repeat for the number of times to modify lines
↓
Display off.
↓
Change settings
Rewrite all display data
Example: Initialize command (CNTCLR) input
Write start
Write data input
↓ The amount to be rewritten
Return command
Repeat for the number of lines to be rewritten.
↓
Display ON
↓
Display OFF
↓
Sleep on
↓ Hold the power supply for 10 ms
Power supply OFF (V_{DD}, V_{SS})

Notes and Cautions:
1) When rewriting all data, do it with the display OFF.
2) Even when partial data is rewritten, do not continually rewrite the same area many times within a single frame interval (i.e. if the display is at 60 Hz, 16.6 mS).
3) Follow the specified sequences when turning the display ON and OFF.
4) Only the following three commands will affect the display because of noise:
   1. Display ON/OFF
   2. Display normal/inverted
   3. Sleep ON/OFF

If there is noise regardless of efforts, periodically insert the above three commands.
When entering data, set the address to start the data entry without using the return command.

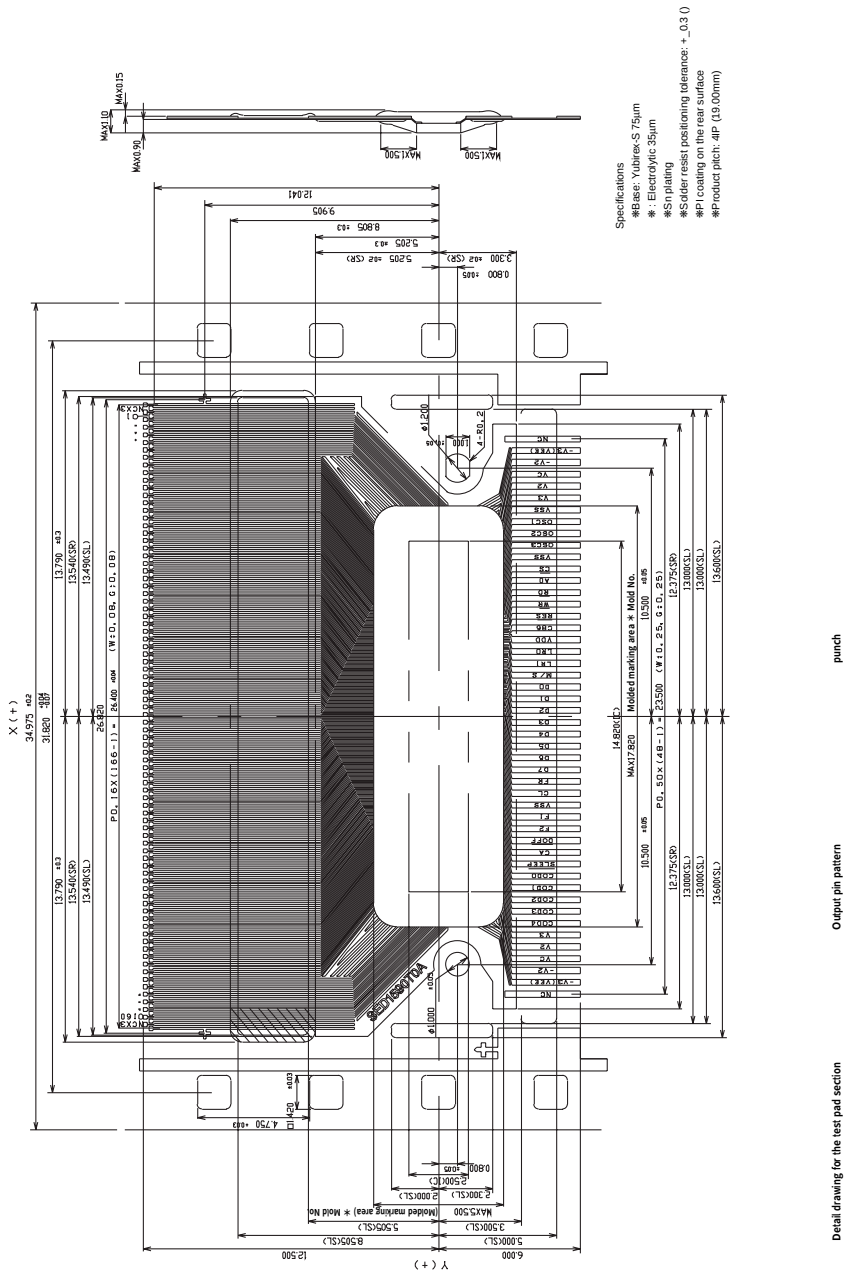
Notes

Be aware of the following when using these development specifications:
1. To facilitate improvements, the contents of these development specifications are subject to change without notice.
2. These development specifications neither guarantee the execution of industrial property rights or other authorities, nor grant execution authorities.

The examples of application found in these development specifications are strictly to assist in the understanding of this product; be aware that we assume absolutely no responsibility for problems in circuits wherein these examples are used.
Pay attention to the following precautions when using the SED1590 Series devices.

[Use When Exposed to Light]
The properties of semiconducting elements change when exposed to light because of the same principle used in everyday solar cells. Thus, exposure to light may cause this IC to malfunction.
(1) Design and package the actual application of the IC in a structure eliminates light.
(2) In test processes, design and package this IC in a structure that eliminates light.
(3) When eliminating light from the IC, eliminate light from the front surface, side surfaces, and back surface of the IC.

[Precautions against external noise, etc.]
(1) Although the SED1590 Series devices can preserve and store the operation status and the indicated data, excessive external noise may force to change the internal status. Consequently, take necessary measures to suppress noise or to avoid influences of the noise when designing their package or when designing a system using them.
(2) We recommend you to program a software which works to refresh the operation statuses (such as re-setting of the commands and re-transference of the indicated data) periodically to deal with occurrences of the sudden noise.


Specifications
*Base: Yubirex-S 75µm
*: Electrolytic 35µm
*Sn plating
*Solder resist positioning tolerance: +_0.3 ()
*PI coating on the rear surface
*Product pitch: 4IP (19.00mm)
Molded marking area * Mod No.
Output pin pattern
punch
Detail drawing for the test pad section
SED1590D0A
X (+)
Y (+)