SED1750

Contents

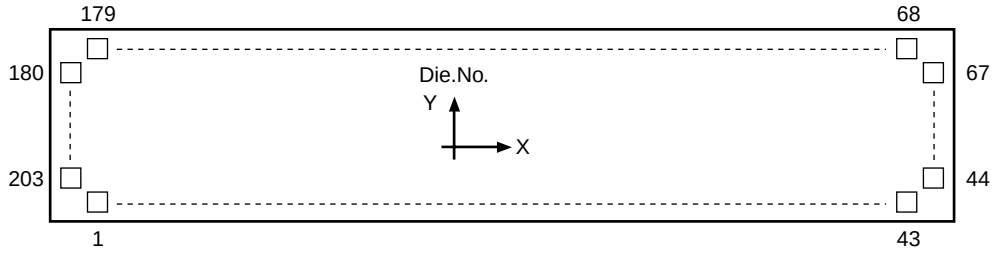
OVERVIEW

The SED1750 is an MLS (Multi Line Selection) driving, 160 output, triple-value low resistance common (low) driver which can realize high picture quality and high speed responses.
Receiving signals from an LCD controller such as the SED1335 or SED1351, it works to make 4-line MLS drives in combination with the SED1580 or in combination with the SED1590 receiving signals direct from the MPU. Employing the SCI7500 as the power IC, the power to use for the MLS drive liquid crystal display system can be prepared easily.
Adopting a slim chip shape which is more advantageous to realize narrower borders with the LCD panels, the SED1750 is capable of making low voltage logic power operations and is applicable to a wide range of applications.
Owing to its pad layout designed to facilitate its installation to the substrate and thanks to its two-way choices of the driver output sequence, the highest working efficiency can be acquired with a 1/160 or 1/320 duty panel.

Features

- LCD driver outputs 160
- Low output ON resistance
- High duty drive supported ..... 1/320 (Reference value)
- Broad range of LC drive voltages ..... + 14 to + 42 V (V_{CC} = 2.7 to 5.5 V)
- Output shift direction pin select is possible
- Can be switched between 140 and 160 outputs
- Non-biased display OFF function
- Logic system power source ..... 2.7 V to 5.5 V
- LC power source offset bias can be adjusted relative to the V_{DDH} and GND levels
- Slim chip shape
- D_{0B} ..... Au Bump die
- T_{0A} ..... TCP

Pad Layout



Chip size	15.62 mm × 2.47 mm
Pad pitch	80 μm (Min.)
Chip thickness	525 μm ± 25 μm

1) Au Bump Specifications (SED1750D_{0B}) Reference Values Only
Au vertical bump
Parallel to Scribe × Perpendicular to Scribe ± Tolerance

Bump Size A	60 μm × 75 μm ± 4 mm (Pad No. 1 to 43, 68 to 179)
Bump Size B	80 μm × 50 μm ± 4 mm (Pad No. 44 to 67, 180 to 203)
Bump height	17 to 28 μm (The details specified in the acceptance specifications.)

Pad Coordinates

Units: µm

Pin	Name	X	Y
1	V_{DDH}	-7522	-1045
2	+V1	-7427	
3	VC	-7332	
4	-V1	-7237	
5	V_{SS}	-7142	
6	SHL	-6804	
7	SEL	-6579	
8	V_{CC}	-6241	
9	LSEL	-5902	
10	DOFF	-5538	
11	FR	-4791	
12	DM	-4323	
13	DM	-3943	
14	DM	-3563	
15	DM	-3183	
16	DM	-2803	
17	CSEL	-2336	
18	LP	-1998	
19	DM	-1162	
20	CIO2	-755	
21	DM	-347	
22	DM	0	
23	DM	347	
24	CIO1	755	
25	DM	1162	
26	YD	1998	
27	DM	2336	
28	DM	2803	
29	DM	3183	
30	DM	3563	
31	DM	3943	
32	DM	4323	
33	DM	4791	
34	DM	5538	
35	F1	5902	
36	DM	6241	
37	F2	6579	
38	TEST1	6804	
39	V_{SS}	7142	
40	-V1	7237	
41	VC	7332	
42	+V1	7427	
43	V_{DDH}	7522	
44	COM1	7655	-935
45	COM2		-855
46	COM3		-775
47	COM4		-695
48	COM5		-615
49	COM6		-535
50	COM7		-455
51	COM8	7655	-375
52	COM9		-295
53	COM10		-215
54	COM11		-135
55	COM12		-55
56	COM13		25
57	COM14		105
58	COM15		185
59	COM16		265
60	COM17		345
61	COM18		425
62	COM19		505
63	COM20		585
64	COM21		665
65	COM22		745
66	COM23		825
67	COM24		905
68	COM25	7419.3	1083
69	COM26	7285.6	
70	COM27	7152	
71	COM28	7018.3	
72	COM29	6884.7	
73	COM30	6751	
74	COM31	6617.3	
75	COM32	6483.7	
76	COM33	6350	
77	COM34	6216.3	
78	COM35	6082.7	
79	COM36	5949	
80	COM37	5815.3	
81	COM38	5681.7	
82	COM39	5548	
83	COM40	5414.3	
84	COM41	5280.7	
85	COM42	5147	
86	COM43	5013.3	
87	COM44	4879.7	
88	COM45	4746	
89	COM46	4612.3	
90	COM47	4478.7	
91	COM48	4345	
92	COM49	4211.4	
93	COM50	4077.7	
94	COM51	3944	
95	COM52	3810.4	
96	COM53	3676.7	
97	COM54	3543	
98	COM55	3409.4	
99	COM56	3275.7	
100	COM57	3142	
101	COM58	3008.4	1083
102	COM59	2874.7	
103	COM60	2741	
104	COM61	2607.4	
105	COM62	2473.7	
106	COM63	2340	
107	COM64	2206.4	
108	COM65	2072.7	
109	COM66	1939	
110	COM67	1805.4	
111	COM68	1671.7	
112	COM69	1538.1	
113	COM70	1404.4	
114	COM71	1270.7	
115	COM72	1137.1	
116	COM73	1003.4	
117	COM74	869.7	
118	COM75	736.1	
119	COM76	602.4	
120	COM77	468.7	
121	COM78	335.1	
122	COM79	201.4	
123	COM80	67.7	
124	COM81	-67.7	
125	COM82	-201.4	
126	COM83	-335.1	
127	COM84	-468.7	
128	COM85	-602.4	
129	COM86	-736.1	
130	COM87	-869.7	
131	COM88	-1003.4	
132	COM89	-1137.1	
133	COM90	-1270.7	
134	COM91	-1404.4	
135	COM92	-1538.1	
136	COM93	-1671.7	
137	COM94	-1805.4	
138	COM95	-1939	
139	COM96	-2072.7	
140	COM97	-2206.4	
141	COM98	-2340	
142	COM99	-2473.7	
143	COM100	-2607.4	
144	COM101	-2741	
145	COM102	-2874.7	
146	COM103	-3008.4	
147	COM104	-3142	
148	COM105	-3275.7	
149	COM106	-3409.4	
150	COM107	-3543	

Pin	Name	X	Y
151	COM108	-3676.7	1083
152	COM109	-3810.4	
153	COM110	-3944	
154	COM111	-4077.7	
155	COM112	-4211.4	
156	COM113	-4345	
157	COM114	-4478.7	
158	COM115	-4612.3	
159	COM116	-4746	
160	COM117	-4879.7	
161	COM118	-5013.3	
162	COM119	-5147	
163	COM120	-5280.7	
164	COM121	-5414.3	
165	COM122	-5548	
166	COM123	-5681.7	
167	COM124	-5815.3	
168	COM125	-5949	

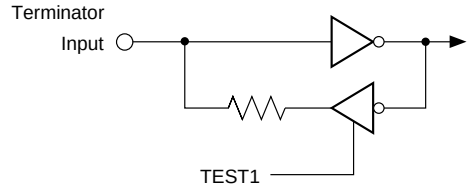
Pin	Name	X	Y
169	COM126	-6082.7	1083
170	COM127	-6216.3	
171	COM128	-6350	
172	COM129	-6483.7	
173	COM130	-6617.3	
174	COM131	-6751	
175	COM132	-6884.7	
176	COM133	-7018.3	
177	COM134	-7152	
178	COM135	-7285.6	
179	COM136	-7419.3	
180	COM137	-7655	905
181	COM138		825
182	COM139		745
183	COM140		665
184	COM141		585
185	COM142		505
186	COM143		425

Pin	Name	X	Y
187	COM144	-7655	345
188	COM145		265
189	COM146		185
190	COM147		105
191	COM148		25
192	COM149		-55
193	COM150		-135
194	COM151		-215
195	COM152		-295
196	COM153		-375
197	COM154		-455
198	COM155		-535
199	COM156		-615
200	COM157		-695
201	COM158		-775
202	COM159		-855
203	COM160		-935

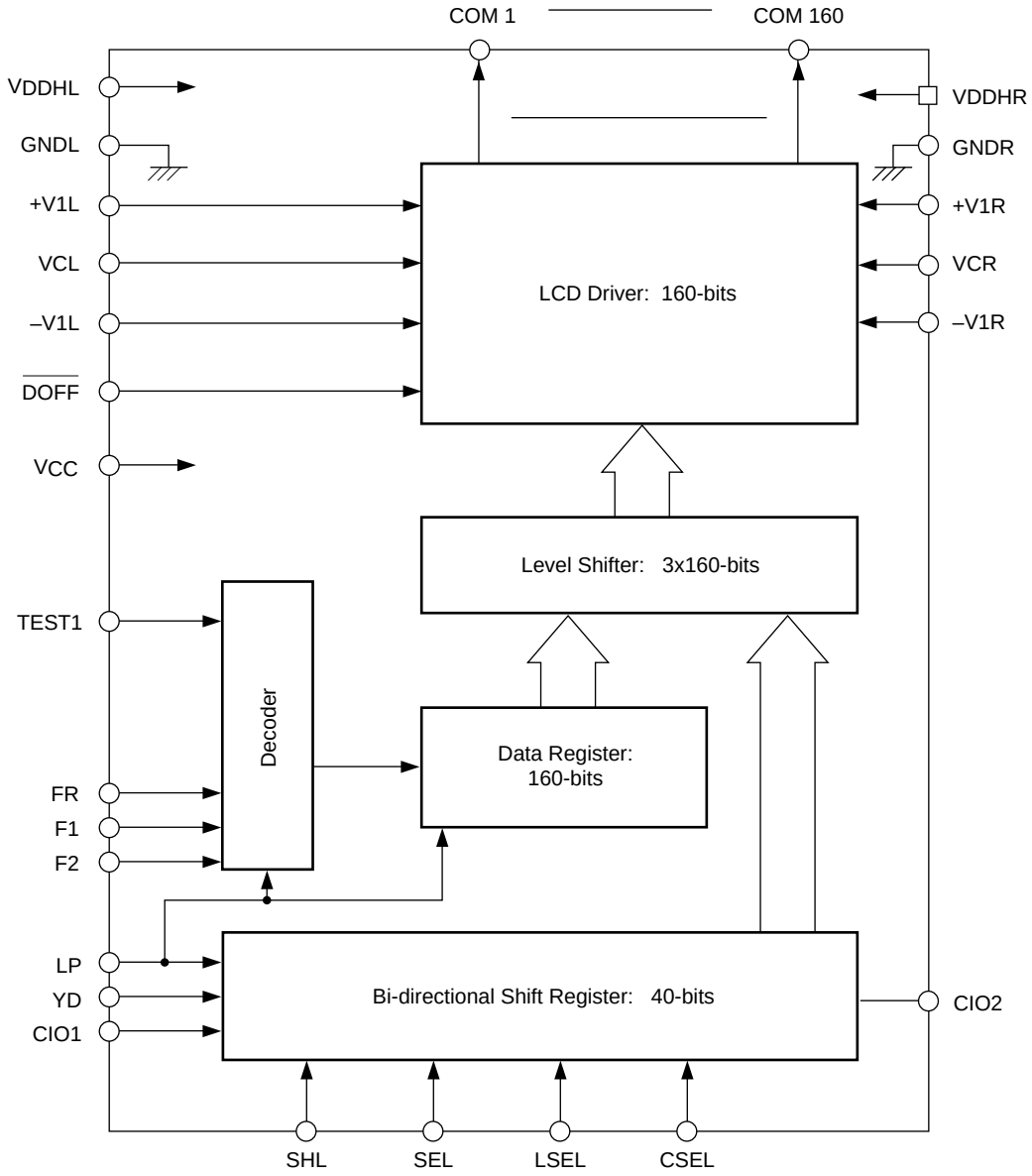
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Number of Terminals</th></tr>
<tr><td>COM1 to
COM160</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>160</td></tr>
<tr><td>CIO1
CIO2</td><td>I/O</td><td>Carry signal I/O.
This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of LP.</td><td>2</td></tr>
<tr><td>YD</td><td>I</td><td>Frame start/pulse input, with terminator. (*1)</td><td>1</td></tr>
<tr><td>F1, F2</td><td>I</td><td>Drive pattern select signal input, with terminator. (*1)</td><td>2</td></tr>
<tr><td>LP</td><td>I</td><td>Shift clock input for display data.
(Triggers on falling edge.) With terminator. (*1)</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and CIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th></th></tr>
<tr><th>CIO1</th><th>CIO2</th></tr>
<tr><td>L</td><td>1(9) → 160(148)</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>160(148) → 1(9)</td><td>Output</td><td>Input</td></tr>
</table>
The numbers in parentheses are for 140 output mode.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Select input for the number of COM output terminals:
160 outputs ←→ 140 outputs
L: COM1 to COM160
H: COM9 to COM148</td><td>1</td></tr>
<tr><td>LSEL</td><td>I</td><td>1/2 H operation select signal input.
L: Normal operation. H: 1/2 operation.</td><td>1</td></tr>
<tr><td>CSEL</td><td>I</td><td>Chip select signal input for when a cascade connection is used.
L: Leading chip
H: Other chips</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1)</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LC display blanking control input. With a low level input, all common outputs are temporarily set to the V_C level. The contents of the latches are maintained. With terminator (*1)</td><td>1</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test1 signal input. Normally tied at L.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL, GNDR</td><td>Power</td><td>Power source for logic:
GND: 0 V , V_{CC}: +2.7 to 5.5 V</td><td>3</td></tr>
<tr><td>V_{CL}, V_{CR}, $+V_{1L}$, $+V_{1R}$, $-V_{1L}$, $-V_{1R}$, V_{DDHL}, V_{DDHR}</td><td>Power</td><td>LC Drive Power:
GND: 0 V,
V_{DDH}: + 14.0 to 42.0 V, $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq$ GND</td><td>8</td></tr>
<tr><td>DM</td><td></td><td>Dummy pad</td><td>19</td></tr>
<tr><td></td><td></td><td>Total</td><td>203</td></tr>
</table>

Note: *1



Block Diagram



Explanation of Each Block

Shift Register

This is a bi-directional shift register used for transmitting common data. The display data shifts on the falling edge of LP.

Level Shifter

The level shifter is a voltage level converter circuit which converts the signal voltage level from a logic system level to the LC driver system voltage level.

LCD Driver

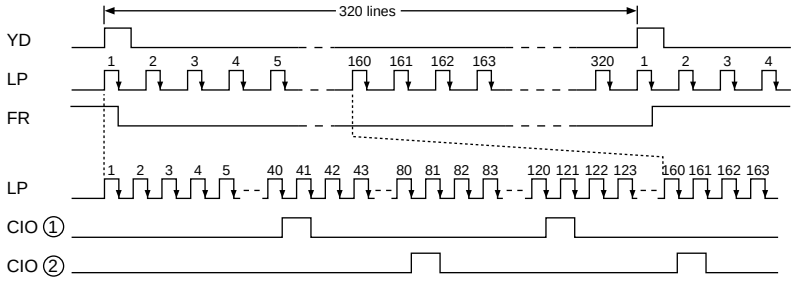
The LCD driver outputs the LC drive voltage.
The relationship between the display blanking signal $\overline{DOFF}$, the field recognition signals F1 & F2, the AC signal FR, and the common output voltage is as follows:

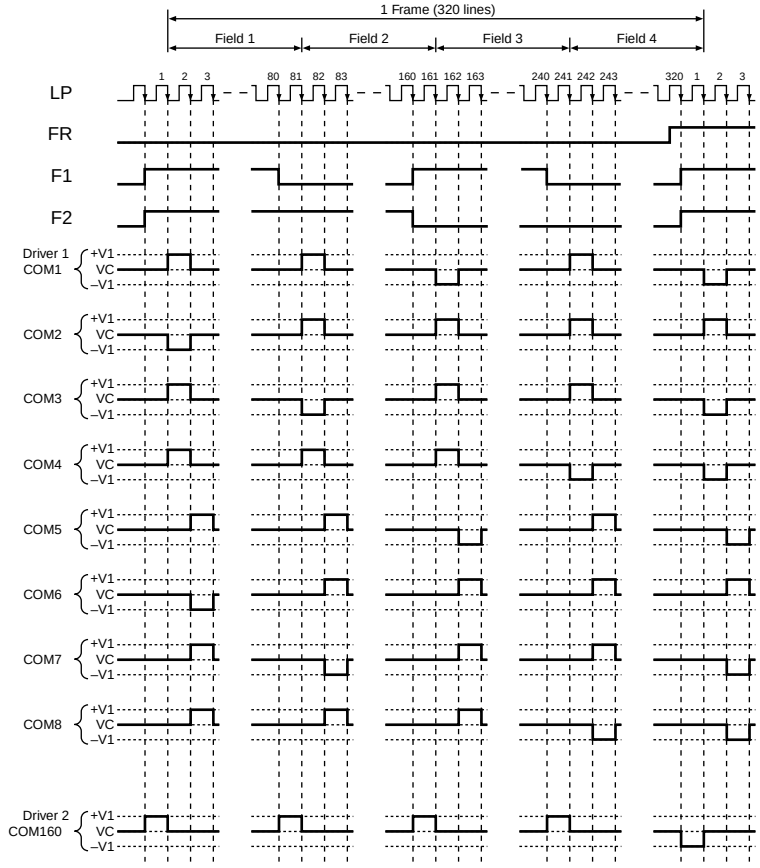
$\overline{DOFF}$	H								L
FR	L				H				—
F1,F2	1,1	0,1	1,0	0,0	1,1	0,1	1,0	0,0	—
Line 1	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	$+V_1$	$-V_1$	V_C
Line 2	$-V_1$	$+V_1$	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	V_C
Line 3	$+V_1$	$-V_1$	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	V_C
Line 4	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	$-V_1$	$+V_1$	V_C

Voltage level relationships: $+V_1 > V_C > -V_1$ (V_C is the center voltage level)

Timing Diagram (1)

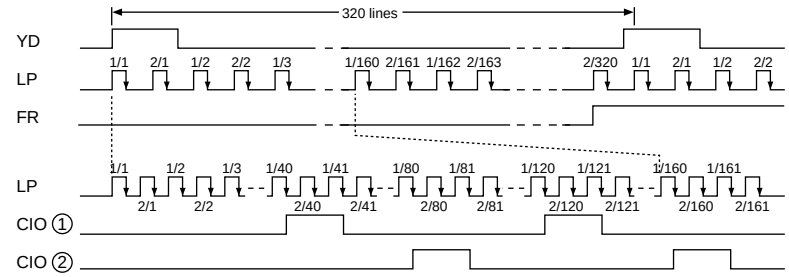
1/320 duty, normal operation.
SHL = L, SEL = L, LSEL = L, CSEL = L (This diagram provided only as a reference.)

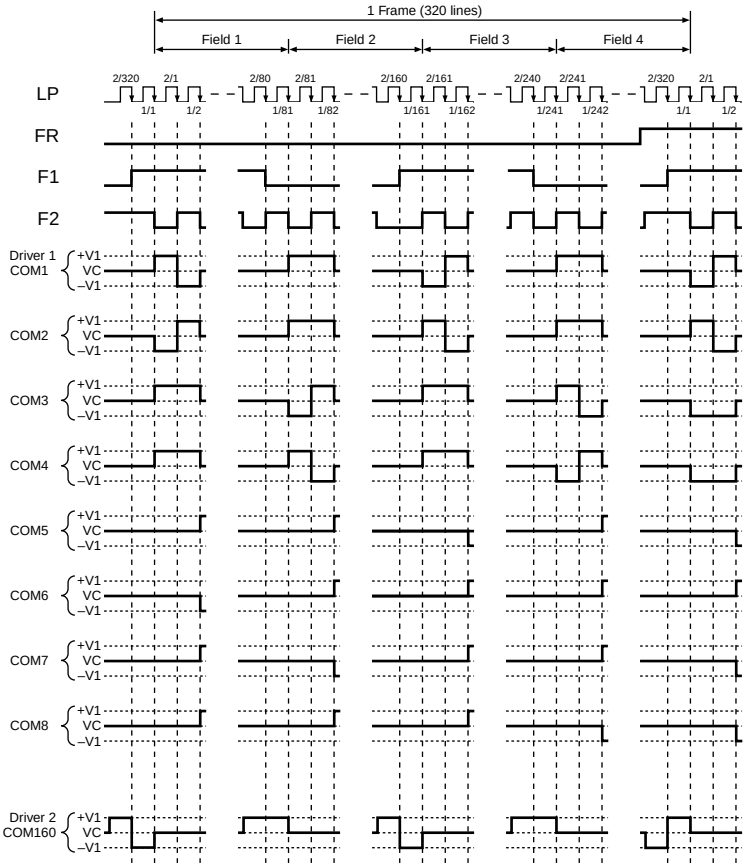




Timing Diagram (2)

1/320 duty, 1/2 H operation.
SHL = L, SEL = L, LSEL = H, CSEL = L (This diagram provided only as a reference.)

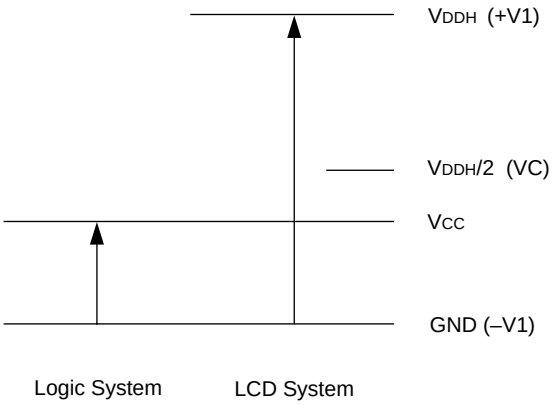




ABSOLUTE MAXIMUM RATINGS

Item	Signal	Rated Value	Units
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to + 45.0	V
Power voltage (3)	± V_1, V_C	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
CIO output current	I_{O1}	20	mA
Operating temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

NOTE 1: The voltages are all relative to GND = 0 V.
NOTE 2: Storage temperature 1 is for the chip alone, and storage temperature 2 is for the TCP product.
NOTE 3: Ensure that the relationship between $+V_1$, V_C, and $-V_1$ is always as follows: $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq GND$.



NOTE 4: The LSI may be permanently damaged if the logic system power is floating or V_{CC} is less than or equal to 2.6 V when power is applied to the LC drive system. Special caution must be paid to the power sequences during power up and power down.

Electrical Characteristics

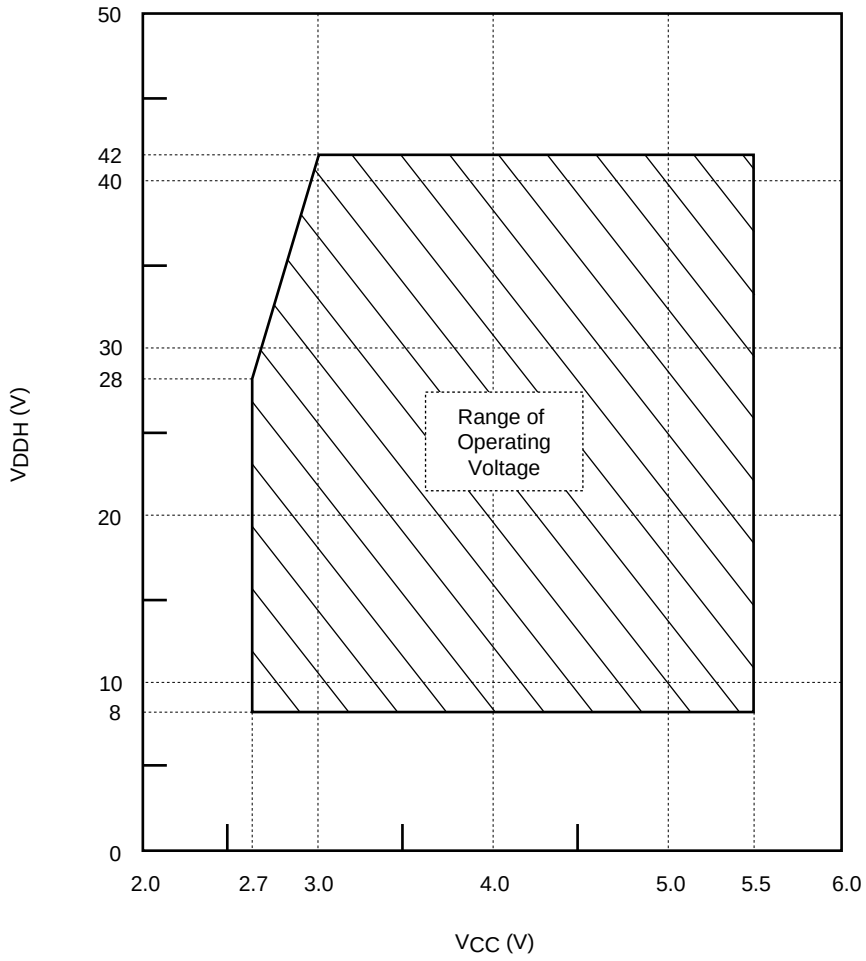
DC Characteristics

Unless otherwise noted, GND = 0 V, V_{CC} = + 5.0 V ± 10%, Ta = –30 to 85°C

Item	Signal	Parameter		Applicable Terminals	Min	Typ	Max	Unit
Power Supply Voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Range Operating Voltages	V_{DDH}	Function		V_{DDH}	8.0		42.0	V
Power Supply Voltage (2)	$+V_1$	Recommended Value		$+V_1$			V_{DDH}	V
Power Supply Voltage (3)	V_C	Recommended Value		V_C		$V_{DDH}/2$		V
Power Supply Voltage (4)	$–V_1$	Recommended Value		$–V_1$	GND			V
High-level Input Voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		CIO1,CIO2,FR, YD,LP,SHL,SEL, LSEL,CSEL, $\overline{DOFF}$,F1,F2, TEST1	0.8V_{CC}			V
Low-level Input Voltage	V_{IL}						0.2V_{CC}	V
High-level Output Voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	CIO1,CIO2	V_{CC}–0.4			V
Low-level Output Voltage	V_{OL}		I_{OL} = 0.3mA				0.4	V
Input Leakage Current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		LP,YD,SHL,SEL, LSEL,CSEL,F1, F2,$\overline{DOFF}$,TEST1, FR			2.0	µA
Input/Output Leakage Current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		CIO1,CIO2			5.0	µA
Static Current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND			25	µA
Output Resistance	R_{COM}	ΔVON = 0.5 V Recommended parameter	V_{DDH} = +30.0V	COM1 to COM120		0.55	0.7	kΩ
			V_{DDH} = +40.0V			0.5	0.7	
Average Operating Consumption Current (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC} V_{IL} = GND, f_{LP} = 22.4 kHz f_{FR} = 70 Hz, Input data: 1/320 No load		V_{CC}		12	25	µA
		V_{CC} = 3.0 V All other parameters the same as V_{CC} = 5.0 V.				8	17	
Average Operating Consumption Current (2)	I_{DDH}	V_{DDH} = $+V_1$ = +30.0 V, V_C = $V_{DDH}/2$, $–V_1$ = 0.0 V, V_{CC} = 5.0 V All other parameters the same as the I_{CC} item.		V_{DDH}		7	13	µA
Input Terminal Capacity	C_I	Freq. = 1 MHz Chip alone Ta = 25°C		LP,YD,SHL,SEL, LSEL,CSEL,F1,F2, $\overline{DOFF}$,TEST1,FR			10	pF
Input/Output Terminal Capacity	$C_{I/O}$			CIO1,CIO2			18	pF

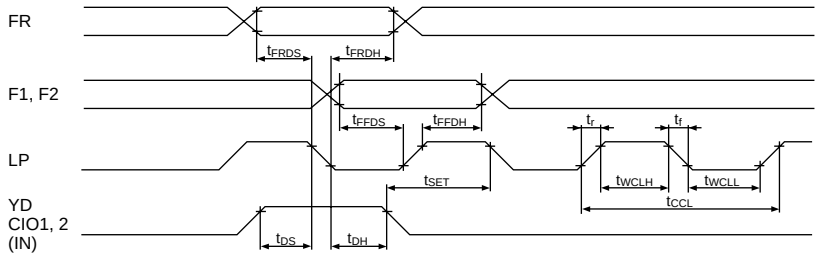
Range of Operating Voltages: V_{CC} – V_{DDH}

It is necessary to set the voltage for V_{DDH} within the V_{CC} – V_{DDH} operating voltage range shown in the diagram below.



AC Characteristics

Input Timing Characteristics



The FR latched at the nth LP is reflected in the output at the n+1th LP.

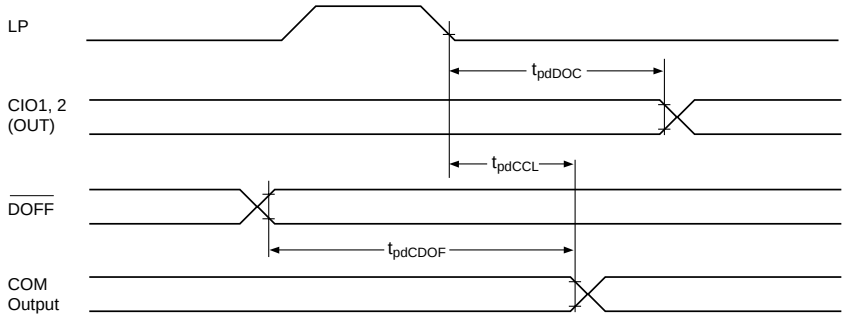
(V_{CC} = +5.0 V ± 10%, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		500		ns
LP "H" Pulse Width	t_{WCLH}		55		ns
LP "L" Pulse Width	t_{WCLL}		330		ns
FR Setup Time	t_{FRDS}		100		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		100		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			50	ns
Input Signal Fall Time	tf			50	ns
CIO Setup Time	t_{DS}		100		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		80		ns

(V_{CC} = +2.7 V to 4.5 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		800		ns
LP "H" Pulse Width	t_{WCLH}		100		ns
LP "L" Pulse Width	t_{WCLL}		660		ns
FR Setup Time	t_{FRDS}		200		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		200		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			100	ns
Input Signal Fall Time	tf			100	ns
CIO Setup Time	t_{DS}		200		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		150		ns

Output Timing Characteristics



(V_{CC} = 5.0 V ± 10%, V_{DDH} = +14.0 to +42.0 V, Ta = –30 to +85°C)

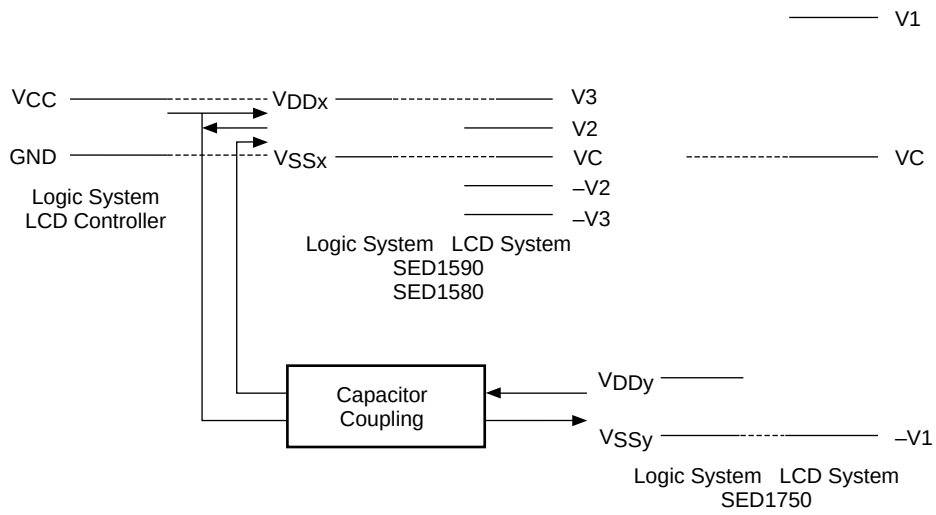
Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		300	ns
Delay time from LP to COM output	t_{pdCCL}			350	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			700	ns

(V_{CC} = +2.7 V to 4.5 V, V_{DDH} = +14.0 to +28.0 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		600	ns
Delay time from LP to COM output	t_{pdCCL}			500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

The Power Supply

Method of Forming Each Voltage Level



When the SED1590 (SED1580) and the SED1750 are used to form an extremely low power module system, the power relationships as shown in the figure above between the SED1590 (SED1580) and SED1750 logic systems, and the LCD system power supply, and the LCD controller power supply are optimal.

In this case, care is required when it comes to signal propagation in the logic system.

LCD Controller	→	SED1580, SED1590	Direct
LCD Controller	→	SED1750	Capacitor coupling is required
SED1580, SED1590	→	SED1750	Capacitor coupling is required
SED1750	→	SED1580, SED1590	Capacitor coupling is required

Cautions at Power Up and Power Down

Because the voltage level in the LCD system is high voltage, if the logic system power supply of this LSI is floating or if V_{CC} is 2.6 V or less when the LCD system high voltage (30 V or above) is applied, or if the LCD drive signal is output before the voltage level that is applied to the LCD system has stabilized, then there is the risk that there will be an over current condition in this LSI, resulting in permanent damage to this LSI.

It is recommended that the display OFF function (DOFF) is used until the LCD system voltage stabilizes to insure that the LCD drive output power level is at the VC level.

Be sure to follow the sequences below when turning the power supplies ON and OFF:

When turning the power supply ON:

Logic system ON → LCD drive system ON, or simultaneously ON.

When turning the power supply OFF:

LCD drive system OFF → Logic system OFF, or simultaneously OFF.

As a countermeasure to guard against over current conditions, it is effective to insert a high-speed fuse or a guard resistance in series with the LC power supply. The guard resistance value must be optimized depending on the capacity of the LC cell.

Example of Connection