SED1751

Contents

OVERVIEW

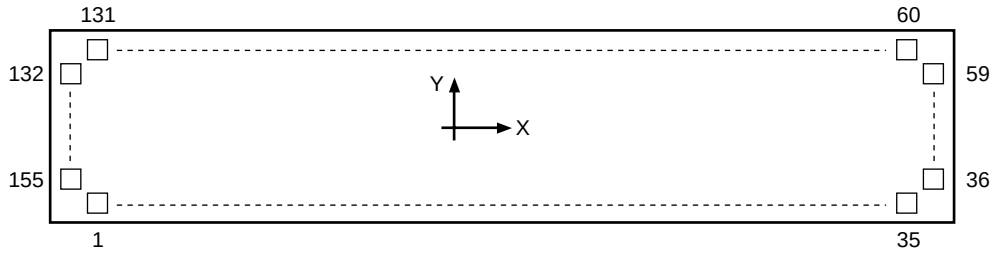
Description

The SED1751 is an 120 output, 3-level low-resistance common (row) driver suitable for high-quality, high-response-speed MLS (Multi Line Selection) driving.
The SED1751 receives signals from LCD controllers such as the SED1335, and when used is used in conjunction with the SED1580, can be used to structure a 4-line MLS drive.
The SED1751 uses a slim-chip form that is useful for making LCD panels slimmer. It also supports reduced logic system voltage operation, making it suitable for a broad range of applications.
The SED1751 has a pad layout supporting easy mounting, and supports bi-directional selection of driver output order, and has the highest use efficiency for 1/240 and 1/480 duty panels.

Features

- LCD driver outputs 120
- Low output ON resistance
- High duty drive supported ..... 1/480 (Reference value)
- Broad range of LC drive voltages ..... + 14 to + 42 V (V_{CC} = 2.7 to 5.5 V)
- Output shift direction pin select is possible
- Can be switched between 100 and 120 outputs
- Non-biased display OFF function
- Logic system power source ..... 2.7 V to 5.5 V
- LC power source offset bias can be adjusted relative to the V_{DDH} and GND levels
- Slim chip shape
- D_{0B} ..... Au Bump die
- T_{0A} ..... TCP

Pad Layout



Chip size 12.19 mm × 2.38 mm
Pad pitch 80 µm (Min.)
Chip thickness 525 µm ± 25 µm

1) Au Bump Specifications (SED1751D_{0B}) Reference Values Only
Au vertical bump
Parallel to Scribe × Perpendicular to Scribe ± Tolerance
Bump Size A 60 µm × 75 µm ± 4 µm (Pad No. 1 to 35, 60 to 131)
Bump Size B 80 µm × 50 µm ± 4 µm (Pad No. 36 to 59, 132 to 155)
Bump height 17 to 28 µm (The details specified in the acceptance specifications.)

Pad Coordinates

Units: µm

Pin	Name	X	Y
1	V_{DDHL}	–5812	–1012
2	$+V_{1L}$	–5717	
3	V_{CL}	–5622	
4	$–V_{1L}$	–5527	
5	GNDL	–5432	
6	SHL	–5094	
7	SEL	–4869	
8	V_{CC}	–4531	
9	LSEL	–4192	
10	$\overline{DOFF}$	–3828	
11	FR	–3081	
12	CSEL	–2336	
13	LP	–1998	
14	DM	–1162	
15	CIO2	–755	
16	DM	–347	
17	DM	0	
18	DM	347	
19	CIO1	755	
20	DM	1162	
21	YD	1998	
22	DM	2336	
23	DM	2674	
24	DM	3081	
25	DM	3489	
26	DM	3828	
27	F1	4192	
28	DM	4531	
29	F2	4869	
30	TEST1	5094	
31	GNDR	5432	
32	$–V_{1R}$	5527	
33	V_{CR}	5622	
34	$+V_{1R}$	5717	
35	V_{DDHR}	5812	

Pin	Name	X	Y
36	COM1	5945	–902
37	COM2		–822
38	COM3		–742
39	COM4		–662
↓	↓	↓	↓
57	COM22	5945	778
58	COM23	5945	858
59	COM24	5945	938
60	COM25	5709	1034
61	COM26	5549	1034
62	COM27	5389	1034
↓	↓	↓	↓
93	COM58	429	1034
94	COM59	269	
95	COM60	109	
96	COM61	–109	
97	COM62	–269	
98	COM63	–429	
↓	↓	↓	↓
129	COM94	–5389	1034
130	COM95	–5549	1034
131	COM96	–5709	1034
132	COM97	–5945	938
133	COM98	–5945	858
134	COM99	–5945	778
↓	↓	↓	↓
152	COM117	–5945	–662
153	COM118		–742
154	COM119		–822
155	COM120		–902

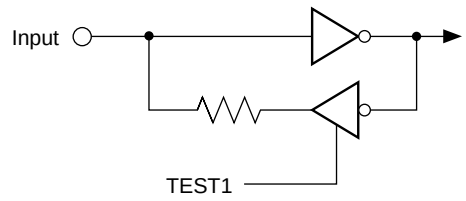
COMn XY coordinates:

COM1 to COM24: (5945, –902 + [80 × (n–1)])
COM25 to COM60: (5709 – [160 × (n–25)], 1034)
COM61 to COM96: (–109 – [160 × (n–61)], 1034)
COM97 to COM120: (–5945, 938 – [80 × (n–97)])

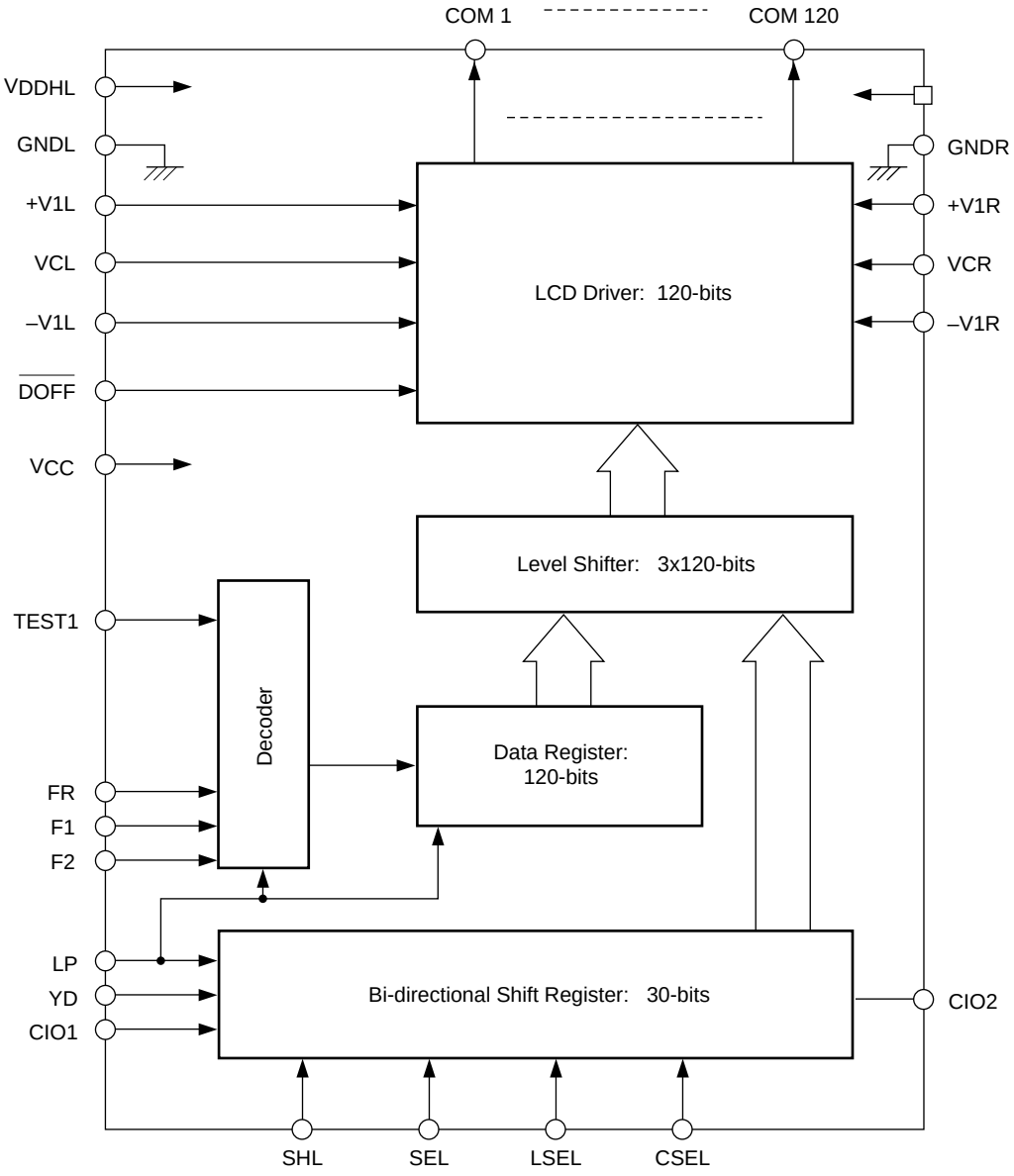
TERMINAL FUNCTIONS

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Number of Terminals</th></tr>
<tr><td>COM1 to COM120</td><td>O</td><td>Common (row) output to drive LC.
Output transition occurs on falling edge of LP.</td><td>120</td></tr>
<tr><td>CIO1
CIO2</td><td>I/O</td><td>Carry signal I/O.
This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of LP.</td><td>2</td></tr>
<tr><td>YD</td><td>I</td><td>Frame start/pulse input, with terminator. (*1)</td><td>1</td></tr>
<tr><td>F1, F2</td><td>I</td><td>Drive pattern select signal input, with terminator. (*1)</td><td>2</td></tr>
<tr><td>LP</td><td>I</td><td>Shift clock input for display data.
(Triggers on falling edge.) With terminator. (*1)</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select and CIO terminal I/O control input.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">Output Shift Direction</th><th colspan="2">CIO</th></tr>
<tr><th>CIO1</th><th>CIO2</th></tr>
<tr><td>L</td><td>1(9) → 120(108)</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>120(108) → 1(9)</td><td>Output</td><td>Input</td></tr>
</table>
The numbers in parentheses are for 100 output mode.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Select input for the number of COM output terminals:
120 outputs ←→ 100 outputs
L: COM1 to COM120
H: COM9 to COM108</td><td>1</td></tr>
<tr><td>LSEL</td><td>I</td><td>1/2 H operation select signal input.
L: Normal operation. H: 1/2 operation.</td><td>1</td></tr>
<tr><td>CSEL</td><td>I</td><td>Chip select signal input for when a cascade connection is used.
L: Leading chip
H: Other chips</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LC drive output AC signal input. With terminator (*1)</td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>LC display blanking control input. With a low level input, all common outputs are temporarily set to the V_C level. The contents of the latches are maintained. With terminator (*1)</td><td>1</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test1 signal input. Normally tied at L.</td><td>1</td></tr>
<tr><td>V_{CC}, GNDL, GNDR</td><td>Power</td><td>Power source for logic:
GND: 0 V , V_{CC}: +2.7 to 5.5 V</td><td>3</td></tr>
<tr><td>V_{CL}, V_{CR}, $+V_{1L}$, $+V_{1R}$, $-V_{1L}$, $-V_{1R}$, V_{DDHL}, V_{DDHR}</td><td>Power</td><td>LC Drive Power:
GND: 0 V,
V_{DDH}: + 14.0 to 42.0 V, $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq$ GND</td><td>8</td></tr>
<tr><td>DM</td><td></td><td>Dummy pad</td><td>11</td></tr>
<tr><td></td><td></td><td>Total</td><td>155</td></tr>
</table>

Note: *1



Block Diagram



Explanation of Each Block

Shift Register

This is a bi-directional shift register used for transmitting common data. The display data shifts on the falling edge of LP.

Level Shifter

The level shifter is a voltage level converter circuit which converts the signal voltage level from a logic system level to the LC driver system voltage level.

LCD Driver

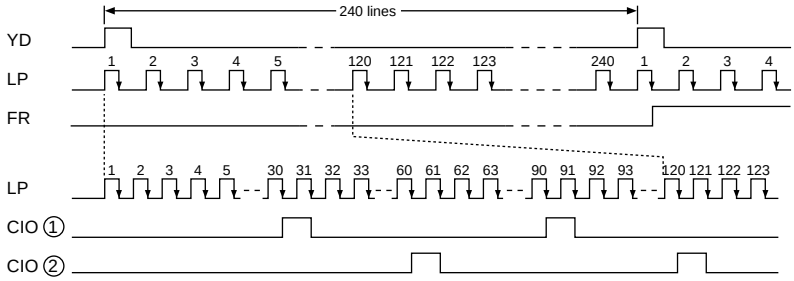
The LCD driver outputs the LC drive voltage.
The relationship between the display blanking signal $\overline{DOFF}$, the field recognition signals F1 & F2, the AC signal FR, and the common output voltage is as follows:

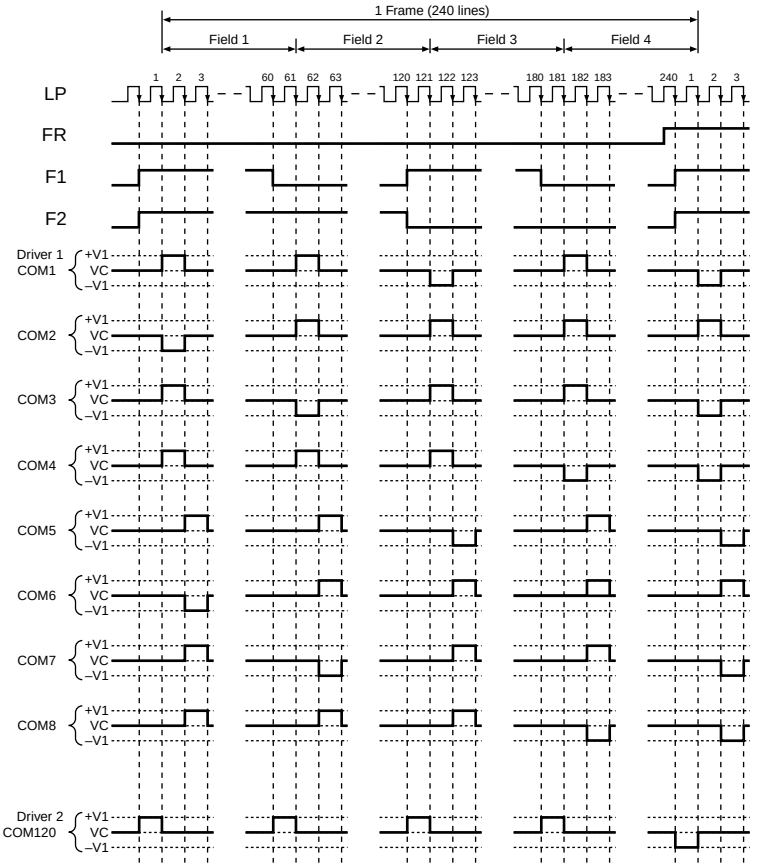
$\overline{DOFF}$	H								L
FR	L				H				—
F1,F2	1,1	0,1	1,0	0,0	1,1	0,1	1,0	0,0	—
Line 1	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	$+V_1$	$-V_1$	V_C
Line 2	$-V_1$	$+V_1$	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	V_C
Line 3	$+V_1$	$-V_1$	$+V_1$	$+V_1$	$-V_1$	$+V_1$	$-V_1$	$-V_1$	V_C
Line 4	$+V_1$	$+V_1$	$+V_1$	$-V_1$	$-V_1$	$-V_1$	$-V_1$	$+V_1$	V_C

Voltage level relationships: $+V_1 > V_C > -V_1$ (V_C is the center voltage level)

Timing Diagram (1)

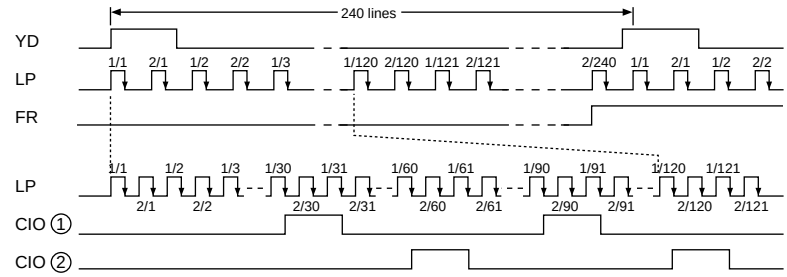
1/240 duty, normal operation.
SHL = L, SEL = L, LSEL = L, CSEL = L (This diagram provided only as a reference.)

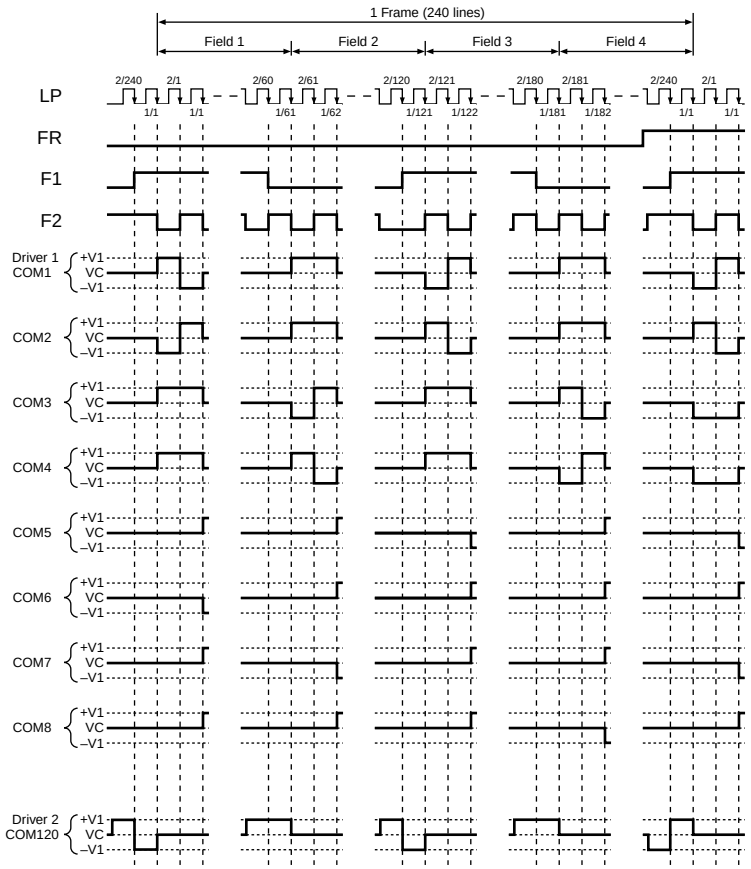




Timing Diagram (2)

1/240 duty, 1/2 H operation.
SHL = L, SEL = L, LSEL = H, CSEL = L (This diagram provided only as a reference.)

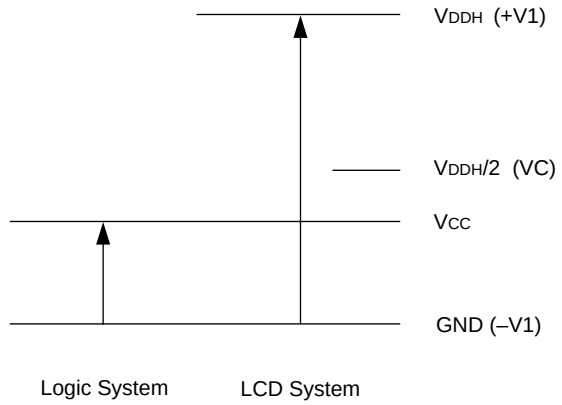




ABSOLUTE MAXIMUM RATINGS

Item	Signal	Rated Value	Units
Power voltage (1)	V_{CC}	–0.3 to +7.0	V
Power voltage (2)	V_{DDH}	–0.3 to + 45.0	V
Power voltage (3)	± V_1, V_C	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
CIO output current	I_{O1}	20	mA
Operating temperature	Topr	–30 to +85	°C
Storage temperature 1	Tstg1	–65 to +150	°C
Storage temperature 2	Tstg2	–55 to +100	°C

NOTE 1: The voltages are all relative to GND = 0 V.
NOTE 2: Storage temperature 1 is for the chip alone, and storage temperature 2 is for the TCP product.
NOTE 3: Ensure that the relationship between $+V_1$, V_C, and $-V_1$ is always as follows: $V_{DDH} \geq +V_1 \geq V_C \geq -V_1 \geq GND$.



NOTE 4: The LSI may be permanently damaged if the logic system power is floating or V_{CC} is less than or equal to 2.6 V when power is applied to the LC drive system. Special caution must be paid to the power sequences during power up and power down.

Electrical Characteristics

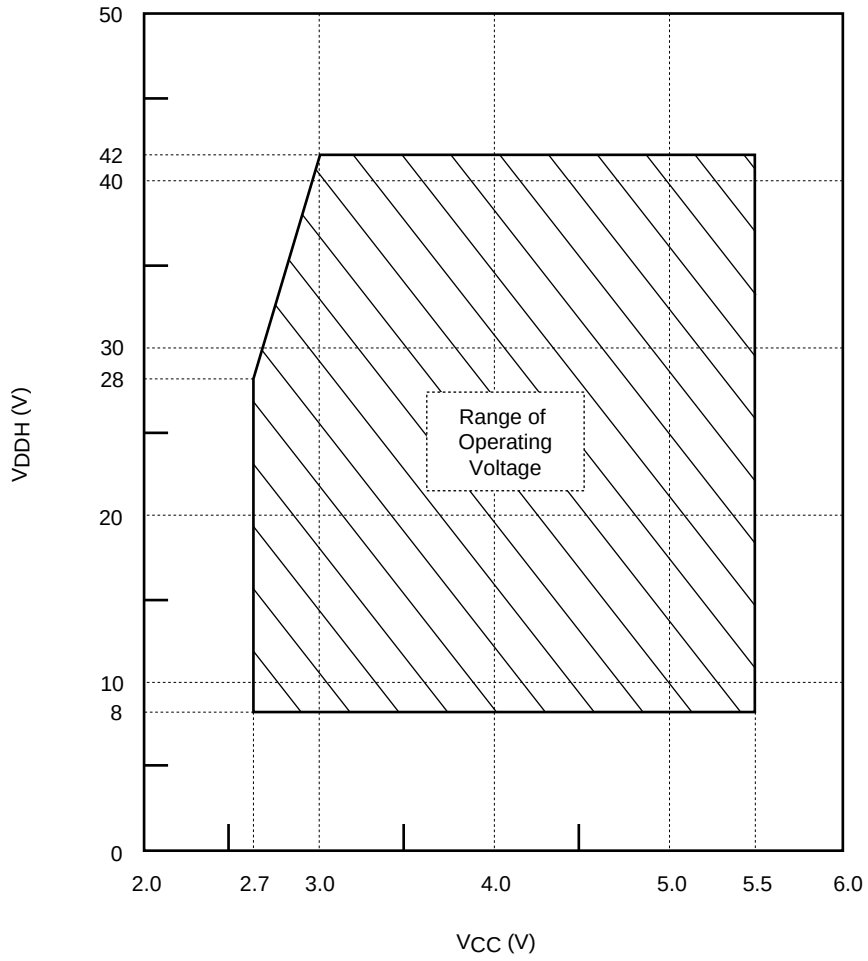
DC Characteristics

Unless otherwise noted, GND = 0 V, V_{CC} = + 5.0 V ± 10%, Ta = –30 to 85°C

Item	Signal	Parameter		Applicable Terminals	Min	Typ	Max	Unit
Power Supply Voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Range Operating Voltages	V_{DDH}	Function		V_{DDH}	8.0		42.0	V
Power Supply Voltage (2)	$+V_1$	Recommended Value		$+V_1$			V_{DDH}	V
Power Supply Voltage (3)	V_C	Recommended Value		V_C		$V_{DDH}/2$		V
Power Supply Voltage (4)	$–V_1$	Recommended Value		$–V_1$	GND			V
High-level Input Voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		CIO1,CIO2,FR, YD,LP,SHL,SEL, LSEL,CSEL, $\overline{DOFF}$,F1,F2, TEST1	0.8V_{CC}			V
Low-level Input Voltage	V_{IL}						0.2V_{CC}	V
High-level Output Voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	CIO1,CIO2	V_{CC}–0.4			V
Low-level Output Voltage	V_{OL}		I_{OL} = 0.3mA				0.4	V
Input Leakage Current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		LP,YD,SHL,SEL, LSEL,CSEL,F1, F2,$\overline{DOFF}$,TEST1, FR			2.0	µA
Input/Output Leakage Current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		CIO1,CIO2			5.0	µA
Static Current	I_{GND}	V_{DDH} = 14.0~42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND			25	µA
Output Resistance	R_{COM}	ΔVON = 0.5 V Recommended parameter	V_{DDH} = +30.0V	COM1 to COM120		0.55	0.7	kΩ
			V_{DDH} = +40.0V			0.5	0.7	
Average Operating Consumption Current (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC} V_{IL} = GND, f_{LP} = 16.8 kHz f_{FR} = 70 Hz, Input data: 1/240 No load		V_{CC}		10	25	µA
		V_{CC} = 3.0 V All other parameters the same as V_{CC} = 5.0 V.				7	17	
Average Operating Consumption Current (2)	I_{DDH}	V_{DDH} = $+V_1$ = +30.0 V, V_C = $V_{DDH}/2$, $–V_1$ = 0.0 V, V_{CC} = 5.0 V All other parameters the same as the I_{CC} item.		V_{DDH}		6	13	µA
Input Terminal Capacity	C_I	Freq. = 1 MHz Chip alone Ta = 25°C		LP,YD,SHL,SEL, LSEL,CSEL,F1,F2, $\overline{DOFF}$,TEST1,FR			10	pF
Input/Output Terminal Capacity	$C_{I/O}$			CIO1,CIO2			18	pF

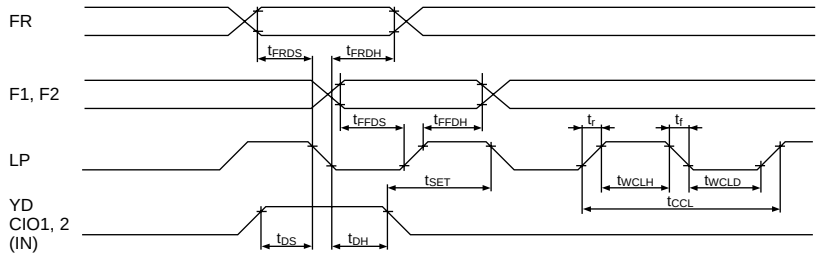
Range of Operating Voltages: $V_{CC} – V_{DDH}$

It is necessary to set the voltage for V_{DDH} within the $V_{CC} – V_{DDH}$ operating voltage range shown in the diagram below.



AC Characteristics

Input Timing Characteristics



The FR latched at the nth LP is reflected in the output at the n+1th LP.

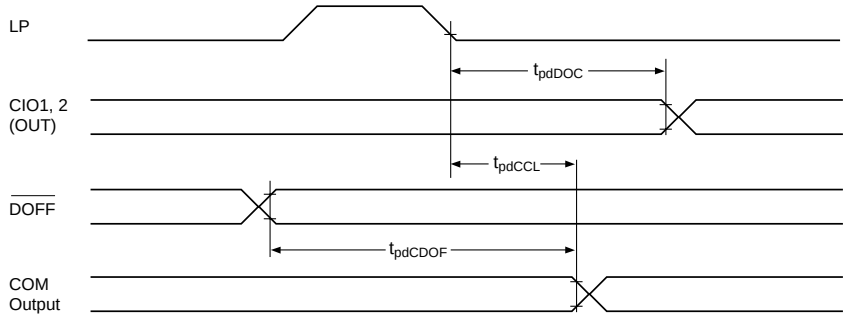
(V_{CC} = +5.0 V ± 10%, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		500		ns
LP "H" Pulse Width	t_{WCLH}		55		ns
LP "L" Pulse Width	t_{WCLL}		330		ns
FR Setup Time	t_{FRDS}		100		ns
FR Hold Time	t_{FRDH}		40		
F1, F2 Setup Time	t_{FFDS}		100		
F1, F2 Hold Time	t_{FFDH}		40		
Input Signal Rise Time	tr			50	ns
Input Signal Fall Time	tf			50	ns
CIO Setup Time	t_{DS}		100		ns
CIO Hold Time	t_{DH}		40		ns
YD → LP Allowable Time	t_{SET}		80		ns

(V_{CC} = +2.7 V to 4.5 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
LP Frequency	t_{CCL}		800		ns
LP "H" Pulse Width	t_{WCLH}		100		ns
LP "L" Pulse Width	t_{WCLL}		660		ns
FR Setup Time	t_{FRDS}		200		ns
FR Hold Time	t_{FRDH}		80		
F1, F2 Setup Time	t_{FFDS}		200		
F1, F2 Hold Time	t_{FFDH}		80		
Input Signal Rise Time	tr			100	ns
Input Signal Fall Time	tf			100	ns
CIO Setup Time	t_{DS}		200		ns
CIO Hold Time	t_{DH}		80		ns
YD → LP Allowable Time	t_{SET}		150		ns

Output Timing Characteristics



(V_{CC} = 5.0 V ± 10%, V_{DDH} = +14.0 to +42.0 V, Ta = –30 to +85°C)

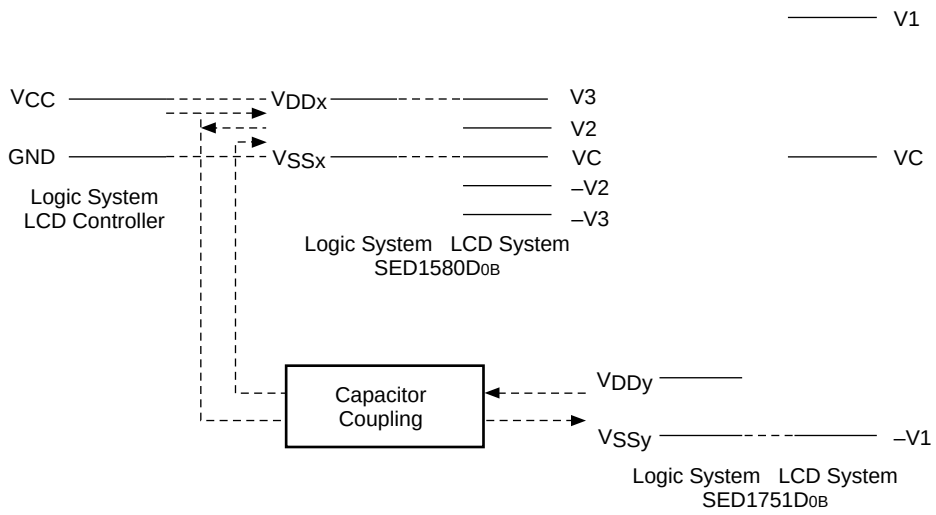
Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		300	ns
Delay time from LP to COM output	t_{pdCCL}			350	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			700	ns

(V_{CC} = +2.7 V to 4.5 V, V_{DDH} = +14.0 to +28.0 V, Ta = –30 to +85°C)

Item	Signal	Parameter	Min	Max	Units
Delay time from LP to CIO output	t_{pdDOC}	C_L = 15 pF V_{DDH} = 14.0 V to 40.0 V		600	ns
Delay time from LP to COM output	t_{pdCCL}			500	ns
Delay time from $\overline{DOFF}$ to COM output	t_{pdCDOF}			1400	ns

The Power Supply

Method of Forming Each Voltage Level



When the SED1580 and the SED1751 are used to form an extremely low power module system, the power relationships as shown in the figure above between the SED1580 and SED1751 logic systems, and the LCD system power supply, and the LCD controller power supply are optimal.
In this case, care is required when it comes to signal propagation in the logic system.

LCD Controller	→	SED1580	Direct
LCD Controller	→	SED1751	Capacitor coupling is required
SED1580	→	SED1751	Capacitor coupling is required
SED1751	→	SED1580	Capacitor coupling is required

Cautions at Power Up and Power Down

Because the voltage level in the LCD system is high voltage, if the logic system power supply of this LSI is floating or if V_{CC} is 2.6 V or less when the LCD system high voltage (30 V or above) is applied, or if the LCD drive signal is output before the voltage level that is applied to the LCD system has stabilized, then there is the risk that there will be an over current condition in this LSI, resulting in permanent damage to this LSI.
It is recommended that the display OFF function (DOFF) is used until the LCD system voltage stabilizes to insure that the LCD drive output power level is at the VC level.
Be sure to follow the sequences below when turning the power supplies ON and OFF:

When turning the power supply ON:

Logic system ON → LCD drive system ON, or simultaneously ON.

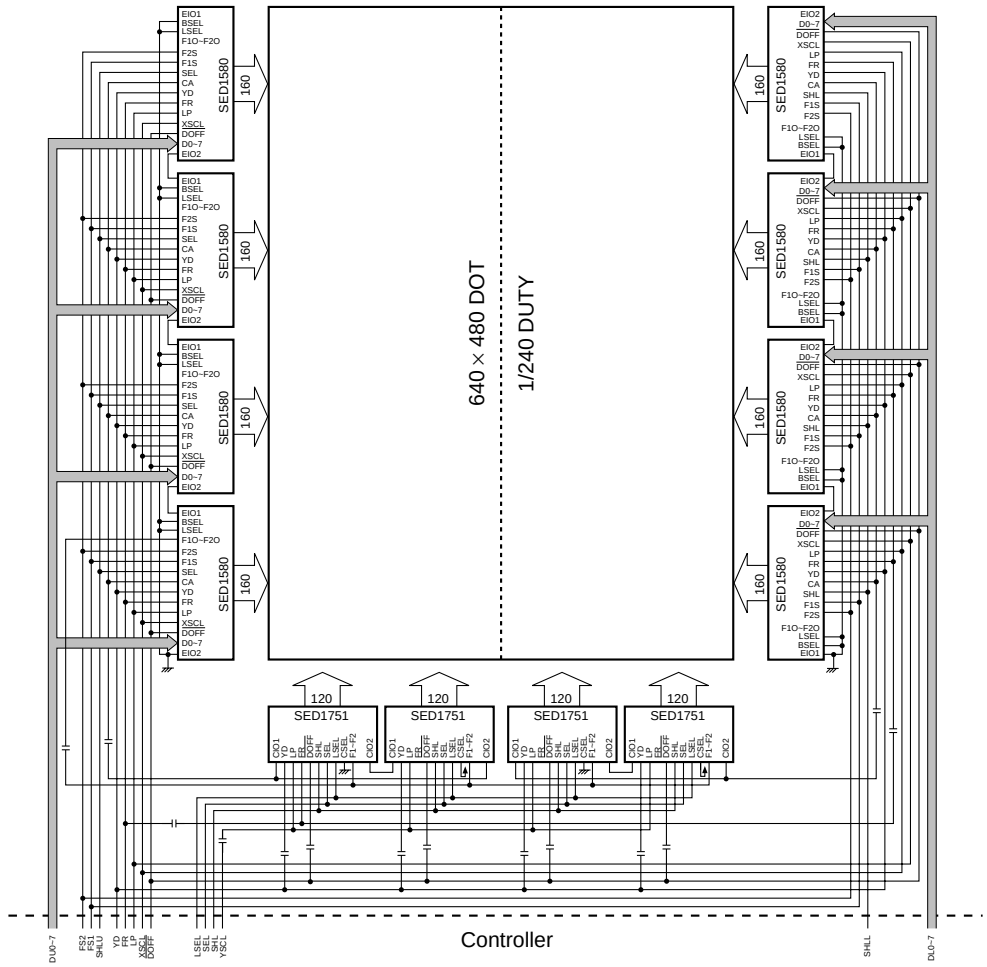
When turning the power supply OFF:

LCD drive system OFF → Logic system OFF, or simultaneously OFF.

As a countermeasure to guard against over current conditions, it is effective to insert a high-speed fuse or a guard resistance in series with the LC power supply. The guard resistance value must be optimized depending on the capacity of the LC cell.

Example of Connection

Large Screen LCD Structure Diagram



Example of External Connections