DESCRIPTION

The SCI7654 C0A/M0A is a CMOS process, charge-pumping DC/DC converter and voltage regulator featuring the very high efficiency but low power consumption. An addition of four, three, or two external capacitors can generate four-, three- or two-time output voltage in negative direction than the input voltage. Also, the built-in voltage regulator can set any output voltage of DC/DC converter and can output the regulated voltage using two external resistances. As the regulator output can have a negative temperature gradient that is required for LCD panels, it is optimum for the LCD panel power supply.

FEATURES

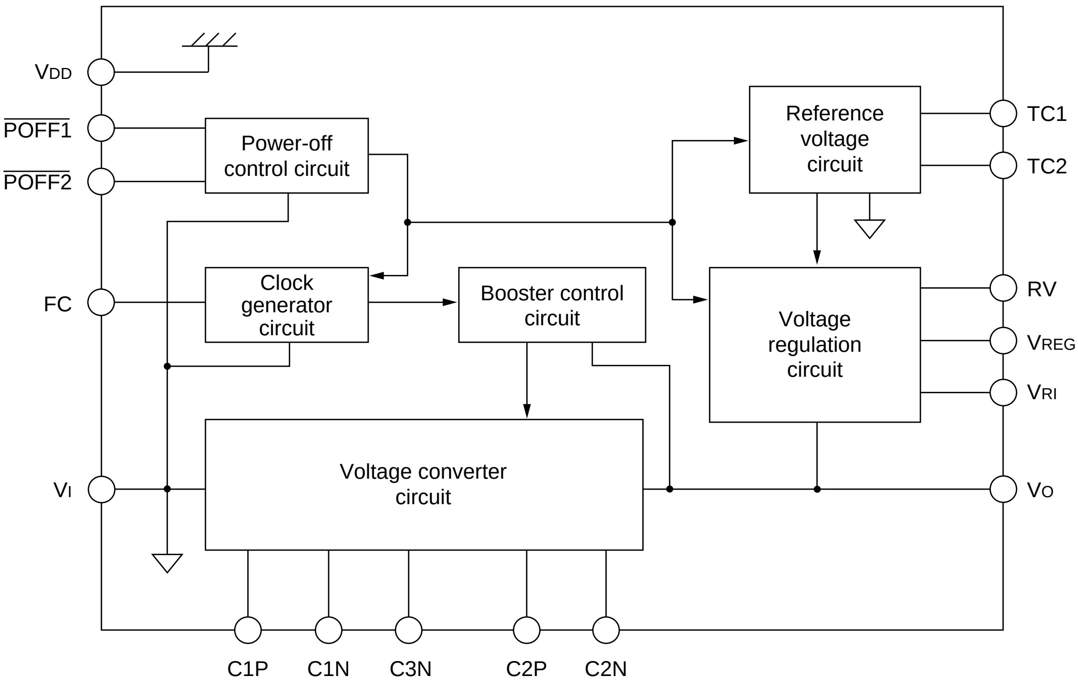
- Charge-pumping, DC-to-DC converter (four-, three- or two-time negative boosting)
- Built-in voltage regulator (regulated voltage output circuit)
- High power conversion efficiency : 95%
- Low current consumption : 130 µA (V_I = –5.0 V during four-time boosting, Typ.)
- High output capacity : 20 mA (Max.)
- Input voltages : –2.4 to –5.5 V (during four-time boosting)
  : 2.4 to –7.3 V (during three-time boosting)
  : 2.4 to –11 V (during two-time boosting)
- DC/DC converter output voltage : |Input voltage| × 4 (Max.)
- Built-in reference voltage for high-precision regulator : 1.5 + –0.05 V (at CT0)
- Temperature gradient function of regulator output voltages : –0.04, –0.15, –0.35, –0.55 (%/°C)
- Low standby current (during power-off) : 5.0 µA
- Power-off by the external signal
- Full built-in oscillator circuit
- Lineup : SCI7654M0A, 16-pin SSOP
  : SCI7654C0A, 16-pin DIP

APPLICATIONS

- Power supply of medium- and small-capacity LCD panels
- Regulated power supply of battery driven devices

BLOCK DIAGRAM

Figure 2.1 Block diagram



PIN DESCRIPTION

Figure 2.2 SCI7654M0A/C0A pin assignment

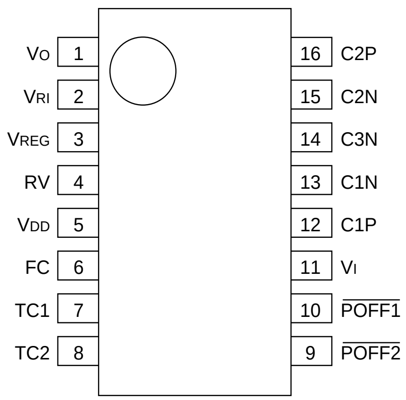


Table 2.1 Functions of the terminal

Pin name	Pin No.	PAD No.	Function
V_O	1	18	Four-time booster output
V_{RI}	2	19	Regulator input
V_{REG}	3	20	Regulator output
R_V	4	21	Regulator output voltage adjustment input
V_{DD}	5	22, 23	Power pin (positive)
FC	6	24	Internal clock frequency input, and clock input in serial/parallel connection
TC1	7	3	Regulator output temperature gradient setup input (1)
TC2	8	4	Regulator output temperature gradient setup input (2)
$\overline{\text{POFF2}}$	9	5	Power-off control input (2)
$\overline{\text{POFF1}}$	10	6	Power-off control input (1)
V_I	11	11, 12	Power voltage (negative)
C1P	12	13	Two- or four-time booster capacitor positive pin
C1N	13	14	Two-time booster capacitor negative pin
C3N	14	15	Four-time booster capacitor negative pin
C2N	15	16	Three-time booster capacitor negative pin
C2P	16	17	Three-time booster capacitor positive pin

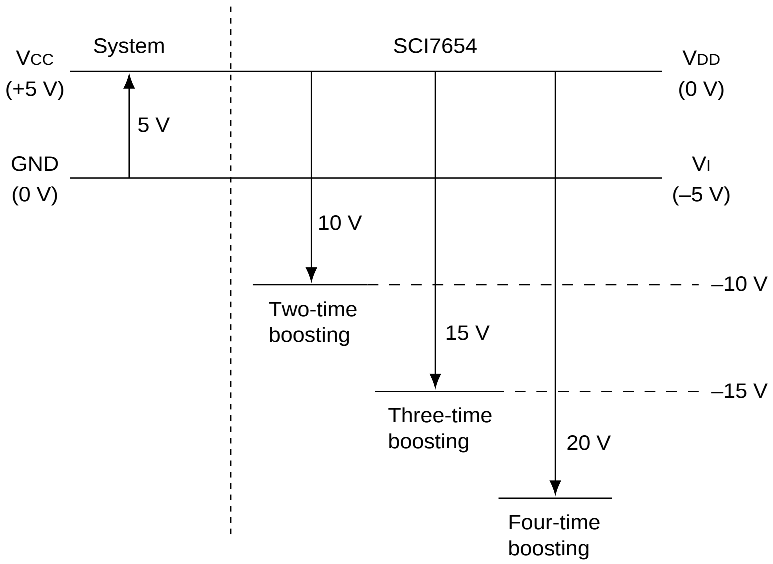
Table 2.2 Absolute maximum ratings

V_{DD} reference

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Input power voltage	V_I	–26.0/N	V_{DD} + 0.3	V	N = Boost time V_I pin
Input pin voltage	V_1	V_I – 0.3	V_{DD} + 0.3	V	$\overline{POFF1}$, $\overline{POFF2}$, TC1, TC2 and FC pins
Output pin voltage 1	V_{OC1}	V_I – 0.3	V_{DD} + 0.3	V	C1P and C2P pins
Output pin voltage 2	V_{OC2}	2 × V_I – 0.3	V_I + 0.3	V	C1N pin
Output pin voltage 3	V_{OC3}	3 × V_I – 0.3	2 × V_I + 0.3	V	C2N pin
Output pin voltage 4	V_{OC4}	4 × V_I – 0.3	3 × V_I + 0.3	V	C3N pin
Regulator input power voltage	V_{RI}	N × V_I – 0.3	V_{DD} + 0.3	V	N = Boost time, V_{RI} pin
Regulator input pin voltage	V_{RV}	N × V_I – 0.3	V_{DD} + 0.3	V	N = Boost time, RV pin
Output voltage	V_O	N × V_I – 0.3	V_{DD} + 0.3	V	N = Boost time V_O and V_{REG} pins
Input current	I_I		80	mA	V_I pin
Output current	I_O		N ≤ 4: 20 N > 4: 80/N	mA	N = Boost time V_O and V_{REG} pins
Allowable loss	Pd		210	mW	Ta ≤ 25°C
Operating temperature	Topr	–30	85	°C	
Storage temperature	Tstg	–55	150	°C	
Soldering temperature and time	Tsol		260 • 10	°C • S	At leads

Notes:
1. An operation exceeding the above absolute maximum ratings may cause a malfunction or permanent damage of devices. The device reliability may drop excessively even if the devices temporarily operate normally.
2. Electrical potential to peripheral systems:
   The SCI7654 common power supply has the highest potential (V_{DD}). The electrical potential given by this specification is based on V_{DD} = 0 V. Take care to avoid a potential problem during connection to a peripheral system.

Figure 2.3 Potential relationship



ELECTRICAL CHARACTERISTICS

Table 2.3 DC characteristics (1)

Ta = –30°C to +85°C, V_{DD} = 0 V, V_I = –5.0 V
unless otherwise noted

Parameter	Symbol	Characteristics	Min.	Typ.	Max.	Unit
Input power voltage	V_I	N = Boost time if CT0 is selected	–22/N		–2.4	V
		N = Boost time if CT1 is selected	–22/N		–2.4	V
		N = Boost time if CT2 is selected	–22/N		–2.4	V
		N = Boost time if CT3 is selected	–22/N		–2.4	V
Boost start input power voltage	V_{STA}	N = Boost time, FC = V_{DD} during no loading	–22/N		–2.4	V
Boost output voltage	V_O		–22			V
Regulator input voltage	V_{RI}		–22		–2.4	V
Regulator output voltage	V_{REG}	I_{REG} = 0, V_{RI} = –22 V R_{RV} = 1MΩ			–2.4	V

Table 2.3 DC characteristics (2)

Ta = –30°C to +85°C, V_{DD} = 0 V, V_I = –5.0 V
unless otherwise noted

Parameter	Symbol	Characteristics	Min.	Typ.	Max.	Unit
Boost output impedance	R_O	I_O = 10 mA, V_I = –5.0 V during 4-time boosting C1, C2, C3, C_O = 10 μF (tantalum)		200	300	Ω
		I_O = 10 mA, V_I = –3.0 V, Ta = 25°C during 4-time boosting C1, C2, C3, C_O = 10 μF (tantalum)		250	300	Ω
Boost power conversion efficiency	Peff	I_O = 2 mA, V_I = –5.0 V during 4-time boosting C1, C2, C3, C_O = 10 μF (tantalum)		95		%
		I_O = 2 mA, V_I = –3.0 V, Ta = 25°C during 4-time boosting C1, C2, C3, C_O = 10 μF (tantalum)		94		%
Booster operation current consumption 1	I_{opr1}	FC = V_{DD}, $\overline{POFF1}$ = V_I, $\overline{POFF2}$ = V_{DD}, V_I = –5.0 V during no loading C1, C2, C3, C_O = 10 μF (tantalum)		130	220	μA
		FC = V_{DD}, $\overline{POFF1}$ = V_I, $\overline{POFF2}$ = V_{DD}, V_I = –3.0 V, Ta = 25°C during no loading C1, C2, C3, C_O = 10 μF (tantalum)		90	150	μA
Booster operation current consumption 2	I_{opr2}	FC = V_I, $\overline{POFF1}$ = V_I, $\overline{POFF2}$ = V_{DD}, V_I = –5.0 V during no loading C1, C2, C3, C_O = 10 μF (tantalum)		520	880	μA
		FC = V_I, $\overline{POFF1}$ = V_I, $\overline{POFF2}$ = V_{DD}, V_I = –3.0 V, Ta = 25°C during no loading C1, C2, C3, C_O = 10 μF (tantalum)		360	600	μA
Regulator operation current consumption	I_{OPVR}	V_{RI} = –20 V, R_{RV} = 1 MΩ during no loading		10	15	μA
Static current	I_Q	$\overline{POFF1}$ = V_I, $\overline{POFF2}$ = V_I FC = V_{DD}			5.0	μA
Input leakage current	I_{LI}	Pins used: $\overline{POFF1}$, $\overline{POFF2}$, FC, TC1, TC2			0.5	μA
Regulated output saturation resistance	R_{SAT} (*1)	0 < I_{REG} < 20 mA R_V = V_{DD} Ta = 25°C		10	20	Ω
Regulated output voltage stability	ΔV_R (*2)	–20 V < V_{RI} < –10 V, I_{REG} = 1 mA V_{REG} = –9 V Ta = 25°C			0.2	%/V

DC/DC Converter & Voltage Regulator

Table 2.3 DC characteristics (3)

Ta = –30°C to +85°C, V_{DD} = 0 V, V_I = –5.0 V
unless otherwise noted

Parameter	Symbol	Characteristics	Min.	Typ.	Max.	Unit
Regulated output load variation	ΔV_O (*3)	V_{RI} = –20 V, V_{REG} = –15 V, Ta = 25°C setup 0 < I_{REG} < 20 mA		30	50	mV
Reference voltage (Ta = 25°C)	V_{REF0}	TC1 = V_{DD}, TC2 = V_{DD}	–1.55	–1.50	–1.45	V
	V_{REF1}	TC1 = V_{DD}, TC2 = V_I	–1.70	–1.50	–1.30	V
	V_{REF2}	TC1 = V_I, TC2 = V_{DD}	–1.90	–1.50	–1.10	V
	V_{REF3}	TC1 = V_I, TC2 = V_I	–2.15	–1.50	–0.85	V
Reference voltage temperature coefficient (*4, *5)	CT0	TC1 = V_{DD}, TC2 = V_{DD}, SSOP product	–0.07	–0.04	0	%/°C
	CT1	TC1 = V_{DD}, TC2 = V_I, SSOP product	–0.25	–0.15	–0.07	%/°C
	CT2	TC1 = V_I, TC2 = V_{DD}, SSOP product	–0.45	–0.35	–0.20	%/°C
	CT3	TC1 = V_I, TC2 = V_I, SSOP product	–0.75	–0.55	–0.30	%/°C
Input voltage level	V_I	V_I = –2.4 to –5.5 V Pins used: $\overline{POFF1}$, $\overline{POFF2}$, FC, TC1, TC2	0.2 V_I			V
	V_{IL}	V_I = –2.4 to –5.5 V Pins used: $\overline{POFF1}$, $\overline{POFF2}$, FC, TC1, TC2			0.8 V_I	V
Booster capacitance	CMAX	Capacitors used: C1, C2 and C3			47	µF

*1 $$R_{SAT} = \frac{\Delta (V_{REG} - V_{RI})}{\Delta I_{REG}}$$

*2 $$\Delta V_R = \frac{V_{REG}(V_{RI} = -20\ V) - V_{REG}(V_{RI} = -10\ V)}{\Delta V_{RI} \bullet V_{REG}(V_{RI} = -10\ V)}$$

*3 $$\Delta V_O = \frac{V_{REG}(I_{REG} = 20\ mA) - V_{REG}(I_{REG} = 0\ mA)}{\Delta I_{REG}}$$

*4 $$CT = \frac{|V_{REF}(50°C)| - |V_{REF}(0°C)|}{50°C - 0°C} \times \frac{100}{|V_{REF}(25°C)|}$$

*5 The reference voltage and temperature coefficient of the chip products may vary depending on the moldings used on each chip. Use these chips only after the temperature test.

Table 2.4 AC characteristics

V_{DD} = 0 V and V_I = –5.0 V
unless otherwise noted

Parameter	Symbol	Characteristics		Min.	Typ.	Max.	Unit
Internal clock frequency 1	f_{CL1}	FC = V_{DD}, $\overline{POFF1}$ = V_I $\overline{POFF2}$ = V_{DD} Pin used: C1P	Ta = 25°C	3.0	4.0	6.0	kHz
			Ta = –30°C to +85°C	2.0	4.0	7.0	kHz
Internal clock frequency 2	f_{CL2}	FC = V_I, $\overline{POFF1}$ = V_I $\overline{POFF2}$ = V_{DD} Pin used: C1P	Ta = 25°C	12.0	16.0	24.0	kHz
			Ta = –30°C to +85°C	8.0	16.0	28.0	kHz

EXPLANATION OF FUNCTIONS

Clock Generator Circuit

As the SCI7654 has a built-in clock generator circuit, no more parts are required for voltage boost control. The clock frequency changes according to the FC pin voltage level as defined on Table 2.5. Low Output mode or High Output mode is selectable. This allows frequency selection according to the used capacitance and load current as the boost output impedance changes depending on the clock frequency and external booster capacitance. However, the High Output mode has the current consumption approximately four times larger than the Low Output mode.

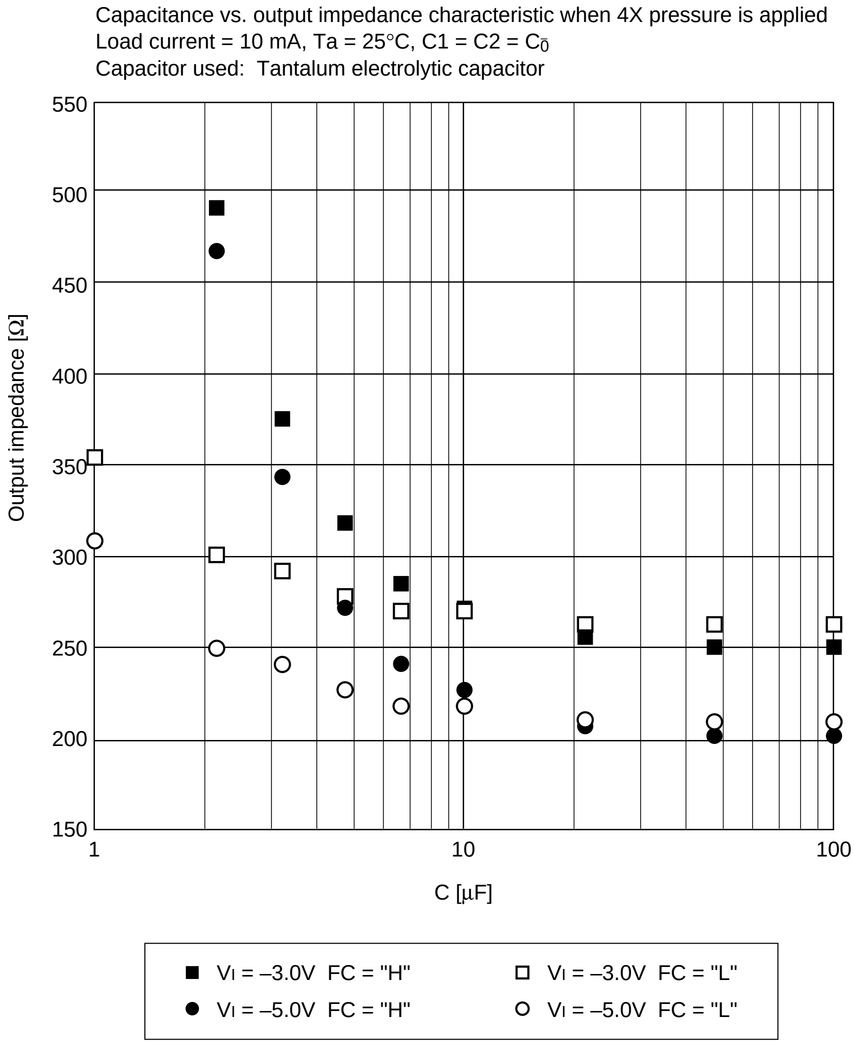
Table 2.5 FC pin setup

FC pin	Mode	Clock frequency	Characteristics			
			Current consumption	Output ripple	Output impedance	Capacitance
H (V_{DD})	Low Output	4.0 kHz (Typ.)	I_{OP} (*1)	V_{RR} (*2)	See Figure A1.	See Figure A1.
L (V_I)	High Output	16.0 kHz (Typ.)	I_{OP} × Approx. 4	V_{RI} × Approx. 1/4	See Figure A1.	See Figure A1.

*1 See the DC characteristics table for current consumption.
*2 See Section Page 2-32 for the output ripple definition and calculation.

Figure A1 Characteristic chart: Capacitance vs. output impedance when 4X pressure is applied

NOTE: This characteristic chart simply indicates an approximate trend in the characteristics, which may vary depending on evaluation environment, parts used, and other factors.

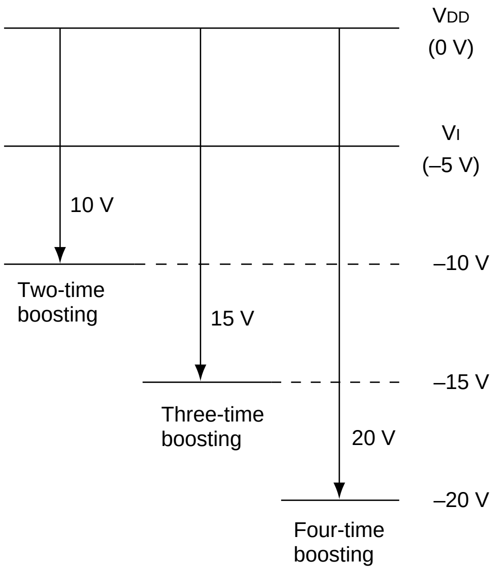


DC/DC Converter & Voltage Regulator

Voltage Converter

The voltage converter, consisting of a boost control circuit and a voltage converter circuit, receives clocks from the clock generator circuit and boosts the input power voltage (V_I) four, three or two times. During four-time boosting, however, the three-time and two-time boost outputs cannot be obtained simultaneously. Figure 2.4 gives the potential relationship during four-, three- and two-time boosting. The C2P pin is also used as the master clock output during parallel connection.

Figure 2.4 Electrical potentials during boosting (at -5V input)



Caution:

- When connecting a capacitor to the C1P, C2P, C1N, C2N, C3N, or V_O pin for voltage conversion, close the capacitor to the IC package as much as possible to minimize the wiring length.

DC/DC Converter & Voltage Regulator

Reference Voltage Circuit

The SCI7654 has a built-in reference voltage circuit for voltage regulation. The regulated voltage (explained in the next "voltage regulator circuit" section) is set depending on the division ratio between this reference voltage and the external resistance. The reference voltage can be used to change the temperature coefficient at pins TC1 and TC2. One of four states can be selected as listed on Table 2.6.

Table 2.6 Setup of reference voltage and temperature coefficient

Mode	TC1 (H = V_{DD}) (L = V_I)	TC2 (H = V_{DD}) (L = V_I)	Reference voltage, V_{REF} (V)			Temperature coefficient, CT (%/°C)		
			Min.	Typ.	Max.	Min.	Typ.	Max.
CT0	H	H	–1.55	–1.5	–1.45	–0.07	–0.04	0
CT1	H	L	–1.70	–1.5	–1.30	–0.25	–0.15	–0.07
CT2	L	H	–1.90	–1.5	–1.10	–0.45	–0.35	–0.20
CT3	L	L	–2.15	–1.5	–0.85	–0.75	–0.55	–0.30

Notes: 1. The reference voltage is given at Ta = 25°C.
2. The reference voltage and temperature coefficient of the chip products may vary depending on the moldings used on each chip. Use these chips only after the temperature test.

The temperature coefficient (CT) is defined by the following equation. The negative sign of the temperature coefficient (CT) means that the $|V_{REF}|$ value decreases when the temperature rises.

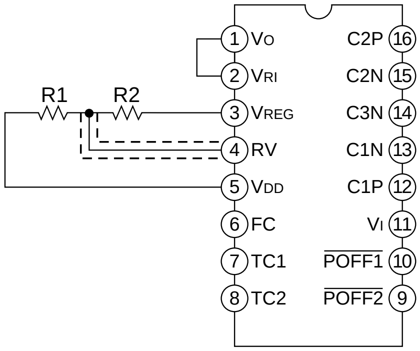
$$CT = \frac{|V_{REF}(50°C)| - |V_{REF}(0°C)|}{50°C - 0°C} \times \frac{100}{|V_{REF}(25°C)|}$$

Notes on TC1 and TC2 pin replacement:
- When replacing the TC1 and TC2 pins after power-on, always select the power-off mode ($\overline{POFF1} = \overline{POFF2} = V_I$) and replace them by each other.

Voltage Regulator Circuit

The voltage regulator circuit regulates a voltage entered in the V_{RI} pin and can output any voltage. It uses the series voltage regulation. As shown in Figure 2.5, the V_{RI} and V_O pins must be short-circuited by a jumper as short as possible except for larger time boosting by using external diodes.
As shown by equation (1), any output voltage can be set by the ratio of external division resistors R1 and R2. The sum of division resistance is recommended to be small as possible to avoid an external noise interference. As the current consumed by division resistors (equation (2)) flows, the 100 ohms to 1M ohms are recommended to use.
The temperature coefficient of the regulated voltage is equal to the temperature coefficient of the reference voltage that is explained in the "reference voltage circuit" section.

Figure 2.5 VREG setup and mounting notes



Setup:

- Relationship between VREG and reference voltage

$$V_{REG} = \frac{R1 + R2}{R1} \times \text{(Reference voltage)} \qquad \text{• • • • Equation (1)}$$

- Current consumption of division resistors

$$I_{REG} = \frac{|V_{REG}|}{R1 + R2} \qquad \text{• • • • Equation (2)}$$

Setup example:

- To output V_{REG} = –18 V by four-time boosting if V_I = –5 V and V_O = –20 V

First, determine the total resistance of division resistors R1 and R2. If the current consumption is assumed to be 20 μA, the total resistance can be obtained from equation (2) as follows:

R1 + R2 = 12V ÷ 20 μA = 900 kΩ

If the reference voltage is -1.5 V, the division resistance ratio can be obtained from equation (1) as follows:

(R1 + R2) / R2 = (–18 V) ÷ (–1.5 V) = 12

Therefore, R1 and R2 are:

R1 = 75 kΩ
R2 = 825 kΩ

Changing the temperature coefficient:

- The temperature coefficient of the regulated voltage depends on the temperature coefficient of the reference voltage (if the division ratio of setup resistors does not depend on the temperature). It is necessary to change the temperature coefficient using thermistors, resistors or others to set any other temperature coefficient of the regulated voltage. The following explains how to calculate the V_{REG} voltage in temperature T.

$$V_{REG}(T) = \left\{1 + \frac{C_{TR2} \times R2(T0)}{C_{TR1} \times R1(T0)}\right\} \times C_{TREF} \times (T - T0) \times V_{REF}(T0) \qquad \bullet\bullet\bullet\bullet \text{ Equation (3)}$$

T_0	: 25°C
C_{TR1}	: Temperature coefficient of resistor R1 (Ratio to the value at 25°C)
C_{TR2}	: Temperature coefficient of resistor R2 (Ratio to the value at 25°C)
C_{TREF}	: Temperature coefficient of internal reference voltage (%/°C)
R1 (T_0)	: R1 value (Ω) at 25°C
R2 (T_0)	: R2 value (Ω) at 25°C
V_{REF} (T_0)	: Internal reference voltage (V) at 25°C

If the temperature coefficient of R1 and R2 is identical in equation (3), the V_{REG} voltage depends on the temperature coefficient of internal reference voltage only.

Application notes on voltage regulator circuit:

- To satisfy the absolute maximum ratings of the SCI7654, the setup resistor(s) must be inserted between V_{DD} and V_{REG} pins of the SCI7654 that uses the voltage regulator. The SCI7654 IC itself may be degraded or destroyed if the R1 resistor is connected to pin V_{DD} of SCI7654 that does not use the regulator during serial connection.
- The regulation voltage adjustment input (pin RV) has the very high input impedance, and its noise insertion can drop the regulator stability. As shown in Figure 2.5, shield the cable between the division resistor and RV pin or use a cable as short as possible between them.

Power-off Control Function

The SCI7654 has the power-off function and turns on or off each circuit function when control signals are entered in the $\overline{\text{POFF1}}$ and $\overline{\text{POFF2}}$ pins from an external system (such as microprocessor) as defined on Table 2.7. This power-off function can also cut the reactive current in parallel connection and other application circuits.

To use the dual-state, power-off control (all ON and all OFF states) only, connect pin $\overline{\text{POFF2}}$ to pin V_I and use only pin $\overline{\text{POFF1}}$ for power-off control.

Table 2.7 Available combination of power-off control

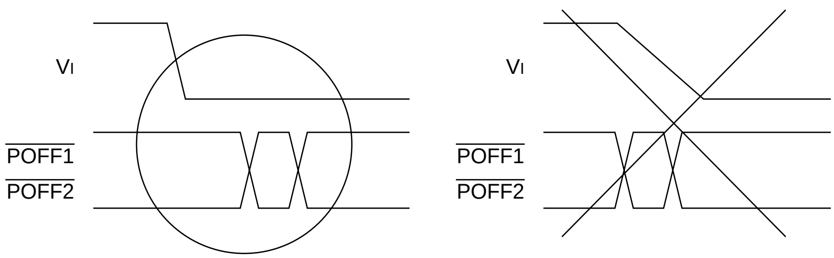
Mode	$\overline{\text{POFF1}}$ (H = V_{DD}) (L = V_I)	$\overline{\text{POFF2}}$ (H = V_{DD}) (L = V_I)	Functions			
			Oscillator	Booster circuit	Regulator circuit	Applications
PS1	H	L	On	On	On	All circuits are turned on.
PS2	L	L	Off	Off (*1)	Off (*2)	All circuits are turned off.
PS3	H	H	Off	On	On	Slave unit side of parallel connection (Booster and regulator)
PS4	L	H	On	On	Off	Master unit side of parallel connection (Booster only)

*1 When the booster circuit is off, approximately V_I + 0.6 V voltage appears at V_O pin.
*2 When the regulator is off, the V_{REG} pin becomes high-impedance state.

Application notes on power-off function:

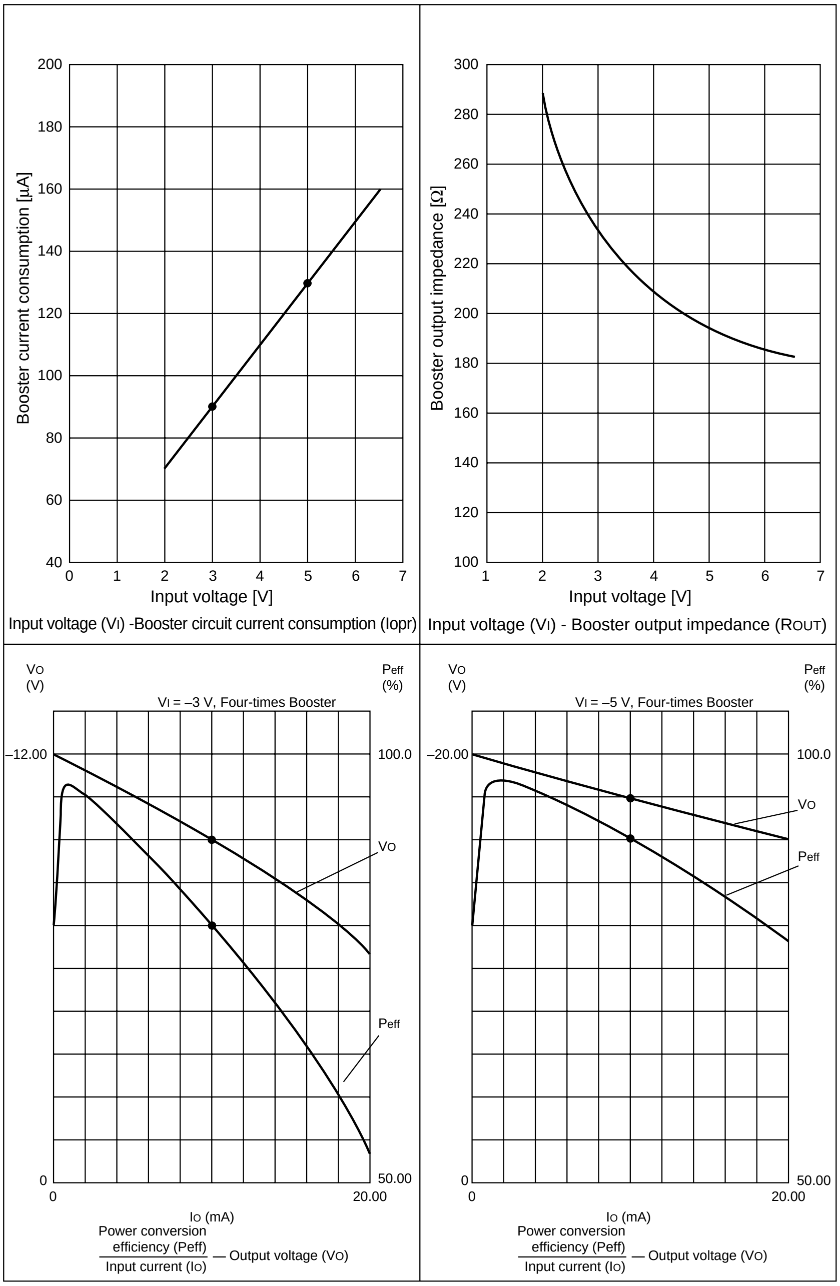
- When using external system signals for power-on control, start to control the power only when V_I voltage becomes stable after power-on. Unstable V_I voltage may destroy the IC permanently during on/off control.

Figure 2.6 Start timing of power-off control



CHARACTERISTICS GRAPHICS

Figure 2.7 Characteristics graphics

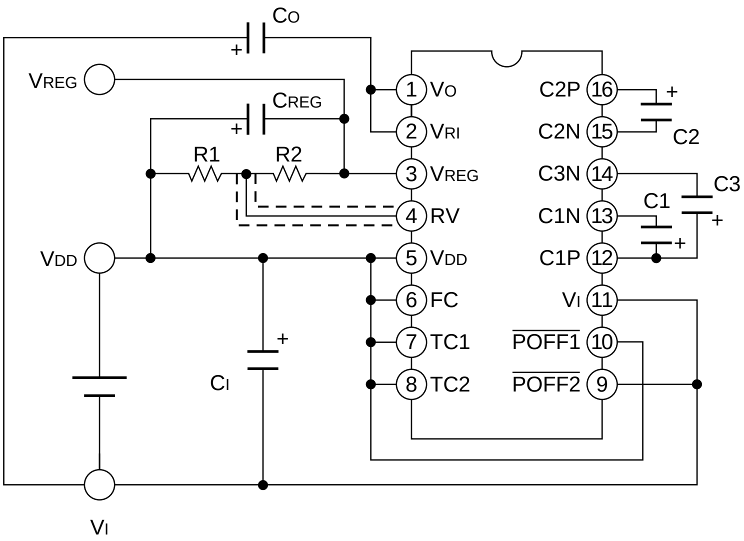


APPLICATION CIRCUIT EXAMPLES

Four-time Booster and Regulator

Figure 2.8 gives a wiring example of four-time booster and regulator that is the typical SCI7654 application. This example boosts the input voltage (VI) four times in negative direction, and outputs the regulated voltage at VREG pin.

Figure 2.8 Wiring example of 4-time booster and regulator



◊ Setup conditions of Figure 2.8
- Internal clock : On (Low Output mode)
- Booster circuit : On
- Regulator : On (if CT = –0.04%/°C)

◊ Power-off procedure
- Set the $\overline{\text{POFF1}}$ pin to logical low (VI) to turn off all circuits.

◊ Regulator
- For the regulator setup and notes, see the “voltage regulator circuit” section.

◊ Application in other setup conditions

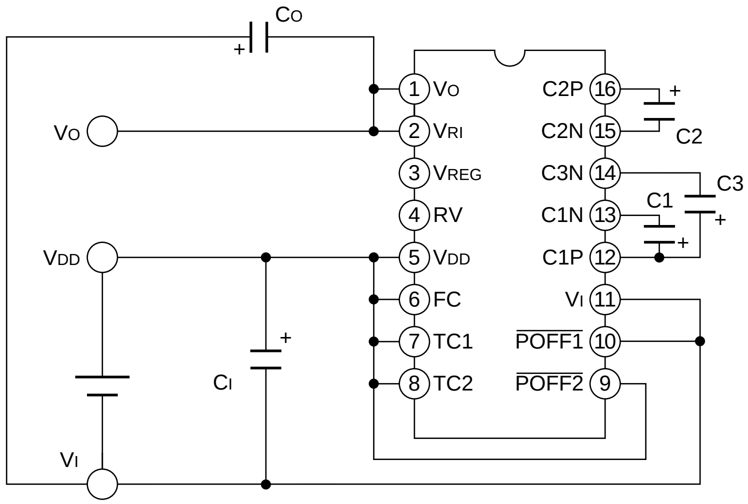
① When used in the High Output mode
- Connect the FC pin to the VI pin.

② When changing the temperature coefficient (CT)
- Change the TC1 and TC2 pin setup by following the definition of Table 2.7.

4-time Booster

Only the booster circuit operates, and it boosts the input voltage (V_I) four times in negative direction and outputs it at the V_O pin. As the regulator is not used, the voltage appearing at the V_O pin may contain ripple components. Figure 2.9 gives a wiring example.

Figure 2.9 Wiring example of 4-time booster

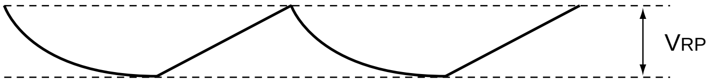


◇ Setup conditions of Figure 2.9
- Internal clock : On (Low Output mode)
- Booster circuit : On
- Regulator : Off

◇ Power-off procedure
- Set the $\overline{POFF2}$ pin to low (V_I) to turn off all circuits.

◇ Ripple voltage
- As the output at V_O pin is unstable, it can contain ripple components as shown in Figure 2.10. The ripple voltage (V_{RP}) increases according to the load current, and it can roughly be calculated by equation (4).

Figure 2.10 Ripple waveforms



$$V_{RP} = \frac{I_O}{2 \cdot f_{CL} \cdot C_O} + I_O \cdot R_{COUT} \qquad \cdots\cdots \text{ Equation (4)}$$

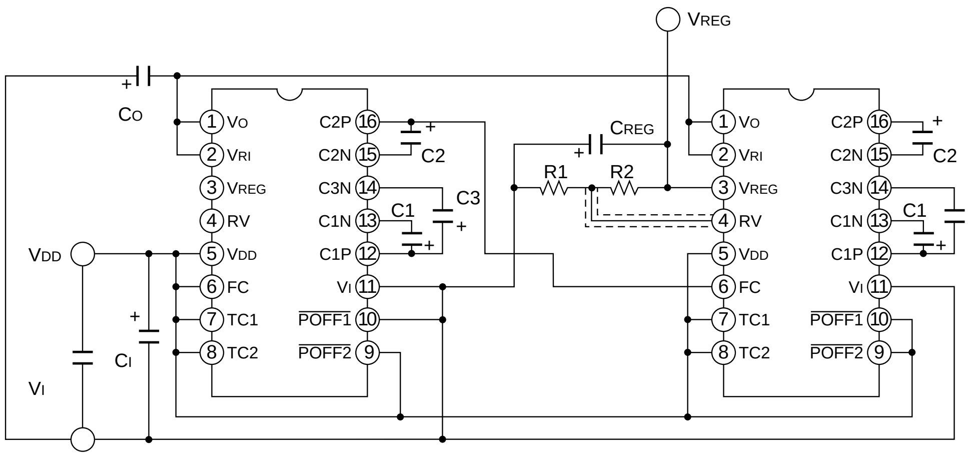
where,
I_O : Load current (A)
f_{CL} : Clock frequency (Hz)
R_{COUT} : Serial equivalent resistance (Ω) of output capacitor C_O

◊ Application in other setup conditions
① When used in the High Output mode
• Connect the FC pin to the V_I pin.

Parallel Connection (for Increased Boosting)

The parallel connection is useful for reduction of booster output impedance or reduction of ripple voltage. In the parallel connection of "n" lines, the booster output impedance can be reduced to approximately "1/n". Only the smoothing capacitor (C_O) for booster output can be used commonly in the parallel connection. When using the regulator, use only one of "n" SCI7654 chips which are in parallel connection. (If multiple regulators are operated in parallel mode, the reactive current consumption occurs.) Figure 2.11 gives a wiring example of 4-time booster and regulator where two SCI7654's are parallelly connected.

Figure 2.11 Parallel connection example



◊ Setup conditions of Figure 2.11

First stage		Second stage	
• Internal clock	: On (Low Output mode)	• Internal clock	: Off
• Booster circuit	: On	• Booster circuit	: On
• Regulator	: Off	• Regulator	: On (if CT = –0.04%/°C)

◊ Power-off procedure

- In Figure 2.11, when the $\overline{\text{POFF2}}$ pin of the first-stage SCI7654 is set to low (V_I), voltage boosting is stopped at the first and second stages. However, the regulator at the second stage does not stop. Therefore, the voltage that is approximately V_I appears at V_{REG} pin during $|V_{REG}| > |V_I|$ setup.
- To set the V_{REG} pin to high-impedance state, set both $\overline{\text{POFF1}}$ and $\overline{\text{POFF2}}$ pins to low at the first and second stages.

◊ Application in other setup conditions

① When used in the High Output mode
- Connect the FC pin of the first-stage SCI7654 to the V_I pin.

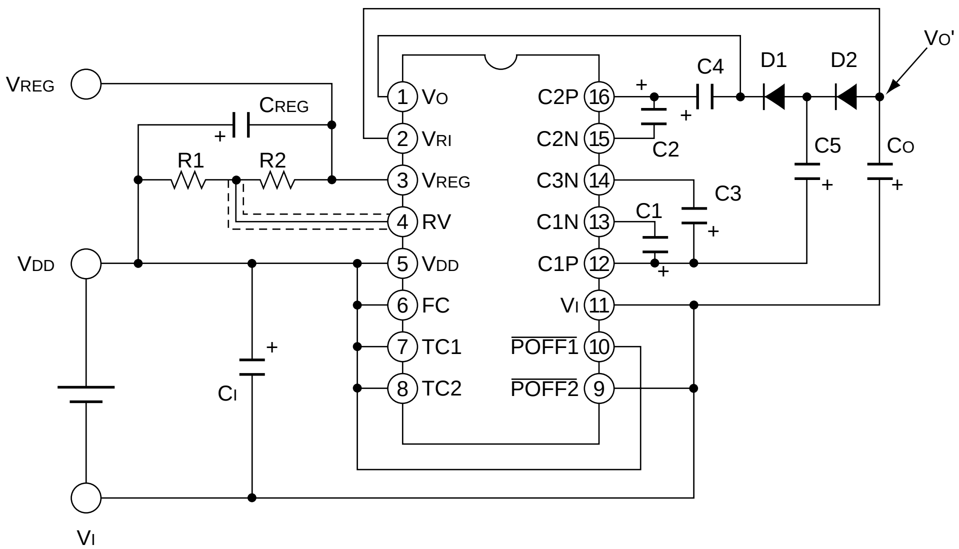
② When changing the temperature coefficient (CT)
- Change the TC1 and TC2 pin setup by following the definition of Table 2.7.

Larger Time Boosting Using Diodes

The SCI7654 can be configured to have the five-time or larger voltage boosting and regulation by adding external diodes. As the booster output impedance increases due to the diode forward voltage drop (V_F), the diodes having a smaller V_F are recommended to use.

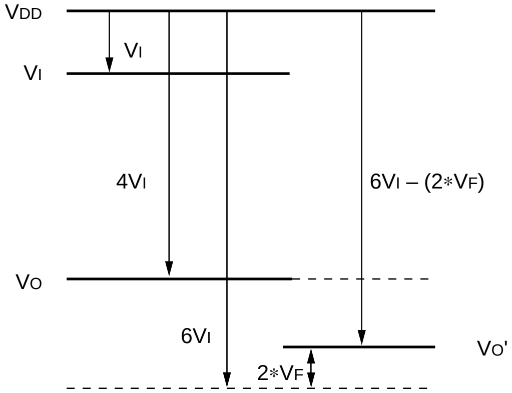
Figure 2.12 gives a wiring example of 6-time booster and regulator that use two diodes. The wiring between V_O and V_{RI} must be minimal. Figure 2.13 provides the potential relationship.

Figure 2.12 Wiring example for 6-time boosting using diodes



◊ Setup conditions of Figure 2.12
• Internal clock : On (Low Output mode)
• Booster circuit : On
• Regulator : On (if CT = –0.04%/°C)

Figure 2.13 Potential relationship during 6-time boosting using diodes



◊ Power-off procedure
• Set the $\overline{\text{POFF1}}$ pin to low (V_I) to turn off all circuits.

◊ Output voltages
• When diodes are used for voltage boosting, the characteristics of diodes directly affect on the voltage boosting characteristics. The forward voltage drop (V_F) of diodes can reduce the booster output voltage. As the example of Figure 2.12 uses two diodes, the drop of "V_F" voltage multiplied by two occurs as shown in Figure 2.13. The booster output voltage is expressed by equation (5).
To increase the $|V_O'|$ value, use the diodes having a smaller V_F.

$$| V_O' | = 6 \times | V_I | - 2 \times V_F \qquad \bullet\bullet\bullet\bullet \text{ Equation (5)}$$

◊ Notes
① Input and output current conditions
To satisfy the input and output current ratings, limit the total current does not exceed the rated input current. The total current means the total boost time multiplied by the output load current. The example of Figure 2.12 has the maximum load current of 13.3 mA (= 80 mA divided by 6).

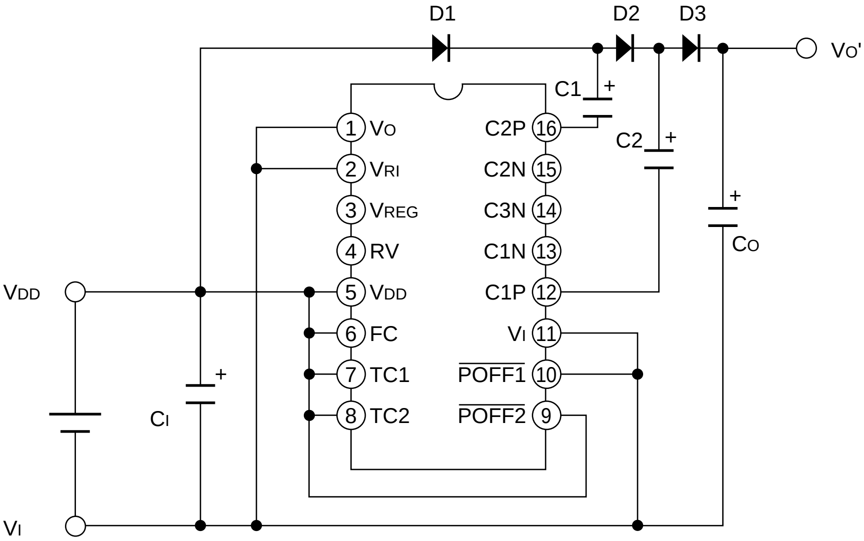
② Input and output voltage conditions
To satisfy the input and output voltage ratings, take care not to violate the electric potential relationship of higher time boosting using diodes. The example of Figure 2.12 must have the "V_I" that can satisfy the input voltage conditions during 6-time boosting (see Table 2.3).

◊ Application in other setup conditions
① When used in the High Output mode
Connect the FC pin to the V_I pin.
② When changing the temperature coefficient (CT)
Change the TC1 and TC2 pin setup by following the definition of Table 2.7.

Positive Voltage Conversion

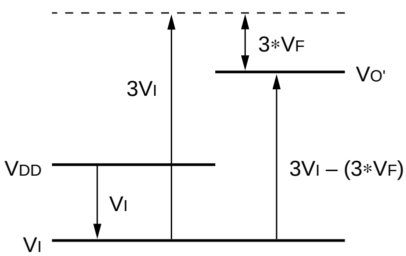
The SCI7654 can also boost up a voltage to the positive potential using external diodes. In such case, however, the regulator function is unavailable. Figure 2.14 gives a wiring example for three-time positive boosting, and Figure 2.15 provides its electrical potential relationship.

Figure 2.14 Wiring example of positive voltage conversion (3-time boosting)



◊ Setup conditions of Figure 2.14
- Internal clock : On (Low Output mode)
- Booster circuit : On
- Regulator : Off

Figure 2.15 Potential relationship during positive voltage conversion (3-time boosting)



◊ Power-off procedure
- Set the $\overline{\text{POFF2}}$ pin to low (V_I) to turn off all circuits.

◊ Two-time boosting
- To boost up a voltage two times, remove capacitor C1 and diode D1 of Figure 2.14, and connect the anode of diode D2 to the V_{DD} pin.

◊ Output voltages

• When diodes are used for voltage boosting, the characteristics of diodes directly affect on the voltage boosting characteristics. The forward voltage drop (V_F) of diodes can reduce the booster output voltage. As the example of Figure 2.14 uses three diodes, the drop of "V_F" voltage multiplied by three occurs. The booster output voltage is expressed by equation (5).
To increase the $|V_O'|$ value, use the diodes having a smaller V_F.

$$| V_O' | = 3 \times | V_I | - (3 \times V_F) \qquad \text{• • • • Equation (6)}$$

◊ Notes

① Input and output current conditions
To satisfy the input and output current ratings, take care to limit the input current below the ratings.

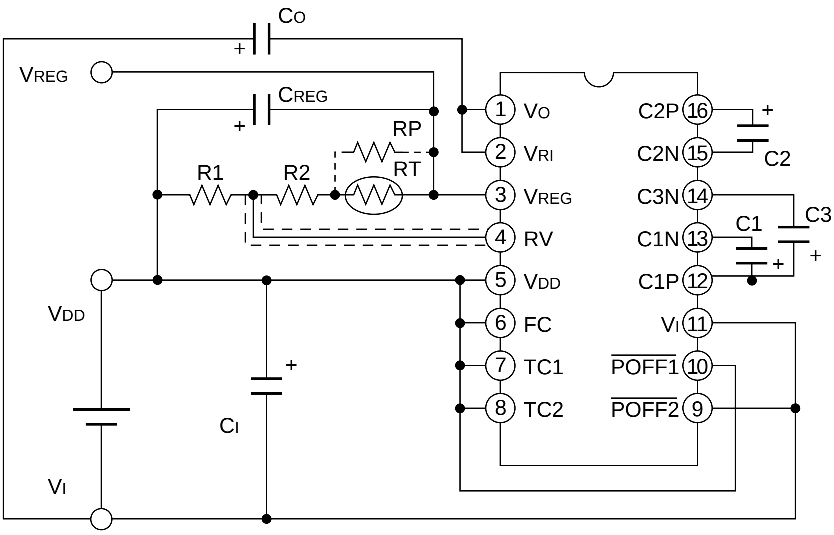
② Input and output voltage conditions
During forward voltage conversion, the input voltage ratings are the same as two-time negative voltage boosting (see Table 2.3).

◊ Application in other setup conditions
When used in the High Output mode, connect the FC pin to the V_I pin.

Wiring Example When Changing the Regulator Temperature Coefficient

The temperature coefficient of the regulator depends on the temperature coefficient of the internal reference voltage. To set another temperature coefficient, use a thermistor resistor or others as shown in Figure 2.16.

Figure 2.16 Wiring example when changing the regulator temperature coefficient



◊ Setup conditions of Figure 2.16
- Internal clock : On (Low Output mode)
- Booster circuit : On
- Regulator : On
- Thermistor resistor : RT

◊ Power-off procedure
- Set the $\overline{\text{POFF1}}$ pin to low (V_I) to turn off all circuits.

◊ Regulator temperature coefficient
- For the regulator setup and notes, see the "voltage regulator circuit" section of the function.
- The thermistor resistor (RT) has the non-linear temperature characteristics. To correct them to the linear characteristics, insert the RP as shown Figure 2.16.

◊ Application in other setup conditions
- When used in the High Output mode, connect the FC pin to the V_I pin.

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3.

Voltage Regulator