SED1230 Series
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

The SED1230 Series is a dot matrix LCD controller driver for character display, and can display a maximum of 48 characters, 4 user-defined characters, and a maximum of 64 symbols by means of 4-bit, 8-bit or serial data sent from a microcomputer.
A built-in character generator ROM is prepared for 256 character types, and each character font consists of 5 × 7 dots. A user-defined character RAM for four characters of 5 × 7 dots are incorporated, and a symbol register is also incorporated. With these, it is possible to apply this Series to display with a high degree of freedom. This Series can operate handy units with a minimum power consumption by means of its low power consumption and standby mode.
The SED1230 Series are classified into SED1230, SED1231, SED1232, and SED1233 depending on the duty of use and the number of display columns.

FEATURES

- Built-in display RAM
  48 characters + 4 user-defined characters + 64 symbols
- CG ROM (for up to 256 characters), CG RAM (4 characters), and symbol register (64 symbols)
- Number of display columns × number of lines
  (12 columns + 1 column for signal) × 4 lines + 52 symbols: SED1230
  (12 columns + 1 column for signal) × 3 lines + 52 symbols: SED1231
  (12 columns + 1 column for signal) × 2 lines + 52 symbols: SED1232
  16 columns × 2 lines + 64 symbols: SED1233
- CR oscillation circuit (on-chip C and R)
- High-speed MPU interface
  Interfacing with both 68 series and 80 series MPU
  Interfacing in 4 bits/8 bits
- Serial interface
- Character font 5 × 7 dots
- Duty ratio 1/16 (SED1232, SED1233)
  1/23 (SED1231)
  1/30 (SED1230)
- Simple command setting
- Built-in liquid crystal driving power circuit
  Power boosting circuit, power regulating circuit, voltage follower × 4
- Built-in electronic volume function
- Low power consumption
  100 μA Max. (In normal operation mode: Including the operating current of the built-in power supply)
  20 μA Max. (In standby display mode)
- Power supply
  V_{DD} - V_{SS} (logic section): –2.4 V to –3.6 V
  V_{DD} - V_5 (liquid crystal drive section)
  : –5.0 V to –11.0 V
- Wide operating temperature range
  Ta = -30 to 85°C
- CMOS process
- Delivery form: Chip SED123∗D$_{*B}$, SED123∗D$_{*E}$, SED123∗D$_{*G}$ (Gold bump product)
  SED123∗D$_{*A}$, SED123∗D$_{*C}$, SED123∗D$_{*F}$ (A1 pad product)
  TCP SED123∗T$_{**}$
- This IC is not designed with a protection against radioactive rays.

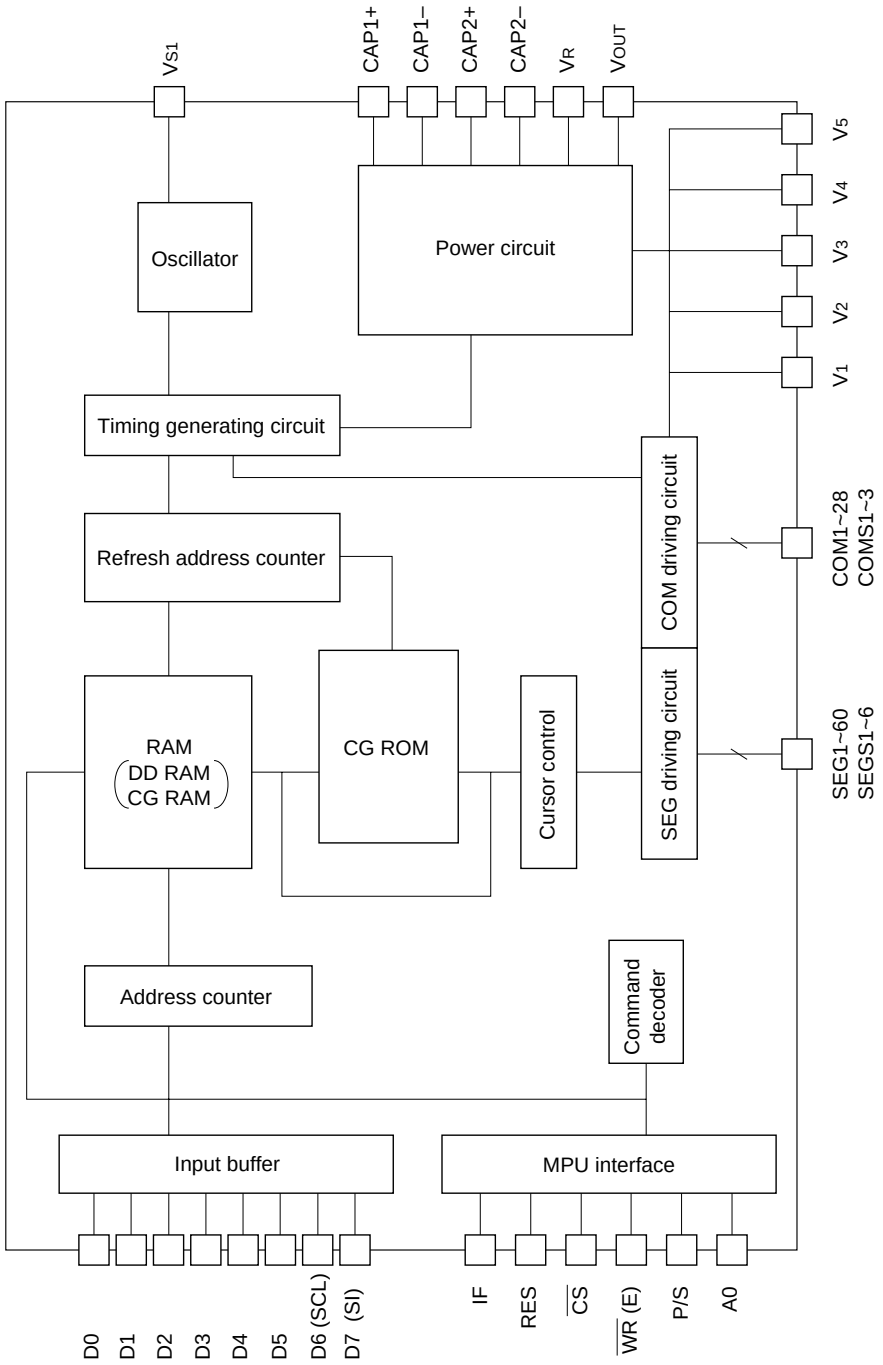
SED1230 Series Chip Specifications

Product name	Duty	No. of digits indicated	No. of lines indicated	Font	V_{REG} temperature slope	Chip thickness	Form at delivery
SED1230D$_{BB}$	1/30	12 columns + 1 column for signal	4 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1230D$_{GB}$	1/30	12 columns + 1 column for signal	4 lines	Table 7 SED123*D$_{G*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1230D$_{GE}$	1/30	12 columns + 1 column for signal	4 lines	Table 7 SED123*D$_{G*}$	–0.17%/°C	525µm	Gold Bump Chip
SED1230D$_{JB}$	1/30	12 columns + 1 column for signal	4 lines	Table 5 SED123*D$_{A*}$	–0.04%/°C	625µm	Gold Bump Chip
SED1230D$_{RE}$	1/30	12 columns + 1 column for signal	4 lines	Table 6 SED123*D$_{B*}$	External Input	525µm	Gold Bump Chip
SED1231D$_{AB}$	1/23	12 columns + 1 column for signall	3 lines	Table 5 SED123*D$_{A*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1231D$_{BE}$	1/23	12 columns + 1 column for signal	3 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	525µm	Gold Bump Chip
SED1231D$_{JB}$	1/23	12 columns + 1 column for signal	3 lines	Table 5 SED123*D$_{A*}$	–0.04%/°C	625µm	Gold Bump Chip
SED1231D$_{MB}$	1/23	12 columns + 1 column for signal	3 lines	Table 5 SED123*D$_{A*}$	External Input	625µm	Gold Bump Chip
SED1232D$_{AB}$	1/16	12 columns + 1 column for signal	2 lines	Table 5 SED123*D$_{A*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1232D$_{BB}$	1/16	12 columns + 1 column for signal	2 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1232D$_{GB}$	1/16	12 columns + 1 column for signal	2 lines	Table 7 SED123*D$_{G*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1232D$_{MB}$	1/16	12 columns + 1 column for signal	2 lines	Table 5 SED123*D$_{A*}$	External Input	625µm	Gold Bump Chip
SED1233D$_{AE}$	1/16	16 columns	2 lines	Table 5 SED123*D$_{A*}$	–0.17%/°C	525µm	Gold Bump Chip
SED1233D$_{BB}$	1/16	16 columns	2 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1233D$_{BE}$	1/16	16 columns	2 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	525µm	Gold Bump Chip
SED1233D$_{GB}$	1/16	16 columns	2 lines	Table 7 SED123*D$_{G*}$	–0.17%/°C	625µm	Gold Bump Chip
SED1233D$_{GE}$	1/16	16 columns	2 lines	Table 7 SED123*D$_{G*}$	–0.17%/°C	525µm	Gold Bump Chip
SED1233D$_{MB}$	1/16	16 columns	2 lines	Table 5 SED123*D$_{A*}$	External Input	625µm	Gold Bump Chip
SED1233D$_{RA}$	1/16	16 columns	2 lines	Table 6 SED123*D$_{B*}$	External Input	625µm	AL-PAD chip
SED1233D$_{2E}$	1/16	16 columns	2 lines	Table 7 SED123*D$_{G*}$	External Input	525µm	Gold Bump Chip
SED1233D$_{3E}$	1/16	16 columns	2 lines	Table 7 SED123*D$_{G*}$	–0.04%/°C	525µm	Gold Bump Chip

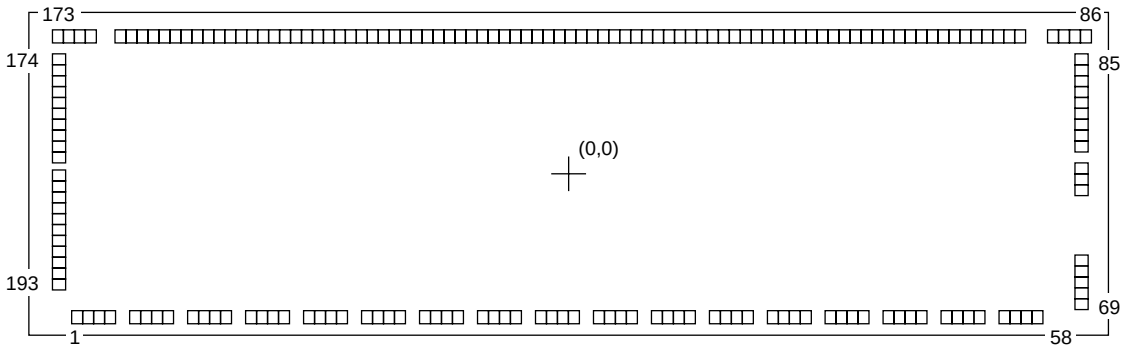
SED1230 Series TCP Specifications

Product name	Duty	No. of digits indicated	No. of lines indicated	Font	V_{REG} temperature slope	Form at delivery
SED1230T$_{01}$	1/30	12 columns + 1 columns for signal	4 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	TCP, 35mm 9IP
SED1230T$_{0A}$	1/30	12 columns + 1 column for signal	4 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	TCP, 48mm 3IP
SED1230T$_{0B}$	1/30	12 columns + 1 column for signal	4 lines	Table 5 SED123*D$_{A*}$	–0.04%/°C	TCP, 48mm 3IP
SED1231T$_{01}$	1/23	12 columns + 1 column for signal	3 lines	Table 5 SED123*D$_{A*}$	–0.04%/°C	TCP, 35mm 9IP
SED1231T$_{02}$	1/23	12 columns + 1 column for signal	3 lines	Table 5 SED123*D$_{A*}$	–0.04%/°C	TCP, 35mm 9IP
SED1231T$_{0B}$	1/23	12 columns + 1 column for signal	3 lines	Table 5 SED123*D$_{A*}$	External Input	TCP, 48mm 3IP
SED1233T$_{0A}$	1/16	16 columns	2 lines	Table 6 SED123*D$_{B*}$	–0.17%/°C	TCP, 48mm 3IP
SED1233T$_{0B}$	1/16	16 columns	2 lines	Table 5 SED123*D$_{A*}$	–0.17%/°C	TCP, 48mm 3IP

BLOCK DIAGRAM



CHIP SPECIFICATION



SED1230D**	1/30 duty	12 columns + 1 signal column
SED1231D**	1/23 duty	12 columns + 1 signal column
SED1232D**	1/16 duty	12 columns + 1 signal column
SED1233D**	1/16 duty	16 columns

↑
#1 Column for CG ROM pattern change

Chip size:	10.23 × 3.11 mm
Pad pitch:	110 µm (Min.)
Chip thickness:	625 (SED123∗D∗A, SED123∗D∗B)
	525 (SED123∗D∗C, SED123∗D∗E)

1) A1 pad specification (SED123∗D∗A)
   Pad size: A 86 µm × 135 µm
   B 135 µm × 86 µm
2) Au bump specification (SED123∗D∗B)
   For reference:
   Bump size A 80 µm × 129 µm
   B 129 µm × 80 µm
   Bump height 22.5 µm

<SED1230D$_{**}$>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SSL}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SSR}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	COM 8	4347	↓
91	COM 9	4237	↓
92	COM10	4127	↓
93	COM11	4017	↓
94	COM12	3906	↓
95	COM13	3796	↓
96	COM14	3686	↓
97	SEGS2	3576	↓
98	SEGS3	3466	↓
99	SEGS4	3355	↓
100	SEG 1	3245	↓
101	SEG 2	3135	↓
102	SEG 3	3025	↓
103	SEG 4	2915	↓
104	SEG 5	2804	↓
105	SEG 6	2694	↓
106	SEG 7	2584	↓
107	SEG 8	2474	↓
108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	–1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	COM28	–3697	1382
164	COM27	–3808	
165	COM26	–3918	
166	COM25	–4028	
167	COM24	–4138	
168	COM23	–4248	
169	COM22	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 to the floating state.

<SED1231D$_{**}$>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SSL}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SSR}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	COM 8	4347	↓
91	COM 9	4237	↓
92	COM10	4127	↓
93	COM11	4017	↓
94	COM12	3906	↓
95	COM13	3796	↓
96	COM14	3686	↓
97	SEGS2	3576	↓
98	SEGS3	3466	↓
99	SEGS4	3355	↓
100	SEG 1	3245	↓
101	SEG 2	3135	↓
102	SEG 3	3025	↓
103	SEG 4	2915	↓
104	SEG 5	2804	↓
105	SEG 6	2694	↓
106	SEG 7	2584	↓
107	SEG 8	2474	↓
108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164		–3808	
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM21	–4940	1136
175	COM20		1026
176	COM19		916
177	COM18		806
178	COM17		696
179	COM16		585
180	COM15		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 and 163 to 169 to the floating state.

<SED1232D$_{**}$>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SSL}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SSR}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	COM 8	4347	↓
91	COM 9	4237	↓
92	COM10	4127	↓
93	COM11	4017	↓
94	COM12	3906	↓
95	COM13	3796	↓
96	COM14	3686	↓
97	SEGS2	3576	↓
98	SEGS3	3466	↓
99	SEGS4	3355	↓
100	SEG 1	3245	↓
101	SEG 2	3135	↓
102	SEG 3	3025	↓
103	SEG 4	2915	↓
104	SEG 5	2804	↓
105	SEG 6	2694	↓
106	SEG 7	2584	↓
107	SEG 8	2474	↓
108	SEG 9	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG10	2253	1382
110	SEG11	2143	
111	SEG12	2033	
112	SEG13	1923	
113	SEG14	1813	
114	SEG15	1702	
115	SEG16	1592	
116	SEG17	1482	
117	SEG18	1372	
118	SEG19	1262	
119	SEG20	1151	
120	SEG21	1041	
121	SEG22	931	
122	SEG23	821	
123	SEG24	711	
124	SEG25	600	
125	SEG26	490	
126	SEG27	380	
127	SEG28	270	
128	SEG29	160	
129	SEG30	49	
130	SEG31	–61	
131	SEG32	–171	
132	SEG33	–281	
133	SEG34	–391	
134	SEG35	–502	
135	SEG36	–612	
136	SEG37	–722	
137	SEG38	–832	
138	SEG39	–942	
139	SEG40	–1053	
140	SEG41	–1163	
141	SEG42	–1273	
142	SEG43	–1383	
143	SEG44	–1493	
144	SEG45	–1604	
145	SEG46	–1714	
146	SEG47	–1824	
147	SEG48	–1934	
148	SEG49	–2044	
149	SEG50	–2155	
150	SEG51	–2265	
151	SEG52	–2375	
152	SEG53	–2485	
153	SEG54	–2595	
154	SEG55	–2706	
155	SEG56	–2816	
156	SEG57	–2926	
157	SEG58	–3036	
158	SEG59	–3146	
159	SEG60	–3257	
160	SEGS4	–3367	
161	SEGS5	–3477	
162	SEGS6	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	(NC)	–3697	1382
164		–3808	
165		–3918	
166		–4028	
167		–4138	
168		–4248	
169		–4359	
170		–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM14	–4940	1136
175	COM13		1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	A0		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 and 163 to 169 to the floating state.

<SED1233D$_{**}$>

Unit: µm

PAD		COORDINATES	
No.	Name	X	Y
1	(NC)	–4793	–1371
2	↓	–4683	↓
3	↓	–4572	↓
4	↓	–4462	↓
5	V_{DD}	–4242	↓
6	↓	–4132	↓
7	↓	–4021	↓
8	↓	–3911	↓
9	V_{SSL}	–3691	↓
10	↓	–3581	↓
11	↓	–3470	↓
12	↓	–3360	↓
13	V_5	–3140	↓
14	↓	–3030	↓
15	↓	–2919	↓
16	↓	–2809	↓
17	V_4	–2589	↓
18	↓	–2479	↓
19	↓	–2368	↓
20	↓	–2258	↓
21	V_3	–2021	↓
22	↓	–1910	↓
23	↓	–1800	↓
24	↓	–1690	↓
25	V_2	–1453	↓
26	↓	–1342	↓
27	↓	–1232	↓
28	↓	–1122	↓
29	V_1	–884	↓
30	↓	–774	↓
31	↓	–664	↓
32	↓	–554	↓
33	V_0	–316	↓
34	↓	–206	↓
35	↓	–96	↓
36	↓	14	↓
37	V_R	235	↓
38	↓	345	↓
39	↓	455	↓
40	↓	565	↓
41	V_{OUT}	803	↓
42	↓	913	↓
43	↓	1023	↓
44	↓	1133	↓
45	CAP2-	1354	↓
46	↓	1464	↓
47	↓	1574	↓
48	↓	1684	↓
49	CAP2+	1905	↓
50	↓	2015	↓
51	↓	2125	↓
52	↓	2235	↓
53	CAP1-	2473	↓
54	↓	2583	↓

PAD		COORDINATES	
No.	Name	X	Y
55	CAP1–	2693	–1371
56	↓	2803	↓
57	CAP1+	3024	↓
58	↓	3134	↓
59	↓	3244	↓
60	↓	3354	↓
61	V_{SSR}	3592	↓
62	↓	3702	↓
63	↓	3812	↓
64	↓	3923	↓
65	V_{DD}	4143	↓
66	↓	4253	↓
67	↓	4363	↓
68	↓	4474	↓
69	(NC)	4883	–1343
70	(NC)	↓	–1233
71	(NC)	↓	–1123
72	(NC)	↓	–1013
73	V_{S1}	4929	–902
74	P/S	↓	–186
75	IF	↓	–76
76	RES	↓	34
77	COMS1	↓	255
78	COMS2	↓	365
79	COM 1	↓	475
80	COM 2	↓	585
81	COM 3	↓	696
82	COM 4	↓	806
83	COM 5	↓	916
84	COM 6	↓	1026
85	COM 7	↓	1136
86	(NC)	4947	1382
87	↓	4836	↓
88	↓	4726	↓
89	↓	4616	↓
90	SEG 1	4347	↓
91	SEG 2	4237	↓
92	SEG 3	4127	↓
93	SEG 4	4017	↓
94	SEG 5	3906	↓
95	SEG 6	3796	↓
96	SEG 7	3686	↓
97	SEG 8	3576	↓
98	SEG 9	3466	↓
99	SEG10	3355	↓
100	SEG11	3245	↓
101	SEG12	3135	↓
102	SEG13	3025	↓
103	SEG14	2915	↓
104	SEG15	2804	↓
105	SEG16	2694	↓
106	SEG17	2584	↓
107	SEG18	2474	↓
108	SEG19	2364	↓

PAD		COORDINATES	
No.	Name	X	Y
109	SEG20	2253	1382
110	SEG21	2143	
111	SEG22	2033	
112	SEG23	1923	
113	SEG24	1813	
114	SEG25	1702	
115	SEG26	1592	
116	SEG27	1482	
117	SEG28	1372	
118	SEG29	1262	
119	SEG30	1151	
120	SEG31	1041	
121	SEG32	931	
122	SEG33	821	
123	SEG34	711	
124	SEG35	600	
125	SEG36	490	
126	SEG37	380	
127	SEG38	270	
128	SEG39	160	
129	SEG40	49	
130	SEG41	–61	
131	SEG42	–171	
132	SEG43	–281	
133	SEG44	–391	
134	SEG45	–502	
135	SEG46	–612	
136	SEG47	–722	
137	SEG48	–832	
138	SEG49	–942	
139	SEG50	–1053	
140	SEG51	–1163	
141	SEG52	–1273	
142	SEG53	–1383	
143	SEG54	–1493	
144	SEG55	–1604	
145	SEG56	–1714	
146	SEG57	–1824	
147	SEG58	–1934	
148	SEG59	–2044	
149	SEG60	–2155	
150	SEG61	–2265	
151	SEG62	–2375	
152	SEG63	–2485	
153	SEG64	–2595	
154	SEG65	–2706	
155	SEG66	–2816	
156	SEG67	–2926	
157	SEG68	–3036	
158	SEG69	–3146	
159	SEG70	–3257	
160	SEG71	–3367	
161	SEG72	–3477	
162	SEG73	–3587	

PAD		COORDINATES	
No.	Name	X	Y
163	SEG74	–3697	1382
164	SEG75	–3808	
165	SEG76	–3918	
166	SEG77	–4028	
167	SEG78	–4138	
168	SEG79	–4248	
169	SEG80	–4359	
170	(NC)	–4627	
171		–4738	
172		–4848	
173		–4958	
174	COM14	–4940	1136
175	COM13		1026
176	COM12		916
177	COM11		806
178	COM10		696
179	COM 9		585
180	COM 8		475
181	COMS3		365
182	SEGS1		255
183	$\overline{A0}$		34
184	$\overline{WR}$		–76
185	CS		–186
186	D7		–296
187	D6		–406
188	D5		–517
189	D4		–627
190	D3		–737
191	D2		–847
192	D1		–957
193	D0		–1068

Note 1 : Be sure to connect the pins V_{SSL} and V_{SSR} outside. They are called V_{SS} in the following text descriptions.

2 : Set the pins of Nos. 69 to 72 to the floating state.

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
V_{DD}	Power supply	Logic + power pin. Also used as MPU power pin V_{CC}.	2
V_{SS}	Power supply	Logic – power pin. Connected to the system GND.	2
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined in the liquid crystal cell is resistance-divided or impedance-converted by operational amplifier, and the resultant voltage is applied. The potential is determined on the basis of V_{DD} and the following equation must be respected. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to pins V_1 to V_4 by built-in power circuit: $V_1 = 1/5\ V_5$ $V_2 = 2/5\ V_5$ $V_3 = 3/5\ V_5$ $V_4 = 4/5\ V_5$	6
V_{S1}	O	Power supply voltage output pin for oscillating circuit. Don't connect this pin to an external load.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Capacitor positive side connecting pin for boosting. This pin connects the capacitor with pin CAP1–.	1
CAP1–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP+.	1
CAP2+	O	Capacitor positive side connecting pin for boosting. This pin connects a capacitor with pin CAP2–.	1
CAP2–	O	Capacitor negative side connecting pin for boosting. This pin connects a capacitor with pin CAP2+.	1
V_{OUT}	O	Output pin for boosting. This pin connects a smoothing capacitor with V_{SS} pin.	1
V_R	I	Voltage regulating pin. This pin gives a voltage between V_{DD} and V_5 by resistance-division of voltage.	1

Pins for System Bus Connection

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 ~ D0</td><td>I</td><td>8-bit input data bus. These pins are connected to a 8-bit or 16-bit standard MPU data bus.
When P/S = “Low”, the D7 and D6 pins are operated as a serial data input and a serial clock input respectively.
<table>
<tr><td>P/S</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“Low”</td><td>SI</td><td>SCL</td><td>—</td><td>$\overline{CS}$</td><td>A0</td></tr>
<tr><td>“High”</td><td>D7</td><td>D6</td><td>D5 ~ D0</td><td>$\overline{CS}$</td><td>A0</td></tr>
</table>
When P/S = “Low,” be sure to fix D5 to D0 to “High” or “Low.”</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually, this pin connects the least significant bit of the MPU address bus and identifies a data command.
0 : Indicates that D0 to D7 are a command.
1 : Indicates that D0 to D7 are display data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>In case of a 68 series MPU, initialization can be performed by changing RES ↓. In case of an 80 series MPU, initialization can be performed by changing ↑.
A reset operation is performed by edge sensing of the RES signal.
An interface type for the 68/80 series MPU is selected by input level after initialization.
“L” : 68 series MPU interface
“H” : 80 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select signal. Usually, this pin inputs the signal obtained by decoding an address bus signal. At the “Low” level, this pin is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$

(E)</td><td>I</td><td><When connecting an 80 series MPU>
Active “Low”. This pin connects the $\overline{WR}$ signal of the 80 series MPU. The signal on the data bus is fetched at the rise of the $\overline{WR}$ signal.
When P/S = “Low,” be sure to fix the $\overline{WR}$ signal to “High” or “Low.”
<When connecting a 68 series MPU>
Active “High”. This pin becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin switches between serial data input and parallel data input.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Serial Clock</td></tr>
<tr><td>“High”</td><td>$\overline{CS}$</td><td>A0</td><td>D0~D7</td><td>–</td></tr>
<tr><td>“Low”</td><td>$\overline{CS}$</td><td>A0</td><td>SI</td><td>SCL</td></tr>
</table></td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>Interface data length select pin for parallel data input.
“High”: 8-bit parallel input
“Low”: 4-bit parallel input
When P/S = “Low”, connect this pin to V_{DD} or V_{SS}.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

SED1230, SED1231, SED1232

Pin name	I/O	Description	Q'ty
COM1~ COM28	O	Common signal output pin (for characters)	28
COMS1~ CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a Vss amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1~ SEG60	O	Segment signal output pin (for characters)	60
SEGS1~ SEGS6	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a Vss amplitude is output. SEGS2, SEGS6: Segment output for signal output	7

SED1233

Pin name	I/O	Description	Q'ty
COM1~ COM14	O	Common signal output pin (for characters)	14
COMS1~ CMOS3	O	Common signal output pin (except for characters) CMOS1: Common output for static drive. In the standby mode only, a Vss amplitude is output. CMOS2, CMOS3: Common output for symbol display	3
SEG1~ SEG80	O	Segment signal output pin (for characters)	80
SEGS1	O	Segment signal output pin (except for characters) SEGS1: Segment output for static drive. In the standby mode only, a Vss amplitude is output.	1

FUNCTIONAL DESCRIPTION

MPU Interface

Selection of interface type

In the SED1230 Series, data transfer is performed through a 8-bit or 4-bit data bus or a serial data input (SI). By selecting "High" or "Low" as P/S pin polarity, a parallel data input or a serial data input can be selected as shown in Table 1.

Table 1

P/S	Type	$\overline{CS}$	A0	$\overline{WR}$	SI	SCL	D0~D7
"High"	Parallel Input	$\overline{CS}$	A0	$\overline{WR}$	—	—	D0~D7
"Low"	Serial Input	$\overline{CS}$	A0	—	SI	SCL	—

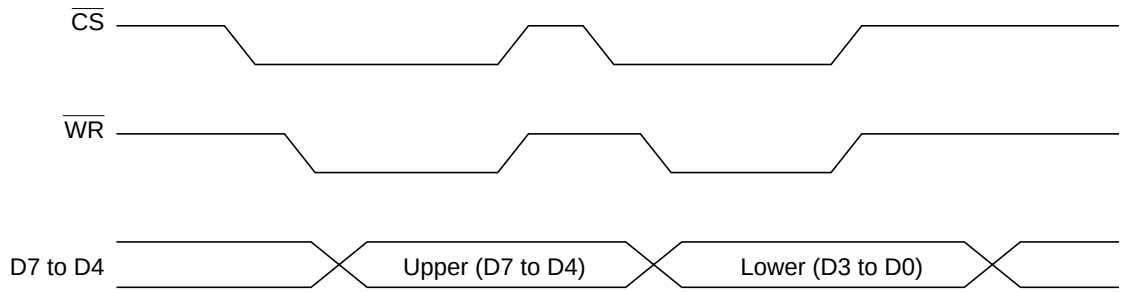
Parallel Input
In the SED1230 Series, when parallel input is selected (P/S = "High"), it can be directly connected to the 80 series MPU bus or 68 series MPU bus, as shown in Table 2, if either "High" or "Low" is selected as RES pin polarity after a reset input, because the RES pin has an MPU select function.
Selection between 8 bits and 4 bits is performed by command.

Table 2

RES input polarity	Type	A0	$\overline{WR}$	$\overline{CS}$	D0~D7
↓ active	68 series	A0	E	$\overline{CS}$	D0~D7
↑ active	80 series	A0	$\overline{WR}$	$\overline{CS}$	D0~D7

Interface with 4-bit MPU interface

When data transfer is performed by 4-bit interface (IF = 0), an 8-bit command, data and address are divided into two parts.



Note: When performing writing in succession, reverse a time exceeding the system cycle time (t_{cyc}) and then perform writing.

Serial interface (P/S = "Low")

The serial interface consists of a 8-bit shift register and a 3-bit counter and acceptance of an SI input or SCL input is enabled in the ship selected status (CS = "Low").
When no chip is selected, the shift register and counter are reset to the initial status.
Serial data is input in the order of D7, D6 .... D0 from the serial data input pin (SI) at the rise of Serial Clock (SCL).
At the rising edge of the 8th serial clock, the serial data is converted into 8-bit parallel data and this data is processed.
The A0 input is used to identify whether the serial data input (SI) is display data or a command. That is, when A0 = "High", it is regarded as display data. When A0 = "Low", it is regarded as a command.
The A0 input is read in and identified at the rise of the 8 x n-th clock of Serial Clock (SCL) after chip selection.
Fig. 1 shows a timing chart of the serial interface.
Regarding the SCL signal, special care must be exercised about terminal reflection and external noise due to a wire length. We recommend the user to perform an operation check with a real machine.
We also recommend the user to periodically refresh the write status of each command to prevent a malfunction due to noise.

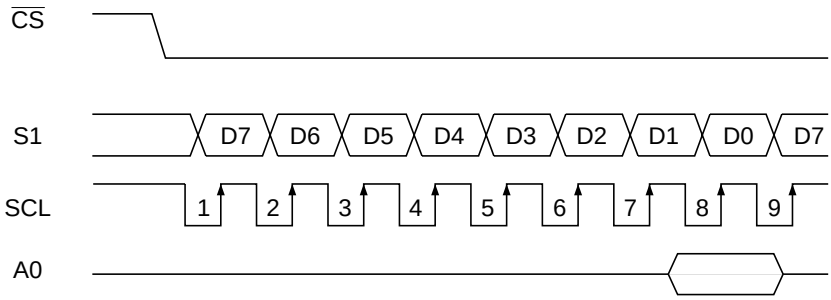


Fig. 1

Identification of data bus signals

The SED1230 series identifies data bus signals, as shown in Table 3, by combinations of A0 and $\overline{WR}$ (E).

Table 3

Common	68 series	80 series	Function
A0	E	$\overline{WR}$	
1	1	0	Writing to RAM and symbol register
0	1	0	Writing to internal register (command)

Chip select

The SED1230 series has a chip select pin ($\overline{CS}$). Only when $\overline{CS}$ = "Low", MPU interfacing is enabled.
In any status other than Chip Select, D0 to D7 and A0, $\overline{WR}$, SI and SCL inputs are invalidated. When a serial input interface is selected, the shift register and counter are reset.

However, the Reset signal is input regardless of the $\overline{CS}$ status.

Power Circuit

This is a low-power-consumption power circuit that generates a voltage required for liquid crystal drive.
The power circuit consists of a boosting circuit, voltage regulating circuit and voltage follower.

The power circuit incorporated in the SED1230 Series is set for a small-scale liquid crystal panel, so that its display quality may be greatly deteriorated if it is used for a liquid crystal panel with a large display capacity.
In this case, an external power supply must be used.

A power circuit function can be selected by power control command. With this, an external power supply and a part of the internal power supply can be used together.

	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	—	
Note 1	×	○	○	V_{OUT}	OPEN
Note 2	×	×	○	$V_5 = V_{OUT}$	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

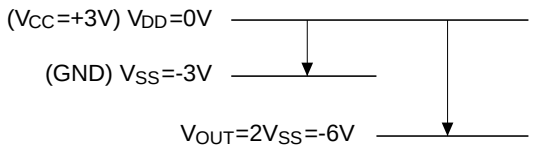
Note 1: When the boosting circuit is turned off, make boosting system pins (CAP1+, CAP1-, CAP2+, CAP2-) open and give a liquid crystal drive voltage to the VOUT pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, make the boosting system pins open, connect between the V5 pin and VOUT pin, and give a liquid crystal drive voltage from the outside.
Note 3: When all the internal power supplies are turned off, supply liquid crystal drive voltages V_1, V_2, V_3, V_4 and V_5 from the outside, and make the CAP1+, CAP1-, CAP2+, CAP2- and VOUT pins open.

Triple boosting circuit

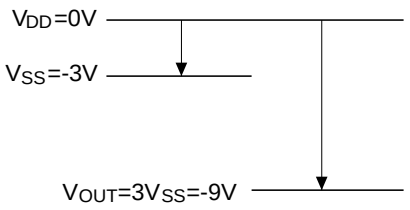
When a capacitor is connected between CAP1+ and CAP1-, between CAP2+ and CAP2-, and between V_{SS} pin and V_{OUT} pin respectively, the potential between the V_{DD} pin and V_{SS} pin is boosted triple and output to the V_{OUT} pin. In case of double boosting, remove the capacitor between CAP2+ and CAP2- in connection for triple boosting operation and strap between CAP2- and V_{OUT} pin. Then, a double boosted output can be obtained from the V_{OUT} pin (CAP2-).

The boosting circuit uses a signal from the oscillator output.

Accordingly, it is necessary that the oscillating circuit must be in operation. The potential relationship of boosting is shown below.



Potential during double boosting



Potential during triple boosting

Voltage regulating circuit

The voltage regulation circuit regulates the boosted voltage developed at Vout. It outputs the regulated LCD driving voltage at the V_5 terminal. An internal resistor can be inserted into the regulation circuit feedback loop providing the following voltage levels at the V_5 terminal.

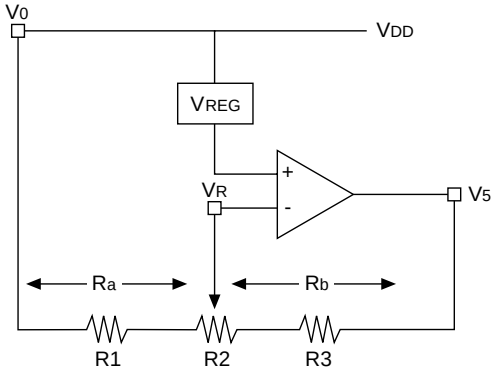
When V_5 is required to be different than the above case, leave the internal feedback resistor out of the circuit. V_5 can be regulated within a range of $|V_5|<|V_{OUT}|$. It may be calculated by the following formula:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots \textcircled{1}$$

Wherein, V_{REG} is the constant voltage source inside the SED1230 Series and the voltage is constant at $V_{REG} \fallingdotseq 3.1V$. The voltage regulation $V_{REG} \fallingdotseq 2.1V$ (TYP.) in option 1, and $V_{REG} = V_{SS}$ in option 2. Voltage regulation of the V_5 output is accomplished by connecting a variable resistor between V_R, V_{DD} and V_5. For fine adjustment of the V_5 voltage, use a combination of fixed resistors R1 and R3 and a variable resistor R2.

The voltage regulator circuit carries a temperature gradient of about -0.17%/ °C under V_{REG} outputs (standard specification), about -0.04%/°C (option). When any other temperature gradient is required, connect a thermistor in series to the output voltage regulating register.

Since the V_R terminal has a high input impedance, it is necessary to take noise suppression measures such as shortening the input wiring and shielding the wiring run.



Example 1:

Condition: $I(R1, R2, R3) \leq 5\mu A$ $V_5 = -6$ to $-8V$

Setting:
$R1+R2+R3 = 8V/5\mu A = 1.6M\Omega$
$8V = (1+Rb/Ra)\ 3.0V$ $Rb/Ra = 1.67$
$6V = (1+Rb/Ra)\ 3.0V$ $Rb/Ra = 1$
$\cdots$
$R1 = 600K\Omega$
$R2 = 200K\Omega$
$R3 = 800K\Omega$

● Voltage Regulation Circuit Using Electronic Contrast Control Register

The contrast control register controls the liquid crystal driving voltage (V_5). This is accomplished by an electronic volume control register set command that adjusts the contrast of the liquid crystal display (see section 1-22).

The commands provide 4-bits of voltage level data to the electronic volume control register. This provides for the selection of 16 different voltage levels for the liquid crystal driving voltage. When using the electronic volume control function, it is necessary to close the voltage regulation circuit using electronic control commands. For reference information, when the electronic volume control registor value is at (1, 1, 1, 1), the constant current value becomes: $I_{REF} \fallingdotseq 3.65uA$.

[An exemplary constant setting when the electronic volume control function is being used]

$$V_5 = \left(1 + \frac{R_b}{R_c}\right) \cdot V_{REG} \quad \cdots\cdots\cdots\cdots\cdots\cdots \textcircled{2}$$

$$\therefore\ R_c = \frac{R_a \times R_I}{R_a + R_I}$$

$$R_I = \frac{V_R}{I_{REF}}$$

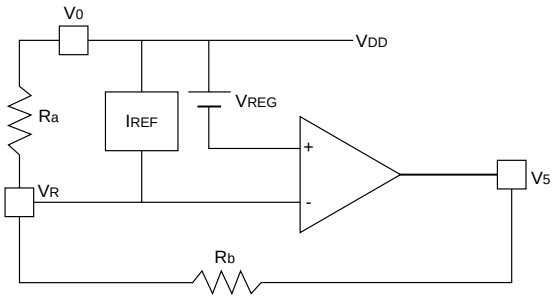


Fig. 9

(1) Determining the V_5 voltage setting range by the electronic volume control
Liquid crystal driving voltage V_5: max. -6V ~ min. -8V
V_5 variable voltage range: 2V

(2) Determining the R_b
R_b = V_5 variable voltage range/ I_{REF} ($I_{REF} \fallingdotseq 3.65\mu A$ Constant current)
= 2V/3.65μA
= 548KΩ

(3) Determining the R_a

$$R_a = \frac{V_{REG}}{(V_5 \text{ voltage setting max} - V_{REG}) / R_b}$$ (Use absolute values for V_{REG} and V_5 voltage settings.)

$$= \frac{3.1V}{(6V - 3.1V) / 548K\Omega}$$

= 585KΩ

(4) Regulating the R_a
Set the electronic volume control register to (D3, D2, D1, D0) = (1, 0, 0, 0) or (0, 1, 1, 1) before matching the R_a value to the optimum contrast.

Since I_{REF} is a simplified constant voltage source, fluctuations upto ± 40% must be taken into consideration, as a dispersion range during manufacture. Meanwhile, the temperature dependency of I_{REF} is: $\Delta I_{REF} \fallingdotseq -0.037\mu A/°C$. Determine the R_a and R_b for the using LCD panel in consideration of the above dispersion and the variation by the temperature.

When using the electronic volume control function, in order to compensate the V_5 voltage for dispersion of V_{REG} and I_{REF}, use a variable registor as R_a and perform optimum contrast adjustment according to the above item (4) with each IC chip.

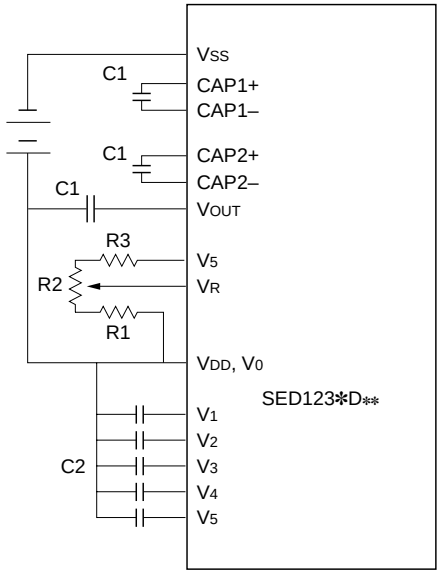
When the electronic volume control function is not being used, set the electronic volume control register to (0, 0, 0, 0) using the RES signal or the electronic volume control register setting command.

Liquid crystal voltage generating circuit

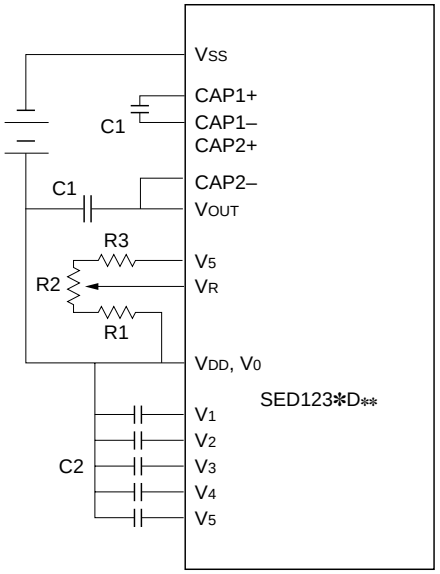
The V_5 potential is resistance-divided inside the IC so that V_1, V_2, V_3 and V_4 potentials are generated for liquid crystal drive.
Furthermore, the V_1, V_2, V_3 and V_4 are impedance-converted by voltage follower and the then supplied to the liquid crystal drive circuit.
The liquid crystal drive voltage is fixed to 1/5 bias.

As shown in the diagrams below, the capacitor (C2) for voltage stabilization must be externally connected to the V1 to V5 pins of liquid crystal power pins.

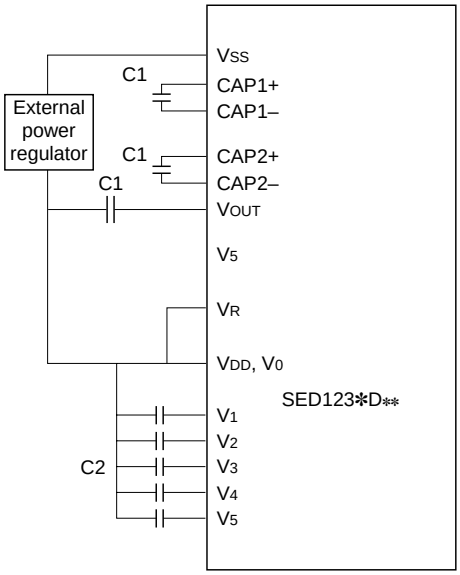
When a built-in power supply is used
Under a triple boosting

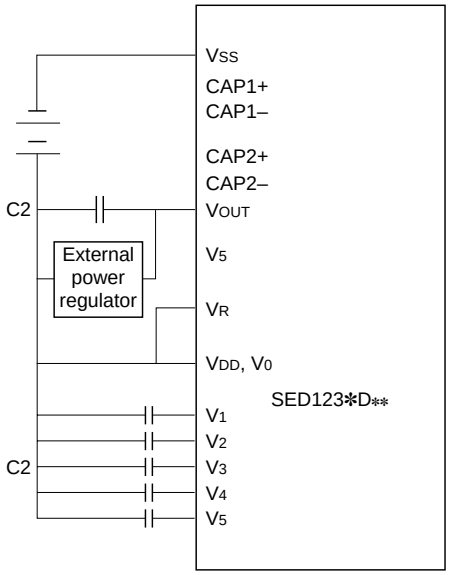


The diagram under a double boosting



When an external power regulator is used
(The built-in power regulator is not used)

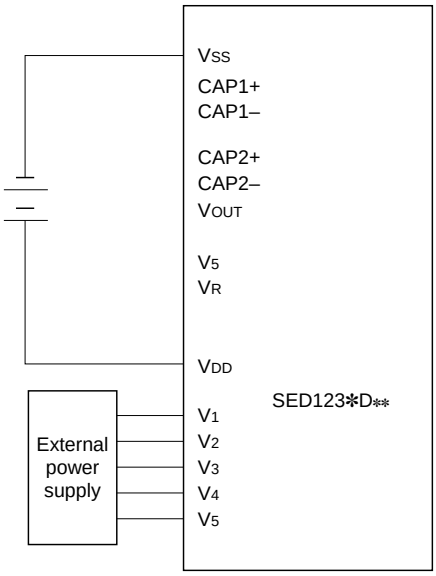




Reference setting values: C1: 0.1 - 4.7 µF
C2: 0.1 µF

We recommend the user to set the optimum values to capacitors C1 and C2 according to the panel size watching the liquid crystal display and drive waveforms.

When a built-in power supply is not used



Low Power Consumption Mode

The SED1230 Series is provided with the standby mode and sleep mode with the object of low power consumption when the unit is in the standby state.

◎ Standby Mode

The standby mode is turned on and off by power save command.

In the standby mode only, static display is enabled by CMOS1 and SEGS1.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : VDD level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : VDD level
   COMS1, SEGS1 : Lighting is enabled by static drive.
   Perform display control using CMOS1 and SEGS1 by static display control command.
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the standby mode is turned on or off.
3. In the operation mode, the status precedent to execution of the standby mode is held.
   The internal circuit for dynamic display output stops.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

◎ Sleep Mode

After the power circuit and oscillating circuit are turned off by command and the power save command is executed, the sleep mode is set. This mode permits reducing current consumption nearly to the static current value.

1. Liquid crystal display output
   COM1 ~ COM28, COMS2, COMS3 : VDD level
   SEG1 ~ SEG60, SEGS2 ~ SEGS6 : VDD level
   COMS1 ~ SEGS1 : VDD level
2. DD RAM, CG RAM and symbol register
   Written contents do not change and are stored regardless of whether the sleep mode is turned on or off.
3. In the operation mode, the status precedent to execution of the sleep mode is held. All the internal circuits stops.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by power save command and power control command.

Reset Circuit

When the RES input goes active, this LSI enters the initialization status.

◎ Initialization status

1. Static display control
   SD0, SD1 = 0 : Display OFF
2. Display ON/OFF control
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   DC = 0 : Double cursor OFF
   D = 0 : Display OFF
3. Power save
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
4. Power control
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
5. System set
   CG = 0 : Not use of CG RAM

As described in 6.1 MPU Interface, the RES pin is connected to the MPU reset pin and performs initialization concurrently with the MPU.

Regarding the reset signal, a pulse of at least 10 µs or more active level must be input as described in 9. DC Characteristics. Usually, the operation status is started in 1 µs from the edge of the RES signal.

In the SED1230 Series where the built-in liquid crystal power circuit is not used, the RES input must be active when the external liquid crystal power supply is turned on.

After the RES pin goes active, each register is cleared and set to the above set status.

Unless initialization is performed by the RES pin when a power supply voltage is applied, the clear disable status may be provided.

COMMANDS

Table 4 shows a command list. In the SED1230 Series, each data bus signal is identified by a combination of A0 and $\overline{WR}$ (E).
Command interpretation and execution are performed by only internal timing. This permits high-speed processing.

- **Outline of Commands**

Command type	Command name	A0	WR
Display control instruction	Cursor Home	0	0
	Static Display Control	0	0
	Display ON/OFF Control	0	0
Power control	Power Save	0	0
	Power Control	0	0
	Electronic Volume Register Set	0	0
Address control instruction	Address Set	0	0
Data input instruction	Data Write	1	0

The execution time of each instruction is determined by the internal processing time of the SED1230 Series. Accordingly, to execute instructions in succession, reserve a time exceeding the cycle time (t_{cyc}) and execute the next instruction.

- **Outline of Commands**

(1) Cursor Home
This command presets the address counter to 30H. When the cursor is displayed, this command moves it to column 1 of line 1.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	*	*	*	*

* : Don't Care

(2) Static Display Control
This command selects display or non-display of static display symbol, and blink ON or OFF. This command is effective in the standby mode only.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	*	*	SD1	SD0

* : Don't Care

SD1, SD2 = 0, 0 : Display OFF
0, 1 : Blink (1 ~ 2 Hz)
SD1, SD2 = 1, 0 : Blink (3 ~ 4 Hz)
1, 1 : All Display ON

(3) Display ON/OFF Control
This command performs display and cursor setting.

Note: Control the symbols that are driven by COMS1 and SEGS1, by the Static Display Control command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	C	B	DC	D

D = 0 : Display OFF
1 : Display ON

DC = 0 : Double cursor OFF
1 : Double cursor ON

B = 0 : Cursor blink OFF
1 : Cursor blink ON
In the blink state, display characters in normal video and display characters in monochrome reverse video are displayed alternately.
The repetition cycle of alternate display is about 1 second.

C = 0 : Non-display of cursor
1 : Display of cursor

The relationship between C and B registers and cursor display is shown in the following table.

C	B	Cursor display
0	0	Non-display
0	1	Non-display
1	0	Display in monochrome reverse video
1	1	Alternate display of display characters in normal video and display characters in monochrome reverse video

The cursor display position corresponds to the position indicated by address counter.

Accordingly, to move the cursor, change the address counter value by the RAM Address Set command or auto increment by writing RAM data.

If the address counter is set at the symbol register position with (C, B) = (1, 0), symbols can be caused to blink selectively.

(4) Power Save

This command is used to control the oscillating circuit and set and reset the standby mode or sleep mode.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	*	*	O	PS

* : Don't Care

PS = 0 : Power save OFF (reset)
1 : Power save ON (set)

O = 0 : Oscillating circuit OFF (stop of oscillation)
1 : Oscillating circuit ON (oscillation)

(5) Power Control

This command is used to control the operation of the built-in power circuit.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	VC	VF	P

P = 0 : Boosting circuit OFF
1 : Boosting circuit ON

Note: To operate the boosting circuit of the SED1230 Series, the oscillating circuit must be in operation.

VF = 0 : Voltage follower OFF
1 : Voltage follower ON

VC = 0 : Voltage regulating circuit OFF
1 : Voltage regulating circuit ON

(6) System Set

This command set the use or non-use of display lines and CG RAM.

Execute this command first after turning on the power supply or after resetting.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	N2	N1	*	PS

* : Don't Care

CG = 0 : Non-use of CG RAM
1 : Use of CG RAM

N2	N1	
0	0	: 2 lines
0	1	: 3 lines
1	0	: 4 lines

(7) Electronic Volume Register Set

This command controls the liquid crystal driving voltage V_5 output from the voltage regulating circuit of the built-in liquid crystal power supply, thereby adjusting the gradation of liquid crystal display.

When data is set in the 4-bit register, the liquid crystal driving voltage can take one of 16 voltage states.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	MSB	*	*	LSB

Hex Code

70H ~7FH

MSB			LSB	$\lvert V_5 \rvert$	$\lvert I_{REF} \rvert$	
0	0	0	0	Small	0.0 μA	
			:	:	:	
			:	:	:	
1	1	1	1	Large	About	3.65 μA

When the electronic volume function is not used, set (A3, A2, A1, A0) = (0, 0, 0, 0).

(8) RAM Address Set

This command sets addresses to write data into the DD RAM, CG RAM and symbol register in the address counter.

When the cursor is displayed, the cursor is displayed at the display position corresponding to the DDRAM address set by this command.

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ADDRESS						

① The settable address length is ADDRESS = 00H to 7FH.

② Before writing data into the RAM, set the data write address by this command. Next, when data is written in succession, the address is automatically incremented.

RAM Map (SED1230, SED1231, SED1232)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM(00H)							–	CGRAM(01H)							–
10H	CGRAM(02H)							–	CGRAM(03H)							–
20H	Unused															
30H	DDRAM line 1														Unused	
40H	DDRAM line 2							For signals							"	
50H	DDRAM line 3														"	
60H	DDRAM line 4														"	
70H	Symbol register														"	

– : Unused
For signals : Output from SEGS2 to SEGS6.

RAM Map (SED1233)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	CGRAM(00H)							–	CGRAM(01H)							–
10H	CGRAM(02H)							–	CGRAM(03H)							–
20H	Unused															
30H	DDRAM line 1															
40H	DDRAM line 2															
50H	DDRAM line 3															
60H	DDRAM line 4															
70H	Symbol register															

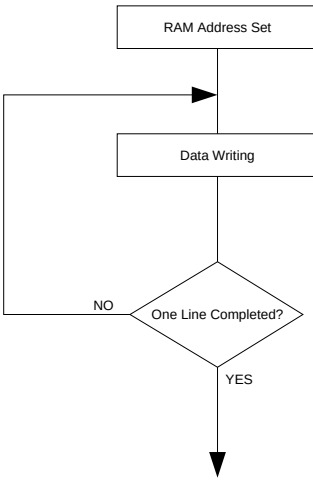
–: Unused

(9) Data Write

A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DATA							

① This command writes data into the DD RAM, CG RAM or symbol register.
② After this command is executed, the address counter is automatically incremented by 1. This permits writing data in succession.

<Example of Data Writing>
The following is an example of writing one-line data into the DD RAM in succession.



Note: When executing instructions in succession, reserve a time exceeding t_{CYC} and execute the next instruction.

Table 4 SED1230 Series Command List

Command	Code										Function
	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Cursor Home	0	0	0	0	0	1	*	*	*	*	Moves the cursor to the home position.
(2) Static Display Control	0	0	0	0	1	0	*	*	SD1	SD0	Sets the display mode of static display symbol SD1, SD0 = 0, 0 (display OFF), 0, 1 (1 - 2 Hz blink), 1, 0 (3 4 Hz blink), 1, 1 (all display ON)
(3) Display ON/OFF Control	0	0	0	0	1	1	C	B	DC	D	Sets cursor ON/OFF (C), cursor blink ON//OFF (B), double cursor ON/OFF (DC) and display ON/OFF (D). C = 1 (cursor ON) 0 (cursor OFF), B = 1 (blink ON) 0 (blink OFF) DC = 1 (double cursor ON) 0 (double cursor OFF), D = 1 (display ON) D = 0 (display OFF)
(4) Power Save	0	0	0	1	0	0	*	*	0	PS	Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (0). PS = 1 (power save ON) 0 (power save OFF), 0 = 1 (oscillating circuit ON) 0 (oscillating circuit OFF)
(5) Power Control	0	0	0	1	0	1	0	VC	VF	P	Sets voltage regulating circuit ON/OFF and boosting circuit ON/OFF (P). VC = 1 (voltage regulating circuit ON) 0 (voltage regulating circuit OFF) VF = 1 (voltage follower ON) 0 (voltage follower OFF), P = 1 (boosting circuit ON) 0 (boosting circuit OFF)
(6) System Set	0	0	0	1	1	0	N2	N1	*	CG	Sets the use or non-use of CG RAM and display lines (N2, N1). CG = 1 (use of CG RAM) 0 (non-use of CG RAM), N2, N1 = 0, 0 (2 lines) 0, 1 (3 lines) 1, 0 (4 lines)
(7) Electronic Volume Register	0	0	0	1	1	1	MSB			LSB	Sets the electronic volume register value.
(8) RAM Address Set	0	0	1	ADDRESS							Sets the DD RAM, CG RAM or symbol register address.
(9) RAM Write	1	0	DATA								Writes data into the DD RAM, CG RAM or symbol register address.
(10) NOP	0	0	0	0	0	0	0	0	0	0	Non-operation command
(11) Test Mode	0	0	0	0	0	0	1	0	1	0	Command for IC chip test. Don't use this command.

CHARACTER GENERATOR

Character Generator ROM (CG ROM)

The SED1230 Series is provided with a character generator ROM consisting of a up to 256-type characters. Each character size is 5 × 7 dots.

Table 5 shows a character code table of the SED1230 Series.
The 4 characters of character codes 00H to 03H are set by the System Set command to specify for which of CG ROM and CG RAM they are to be used.

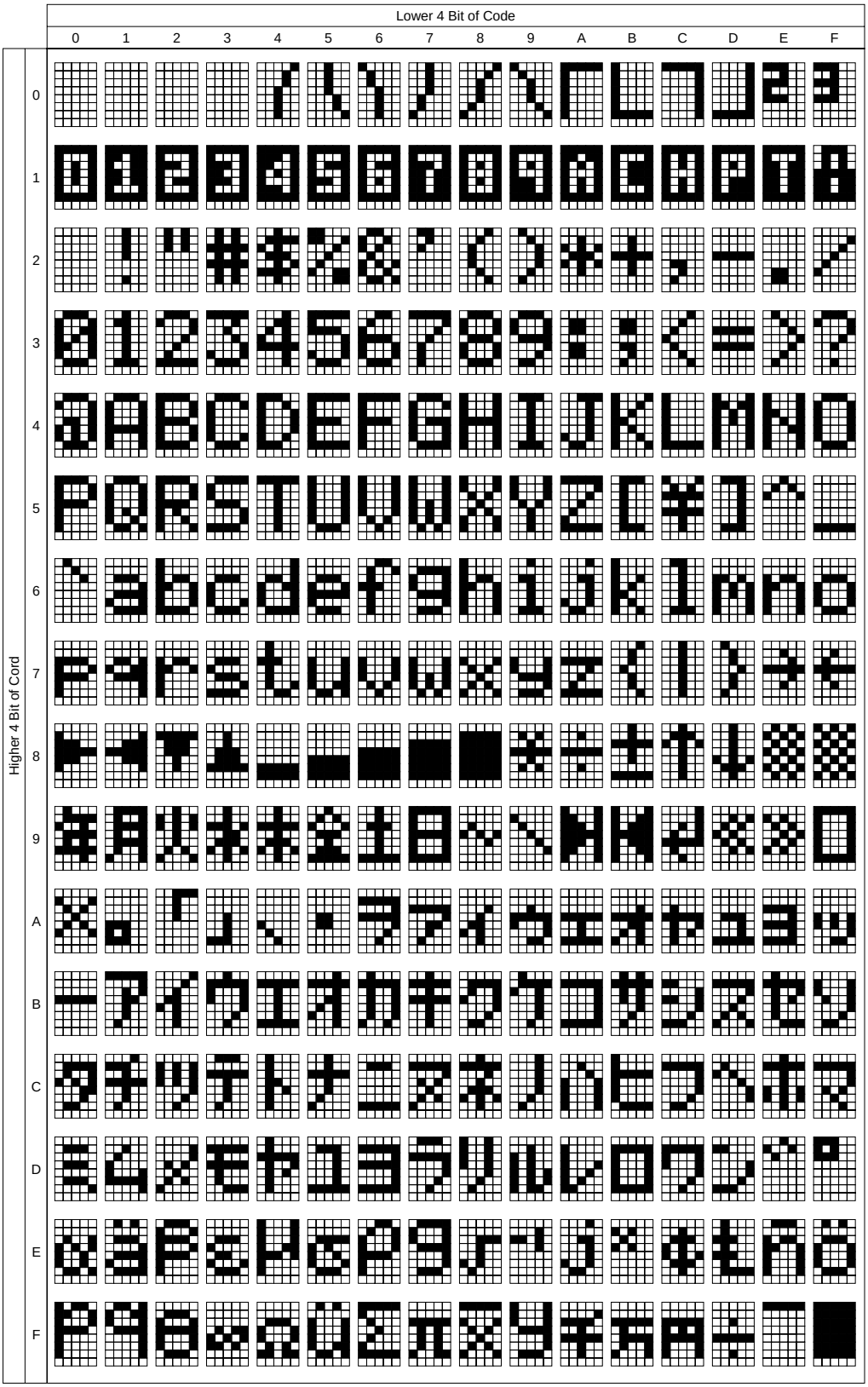
The CG ROM of the SED1230 Series is a mask ROM and compatible with the user-dedicated CG ROM. Please ask us for further information of it.

Regarding changed CG ROM, it is defined in product name as follows:

(Example) S E D 1 2 3 0 D 0 B
↑
Digit for CG ROM pattern change

SED123* DA*

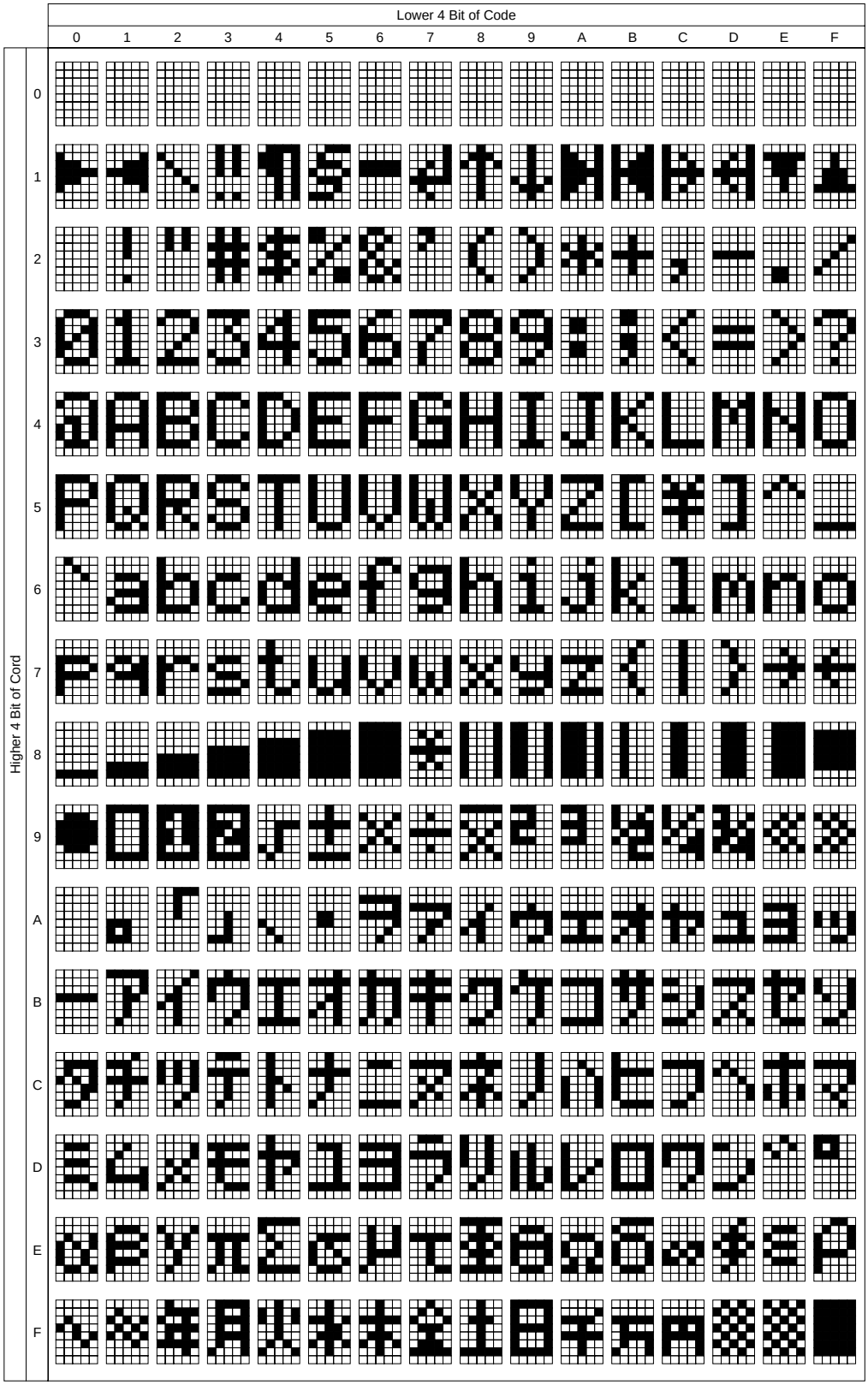
Table 5



SED123* DB*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

SED123* DG*


Lower 4 Bit of Code
0 1 2 3 4 5 6 7 8 9 A B C D E F
Higher 4 Bit of Cord
0 1 2 3 4 5 6 7 8 9 A B C D E F

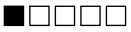
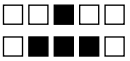
Character Generator RAM (CG RAM)

The SED1230 Series is provided with a CG RAM that permits user-programming character patterns so that they can be displayed with a high degree of freedom for signal display.

Before using the CG RAM, select the use of CG RAM by the System Set command.

The capacity of the CG RAM is 140 bits and arbitrary patterns of 4 types consisting of 5×7 dots can be registered.

The relationship among CG RAM patterns, CG RAM addresses, and character codes is shown below.

Character code	RAM address		CGRAM data (character pattern) D7 D0								Display
00H	00H~06H	0	*	*	*	0	1	1	1	1	
02H	10H~16H	1	*	*	*	1	0	0	0	0	
		2	*	*	*	1	0	0	0	0	
		3	*	*	*	0	1	1	1	1	
		4	*	*	*	0	0	0	0	1	
		5	*	*	*	0	0	0	0	1	
		6	*	*	*	1	1	1	1	0	
01H	08H~0EH	8	*	*	*	0	0	1	0	0	
03H	18H~1EH	9	*	*	*	0	0	1	0	0	
		A	*	*	*	0	1	1	1	0	
		B	*	*	*	0	1	1	1	0	
		C	*	*	*	0	1	1	1	0	
		D	*	*	*	1	1	1	1	1	
		E	*	*	*	1	1	1	1	1	

Unused

Character data

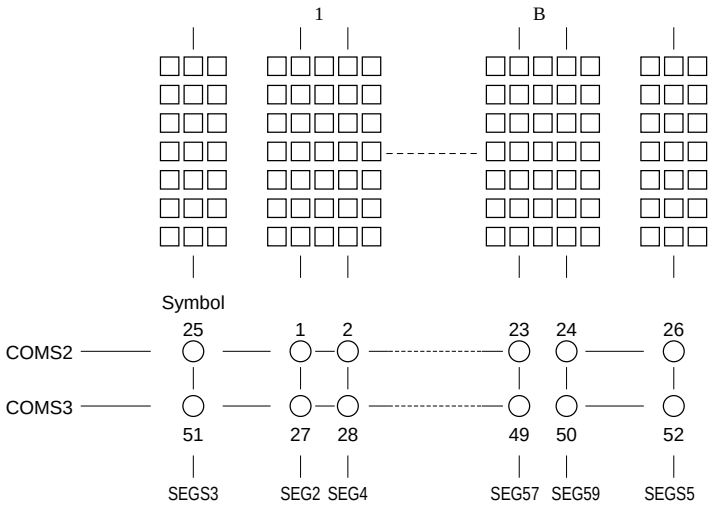
1: Display

0: Non-display

Symbol Register

The SED1230 Series is provided with a symbol register that permits displaying each symbol so that symbol display may be performed on the screen.
The capacity of the symbol register is 64 bits. In case of 12 digits, 48 symbols can be displayed. In case of 16 digits, 64 symbols can be displayed.
The relationship among symbol register display patterns, RAM addresses and write data is shown below.

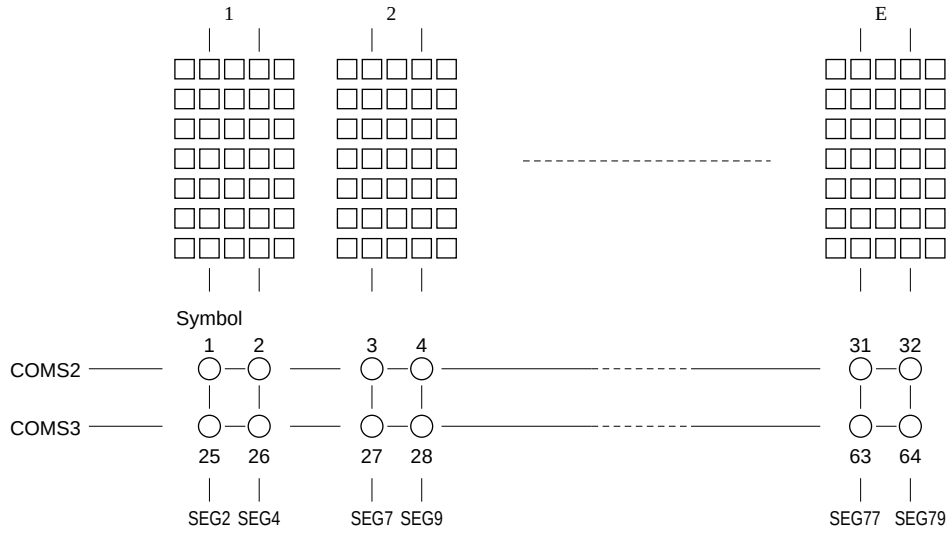
(1) SED1230, SED1231, SED1232



RAM address		Symbol Bits D7							D0
70H~7CH	0	*	*	*	27	1	28	2	*
	1	*	*	*	29	3	30	4	*
	:	:							
	B	*	*	*	49	23	50	24	*
	C	*	*	*	51	25	52	26	*

Bit
1: Display
0: Not display

(2) SED1233



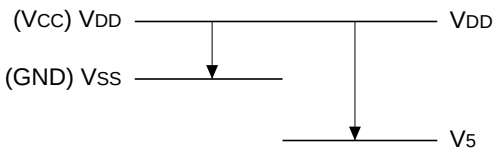
RAM address		Symbol Bits								Bit
		D7	D6	D5	D4	D3	D2	D1	D0	
70H~7FH	0	*	*	*	33	1	34	2	*	1: Display
	1	*	*	*	35	3	36	4	*	0: Not display
	:	:								
	E	*	*	*	61	29	62	30	*	
	F	*	*	*	63	31	64	32	*	

Notes 1: If the symbol segment size is 1.5 times or more greater than the other dots, it is recommended to be divided into COMS2 and COMS3 and driven separately.

2: The segments other than symbol display must not be crossed through COMS2 or COMS3. The COMS3 symbol register must be set to all zeros if crossing.

ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Power supply voltage (1)		V_{SS}	–6.0~+0.3	V
Power supply voltage (2)		V_5	–12.0~+0.3	V
Power supply voltage (3)		V_1, V_2, V_3, V_4	V_5~+0.3	V
Input voltage		V_{IN}	V_{SS}–0.3~+0.3	V
Output voltage		V_O	V_{SS}–0.3~+0.3	V
Operating temperature		T_{opr}	–30~+85	°C
Storage temperature	TCP	T_{str}	–55~+100	°C
	Bare chip		–65~+125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. For voltages of V_1, V_2, V_3 and V_4, keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and $V_{DD} \geq V_{SS} \geq V_5 \geq V_{OUT}$ at all times.
3. If the LSI is used exceeding the absolute maximum ratings, it may lead to permanent destruction. In ordinary operation, it is desirable to use the LSI in the condition of electrical characteristics. If the LSI is used out of this condition, it may cause a malfunction of the LSI and have a bad effect on the reliability of the LSI.

DC CHARACTERISTICS

V_{DD} = 0 V, V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified.

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Power supply voltage (1)	Recommended operation	V_{SS}			–3.6	–3.0	–2.4	V	V_{SS}
	Operable				–5.5	–3.0	–2.4		*1
Power supply voltage (2)	Recommended operation	V_5			–8.0		–5.0	V	V_5
	Operable				–11.0		–4.5		*2
	Operable	V_1, V_2			0.6×V_5		V_{DD}	V	V_1, V_2
	Operable	V_3, V_4			V_{DD}		0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHC}			0.2×V_{SS}		V_{DD}	V	*3
Low-level input voltage		V_{ILC}			V_{SS}		0.8×V_{SS}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS} –1.0			1.0		µA	*3
LC driver ON resistance		R_{ON}	Ta=25°C V_5=–7.0V ΔV=0.1V			20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}				0.1	5.0	µA	V_{DD}
Dynamic current consumption		I_{DD}	Display state	V_5 = –7 V without load			100	µA	V_{DD} *5
			Standby state	Oscillation ON, Power OFF			20	µA	V_{DD} *6
			Sleep state	Oscillation OFF, Power OFF			5	µA	V_{DD}
			Access state	f_{cyc}=200KHz			500	µA	V_{DD} *7
Frame frequency		f_{FR}	Ta=25°C	V_{SS}=–3.0V	70	100	130	Hz	*11
Input pin capacity		C_{IN}	Ta=25°C	f=1MHz		5.0	8.0	pF	*3

Reset time	t_R		1.0			µs	*8
Reset pulse width	t_{RW}		10			µs	*9
Reset start time	t_{RES}		50			ns	*9

Built-in power supply	Input voltage	V_{SS}		–3.6		–2.4	V	*10
	Booster output voltage	V_{OUT}	Double boosting state	–7.2			V	V_{OUT}
			Triple boosting state	–10.8				
	Voltage follower operating voltage	V_5		–11.0		–4.5	V	
	Reference voltage (standard)	V_{REG}	Ta = 25°C	–3.5	–3.1	–2.7	V	*12
	Reference voltage (option 1)	$V_{REG(VS1)}$	Ta = 25°C	–2.4	–2.1	–1.8	V	*12
	Reference voltage (option 2)	$V_{REG(VSS)}$	Ta = 25°C	V_{SS}	V_{SS}	V_{SS}	V	*12

*1: A wide operating voltage range is guaranteed but an abrupt voltage variation in the access status of the MPU is not guaranteed.

*2: The operating voltage range is applicable to the case where an external power supply is used.

*3: D0 ~ D5, D6 (SCL), D7 (SI), A0, RES, $\overline{CS}$ $\overline{WR}$ (E), P/S, IF

*4: This is a resistance value when a voltage of 0.1 V is applied between output pin SEGn, SEGSn, COMn or COMSn, and each power pin (V_1, V_2, V_3 or V_4). It is specified in the range of operating voltage (2).

R_{ON} = 0.1 V / ΔI

(ΔI: Current flowing when 0.1 V is applied between the power and output)

*5: Character "  " display. This is applicable to the case where no access is made from the MPU and the built-in power circuit and oscillating circuit are in operation.

*6: This is applicable to the case where the built-in power circuit is OFF and the oscillating circuit is in operation in the standby mode.

*7: Current consumption when data is always written by f_{cyc}.
The current consumption in the access state is almost proportional to the access frequency (f_{cyc}).
When no access is made, only I_{DD} (I) occurs.

8: t_R (reset time) indicates the internal circuit reset completion time from the edge of the RES signal. Accordingly, the SED123 usually enters the operating state after t_R.

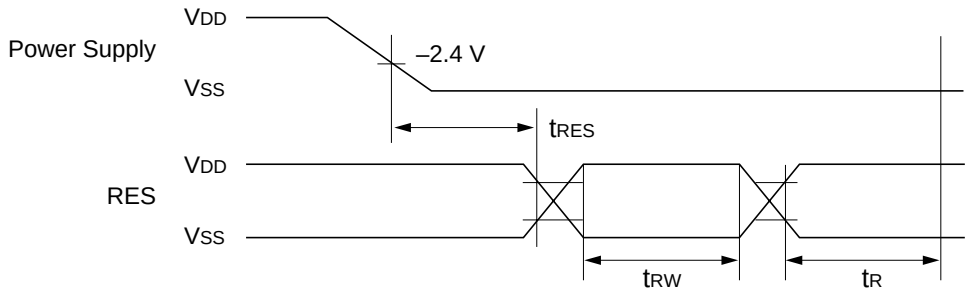
*9: Specifies the minimum pulse width of the RES signal. It is reset when a signal having the pulse width greater than t_{RW} is entered.

*10: When operating the boosting circuit, the power supply V_{SS} must be used within the input voltage range.

*11: The f_{OSC} frequency of the oscillator circuit for internal circuit drive may differ from the f_{BST} boosting clock on some models. The following provides the relationship between the f_{OSC} frequency, f_{BST} boosting clock, and f_{FR} frame frequency.

f_{OSC} = (No. of digits) × (1/Duty) × f_{FR}
f_{BST} = (1/2) × (1/No. of digits) × f_{OSC}
Example: The SED1230 has 13 digits of display and 1/30 duty.
f_{OSC} = 13 × 30 × 100 = 39 kHz
f_{BST} = (1/2) × (1/13) × 39 K = 1.5 kHz

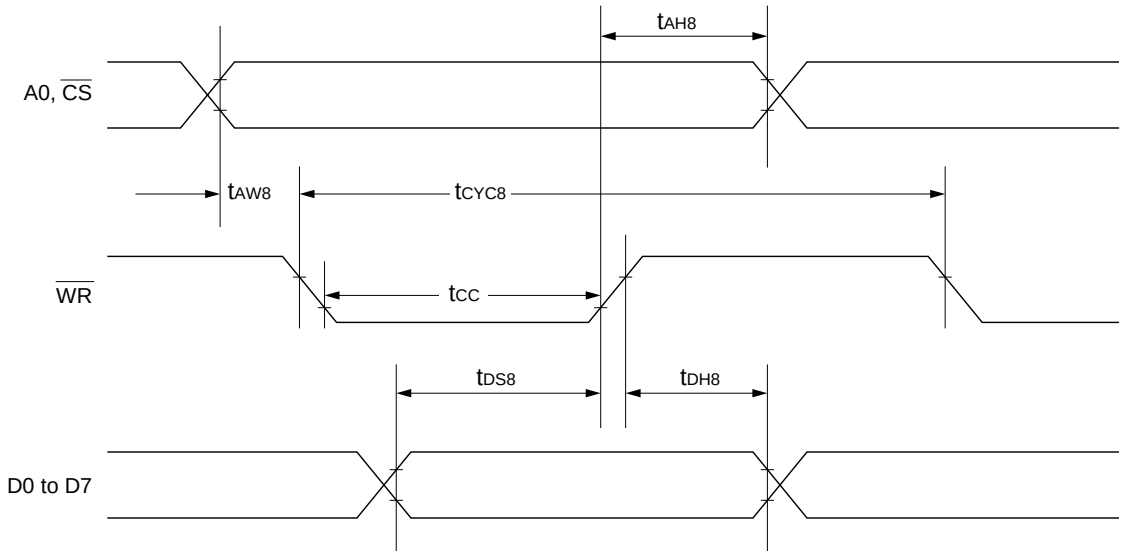
*12: The V_{REG} reference voltage has the temperature characteristics of approximately –0.17%/°C (standard specifications). An optional model having the temperature characteristics of approximately –0.04%/°C is also available. The voltage of power supply terminal V_{SS} can be selected as the reference power supply as an option without using the reference voltage inside the IC. In this case, however, a regulator is used for the external power supply (V_{DD} – V_{SS}). The voltage accuracy of V5 depends on that of the regulator used. The CGROM modification rules apply to the optional models.



All signal timings are based on 20% and 80% of V_{SS} signals.

TIMING CHARACTERISTICS

(1) System Bus Write Characteristic I (80 series MPU)

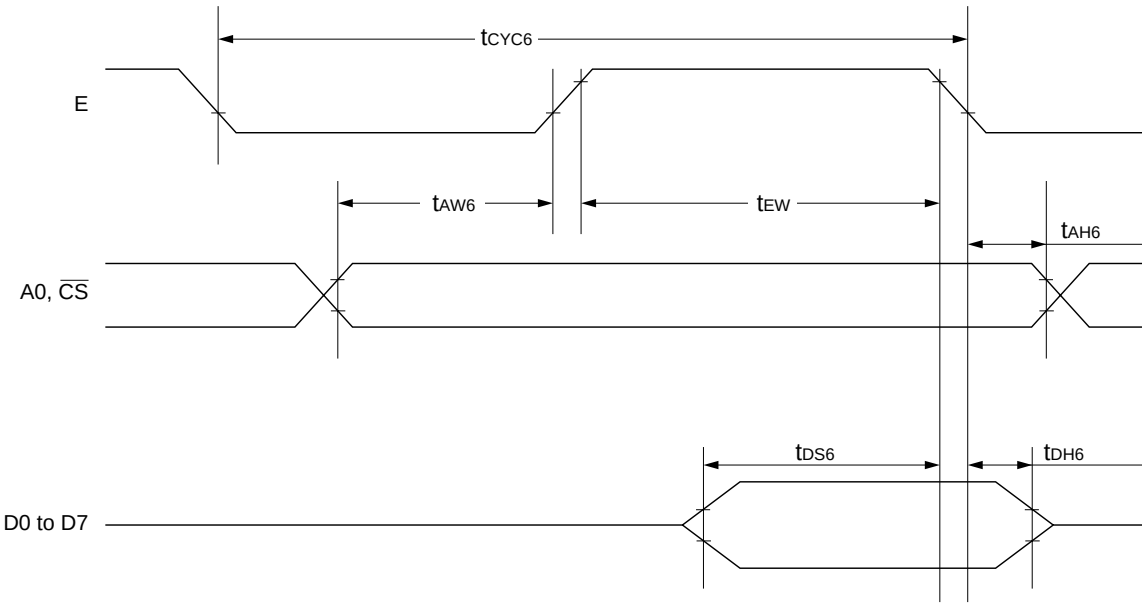


[V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		30		ns
Address setup time		t_{AW8}		60		ns
System cycle time	$\overline{WR}$	t_{CYC8}	V_{SS} = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Control pulse width ($\overline{WR}$)		t_{CC}	V_{SS} = –3.0	100		ns
			–2.7	120		
			–2.4	150		
Data setup time	D0 ~ D7	t_{DS8}		100		ns
Data hold time		t_{DH8}		50		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of V_{SS}.
*3: For A0 and $\overline{CS}$, the same time is not required. Input signals so that A0 and $\overline{CS}$ may satisfy t_{AW8} and t_{AH8} respectively.

(2) System Bus Write Characteristic II (68 series MPU)

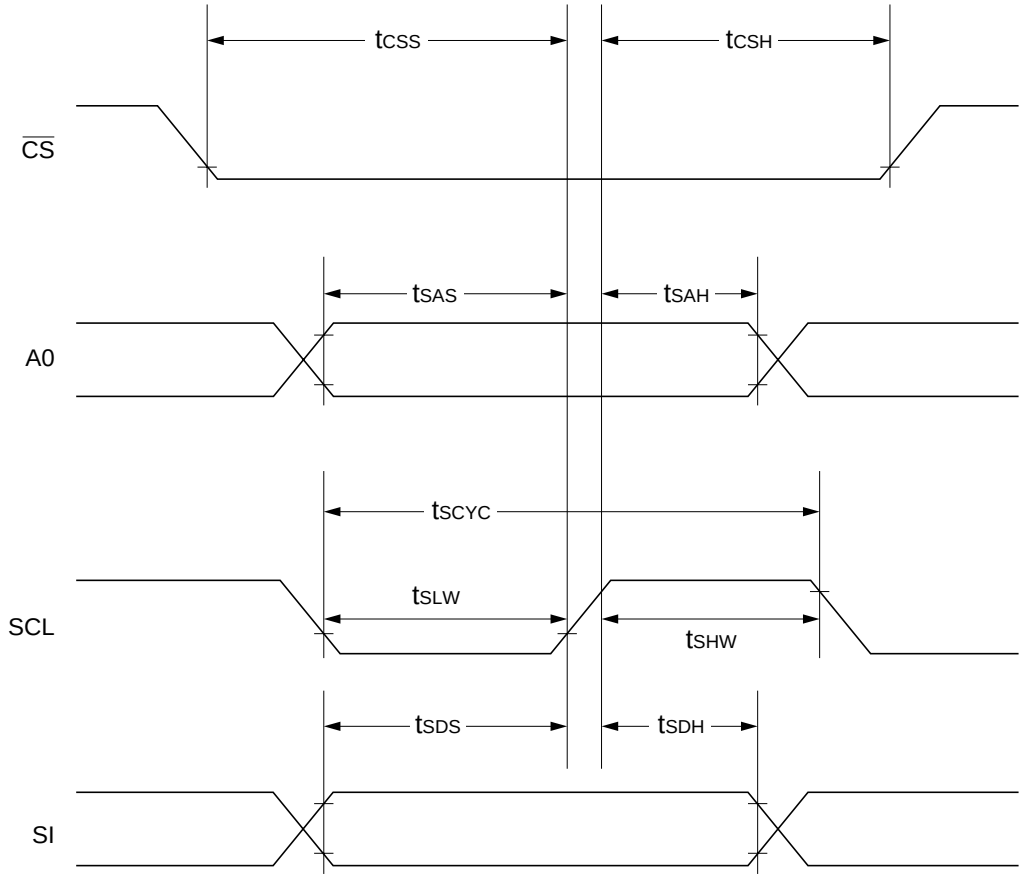


[VSS = –3.6 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	t CYC6	VSS = –3.0	500		ns
			–2.7	550		
			–2.4	650		
Address setup time		t AW6		60		
Address hold time		t AH6		30		ns
Data setup time	D0 ~ D7	t DS6		100		ns
Data hold time		t DH6		50		ns
Enable pulse width	E	t EW	VSS = –3.0	100		ns
			–2.7	120		
			–2.4	150		

*1: tCYC6 denotes the cycle of the E signal in the $\overline{CS}$ active state. tCYC6 must be reserved after $\overline{CS}$ becomes active.
*2: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*3: Every timing is specified on the basis of 20% and 80% of VSS.
*4: For A0 and $\overline{CS}$, the same timing is not required. Input signals so that A0 and $\overline{CS}$ may satisfy tAW6 and tAH6 respectively.

(3) Serial Interface



[V_{SS} = –3.6 V to –2.4 V, Ta = –30 to 85°C]

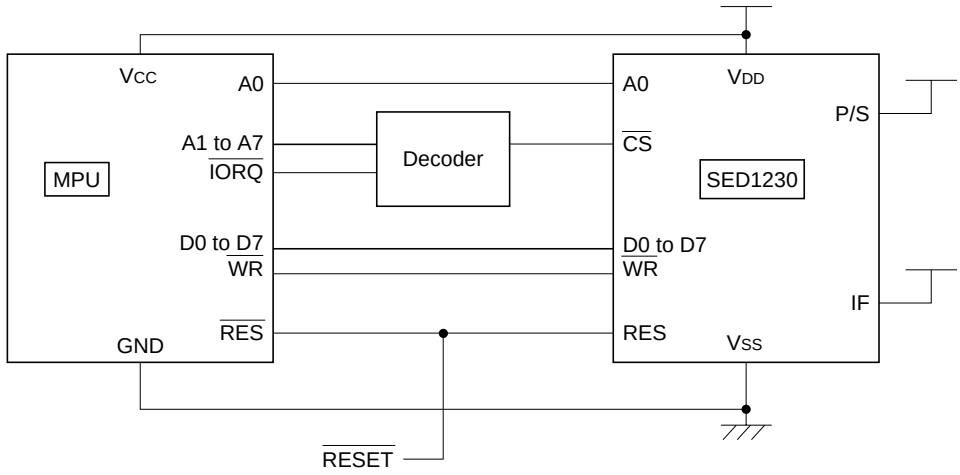
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	t_{SCYC}	V_{SS} = –3.0	700		ns
			–2.7	800		ns
			–2.4	1000		ns
SCL "H" pulse width		t_{SHW}		300		ns
SCL "L" pulse width		t_{SLW}		300		ns
Address setup time	A0	t_{SAS}		50		ns
Address hold time		t_{SAH}	V_{SS} = –3.0	350		ns
			–2.7	400		ns
			–2.4	500		ns
Data setup time	SI	t_{SDS}		50		ns
Data hold time		t_{SDH}		50		ns
$\overline{CS}$-SCL time	$\overline{CS}$	t_{CSS}		150		ns
		t_{CSH}	V_{SS} = –3.0	550		ns
			–2.7	650		ns
			–2.4	700		ns

*1: For the rise and fall of an input signal, set a value not exceeding 25 ns.
*2: Every timing is specified on the basis of 20% and 80% of V_{SS}.

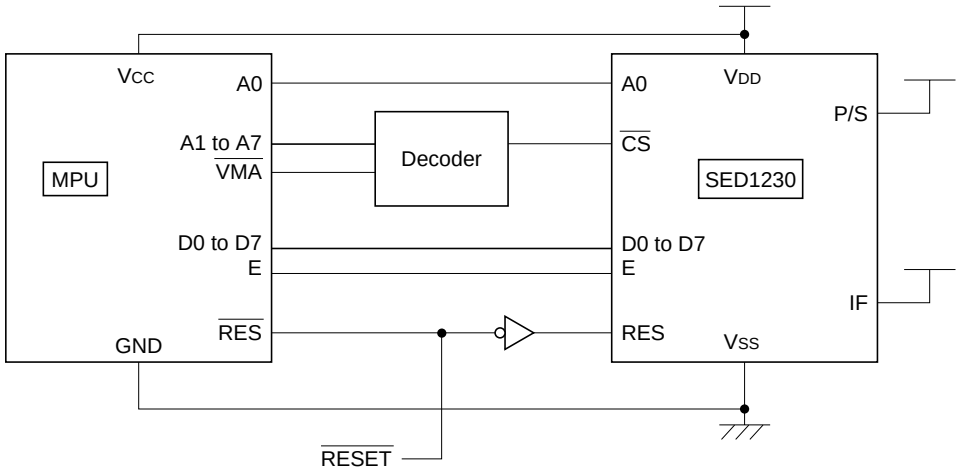
MPU INTERFACE (REFERENCE EXAMPLES)

The SED1230 Series can be connected to the 80 series MPU and 68 series MPU. When an serial interface is used, the SED1230 Series can be operated by less signal lines.

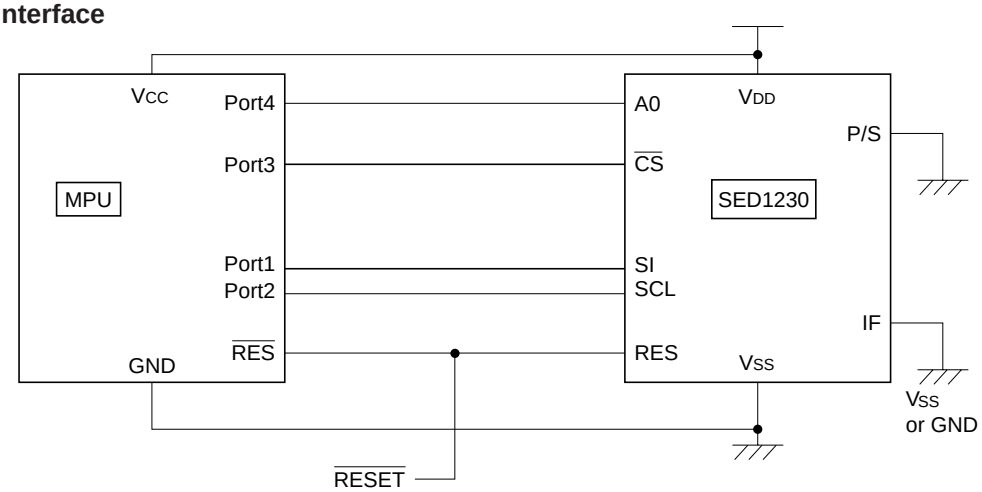
80 Series MPU



68 Series MPU

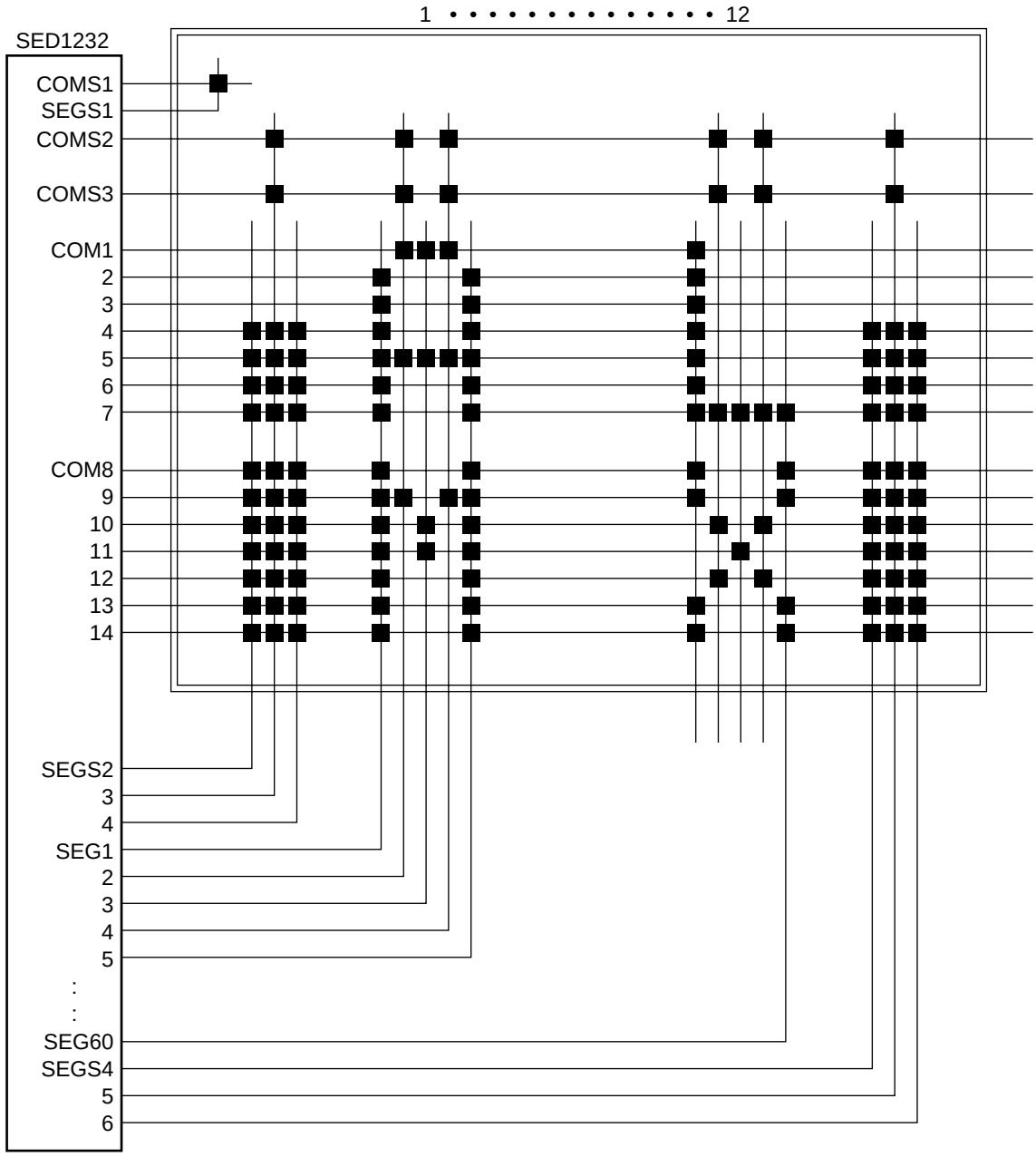


Serial Interface



INTERFACE TO LCD CELLS (REFERENCE)

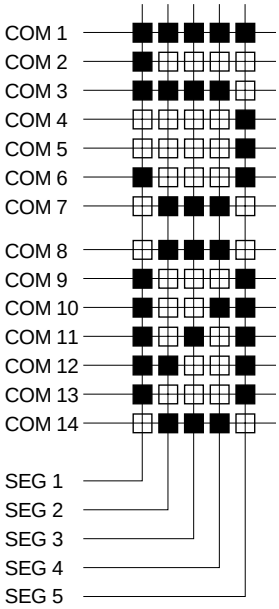
12 columns by 2 lines, 5 × 7-dot matrix segments and symbols

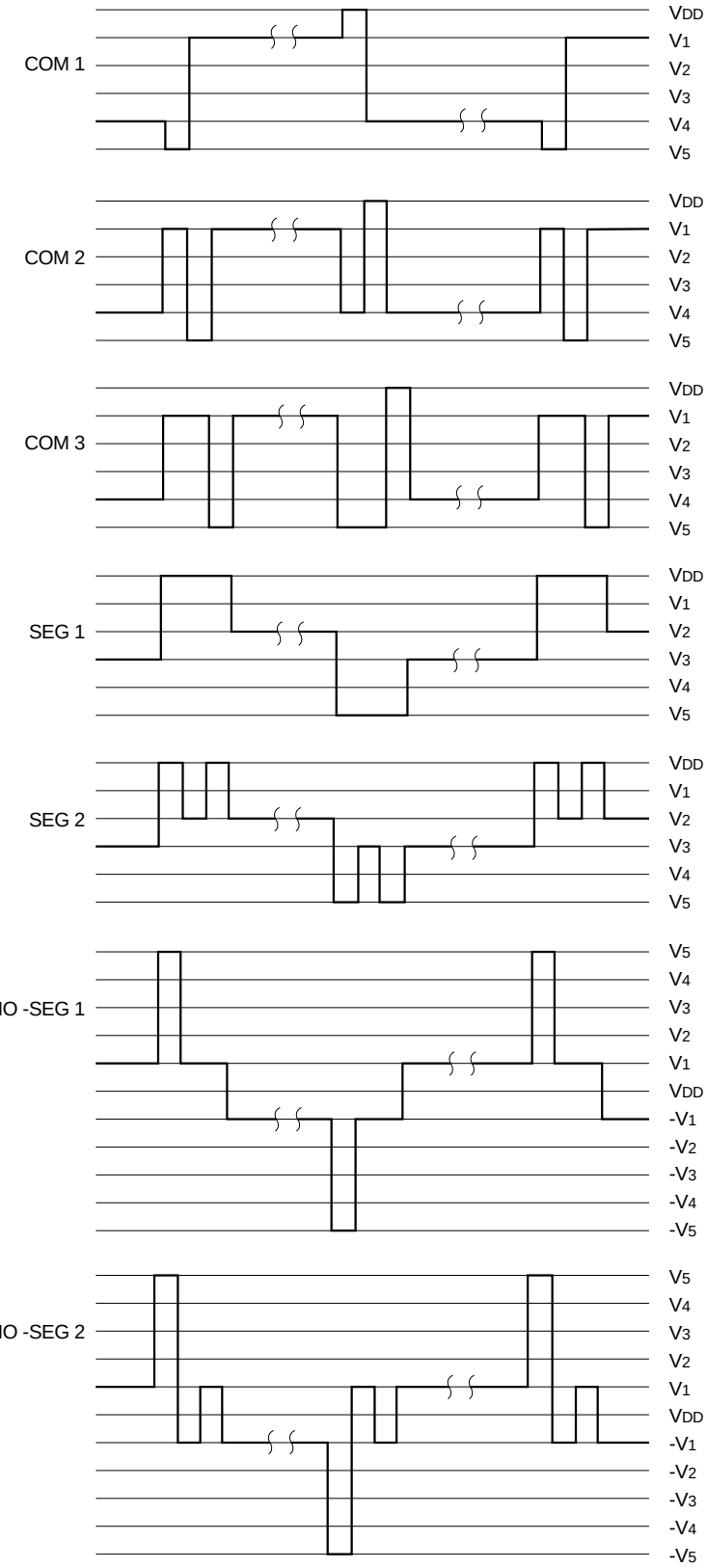


■ System Setup

N2	N1
0	0

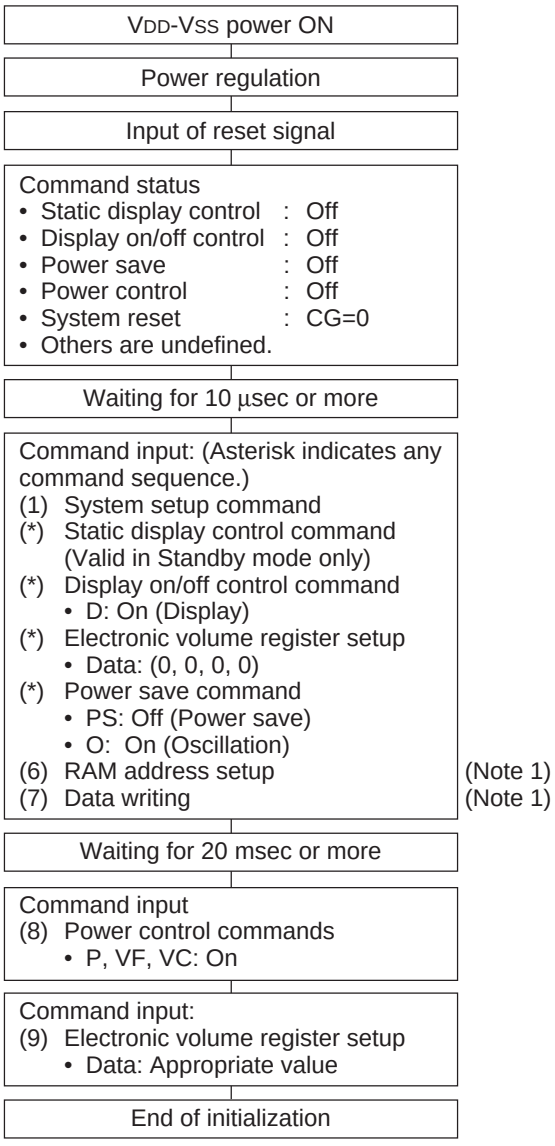
LIQUID CRYSTAL DRIVE WAVEFORMS (B WAVEFORMS)



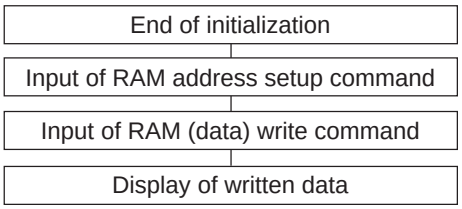


INSTRUCTION SETUP EXAMPLE (REFERENCE ONLY)

(1) Initial setup



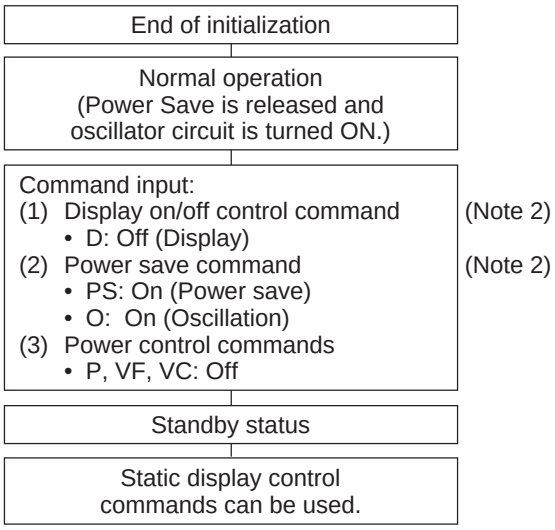
(2) Display mode



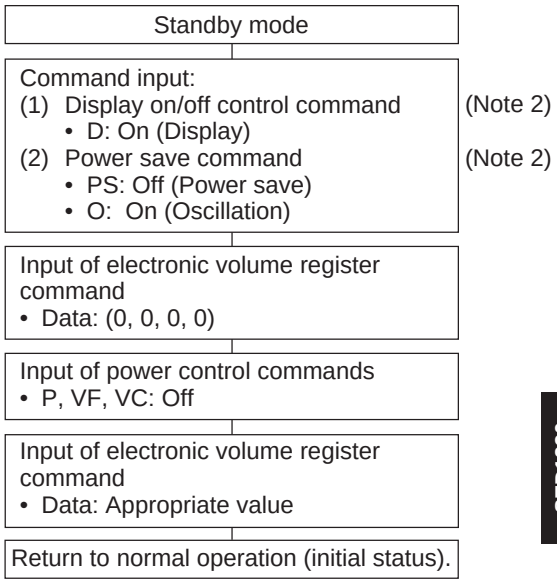
Note 1: Commands (6) and (7) initialize the RAM. The display contents must first be set. The non-display area must satisfy the following conditions (for RAM clear).
- DDRAM: Write the 20H data (character code).
- CGRAM: Write the 00H data (null data).
- Symbol register: Write the 00H data (null data).

As the RAM data is unstable during reset signal input (after power-on), null data must be written. If not, unexpected display may result.

(3-1) Selecting the Standby mode

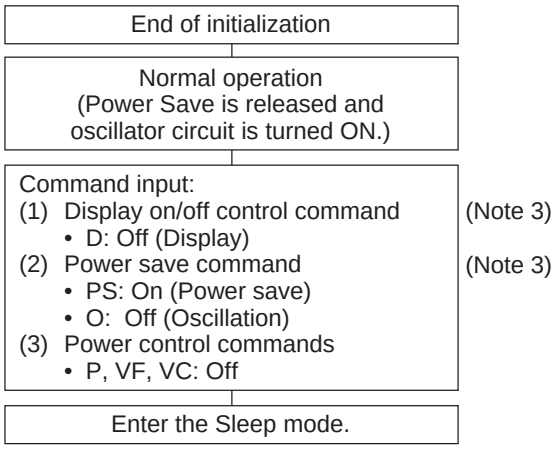


(3-2) Releasing the Standby mode

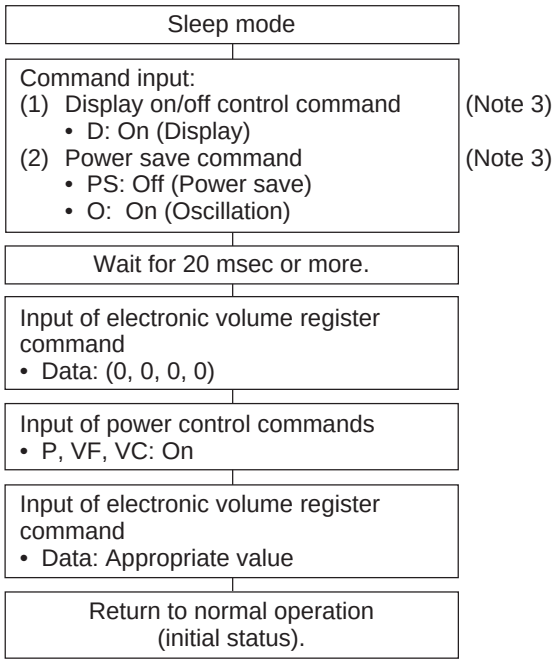


Note 2: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.

(4-1) Selecting the Sleep mode



(4-2) Releasing the Sleep mode



Note 3: Commands (1) and (2) can be entered in any order. Also, command (1) is optional.