SED1240 Series
LCD Controller/Drivers

Technical Manual

Contents

OVERVIEW

The SED1240 Series is a character display dot matrix LCD controller driver. This driver can display up to 64 characters and 6 user-defined characters, and up to 160 symbols according to the 4-bit, 8-bit or serial data which is sent from a microcomputer.
The built-in character generator ROM is provided with up to 544 types of character fonts having a structure of 5 × 8 dots. Up to 256 types can be continuously called by register option selection. This can cope with many different character fonts by uses and countries and permits a wider range of use. This driver incorporates a user-defined character RAM for 6 characters of 5 × 8 dots and can be used for the display of higher degree of freedom by means of a symbol register.
The driver can operate handy units at the minimum power consumption by using its merit of lower power consumption, standby mode, and sleep mode.

FEATURES

- Built-in display data RAM 80-character + 6-character user-defined characters + 160 symbols
- CGROM (for up to 544 characters), CGRAM (6 characters), symbol register (160 symbols)
- Display digits × Number of lines
  <Ordinary mode>
  ① (16 digits) × 4 lines + 160 symbols + 10 static irons (SED1240)
  ② (16 digits) × 3 lines + 160 symbols + 10 static icons (SED1241)
  ③ (16 digits) × 2 lines + 160 symbols + 10 static icons (SED1242)
  <Standby mode>
  ① 10 static icons (SED1240)
  ② 10 static icons (SED1241)
  ③ 10 static icons (SED1242)
- Vertical double-size display function
- Line vertical scroll function
- Line blink function
- Symbol blink function
- Built-in CR oscillating circuit (Built-in C, R)
- External clock input
- High-speed MPU interface
  Interface with both MPUs of 68 series/80 series
  Interface by 4 bits/8 bits
- Serial interface
- Character font 5 × 8 dots
- Duty ratio ① 1/34 (SED1240)
  ② 1/26 (SED1241)
  ③ 1/18 (SED1242)
- Simple command setup
- Built-in liquid crystal drive power circuit
  The boosting circuit, voltage regulating circuit, voltage follower × 4, and resistor for power regulating circuit for bias select commands are incorporated.
- Built-in electronic volume function
- Lower power consumption

80 μA max	(at ordinary operation (during display): Including the internal power supply operating current)
500 μA max	(at ordinary operation (during access): fcyc = 200 KHz, including the internal power supply operating current)
20 μA max	(in standby mode: Oscillation ON, power OFF, static icon display)
5 μA max	(in sleep mode: oscillation OFF, power OFF, display OFF)

- Power supply:

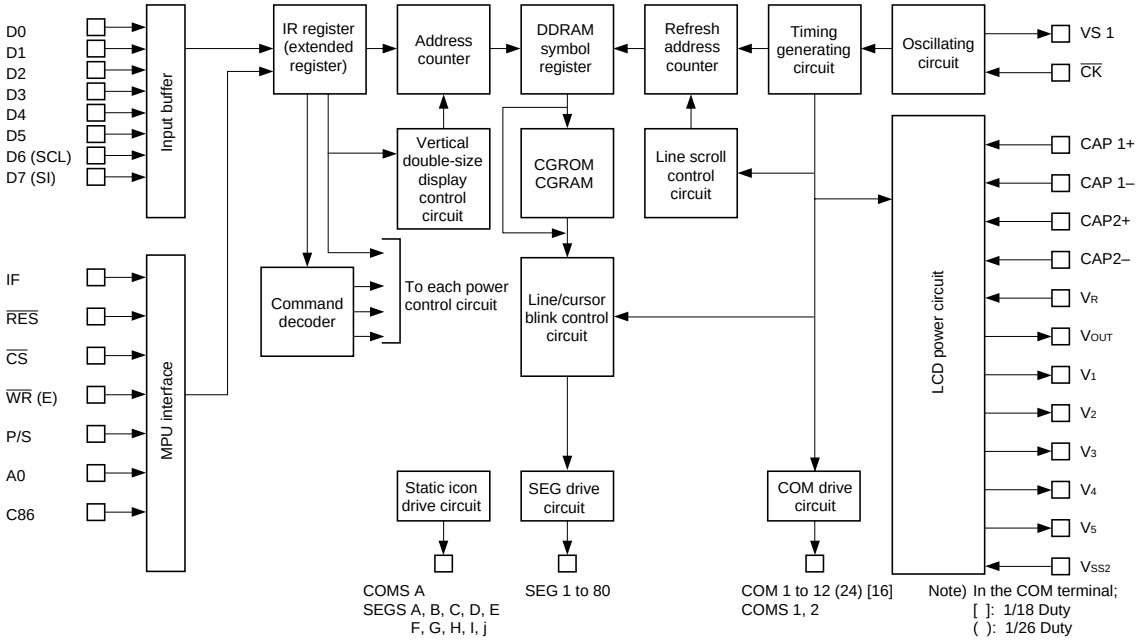
V_{DD} - V_{SS}	1.8 V to 5.5 V
V_{DD} - V_{SS2}	1.8 V to 5.5 V
V_{DD} - V_5	5.5 V to 16.0 V

- Wide operating temperature range
  Ta = –30 to +85°C
- CMOS process
- Pad pitch 90 μm Min
- Delivery form

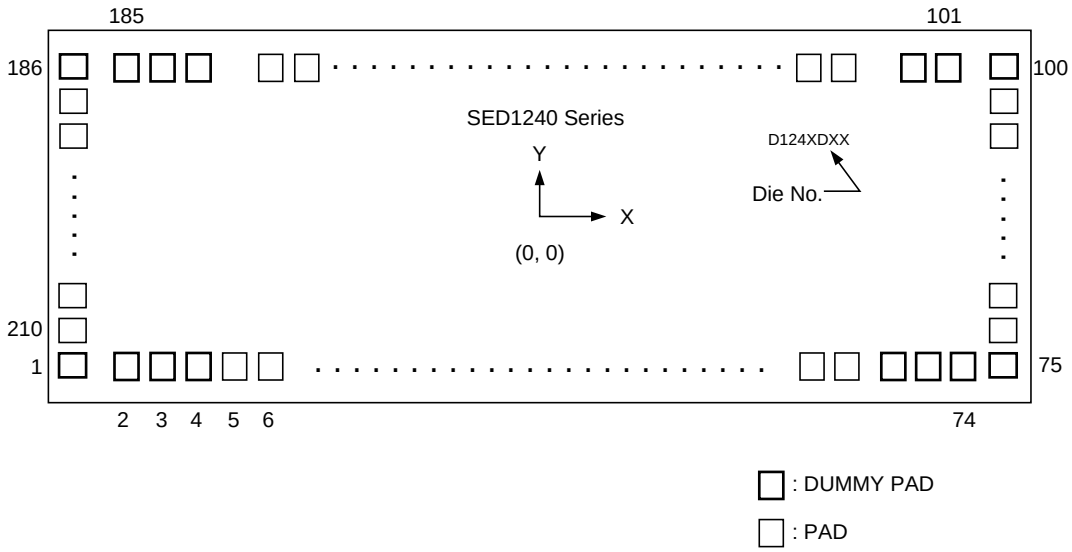
Chip (gold bump product)	SED124∗D**
TCP	SED124∗T**

- This IC is not designed against radiation and strong light and noise.

BLOCK DIAGRAM



CHIP SPECIFICATIONS



SED124∗∗∗∗

Digits for CGROM pattern change
Number of display lines
0: 4-line display
1: 3-line display
2: 2-line display

Chip size:	8.70 × 2.80 mm
Pad pitch:	90 µm (Min.)
Chip thickness (reference value):	625 ± 50 µm (SED124∗D∗∗)

Au bump specifications

Bump size	A TYPE	60.0 µm × 81.5 µm
	B TYPE	81.5 µm × 60.0 µm
	C TYPE	85.0 µm × 85.0 µm
	D TYPE	60.0 µm × 85.0 µm
Bump height (reference value)		22.5 µm ± 5.5 µm

(For bump types, refer to the pad coordinate diagram.)

Note: The board of this IC has V_{DD} potential. It is recommended to stabilize power supply by connecting the board to the V_{DD} potential at the time of mounting.

<Pad Coordinates> SED1240***

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	

PAD			COORDINATES	
No.	Name	[BUMP TYPE]	X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]		–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]		1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
109	SEG7	[A TYPE]	3009	1240
110	SEG8	[A TYPE]	2919	
111	SEG9	[A TYPE]	2830	
112	SEG10	[A TYPE]	2740	
113	SEG11	[A TYPE]	2650	
114	SEG12	[A TYPE]	2561	
115	SEG13	[A TYPE]	2471	
116	SEG14	[A TYPE]	2381	
117	SEG15	[A TYPE]	2291	
118	SEG16	[A TYPE]	2202	
119	SEG17	[A TYPE]	2112	
120	SEG18	[A TYPE]	2022	
121	SEG19	[A TYPE]	1933	
122	SEG20	[A TYPE]	1843	
123	SEG21	[A TYPE]	1753	
124	SEG22	[A TYPE]	1664	
125	SEG23	[A TYPE]	1574	
126	SEG24	[A TYPE]	1484	
127	SEG25	[A TYPE]	1394	
128	SEG26	[A TYPE]	1305	
129	SEG27	[A TYPE]	1215	
130	SEG28	[A TYPE]	1125	
131	SEG29	[A TYPE]	1036	
132	SEG30	[A TYPE]	946	
133	SEG31	[A TYPE]	856	
134	SEG32	[A TYPE]	767	
135	SEG33	[A TYPE]	677	
136	SEG34	[A TYPE]	587	
137	SEG35	[A TYPE]	497	
138	SEG36	[A TYPE]	408	
139	SEG37	[A TYPE]	318	
140	SEG38	[A TYPE]	228	
141	SEG39	[A TYPE]	139	
142	SEG40	[A TYPE]	49	
143	SEG41	[A TYPE]	–41	
144	SEG42	[A TYPE]	–130	
145	SEG43	[A TYPE]	–220	
146	SEG44	[A TYPE]	–310	
147	SEG45	[A TYPE]	–400	
148	SEG46	[A TYPE]	–489	
149	SEG47	[A TYPE]	–579	
150	SEG48	[A TYPE]	–669	
151	SEG49	[A TYPE]	–758	
152	SEG50	[A TYPE]	–848	
153	SEG51	[A TYPE]	–938	
154	SEG52	[A TYPE]	–1027	
155	SEG53	[A TYPE]	–1117	
156	SEG54	[A TYPE]	–1207	
157	SEG55	[A TYPE]	–1297	
158	SEG56	[A TYPE]	–1386	
159	SEG57	[A TYPE]	–1476	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
160	SEG58	[A TYPE]	–1566	1240
161	SEG59	[A TYPE]	–1655	
162	SEG60	[A TYPE]	–1745	
163	SEG61	[A TYPE]	–1835	
164	SEG62	[A TYPE]	–1924	
165	SEG63	[A TYPE]	–2014	
166	SEG64	[A TYPE]	–2104	
167	SEG65	[A TYPE]	–2194	
168	SEG66	[A TYPE]	–2283	
169	SEG67	[A TYPE]	–2373	
170	SEG68	[A TYPE]	–2463	
171	SEG69	[A TYPE]	–2552	
172	SEG70	[A TYPE]	–2642	
173	SEG71	[A TYPE]	–2732	
174	SEG72	[A TYPE]	–2821	
175	SEG73	[A TYPE]	–2911	
176	SEG74	[A TYPE]	–3001	
177	SEG75	[A TYPE]	–3091	
178	SEG76	[A TYPE]	–3180	
179	SEG77	[A TYPE]	–3270	
180	SEG78	[A TYPE]	–3360	
181	SEG79	[A TYPE]	–3449	
182	SEG80	[A TYPE]	–3539	
183	NC	[A TYPE]	–3704	
184	NC	[A TYPE]	–3810	
185	NC	[A TYPE]	–3915	
186	NC	[B TYPE]	–4191	1251
187	COMS2	[B TYPE]		1131
188	COM32	[B TYPE]		1041
189	COM31	[B TYPE]		951
190	COM30	[B TYPE]		861
191	COM29	[B TYPE]		772
192	COM28	[B TYPE]		682
193	COM27	[B TYPE]		592
194	COM26	[B TYPE]		503
195	COM25	[B TYPE]		413
196	COM24	[B TYPE]		323
197	COM23	[B TYPE]		234
198	COM22	[B TYPE]		144
199	COM21	[B TYPE]		54
200	COM20	[B TYPE]		–36
201	COM19	[B TYPE]		–125
202	COM18	[B TYPE]		–215
203	COM17	[B TYPE]		–305
204	COMS2	[B TYPE]		–394
205	SEGSA	[B TYPE]		–497
206	SEGSB	[B TYPE]		–617
207	SEGSC	[B TYPE]		–737
208	SEGSD	[B TYPE]		–858
209	SEGSE	[B TYPE]		–978
210	COMSA	[B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it is the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.

<Pad coordinates> SED1241***

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]		–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]		1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
109	SEG7	[A TYPE]	3009	1240
110	SEG8	[A TYPE]	2919	
111	SEG9	[A TYPE]	2830	
112	SEG10	[A TYPE]	2740	
113	SEG11	[A TYPE]	2650	
114	SEG12	[A TYPE]	2561	
115	SEG13	[A TYPE]	2471	
116	SEG14	[A TYPE]	2381	
117	SEG15	[A TYPE]	2291	
118	SEG16	[A TYPE]	2202	
119	SEG17	[A TYPE]	2112	
120	SEG18	[A TYPE]	2022	
121	SEG19	[A TYPE]	1933	
122	SEG20	[A TYPE]	1843	
123	SEG21	[A TYPE]	1753	
124	SEG22	[A TYPE]	1664	
125	SEG23	[A TYPE]	1574	
126	SEG24	[A TYPE]	1484	
127	SEG25	[A TYPE]	1394	
128	SEG26	[A TYPE]	1305	
129	SEG27	[A TYPE]	1215	
130	SEG28	[A TYPE]	1125	
131	SEG29	[A TYPE]	1036	
132	SEG30	[A TYPE]	946	
133	SEG31	[A TYPE]	856	
134	SEG32	[A TYPE]	767	
135	SEG33	[A TYPE]	677	
136	SEG34	[A TYPE]	587	
137	SEG35	[A TYPE]	497	
138	SEG36	[A TYPE]	408	
139	SEG37	[A TYPE]	318	
140	SEG38	[A TYPE]	228	
141	SEG39	[A TYPE]	139	
142	SEG40	[A TYPE]	49	
143	SEG41	[A TYPE]	–41	
144	SEG42	[A TYPE]	–130	
145	SEG43	[A TYPE]	–220	
146	SEG44	[A TYPE]	–310	
147	SEG45	[A TYPE]	–400	
148	SEG46	[A TYPE]	–489	
149	SEG47	[A TYPE]	–579	
150	SEG48	[A TYPE]	–669	
151	SEG49	[A TYPE]	–758	
152	SEG50	[A TYPE]	–848	
153	SEG51	[A TYPE]	–938	
154	SEG52	[A TYPE]	–1027	
155	SEG53	[A TYPE]	–1117	
156	SEG54	[A TYPE]	–1207	
157	SEG55	[A TYPE]	–1297	
158	SEG56	[A TYPE]	–1386	
159	SEG57	[A TYPE]	–1476	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
160	SEG58	[A TYPE]	–1566	1240
161	SEG59	[A TYPE]	–1655	
162	SEG60	[A TYPE]	–1745	
163	SEG61	[A TYPE]	–1835	
164	SEG62	[A TYPE]	–1924	
165	SEG63	[A TYPE]	–2014	
166	SEG64	[A TYPE]	–2104	
167	SEG65	[A TYPE]	–2194	
168	SEG66	[A TYPE]	–2283	
169	SEG67	[A TYPE]	–2373	
170	SEG68	[A TYPE]	–2463	
171	SEG69	[A TYPE]	–2552	
172	SEG70	[A TYPE]	–2642	
173	SEG71	[A TYPE]	–2732	
174	SEG72	[A TYPE]	–2821	
175	SEG73	[A TYPE]	–2911	
176	SEG74	[A TYPE]	–3001	
177	SEG75	[A TYPE]	–3091	
178	SEG76	[A TYPE]	–3180	
179	SEG77	[A TYPE]	–3270	
180	SEG78	[A TYPE]	–3360	
181	SEG79	[A TYPE]	–3449	
182	SEG80	[A TYPE]	–3539	
183	NC	[A TYPE]	–3704	
184	NC	[A TYPE]	–3810	
185	NC	[A TYPE]	–3915	
186	NC	[B TYPE]	–4191	1251
187	COMS2	[B TYPE]		1131
188	*COM32	[B TYPE]		1041
189	*COM31	[B TYPE]		951
190	*COM30	[B TYPE]		861
191	*COM29	[B TYPE]		772
192	*COM28	[B TYPE]		682
193	*COM27	[B TYPE]		592
194	*COM26	[B TYPE]		503
195	*COM25	[B TYPE]		413
196	*COM24	[B TYPE]		323
197	*COM23	[B TYPE]		234
198	*COM22	[B TYPE]		144
199	*COM21	[B TYPE]		54
200	*COM20	[B TYPE]		–36
201	*COM19	[B TYPE]		–125
202	*COM18	[B TYPE]		–215
203	*COM17	[B TYPE]		–305
204	COMS2	[B TYPE]		–394
205	SEGSA	[B TYPE]		–497
206	SEGSB	[B TYPE]		–617
207	SEGSC	[B TYPE]		–737
208	SEGSD	[B TYPE]		–858
209	SEGSE	[B TYPE]		–978
210	COMSA	[B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.
*: Don't connect COM17 to COM32.

<Pad coordinates> SED1242***

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
1	NC	[B TYPE]	–4191	–1250
2	NC	[C TYPE]	–3941	–1237
3	NC	[C TYPE]	–3836	
4	NC	[C TYPE]	–3555	
5	A0	[C TYPE]	–3403	
6	$\overline{WR}$	[C TYPE]	–3283	
7	$\overline{CS}$	[C TYPE]	–3163	
8	D7	[C TYPE]	–3043	
9	D6	[C TYPE]	–2922	
10	D5	[C TYPE]	–2802	
11	D4	[C TYPE]	–2682	
12	D3	[C TYPE]	–2562	
13	D2	[C TYPE]	–2441	
14	D1	[C TYPE]	–2321	
15	D0	[C TYPE]	–2201	
16	V_{DD}	[D TYPE]	–2089	
17	V_{DD}	[D TYPE]	–1999	
18	V_{DD}	[D TYPE]	–1909	
19	V_{SS}	[D TYPE]	–1820	
20	V_{SS}	[D TYPE]	–1730	
21	V_5	[D TYPE]	–1641	
22	V_5	[D TYPE]	–1551	
23	V_4	[D TYPE]	–1461	
24	V_4	[D TYPE]	–1371	
25	V_3	[D TYPE]	–1282	
26	V_3	[D TYPE]	–1192	
27	V_2	[D TYPE]	–1102	
28	V_2	[D TYPE]	–1013	
29	V_1	[D TYPE]	–923	
30	V_1	[D TYPE]	–833	
31	V_0	[D TYPE]	–744	
32	V_0	[D TYPE]	–654	
33	V_R	[D TYPE]	–564	
34	V_R	[D TYPE]	–474	
35	V_{OUT}	[D TYPE]	–385	
36	V_{OUT}	[D TYPE]	–295	
37	CAP2–	[D TYPE]	–205	
38	CAP2–	[D TYPE]	–116	
39	CAP2+	[D TYPE]	–26	
40	CAP2+	[D TYPE]	64	
41	CAP1–	[D TYPE]	153	
42	CAP1–	[D TYPE]	243	
43	CAP1+	[D TYPE]	333	
44	CAP1+	[D TYPE]	423	
45	V_{SS}	[D TYPE]	512	
46	V_{SS}	[D TYPE]	602	
47	V_{SS2}	[D TYPE]	692	
48	V_{SS2}	[D TYPE]	781	
49	V_{DD}	[D TYPE]	871	
50	V_{DD}	[D TYPE]	961	
51	V_{DD}	[D TYPE]	1050	
52	$\overline{CK}$	[C TYPE]	1183	
53	V_{S1}	[C TYPE]	1303	
54	V_{SS}	[C TYPE]	1423	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
55	P/S	[C TYPE]	1543	–1237
56	V_{DD}	[C TYPE]	1664	
57	IF	[C TYPE]	1784	
58	V_{SS}	[C TYPE]	1904	
59	C86	[C TYPE]	2024	
60	V_{DD}	[C TYPE]	2145	
61	$\overline{RES}$	[C TYPE]	2265	
62	V_{DD}	[C TYPE]	2385	
63	(FSA)	[C TYPE]	2505	
64	(FSB)	[C TYPE]	2636	
65	(FSC)	[C TYPE]	2767	
66	(FS0)	[C TYPE]	2897	
67	(FS1)	[C TYPE]	3028	
68	(FS2)	[C TYPE]	3159	
69	(FS3)	[C TYPE]	3289	
70	V_{DD}	[C TYPE]	3420	
71	V_{DD}	[C TYPE]	3550	
72	NC	[C TYPE]	3689	
73	NC	[C TYPE]	3794	
74	NC	[C TYPE]	3899	
75	NC	[B TYPE]	4191	–1250
76	COMSA	[B TYPE]		–1098
77	SEGSF	[B TYPE]		–978
78	SEGSG	[B TYPE]		–858
79	SEGSH	[B TYPE]		–737
80	SEGSI	[B TYPE]		–617
81	SEGSJ	[B TYPE]		–497
82	COMS1	[B TYPE]		–394
83	COM1	[B TYPE]		–305
84	COM2	[B TYPE]		–215
85	COM3	[B TYPE]		–125
86	COM4	[B TYPE]		–36
87	COM5	[B TYPE]		54
88	COM6	[B TYPE]		144
89	COM7	[B TYPE]		234
90	COM8	[B TYPE]		323
91	COM9	[B TYPE]		413
92	COM10	[B TYPE]		503
93	COM11	[B TYPE]		592
94	COM12	[B TYPE]		682
95	COM13	[B TYPE]		772
96	COM14	[B TYPE]		861
97	COM15	[B TYPE]		951
98	COM16	[B TYPE]		1041
99	COMS1	[B TYPE]		1131
100	NC	[B TYPE]		1251
101	NC	[A TYPE]	3915	1240
102	NC	[A TYPE]	3810	
103	SEG1	[A TYPE]	3547	
104	SEG2	[A TYPE]	3458	
105	SEG3	[A TYPE]	3368	
106	SEG4	[A TYPE]	3278	
107	SEG5	[A TYPE]	3188	
108	SEG6	[A TYPE]	3099	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
109	SEG7	[A TYPE]	3009	1240
110	SEG8	[A TYPE]	2919	
111	SEG9	[A TYPE]	2830	
112	SEG10	[A TYPE]	2740	
113	SEG11	[A TYPE]	2650	
114	SEG12	[A TYPE]	2561	
115	SEG13	[A TYPE]	2471	
116	SEG14	[A TYPE]	2381	
117	SEG15	[A TYPE]	2291	
118	SEG16	[A TYPE]	2202	
119	SEG17	[A TYPE]	2112	
120	SEG18	[A TYPE]	2022	
121	SEG19	[A TYPE]	1933	
122	SEG20	[A TYPE]	1843	
123	SEG21	[A TYPE]	1753	
124	SEG22	[A TYPE]	1664	
125	SEG23	[A TYPE]	1574	
126	SEG24	[A TYPE]	1484	
127	SEG25	[A TYPE]	1394	
128	SEG26	[A TYPE]	1305	
129	SEG27	[A TYPE]	1215	
130	SEG28	[A TYPE]	1125	
131	SEG29	[A TYPE]	1036	
132	SEG30	[A TYPE]	946	
133	SEG31	[A TYPE]	856	
134	SEG32	[A TYPE]	767	
135	SEG33	[A TYPE]	677	
136	SEG34	[A TYPE]	587	
137	SEG35	[A TYPE]	497	
138	SEG36	[A TYPE]	408	
139	SEG37	[A TYPE]	318	
140	SEG38	[A TYPE]	228	
141	SEG39	[A TYPE]	139	
142	SEG40	[A TYPE]	49	
143	SEG41	[A TYPE]	–41	
144	SEG42	[A TYPE]	–130	
145	SEG43	[A TYPE]	–220	
146	SEG44	[A TYPE]	–310	
147	SEG45	[A TYPE]	–400	
148	SEG46	[A TYPE]	–489	
149	SEG47	[A TYPE]	–579	
150	SEG48	[A TYPE]	–669	
151	SEG49	[A TYPE]	–758	
152	SEG50	[A TYPE]	–848	
153	SEG51	[A TYPE]	–938	
154	SEG52	[A TYPE]	–1027	
155	SEG53	[A TYPE]	–1117	
156	SEG54	[A TYPE]	–1207	
157	SEG55	[A TYPE]	–1297	
158	SEG56	[A TYPE]	–1386	
159	SEG57	[A TYPE]	–1476	

PAD			COORDINATES	
No.	Name [BUMP TYPE]		X	Y
160	SEG58	[A TYPE]	–1566	1240
161	SEG59	[A TYPE]	–1655	
162	SEG60	[A TYPE]	–1745	
163	SEG61	[A TYPE]	–1835	
164	SEG62	[A TYPE]	–1924	
165	SEG63	[A TYPE]	–2014	
166	SEG64	[A TYPE]	–2104	
167	SEG65	[A TYPE]	–2194	
168	SEG66	[A TYPE]	–2283	
169	SEG67	[A TYPE]	–2373	
170	SEG68	[A TYPE]	–2463	
171	SEG69	[A TYPE]	–2552	
172	SEG70	[A TYPE]	–2642	
173	SEG71	[A TYPE]	–2732	
174	SEG72	[A TYPE]	–2821	
175	SEG73	[A TYPE]	–2911	
176	SEG74	[A TYPE]	–3001	
177	SEG75	[A TYPE]	–3091	
178	SEG76	[A TYPE]	–3180	
179	SEG77	[A TYPE]	–3270	
180	SEG78	[A TYPE]	–3360	
181	SEG79	[A TYPE]	–3449	
182	SEG80	[A TYPE]	–3539	
183	NC	[A TYPE]	–3704	
184	NC	[A TYPE]	–3810	
185	NC	[A TYPE]	–3915	
186	NC	[B TYPE]	–4191	1251
187	COMS2	[B TYPE]		1131
188	*COM32	[B TYPE]		1041
189	*COM31	[B TYPE]		951
190	*COM30	[B TYPE]		861
191	*COM29	[B TYPE]		772
192	*COM28	[B TYPE]		682
193	*COM27	[B TYPE]		592
194	*COM26	[B TYPE]		503
195	*COM25	[B TYPE]		413
196	*COM24	[B TYPE]		323
197	*COM23	[B TYPE]		234
198	*COM22	[B TYPE]		144
199	*COM21	[B TYPE]		54
200	*COM20	[B TYPE]		–36
201	*COM19	[B TYPE]		–125
202	*COM18	[B TYPE]		–215
203	*COM17	[B TYPE]		–305
204	COMS2	[B TYPE]		–394
205	SEGSA	[B TYPE]		–497
206	SEGSB	[B TYPE]		–617
207	SEGSC	[B TYPE]		–737
208	SEGSD	[B TYPE]		–858
209	SEGSE	[B TYPE]		–978
210	COMSA	[B TYPE]		–1098

(FS*) : This is a FUSE adjusting pin. Set it in the floating state.
$\overline{CK}$ pin : Fix it to V_{DD} when it is not used.
*: Don't connect COM17 to COM32.

DESCRIPTION OF PINS

Power Pins

Pin name	I/O	Description	Q'ty
Board potential		IC board is based on V_{DD} potential. To lock the board potential with V_{DD}.	
V_{DD}	Power supply	Connected to the logic power supply. This is used in common with the MPU power pin V_{CC}.	6
V_{SS}	Power supply	0 V power pin that is connected to system GND.	4
V_0, V_1 V_2, V_3 V_4, V_5	Power supply	Multi-level power supply for liquid crystal drive. The voltage determined for the liquid crystal cell is applied by resistance-division or impedance conversion by operational amplifier. The potential is determined on V_{DD} and the following relations must be observed. $V_{DD} = V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{DD} \geq V_5 \geq V_{OUT}$ $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$ When the built-in power supply is ON, the following voltages are given to V1 to V4 by command selection. $V_1 = 1/5\ V_5$ ($1/4\ V_5$) $V_2 = 2/5\ V_5$ ($2/4\ V_5$) $V_3 = 3/5\ V_5$ ($2/4\ V_5$) $V_4 = 4/5\ V_5$ ($3/4\ V_5$)	6
V_{S1}	O	Supply voltage output pin for oscillating circuit. Don't connect a load to the outside.	1

LCD Power Circuit Pins

Pin name	I/O	Description	Q'ty
CAP1+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP1– pin.	1
CAP1–	O	Boosting condenser negative side connecting pin. Condenser is connected with the CAP1+ pin.	1
CAP2+	O	Boosting condenser positive side connecting pin. Condenser is connected with the CAP2– pin.	1
CAP2–	O	A boosting condenser negative side connecting pin. Condenser is connected with the CAP2+ pin.	1
V_{OUT}	O	Output pin for boosting. Smoothing condenser is connected with V_{DD}.	1
V_R	I	Voltage adjusting pin. Voltage between V_{DD} and V_5 is given by resistance-division.	1
V_{SS2}	I	Boosting power pin. The voltage between V_{DD} and V_{SS2} is boosted by a specified multiple.	1

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Q'ty</th></tr>
<tr><td>D7 (SI)
D6 (SCL)
D5 to D0</td><td>I</td><td>8-bit input data bus which is connected to the 16-bit standard MPU data bus.
Pin D7 and pin D6 function as a serial data input and a serial clock input at P/S = “L”, respectively.
<table>
<tr><th>Pin / Mode</th><th>P/S</th><th>C86</th><th>IF</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3-D0</th><th>$\overline{CS}$</th><th>A0</th><th>$\overline{WR}$</th></tr>
<tr><td>Serial I/F</td><td>“L”</td><td>H or L</td><td>—</td><td>SI</td><td>SCL</td><td>OPEN</td><td>OPEN</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>—</td></tr>
<tr><td>68I/F 8bit</td><td>“H”</td><td>“H”</td><td>“H”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>68I/F 4bit</td><td>“H”</td><td>“H”</td><td>“L”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>E</td></tr>
<tr><td>80I/F 8bit</td><td>“H”</td><td>“L”</td><td>“H”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3-D0</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
<tr><td>80I/F 4bit</td><td>“H”</td><td>“L”</td><td>“L”</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>OPEN</td><td>$\overline{CS}$</td><td>A0</td><td>$\overline{WR}$</td></tr>
</table>
C86: An MPU selecting pin
OPEN: OPEN is allowable, but it is recommend to fix it to one of potentials as a matter of noise-resistance characteristic.
—: Either “H” or “L” is allowable, but the potential should be fixed.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Usually used to distinguish data from a command to which the LSB of the MPU address bus is connected.
“L” : Indicates that D0 to D7 are of a command.
“H” : Indicates that D0 to D7 are of data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset pin for initializing the whole IC. Be sure to input it once when the power supply is turned on. A reset operation is performed at the “L” level of the $\overline{RES}$ signal.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU selecting pin. Fix it to “H” or “L” depending on the MPU to be used.
“L” : 80 series MPU interface
“H” : 68 series MPU interface</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip selecting pin. Usually, it inputs a signal that is obtained by decoding an address signal. Chip selection is enabled at the “L” level.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(E)</td><td>I</td><td><When the 80 series MPU is selected> Active “L”
A pin for connecting the WR signal of the 80 series MPU.
The signal on the data bus is latched at the rise of the $\overline{WR}$ signal.
<When the 68 series MPU is connected> Active “H”
Becomes an enable clock input of the 68 series MPU.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>A pin for selecting either serial interface or parallel interface.
“L” : Serial interface
“H” : Parallel interface</td><td>1</td></tr>
<tr><td>IF</td><td>I</td><td>A data bit length selecting pin at parallel interface.
“H” : 8-bit parallel interface
“L” : 4-bit parallel interface
At P/S = “L”, set pins D3 to D0 to V_{DD} or V_{SS}, or OPEN.</td><td>1</td></tr>
<tr><td>$\overline{CK}$</td><td>I</td><td>An external clock input pin.
When using the internal oscillating circuit, fix it to “H”.
When using an external clock input, the internal oscillating circuit must be turned off by command.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Circuit Signals

Dynamic Drive Pins [SED1240]

Pin name	I/O	Description	Q'ty
COM1 to COM32	O	Common signal output pins (for characters)	32
COMS1, COMS2	O	Common signal output pins (for others than characters) COMS1, COMS2: Symbol output command output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [SED1241]

Pin name	I/O	Description	Q'ty
COM1 to COM24	O	Common signal output pins (for characters)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Dynamic Drive Pins [SED1242]

Pin name	I/O	Description	Q'ty
COM1 to COM16	O	Common signal output pins (for characters) (Keep COM17 to COM32 unconnected.)	16
COMS1, COMS2	O	Common signal output pins (for others than characters) CMOS1, CMOS2: Symbol display common output	4
SEG1 to SEG80	O	Segment signal output pins (for characters)	80

Static Drive Pins

Pin name	I/O	Description	Q'ty
COMSA	O	Common signal output pin (for static icons)	2
SEGS A to J	O	Segment signal output pins (for static icons)	10

Note: For the electrode of the liquid crystal display panel connected to the static drive terminal, it is recommended use the pattern separated from the electrode connected to the dynamic drive terminal. If this pattern is too close, the liquid crystal and electrode may be deteriorated.

DESCRIPTION OF FUNCTIONS

MPU Interfaces

In the SED1240 series, an MPU type, interface bit length and interface method can be selected depending on pins IF, P/S and C86.

Selection of MPU

In the SED1240 series, when parallel input is selected (P/S = "H"), pin C86 has an MPU selecting function.
When either "H" or "L" is selected as the polarity of pin C86, the 80 series MPU or 68 series MPU can be selected as shown in Table 1.
Selection of an interface bit length (8 bits, 4 bits) is performed by pin IF.

Table 1

MPU type	Pin C86 state	Polarity of $\overline{RES}$ function input	MPU connection			
			A0	$\overline{WR}$	$\overline{CS}$	D0 to D7
68 series	High level	Low level active	A0	E	$\overline{CS}$	D0 to D7
80 series	Low level		A0	$\overline{WR}$	$\overline{CS}$	D0 to D7

Selection of interface type

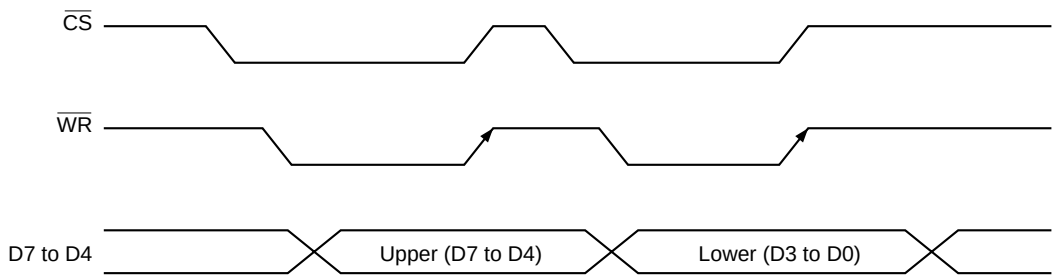
In the SED1240 series, it is possible to select an 8-bit or 4-bit parallel interface or a serial interface that permits a data transfer through a serial input (SI). As the selecting method, set the polarity of pins of P/S and IF to "H" or "L".

Table 2

Interface type	Interface bit length	Selecting pin state		Pin state										
		P/S	IF	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	8 bits	H	H	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Parallel	4 bits	H	L	$\overline{CS}$	A0	$\overline{WR}$	D7	D6	D5	D4	OPEN or H or L			
Serial	1 bit	L	H or L	$\overline{CS}$	A0	H or L	SI	SCL	OPEN or H or L					

Interface with 4-bit MPU

When data is transferred by a 4-bit interface (IF = 0), 8-bit commands, data and addresses are divided into 2 parts for transfer. A timing example of the 80 series MPU is shown below.



Note: For continuous writing, perform it after securing a time exceeding the system cycle time (t_{cyc}).

Serial interface (P/S = "L")

The serial interface consists of an 8-bit shift register and a 3-bit counter, and becomes ready to accept an SI input or SCL input in the chip selected state ($\overline{CS}$ = "L").
Unless any chip is selected, the shift register and the counter are reset to the initial state. (Refresh state)
Data is input in the order of D7, D6, ... D0 from the serial data input pin (SI) at the rise of the serial clock (SCL). At the rising edge of the 8th serial clock, the data is converted into parallel data.
Whether the serial data input (SI) is display data or a command is identified and judged by A0 input. When A0 = "H", the data becomes display data. When A0 = "L", the data becomes a command. The A0 input is read and identified at the rise of the 8 × nth serial clock (SCL) after chip selection.

Fig. 1 shows a timing chart of the serial interface. In case of the SCL signal, extreme care should be taken about terminal reflection and external noise due to a wiring length. Accordingly, it is recommended to make an operation check.
It is also recommended to periodically refresh the each command write state to prevent a malfunction from being caused by noise.

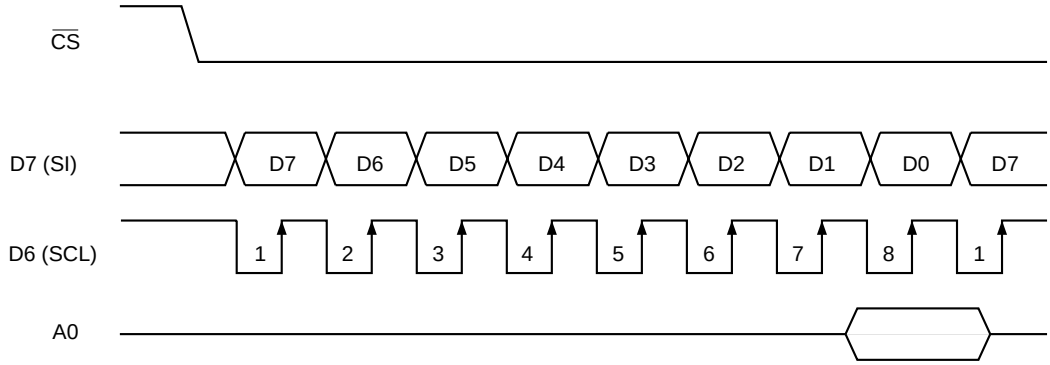


Fig. 1 Serial Interface Input Timing

Identification of data bus signals

The SED1240 series identifies each data bus signal by a combination of A0 and $\overline{WR}$ (E) as shown in Table 3.

Table 3

Common	68 series	80 series	Function
A0	(E)	$\overline{WR}$	
1	1	0	Writes into the RAM and symbol register.
0	1	0	Writes into the internal register (commands)

Chip select

The SED1240 series has chip select pin $\overline{CS}$. Only when $\overline{CS}$ = "L", the MPU interface is enabled. In the other states than the chip select state, D0 to D7 and A0, $\overline{WR}$, SI, and SCL inputs are invalidated. When an serial input interface is selected, the shift register and the counter are reset. However, the $\overline{RES}$ input can be performed regardless of the $\overline{CS}$ state.

Power Circuit

The power circuit built in the SED1240 series is a low power consumption power circuit that generates a voltage required for liquid crystal drive, and consists of a boosting circuit, voltage regulating circuit, and voltage follower.
The power circuit capacity is set for a small-scale liquid crystal panel.
In the case of a liquid crystal panel with a large display capacity, the display quality may be remarkably degraded. In this case, an external power supply is required.
Functional selection is performed by power control commands.
Some parts of the external power supply and the internal power supply can be used together.

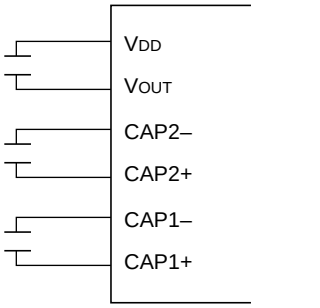
Table 4

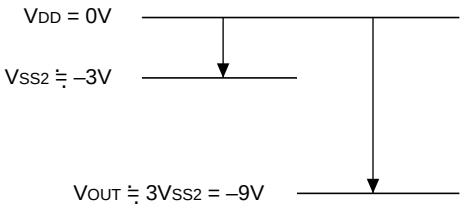
	Boosting circuit	Voltage regulating circuit	Voltage follower	External voltage input	Boosting system pin
	○	○	○	V_{SS2}	USE
Note 1	×	○	○	V_{OUT}, V_{SS2}	OPEN
Note 2	×	×	○	V_5, V_{SS2}	OPEN
Note 3	×	×	×	V_1, V_2, V_3, V_4, V_5	OPEN

Note 1: When the boosting circuit is turned off, set the boosting system pins (CAP1+, CAP1–, CAP2+, CAP2–) to OPEN so that liquid crystal drive voltages may be applied to the V_{OUT} pin from the outside.
Note 2: When the voltage regulating circuit is not used with the boosting circuit OFF, set the V_{OUT} pin and the boosting system pins to OPEN and connect the V_5 pin to give liquid crystal drive voltages from the outside.
Note 3: When all the built-in power supplies are turned off, liquid crystal drive voltages V_1, V_2, V_3, V_4, and V_5 are supplied from the outside and set the CAP1+, CAP1–, V_{SS2} and V_{OUT} pins to OPEN.

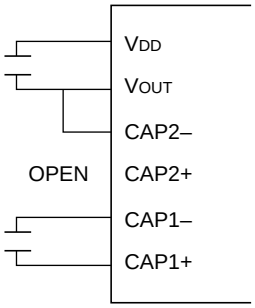
Boosting circuit

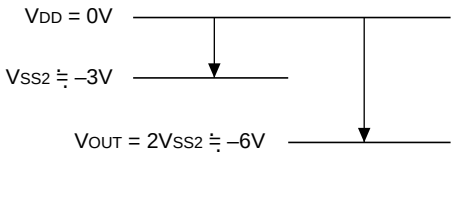
The SED1240 series is provided with a boosting circuit for triple boosting and double boosting for the potential between V_{DD} and V_{SS2}.
For triple boosting, connect a capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, and between V_{DD} and V_{OUT}, and the V_{DD} - V_{SS2} potential is triple-boosted to the negative side and output to the V_{OUT} pin.
For double boosting, connect a capacitor between CAP1+ and CAP1– and between V_{DD} and V_{OUT}, set CAP2+ to OPEN, and connect CAP2– to V_{OUT}, and the V_{DD} - V_{SS2} potential is double-boosted to the negative side and output to the V_{OUT} pin.
Because the boosting circuit uses signals from the oscillator output, the internal oscillating circuit or the external clock must be in operation.
The relation of boosting voltages is shown below.
Set the potential between the V_{DD} and V_{SS2} to ensure that the V_{OUT} does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} (V_5) when double or triple boosted.





Potential relation of triple boosting voltages





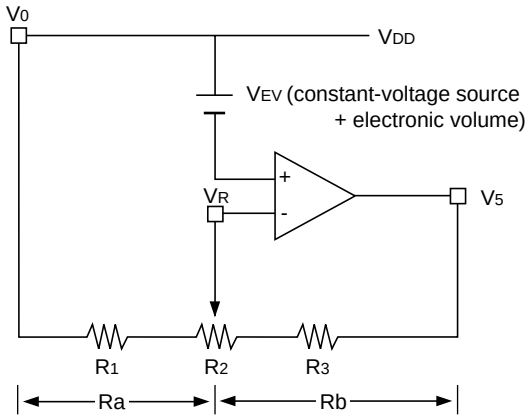
Potential relation of double boosting voltages

* Set the V_{SS2} voltage range to ensure that V_{OUT} terminal voltage does not exceed the permissible operating voltage range of V_{SS} - V_{OUT} and absolute maximum rating.

Voltage regulating circuit

The boosting voltage generated at V_{OUT} is output as a liquid crystal drive voltage of V_5 through the voltage regulating circuit.
The SED1240 series is provided with a high-precision constant-voltage source, a 32-step electronic volume function, and a V_5 voltage regulating resistor. This permits constructing a high-precision voltage regulating circuit with a small quantity of parts. The voltage regulating circuit outputs V_{EV} and has a temperature gradient of about –0.04%.
As the V_5 voltage regulating resistor, a built-in resistor or an external resistor can be selected by command as a matter of configuration.

[When using an external resistor (No use of V_5 voltage regulating built-in resistor is set by command.)]
The V_5 voltage can be obtained from the following expression ① by adjusting resistors Ra and Rb within the range of $|V_5| < |V_{OUT}|$.



$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

In this case, V_{EV} is determined by the constant-voltage source in the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq$ 2.0 V, being constant.
For voltage adjustment of V_5 output, connect a variable resistor among V_R, V_{DD}, and V_5. For fine voltage adjustment of V_5 output, it is recommended to combine fixed resistors R1 and R3 with variable resistor R2.

[R1, R2 and R3 setup example]

- R1 + R2 + R3 = 1.2 MΩ (Determined by the current value I_{05} flowing between V_{DD} and V_5. Supposing $I_{05} \leq 5$ μA)
- Minimum voltage of V_5: –6 V (Determined by liquid crystal characteristic)
- Variable voltage range by R2: –4 to –6 V (Determined by the liquid crystal characteristic)
- When the electronic volume register is set to (0, 0, 0, 0, 0), V_{EV} = 2.0 V (TYP). Accordingly, each resistor value can be calculated by the above conditions and expression ① as follows.

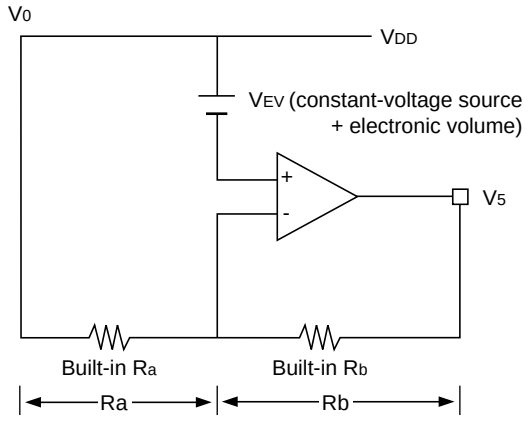
R1 = 400 KΩ
R2 = 200 KΩ
R3 = 600 KΩ

Note 1: The input impedance of the V_R pin is high, so it is necessary to take a proper measure against noise for short wiring and shielding wiring.

[When using the V_5 voltage regulating built-in resistor (Use of V_5 voltage regulating built-in resistor is set by command.)]
When the V_5 voltage regulating built-in resistor and the electronic volume function are used, the liquid crystal supply voltage V_5 can be controlled and the density of liquid crystal display can be controlled by commands only without adding any external resistor.
The V_5 voltage can be obtained by the following expression ② by adjusting resistors Ra and Rb within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots ②$$

In this case, V_{EV} is determined by the constant-voltage source within the IC and by setting the electronic volume. When the electronic volume value is (00000), $V_{REG} \fallingdotseq 2.0$ V, being constant.



The voltage range of the V_5 output can be adjusted by changing the built-in resistor ratio (1 + Rb/Ra) by command. Reference values are shown in Table 5 and Fig. 2.

Table 5 V_5 voltage regulating built-in resistor ratio set values (reference values)

Command		(1 + Rb/Ra)
IR1	IR0	
0	0	2.81
0	1	3.27
1	0	3.72
1	1	4.21

V5 voltage by V5 voltage regulating built-in resistor ratio set value and electronic volume resistor value (reference value)
[Fig. 2]

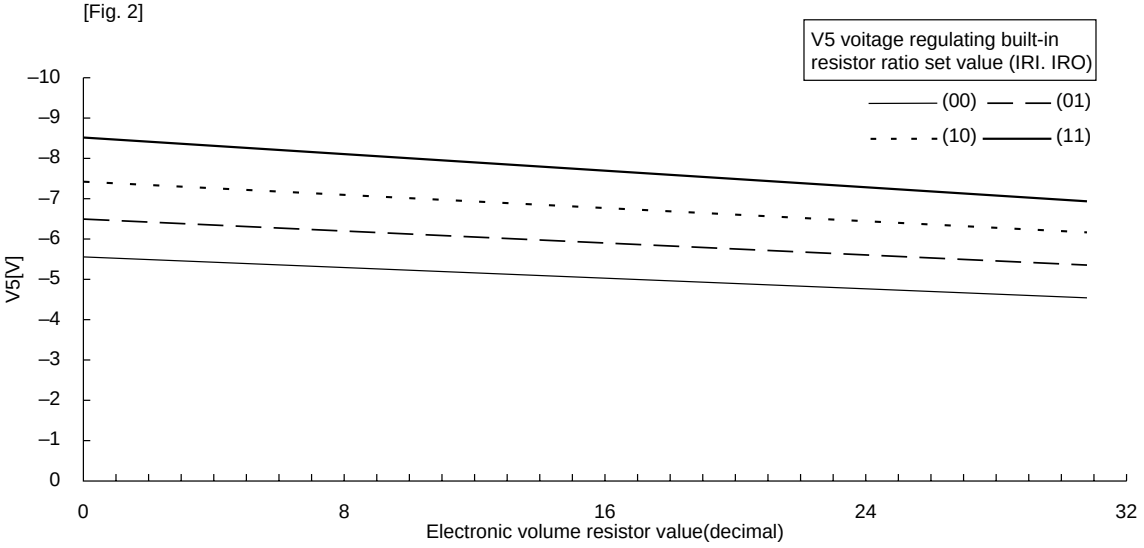
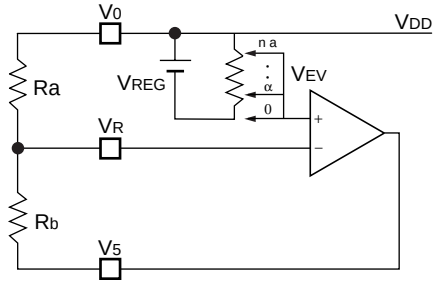


Fig. 2

- Voltage regulating circuit using the electronic volume function
  When the electronic volume function is used, the liquid crystal drive voltage V_5 can be controlled by the command to adjust the density of liquid crystal display. Regarding this method, set 5-bit data in the electronic volume register, and the liquid crystal drive voltage V_5 can take one of 32 states of voltage value.
  When the electronic volume function is used, the voltage regulating circuit must be turned on by the power control command.

[Constant setup example when using the electronic volume function]



$$V_5 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV}$$

However: $V_{EV} = V_{REG} - \alpha$

$\alpha = V_{REG} / 150$

Table 6

No.	Electronic volume register	α	V_5
0	(0, 0, 0, 0, 0)	0	Large
1	(0, 0, 0, 0, 1)	1α	•
2	(0, 0, 0, 1, 0)	2α	•
3	(0, 0, 0, 1, 1)	3α	•
•	•	•	•
•	•	•	•
30	(1, 1, 1, 1, 0)	n-1α	•
31	(1, 1, 1, 1, 1)	nα	Small

When the electronic volume function is not used, set the electronic volume register to (0,0,0,0,0).

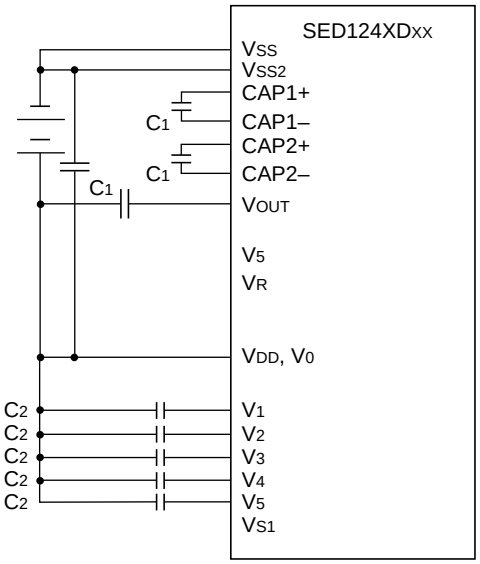
Liquid crystal voltage generating circuit

The V_5 potential is resistance-divided by the built-in resistor of the IC or external resistors Ra and Rb, generating potentials V_1, V_2, V_3, and V_4 required for liquid crystal drive. Furthermore, potentials V_1, V_2, V_3, and V_4 are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

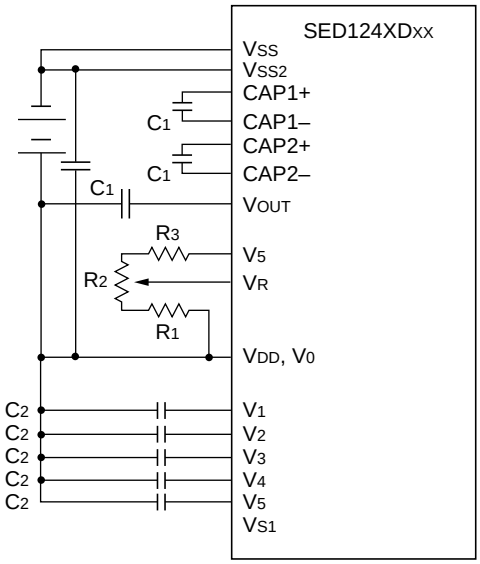
Regarding the liquid crystal drive voltage, the 1/5 bias or 1/4 bias can be selected by command. For liquid crystal power pins, capacitors C2 for voltage stabilization must be connected to pins V_1 to V_5 externally.
A reference circuit example of each case is shown below.

① Using all of the boosting circuit, power regulating circuit, and voltage follower

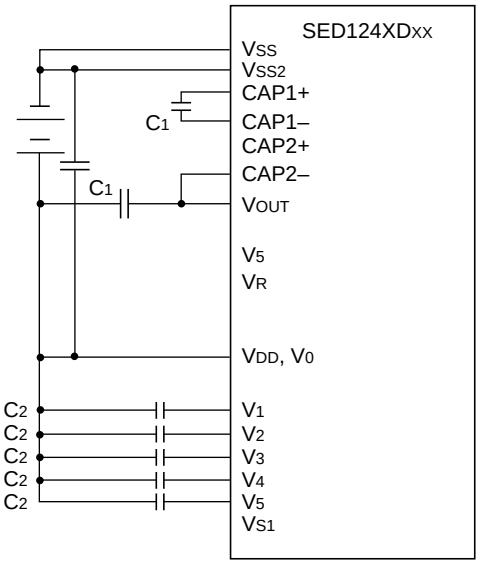
[When using a V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



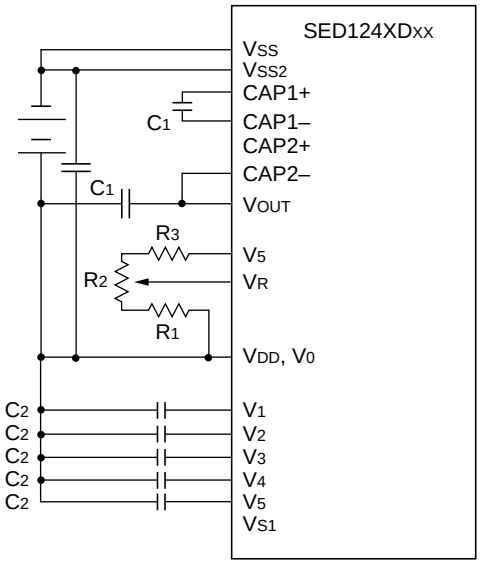
[When using no V_5 voltage regulating built-in resistor]
(Example of V_{SS2} = V_{SS}, triple boosting)



(Example of V_{SS2} = V_{SS}, double boosting)



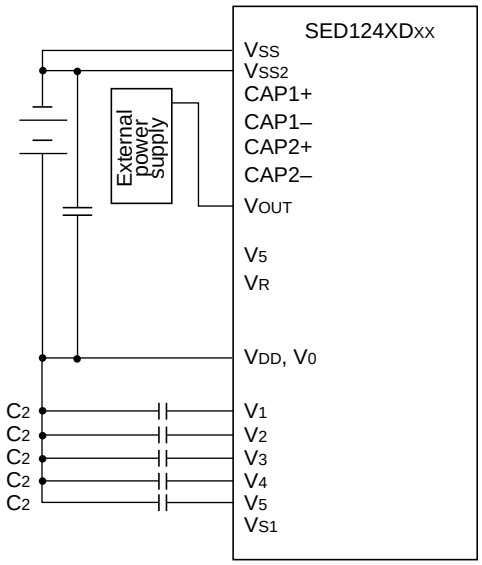
(Example of V_{SS2} = V_{SS}, double boosting)



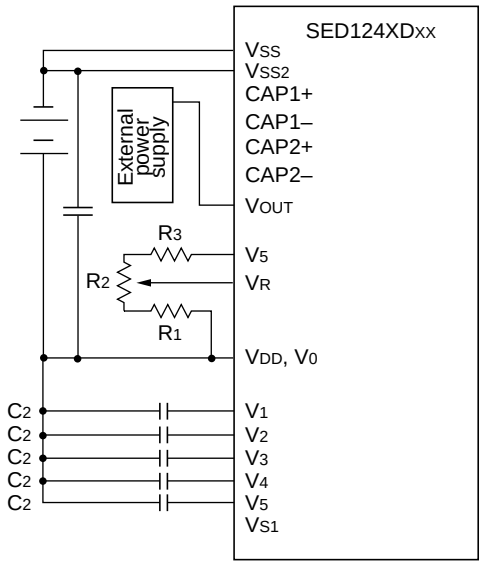
Reference set values: C_1: 0.47 to 4.7 µF It is recommended to set optimum values suitable for the panel size in
C_2: 0.1 to 4.7 µF capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

② Using only the voltage regulating circuit and the voltage follower.

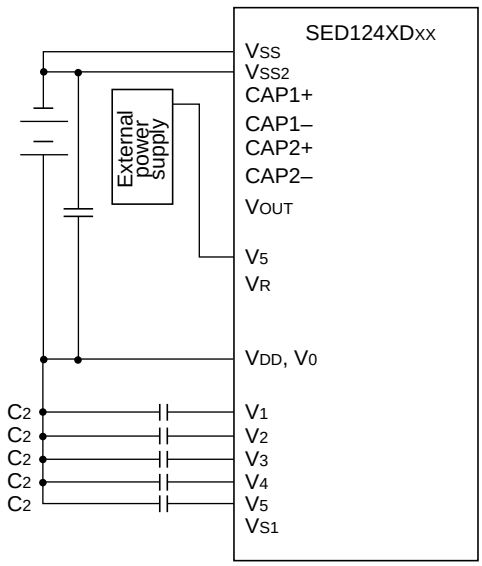
[When using a V_5 voltage regulating built-in resistor]
(Example of $V_{SS2} = V_{SS}$)



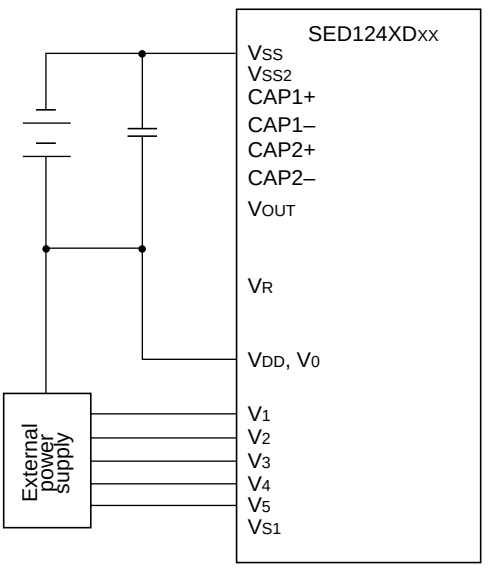
[When using no V_5 voltage regulating built-in resistor]
(Example of $V_{SS2} = V_{SS}$)



(Example of $V_{SS2} = V_{SS}$)



(Example of $V_{SS2} = V_{SS}$)



Reference set values: C_1: 0.47 to 4.7 µF It is recommended to set optimum values suitable for the panel size in
C_2: 0.1 to 4.7 µF capacitors C_1 and C_2 while watching the liquid crystal display and drive waveforms.

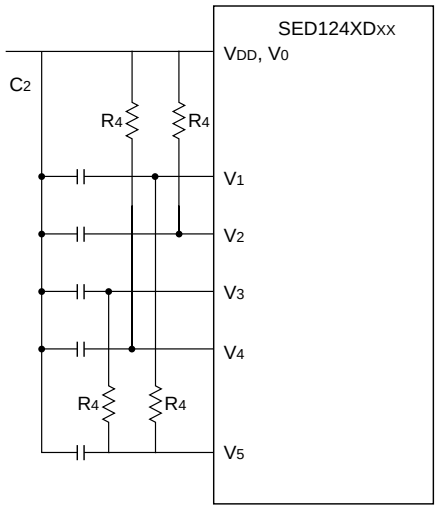
*1 Because the input impedance of the V_R pin is high, use a short wire and a shielding wire.

*2 Determine C_1 and C_2 values depending on the size of the LCD panel to be driven. Set proper values that permit stabilizing the liquid crystal drive voltages.

[Setting example]
- Turn on the voltage regulating circuit and the voltage follower and give a voltage to V_{OUT} from the outside.
- Display a LCD heavy load pattern like horizontal stripes and determine a C_2 value so that the liquid crystal drive voltages (V_1 to V_5) may be stabilized. However, it is necessary to set the same capacity value in C_2 in every case.
- Next, turn on the built-in power supply and determine a C_1 value.

*3 Connect a capacity between V_{DD} and V_{SS} for voltage stabilization.

When driving a liquid crystal panel with heavy alternating or direct current load using an internal power supply circuit, we recommend that you connect an external resistance in order to stabilize the level of the internal voltage follower outputs V_1, V_2, V_3 and V_4.



Reference setting value: R_4: 100 k ohm to 1 M ohm

For resistance value R_4, we recommend that you set it to an optimum value according to the liquid crystal panel indication and the drive waveform.

High power mode

The power circuit built-in the SED1240 series is a low power consumption type. (when the high power mode is OFF)
Accordingly, in the case of a large load liquid crystal or panel, the display quality may be degraded. In this case, the display quality can be improved by entering HPM = '1' by command. Before determining whether or not to use this mode, it is recommended to make a display check with a real machine.
In case the display quality cannot be improved satisfactorily though the high power mode is set, a liquid crystal drive power must be supplied from the outside.

Low Power Consumption Mode

The SED1240 series is provided with the standby mode/ sleep mode to attain low power consumption in the standby status of the unit.

● Standby mode
The standby mode is turned on and off by the power save command and display off/booster circuit off command. Only static icons can be displayed.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Can be caused to come on by static drive.
   Control the static icon display by SEGSA, B, C, D, E, F, G, H, I, J, COMSA by the static icon RAM.
2. Contents of DDRAM, CGRAM, and symbol register
   The written contents are kept in memory regardless of the ON/OFF status of the standby mode.
3. The operation mode remains in the status provided before execution of the standby mode. The internal circuit for dynamic display output is stopped.
4. Oscillating circuit
   For static display, the oscillating circuit must be ON.

● Sleep mode
Turn off the power circuit and the oscillating circuit, set '0' in all the data of the static icon register, and execute the power save command.
Then, the sleep mode is set and the current consumption can be reduced to a value close to the static current.

1. Liquid crystal display output
   COM1 to COM32, COMS1, COMS2: VDD level
   SEG1 to SEG80, SEGS1, 2, 4, 5: VDD level
   SEGSA, B, C, D, E, F, G, H, I, J, COMSA: Set '0' in all the data of the static icon register and blink ON/ OFF (for static icons).
2. Contents of SSRAM, CGRAM and symbol register
   The written contents can be kept in memory regardless of the ON/OFF status of the sleep mode.
3. The operation mode remains in the status provided before execution of the sleep mode. All the internal circuits are stopped.
4. Power circuit and oscillating circuit
   Turn off the built-in power supply and oscillating circuit by the power save command and the power control command.

* Caution: If the oscillating circuit is stopped with the static icon register data and blinking kept off, previous display will remain on the icon. To avoid this, be sure to turn off the data and blinking before stopping the oscillating circuit.

Reset Circuit

When the $\overline{RES}$ input becomes active, this LSI will be put into the initial setup status. Resetting is performed at the 'L' level of the $\overline{RES}$ input signal.

● Initial setup status

1. Line scroll register
   LS1, 0 = 0 : Scroll amount 0 line
2. Line blink control

LB4 = 0 : DDRAM line 4 blink OFF
LB3 = 0 : DDRAM line 3 blink OFF
LB2 = 0 : DDRAM line 2 blink OFF
LB1 = 0 : DDRAM line 1 blink OFF

3. Vertical double-size display register
   DD4 = 0 : Line 4 is displayed in standard form.
   DD3 = 0 : Line 3 is displayed in standard form.
   DD2 = 0 : Line 2 is displayed in standard form.
   DD1 = 0 : Line 1 is displayed in standard form.
4. Display ON/OFF register
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
   D = 0 : Display OFF
   RE = 0 : Extended register OFF
5. Power save register
   O = 0 : Oscillating circuit OFF
   PS = 0 : Power save OFF
6. Power control register
   HPM = 0 : High power mode OFF
   VC = 0 : Voltage regulating circuit OFF
   VF = 0 : Voltage follower OFF
   P = 0 : Boosting circuit OFF
   IRS = 1 : For built-in resistor
   BAS = 0 : 1/5 bias
   IR1,0 = 00 : Rb/Ra = small
7. System set register
   CG = 0 : CGRAM not used
   CS = 0 : Left shift
   SS = 0 : Normal display
   R1, 0 = 0 : Standard ROM + OPTION ROM1
8. Electronic volume
   (0,0,0,0,0)
9. Static icon ON/OFF control
   (SEGSA, B, C, D, E, F, G, H, I, J) =
   (0,0,0,0,0,0,0,0,0,0): Display OFF
10. Static icon blink control
    (SEGSA, B, C, D, E, F, G, H, I, J) =
    (0,0,0,0,0,0,0,0,0,0): Blink OFF

As seen in MPU Interface, the RES pin inputs data at the same timing as MPU resetting and performs initialization concurrently with the MPU. However, if this pin is put into the high impedance for a certain period after the MPU bus and ports are reset, perform a reset input after the input to the SED1240 series is definitively set.

For the reset signal, it is necessary to input '0' level pulses at least for 10 µs as described in DC Characteristics. The ordinary operation will be started in 1 µs or more after the rising edge of the RES signal. When the RES pin becomes active, each register will be cleared and set to the above setup status.

If initialization is not executed by the RES pin when the supply voltage is applied, a clear disable status may appear.

In case the built-in liquid crystal power circuit is not used, the $\overline{RES}$ input must be active when the external liquid crystal power supply is turned on.

DESCRIPTION OF COMMANDS

Table 7 shows a command table. The SED1240 series identifies each data/command by a combination of A0 and $\overline{WR}$ (E).

An extended command can be selected by the RE bit in the command.

Interpreting and executing commands are performed only at the internal timing. This permits high-speed processing.

Overview of Commands

Table 7

Command type	Command name	RE	A0	$\overline{WR}$
Display control instructions	Cursor Home	0	0	0
	Display ON/OFF Control	0/1	0	0
	Line Blink Control	0	0	0
	Line Scroll Control	1	0	0
	Static Icon Display Control	0	1	0
	Static Icon Display Blink Control	0	1	0
	Vertical Double-size Display Control	1	0	0
Power control	Power Save	0/1	0	0
	Power Control (1)	0	0	0
	Power Control (2)	1	0	0
	Electronic Volume Control	0	1	0
System set	System Set (1)	0	0	0
	System Set (2)	1	0	0
Address control instructions	DDRAM, Symbol Register	0	0	0
	CGRAM	1	0	0
Data input instruction	Data Write	0/1	1	0

The execution time of each instruction is determined by the internal processing time of the SED1240 series. Accordingly, for executing an instruction, secure a time exceeding the cycle time (tcyc) and then execute the instruction.

Table 8 SED1240 Series Command Table

<table>
<tr><th rowspan="2">Command</th><th colspan="11">Code</th><th rowspan="2">Function</th></tr>
<tr><th>RE</th><th>A0</th><th>WR</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">(1) Cursor Home/ Line Scroll Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td><td>*</td><td>*</td><td>Moves the cursor to the home position.
(Set the address to 30H.)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>*</td><td>*</td><td>LS1</td><td>LS0</td><td>Specifies the number of display scrolls in units of line.
<table><tr><th>LS1</th><th>LS0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Scroll amount 0 line</td></tr><tr><td>0</td><td>1</td><td>One-line upward scroll</td></tr><tr><td>1</td><td>0</td><td>Two-line upward scroll</td></tr><tr><td>1</td><td>1</td><td>Three-line upward scroll</td></tr></table></td></tr>
<tr><td rowspan="2">(2) Line Blink/ Vertical Double-size Display Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>LB4</td><td>LB3</td><td>LB2</td><td>LB1</td><td>Exerts blink control for each specified line.
LB4 = 1 (Blinks the display for line 4 of DDRAM in black-and-white reverse form.)
LB4 = 0 (Does not blink the display for line 4 of DDRAM.)
LB3 = 1 (Blinks the display for line 3 of DDRAM in black-and-white reverse form.)
LB3 = 0 (Does not blink the display for line 3 of DDRAM.)
LB2 = 1 (Blinks the display for line 2 of DDRAM in black-and-white-reverse form.)
LB2 = 0 (Does not blink the display for line 2 of DDRAM.)
LB1 = 1 (Blinks the display for line 1 of DDRAM in black-and-white reverse form.)
LB1 = 0 (Does not blink the display for line 1 of DDRAM.)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DD4</td><td>DD3</td><td>DD2</td><td>DD1</td><td>Displays the specified DDRAM line in vertical double-size form.
DD4 = 1 (Displays the data for line 4 of DDRAM in vertical double-size form.)
DD4 = 0 (Displays the data for line 4 of DDRAM in standard form.)
DD3 = 1 (Displays the data for line 3 of DDRAM in vertical double-size form.)
DD3 = 0 (Displays the data for line 3 of DDRAM in standard form.)
DD2 = 1 (Displays the data for line 2 of DDRAM in vertical double-size form.)
DD2 = 0 (Displays the data for line 2 of DDRAM in standard form.)
DD1 = 1 (Displays the data for line 1 of DDRAM in vertical double-size form.)
DD1 = 0 (Displays the data for line 1 of DDRAM in standard form.)</td></tr>
</table>

<table>
<tr><th rowspan="2">Command</th><th colspan="11">Code</th><th rowspan="2">Function</th></tr>
<tr><th>RE</th><th>A0</th><th>WR</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>(3) Display ON/OFF/ Extended Register ON/OFF Control</td><td>0/1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C</td><td>B</td><td>RE</td><td>D</td><td>Sets cursor ON/OFF, cursor blink ON/OFF (B), display ON/OFF (D), use/no-use of extended register (RE), and electronic volume LBS (RE).
C= 1 (cursor ON) C = 0 (cursor OFF)
B = 1 (blink ON) B = 0 (blink OFF)
D = 1 (display ON) D = 0 (display OFF)
RE = 1 (extended register ON) RE = 0 (extended register OFF)</td></tr>
<tr><td>(4) Power Save Control</td><td>0/1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>*</td><td>*</td><td>0</td><td>PS</td><td>Sets power save ON/OFF (PS) and oscillating circuit ON/OFF (O).
PS = 1 (power save ON) PS = 0 (power save OFF)
O = 1 (oscillation ON) O = 0 (oscillation OFF)</td></tr>
<tr><td rowspan="2">(5) Power Control</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>HPM</td><td>VC</td><td>VF</td><td>P</td><td>Sets high power mode ON/OFF (HPM), voltage regulating circuit ON/OFF (VC), voltage follower ON/OFF (VF), and boosting circuit ON/OFF (P).
HPM = 1 (high power mode ON) HPM = 0 (high power mode OFF)
VC = 1 (voltage regulating circuit ON) VC = 0 (voltage regulating circuit OFF)
VF = 1 (voltage follower ON) VF = 0 (voltage follower OFF)
P = 1 (boosting circuit ON) P = 0 (boosting circuit OFF)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>IRS</td><td>BAS</td><td>IR1</td><td>IR0</td><td>Sets V_5 voltage regulating resistor selection (IRS), LCD bias set (BAS), and V_5 voltage regulating built-in resistor ratio set (IR1, IR0).
IRS = 1 (use of built-in resistor) IRS = 0 (no use of built-in resistor)
BAS = 1 (1/4 bias) BAS = 0 (1/5 bias)
(IR1, IR0) = (11, 10, 01, 00) ... (Rb/Ra ratio large to small)</td></tr>
<tr><td rowspan="2">(6) System Set</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>R1</td><td>R0</td><td>CS</td><td>CG</td><td>Sets ROM option (R1, R0), use/no use of CGRAM (CG), and COM shift direction (CS)
CG = 1 (use of CGRAM) CG = 0 (no use of CGRAM)
CS = 1 (right shift) CS = 0 (left shift)
<table><tr><th>R1</th><th>R0</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Standard ROM + OPTION ROM1</td></tr><tr><td>0</td><td>1</td><td>Standard ROM + OPTION ROM2</td></tr><tr><td>1</td><td>0</td><td>Standard ROM + OPTION ROM3</td></tr><tr><td>1</td><td>1</td><td>Standard ROM + OPTION ROM4</td></tr></table></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>*</td><td>*</td><td>SS</td><td>*</td><td>Sets the normal/reverse display (SS) of each segment character.
SS = 1 (reverse) SS = 0 (normal)</td></tr>
<tr><td rowspan="2">(7) RAM Address Set</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="7">ADDRESS</td><td>Sets the address of DDRAM, static icon RAM or electronic volume RAM.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td colspan="7">ADDRESS</td><td>Sets the address of CGRAM or symbol register RAM.</td></tr>
</table>

Command	Code											Function
	RE	A0	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(8) RAM Data Write	0/1	1	0	DATA								Writes data into the DDRAM, CGRAM, symbol register RAM, static icon RAM or electronic volume RAM. This is determined by the address set instruction executed immediately before writing data.
(9) NOP	0/1	0	0	0	0	0	0	0	0	0	0	A command for NON-OPERATION. This also serves as a test mode clear command, so it is recommended to input it periodically.
(10) Test Mode	0/1	0	0	0	0	0	0	*	*	*	*	A command for IC chip test. Don't use this command.

Description of Command Functions

Cursor home

Function: Presets the address counter to 30H. Only when the previous RAM access is made to the area of RE = 0 of the RAM map, the cursor is moved to digit 1 on line 1 if the cursor is displayed.
If line scroll is set, it is cleared to the scroll amount = 0 line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	*	*	*	*

* : Don't Care

Line scroll control

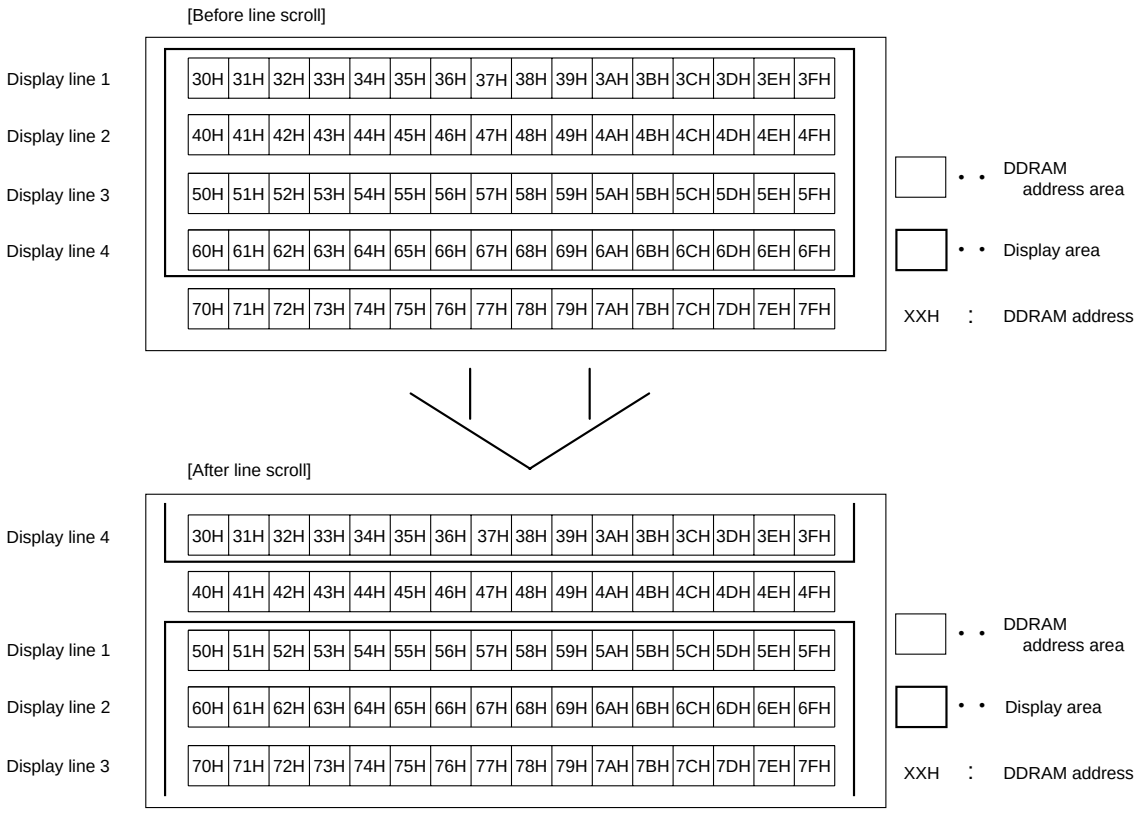
Function: Controls the display scroll amount for each line.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	*	*	LS1	LS0

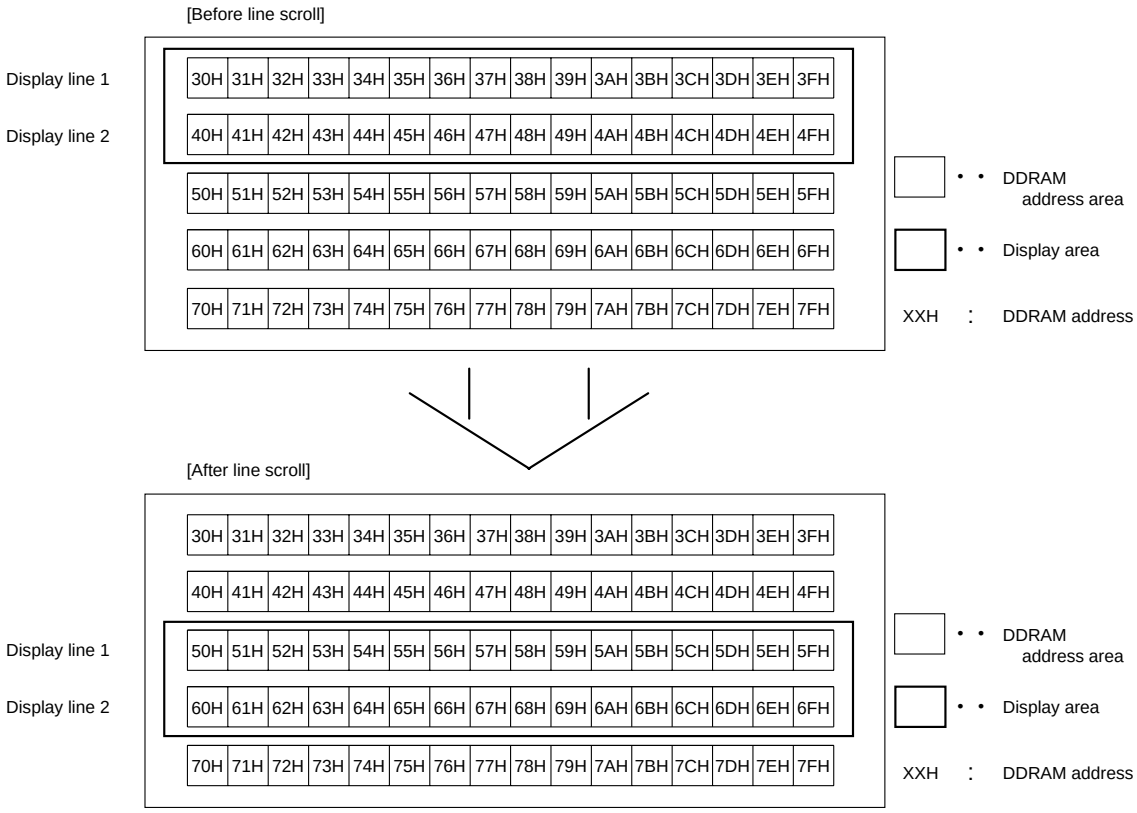
* : Don't Care

LS1	LS0	Function
0	0	Scroll amount 0 line
0	1	Scrolls 1 line upward. (display line 1 from DDRAM line 2)
1	0	Scrolls 2 lines upward. (display line 1 from DDRAM line 3)
1	1	Scrolls 3 lines upward. (display line 1 from DDRAM line 4)

• When 2-line scroll has been performed upward at the 4-line display



• When 2-line scroll has been performed upward at the 2-line display [(LS1, LS2) = (1, 0)]



Line blink display control

Function: Displays the specified line in back-and-while reverse form.
The specified line corresponds to the address line of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	LB4	LB3	LB2	LB1

- Displays the specified line of the DDRAM in black-and-white form by setting LB4 to LB1.
  - LB4 = 0 : Displays the data for line 4 of the DDRAM in standard form. (no blink) [DDRAM 60H to 6FH]
  - LB4 = 1 : Displays the data for line 4 of DDRAM in black-and-white reverse blink form. [DDRAM 60H to 6FH]
  - LB3 = 0 : Displays the data for line 3 of the DDRAM in standard form. (no blink) [DDRAM 50H to 5FH]
  - LB3 = 1 : Displays the data for line 3 of the DDRAM in black-and-white reverse blink form. [DDRAM 50H to 5FH]
  - LB2 = 0 : Displays the data for line 2 of the DDRAM in standard form. (no blink) [DDRAM 40H to 4FH]
  - LB2 = 1 : Displays the data for line 2 of the DDRAM in black-and-white reverse blink form. [DDRAM 40H to 4FH]
  - LB1 = 0 : Displays the data for line 1 of the DDRAM in standard form. (no blink) [DDRAM 30H to 3FH]
  - LB1 = 1 : Displays the data for line 1 of the DDRAM in black-and-white reverse blink form. [DDRAM 30H to 3FH]
- f_{BLINK} = 1 to 2Hz.
- Blinking is performed at the same frequency as cursor blink.
  If blinking is caused to occur at the same time, the cursor position will be hard to know.

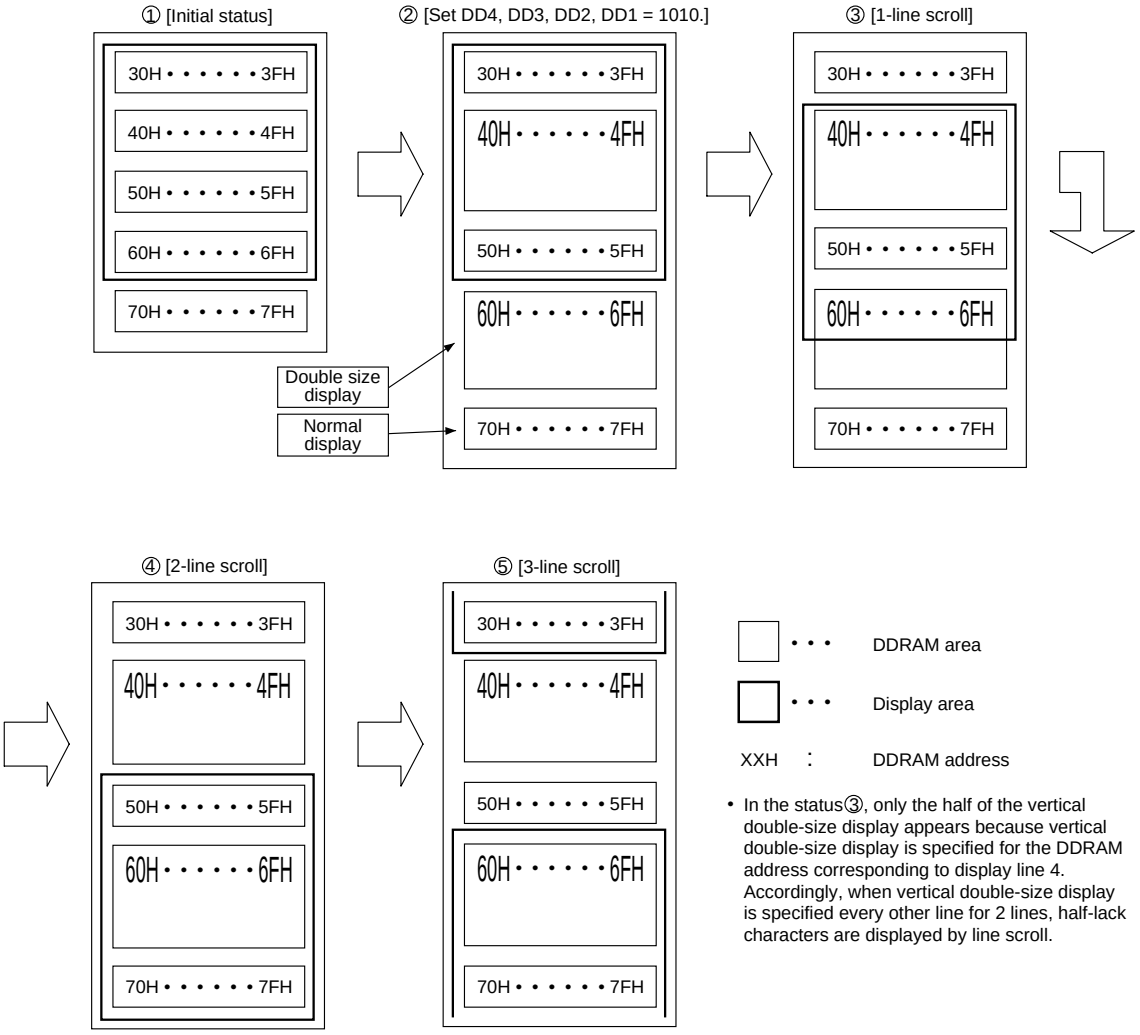
Vertical double-size display control

Function: Displays the specified line in vertical double-size form.
The specified line corresponds to the address of the DDRAM.
(Not the display line)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	DD4	DD3	DD2	DD1

- Displays the specified line of the DDRAM in vertical double-size form by setting DD4 to DD1.
  - DD4 = 0 : Displays the data for line 4 of the DDRAM in standard form. [DDRAM 60H to 6FH]
  - DD4 = 1 : Displays the data for line 4 of the DDRAM in vertical double-size form. [DDRAM 60H to 6FH]
  - DD3 = 0 : Displays the data for line 3 of the DDRAM in standard form. [DDRAM 50H to 5FH]
  - DD3 = 1 : Displays the data for line 3 of the DDRAM in vertical double-size form. [DDRAM 50H to 5FH]
  - DD2 = 0 : Displays the data for line 2 of the DDRAM in standard form. [DDRAM 40H to 4FH]
  - DD2 = 1 : Displays the data for line 2 of the DDRAM in vertical double-size form. [DDRAM 40H to 3FH]
  - DD1 = 0 : Displays the data for line 1 of the DDRAM in standard form. [DDRAM 30H to 3FH]
  - DD1 = 1 : Displays the data for line 1 of the DDRAM in vertical double-size form. [DDRAM 30H to 3FH]

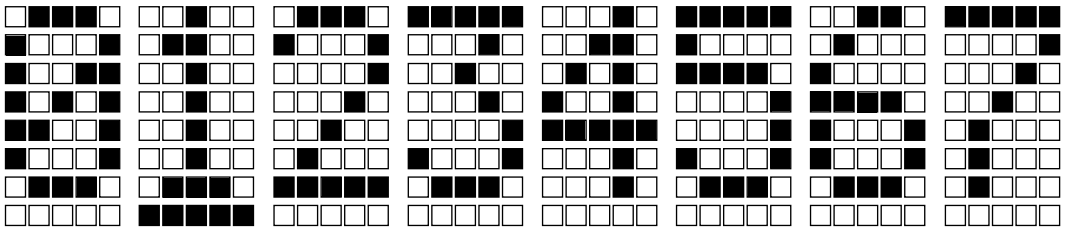
- Example of vertical double-size display
  An example of 4-line display will be cited for explanation.

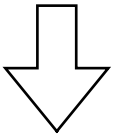


- In the status③, only the half of the vertical double-size display appears because vertical double-size display is specified for the DDRAM address corresponding to display line 4. Accordingly, when vertical double-size display is specified every other line for 2 lines, half-lack characters are displayed by line scroll.

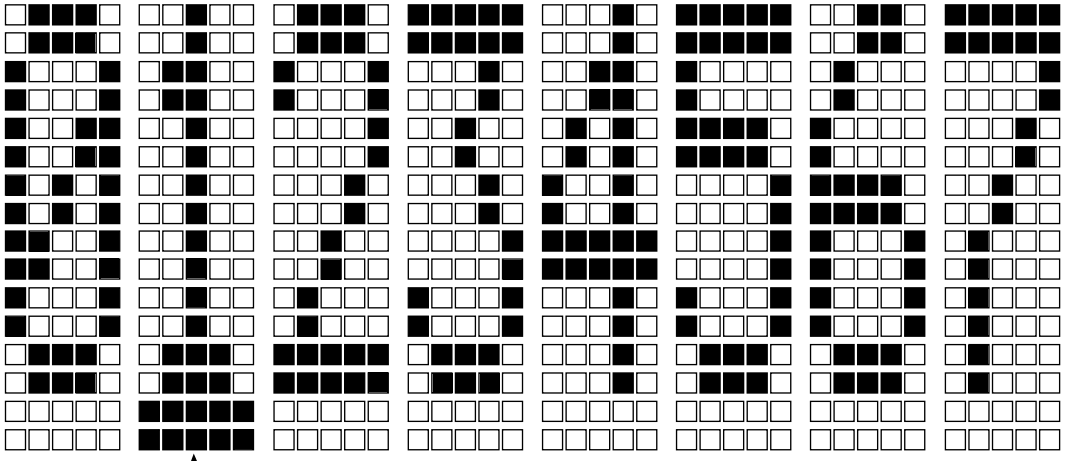
- Example of vertical double-size display (characters)

[Standard display]





[Vertical double-size display]



Display ON/OFF control

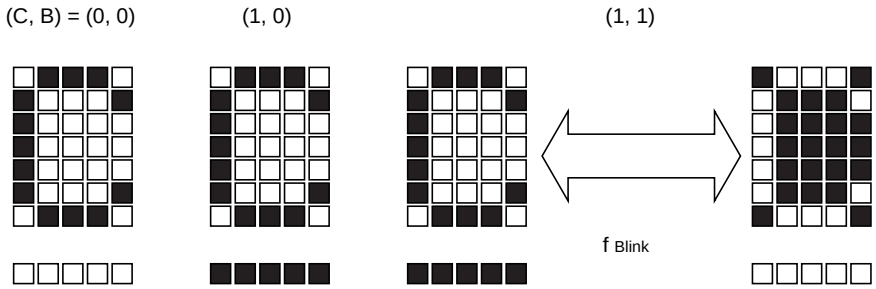
Function: Sets both display and cursor ON/OFF, and extended register access.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	1	1	C	B	RE	D

- Display ON/OFF is specified by setting D.
  D = 0 : Display ON
  D = 1 : Display ON
- Character blink ON/OFF at the cursor position is specified by setting B. However, when the cursor is OFF, this bit is invalidated.
  B = 0 : Cursor blink OFF
  B = 1 : Cursor blink ON
- Cursor ON/OFF is specified by setting C.
  C = 0 : No display of cursor
  C = 1 : Display of cursor
- Extended register access is specified by setting RE.
  RE = 0 : Extended register OFF
  RE = 1 : Extended register ON
- The relation between C/B register and cursor display is shown in the following table.

C	B	Cursor display
0	0	No display (fixed)
0	1	No display (fixed)
1	0	Display of under-bar cursor
1	1	Alternate display of display characters and black-and-white reversed display characters

- Example of cursor display



The cursor display position is indicated by the address counter. Accordingly, when moving the cursor, change the address counter value by the RAM address set command or the auto increment by the RAM data write command.
To display the under-bar cursor when character data (CGRAM) at the cursor position, the position corresponding to the cursor position will be displayed in black-and-white reverse form.
If the address counter is set to the symbol register position at (C, B) = (1, 1), symbols can be caused to blink selectively (every 5 dots because symbols correspond to characters).

Power save

Function: Controls the oscillating circuit and sets and resets the power save mode and the sleep mode.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	1	0	0	*	*	O	PS

* : Don't Care

- Power save mode ON/OFF is specified by setting PS.
  PS = 0 : Power save OFF (reset)
  PS = 1 : Power save ON (set)
- Oscillating circuit ON/OFF is specified by setting O.
  O = 0 : Oscillating circuit OFF (stop of oscillation)
  O = 1 : Oscillating circuit ON (start of oscillation)

Power control (1)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	HPM	VC	VF	P

∗ : Don't Care

- Boosting circuit ON/OFF is specified by setting P. For operating the boosting circuit, the oscillating circuit must be in operation.
  P = 0 : Boosting circuit OFF
  P = 1 : Boosting circuit ON
- Voltage follower ON/OFF is specified by setting VF.
  VF = 0 : Voltage follower OFF
  VF = 1 : Voltage follower ON
- Voltage regulating circuit ON/OFF is specified by setting VC.
  VC = 0 : Voltage regulating circuit OFF
  VC = 1 : Voltage regulating circuit ON.
- High power mode ON/OFF is specified by setting HPM.
  HPM = 0 : High power mode OFF
  HPM = 1 : High power mode ON

Power control (2)

Function: Controls the operation of the built-in power circuit.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	IRS	BAS	IR1	IR0

∗ : Don't Care

- The relation of IR0 and option combinations is shown in the following table.

IR1	IR0	(1 + Rb/Ra)
0	0	Small
0	1	↓
1	0	
1	1	Large

- Bias selection is performed by setting BAS.
  BAS = 0 : 1/5 bias
  BAS = 1 : 1/4 bias
- Either built-in V5 voltage regulating resistor or external resistor (no use of built-in resistor) is selected by setting IRS.
  IRS = 0 : No use of built-in resistor
  IRS = 1 : Use of built-in resistor

System set (1)

Function: Selects an option ROM and sets the common shift direction and the use/no use of CGRAM.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	R1	R0	CS	CG

- The relation of R1 and R0 combinations is shown in the following figure.

R1	R0	ROM combination
0	0	Standard ROM (160 characters or 154 characters) + option ROM1 (96 characters)
0	1	Standard ROM (160 characters or 154 characters) + option ROM2 (96 characters)
1	0	Standard ROM (160 characters or 154 characters) + option ROM3 (96 characters)
1	1	Standard ROM (160 characters or 154 characters) + option ROM4 (96 characters)

- The COM shift direction is specified by setting CS.
  CS = 0 : COM left shift (COM1 → COM32 → COMS1 → COMS2)
  CS = 1 : COM right shift (COM32 → COM1 → COMS1 → COMS2)
- The use/no use of CGRAM is specified by setting CG.
  CG = 0 : No use of CGRAM
  CG = 1 : Use of CGRAM

System set (1)

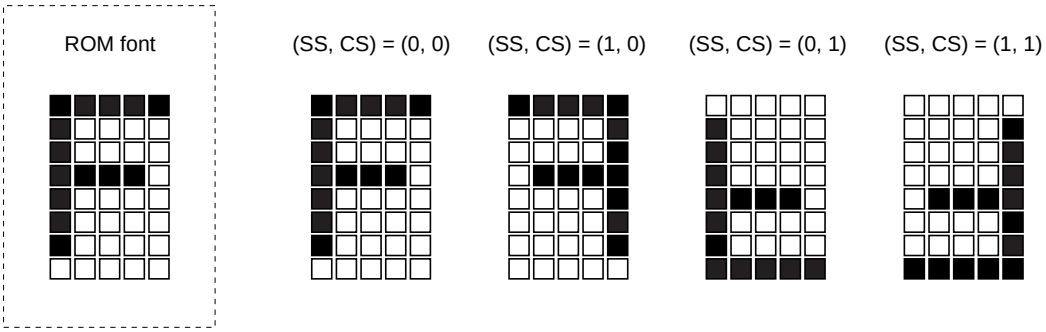
Function: sets the normal/reverse display of SEG characters.
This function operates for each character.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	*	*	SS	*

∗ : Don't Care

- The normal/reverse display of SEG is specified by setting SS.
  SS = 0 : Normal display of SEG
  SS = 1 : Reverse display of SEG
- For the symbol register RAM output, only the normal display is available.

• Example of display (compared by the same mounting method)



RAM address set (1) [DDRAM, static icon RAM, electronic volume RAM]

Function: Sets the address for writing data into the DDRAM, static icon RAM (including blink control), and electronic volume RAM in the address counter. When the cursor appears, it is displayed at the display position corresponding to the DDRAM address set by this command. (When the static icon RAM or electronic volume RAM is specified, the cursor disappears on the display.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ADDRESS						

① The settable address is the address 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, when data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 0, 09H is for testing. Be sure not to use it!

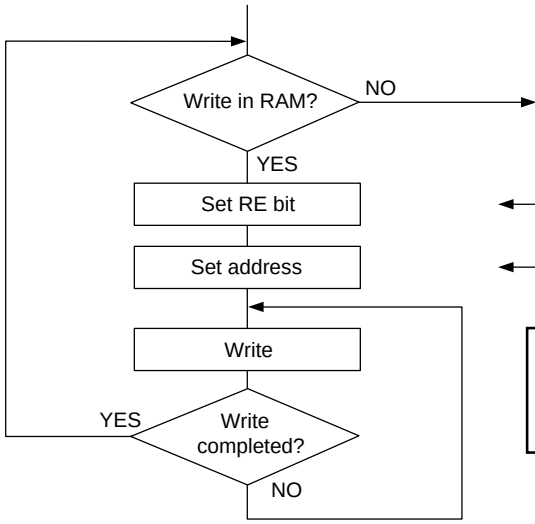
RAM address set (2) [CGRAM, symbol register RAM]

Function: Sets the address for writing data into the CGRAM or symbol register RAM in the address counter.
When the CGRAM address is set, the cursor will disappear on the display. When the symbol register RAM is set, the cursor moves to the corresponding symbol position, causing this symbol to blink selectively.
When the cursor home command is executed immediately after execution of this instruction (before execution of RAM Address Set (1)), the cursor will not be displayed. (Because the address is set at address 30H of RE-1 of the RAM map.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	ADDRESS						

① The settable address of the address of 00H to 7FH in D6 to D0.
② When writing data in the RAM, set the address for writing data by this command. Next, if data is written in succession, the address will be automatically incremented. (00H to 7FH → 00H)
③ RE = 1, 30H - 5FH i8s set to No Use. It is not available.

<Example of Address Set>



Note: When making access to the RAM after a change of the RE bit, be sure to set the address. If not, the contents of the RAM will be abnormal on the display.

[SED1240 RAM map] (4-line 16-digit display)

RE	High \ Low order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST		Unused				
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI :Static icon RAM
SIB :Static icon blink control RAM
EV :Electronic volume RAM
TEST :Testing register. Don't use it.

[SED1240 Series RAM map] (2-line 16-digit display)

RE	Low order / High order	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0XH	SI		SIB		Unused				EV	TEST	Unused					
	1XH	Unused															
	2XH	Unused															
	3XH	DDRAM line 1															
	4XH	DDRAM line 2															
	5XH	DDRAM line 3															
	6XH	DDRAM line 4															
	7XH	DDRAM line 5															
1	0XH	CGROM(00H)								CGROM(01H)							
	1XH	CGROM(02H)								CGROM(03H)							
	2XH	CGROM(04H)								CGROM(05H)							
	3XH	Unused															
	4XH	Unused															
	5XH	Unused															
	6XH	Symbol register															
	7XH	Symbol register															

Symbol register:
COMS1, 2

For static icon:
COMSA, SEGSA - J

SI :Static icon RAM
SIB :Static icon blink control RAM
EV :Electronic volume RAM
TEST :Testing register. Don't use it.

[Display range of each master]

The following shows the display range for the DDRAM area when the vertical double size is unspecified and scroll amount is 0 line:

SED1240 (4 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
	4th line on display	RE = 0	60H to 6FH
SED1241 (3 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH
	3rd line on display	RE = 0	50H to 5FH
SED1242 (2 lines by 16 columns)	1st line on display	RE = 0	30H to 3FH
	2nd line on display	RE = 0	40H to 4FH

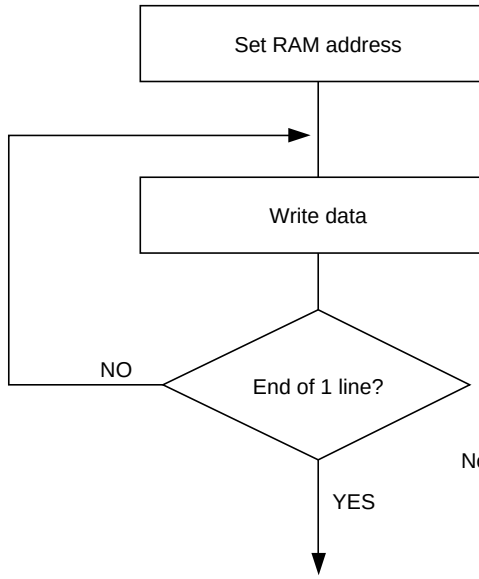
RAM data write

Function: Writes data in the RAM areas of the DDRAM, CGRAM, symbol register RAM, static icon RAM, and electronic volume RAM.
Before this command, be sure to execute the address set command.
After that, each time data is written, the address will be automatically incremented. (Regarding the RE bit, the contents set by the command will be kept in memory.)

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	0	DATA							

① Data is written into the DDRAM, CGRAM, symbol register RAM, static icon RAM, or electronic volume RAM.
② The address counter is automatically incremented by 1, so data can be written in succession. However, the address counter advances from 00H to 7FH to 00H. Accordingly, when writing data into the CGRAM, take care not to write it at the addresses subsequent to 30H.

<Data write example>
An example of writing one line of data into the DDRAM continuously is shown below.



Note: Before executing instructions in succession, secure a time exceeding t_{CYC} and then execute them.

NOP

Function: A no-operation command. No operation is performed functionally. However, because a test mode reset function exists inside, the test mode can be reset if the IC is put into this mode by an effect of noise.
It is recommended to add this command at each breakpoint of the program.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	0	0	0	0

Test mode

Function: An IC test mode set command. Don't use it in any case.

RE	A0	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0/1	0	0	0	0	0	0	*	*	*	*

CHARACTER GENERATOR

Character Generator ROM (CGROM)

The SED1240 series is provided with a character generator ROM consisting of up to 544 types of characters. Each character size is of a structure of 5×8 dots.
A character code table of the SED1240 series is shown in CGROM Table X to X. In this case, which of CGROM and CGRAM should be used for the 6 characters of 00H to 05H of the character code is specified by the system set command.

The CGROM of the SED1240 series is a mask ROM and is compatible with the user's own CGROM. Please ask our sales department for further information.

The following shows the standard font specified for SED1240 series:

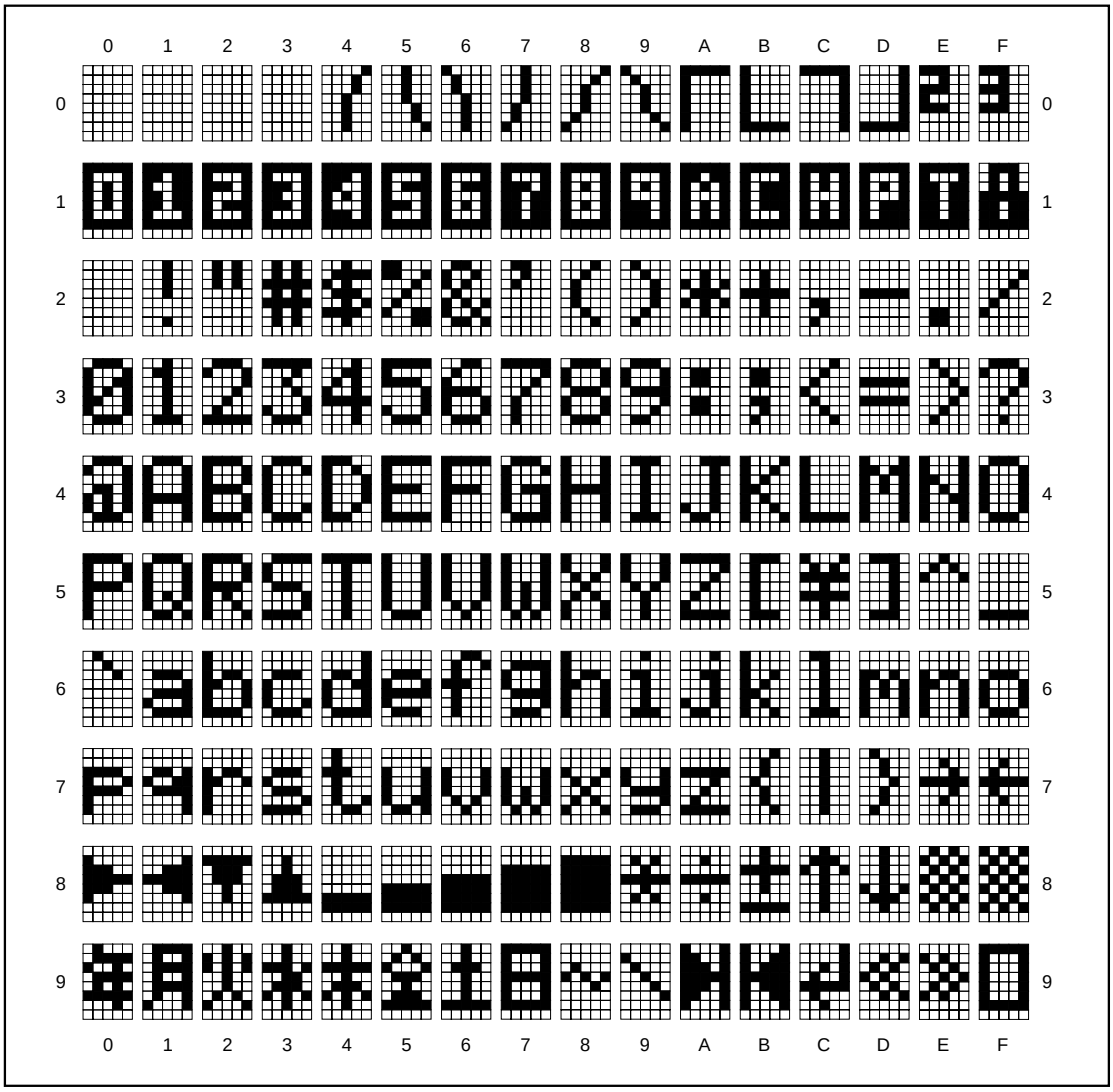
SED1240DAB, SED1240T0A: JISS1 (Font A)
SED1240DBB, SED1240T0B : ASCII (Font B)
SED1240DGB, SED1240T0G: JISS2 (Font G)

SED1241DAB, SED1241T0A: JISS1 (Font A)
SED1241DBB, SED1241T0B : ASCII (Font B)
SED1241DGB, SED1241T0G: JISS2 (Font G)

SED1242DAB, SED1242T0A: JISS1 (Font A)
SED1242DBB, SED1242T0B : ASCII (Font B)
SED1242DGB, SED1242T0G: JISS2 (Font G)

Lower 4 Bit of Code

Higher 4 Bit of Code



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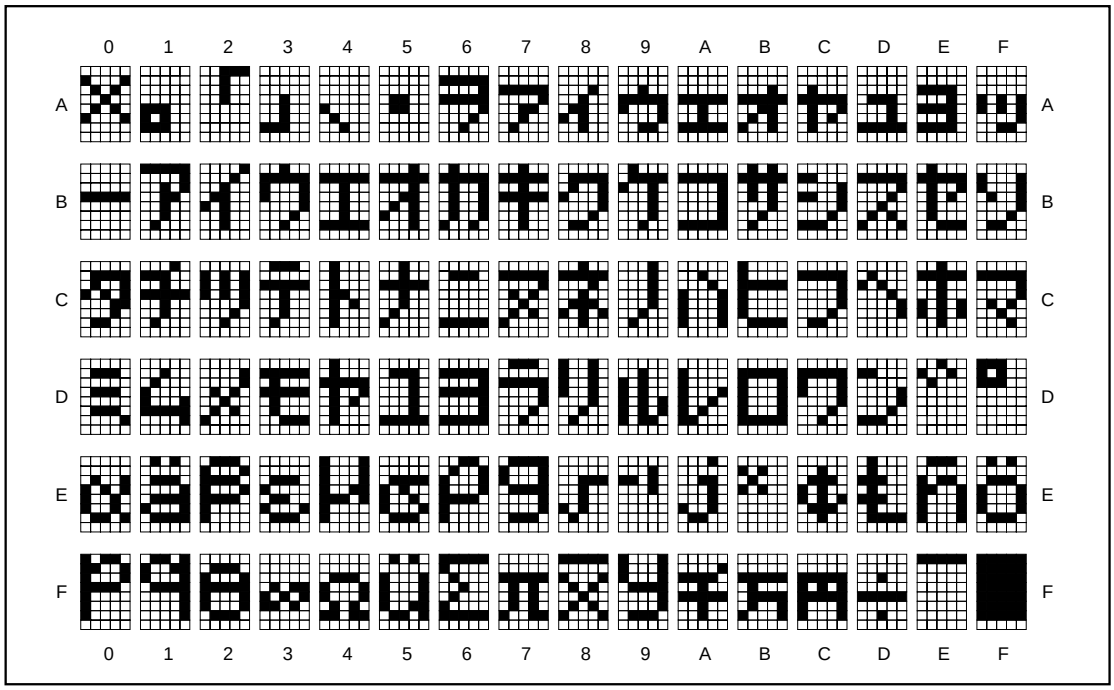

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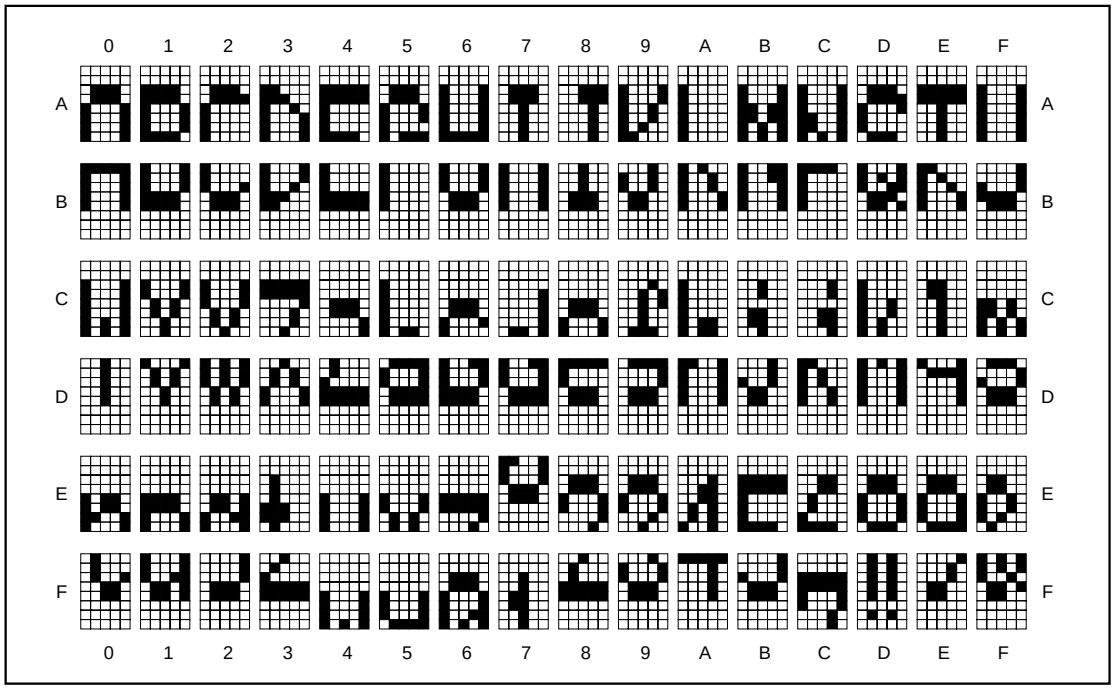

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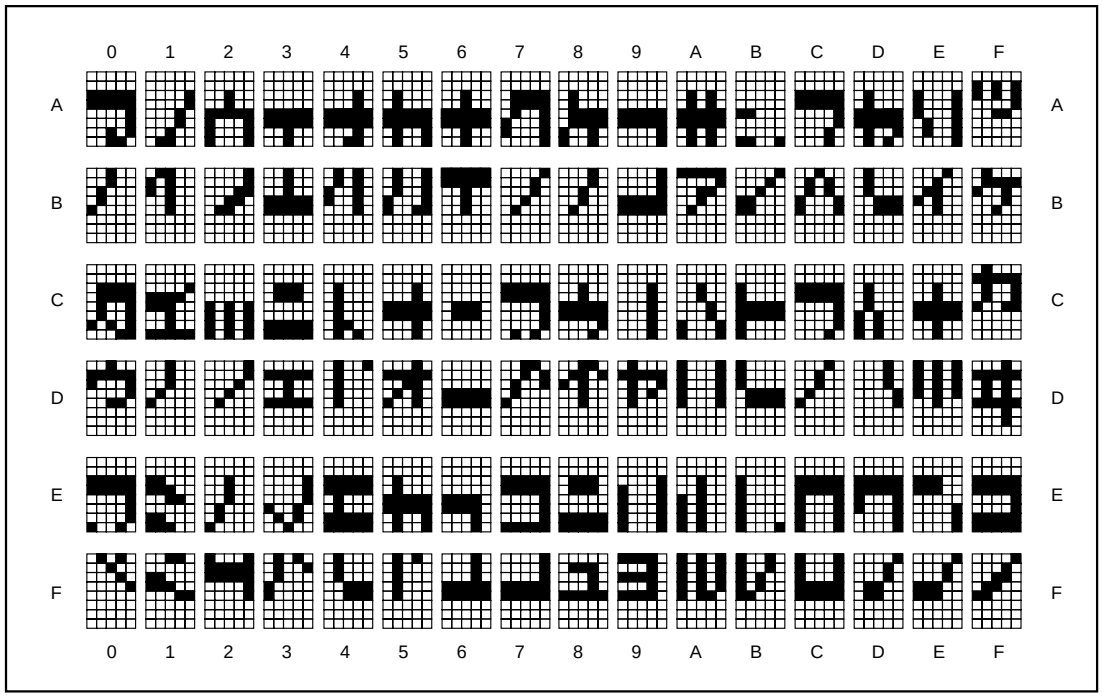

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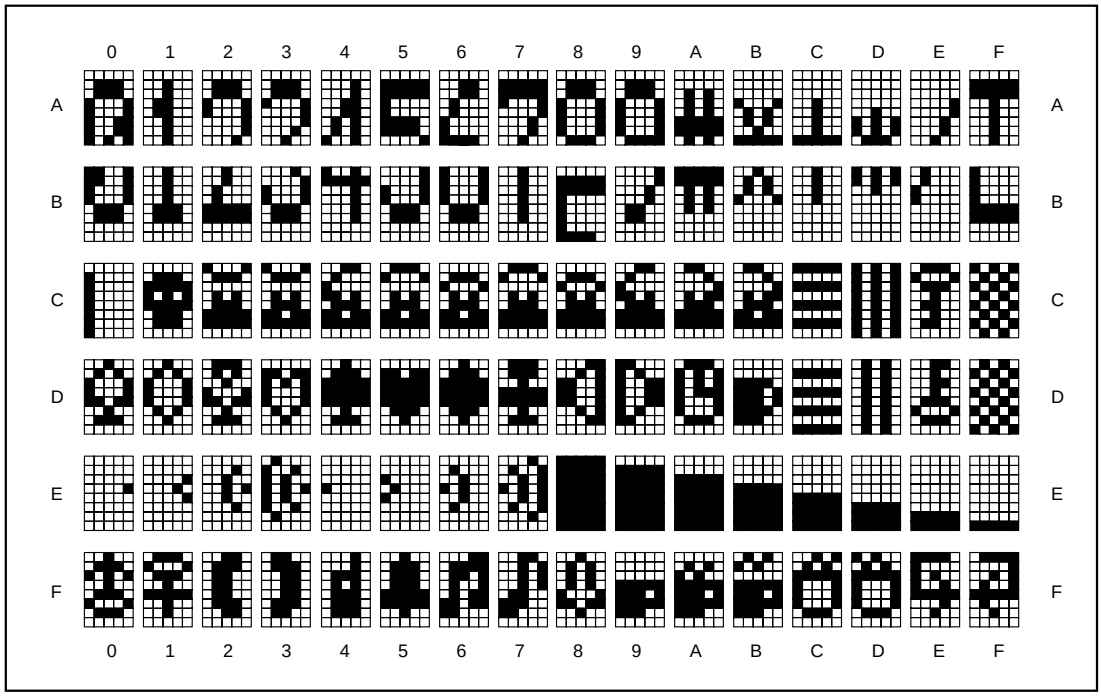

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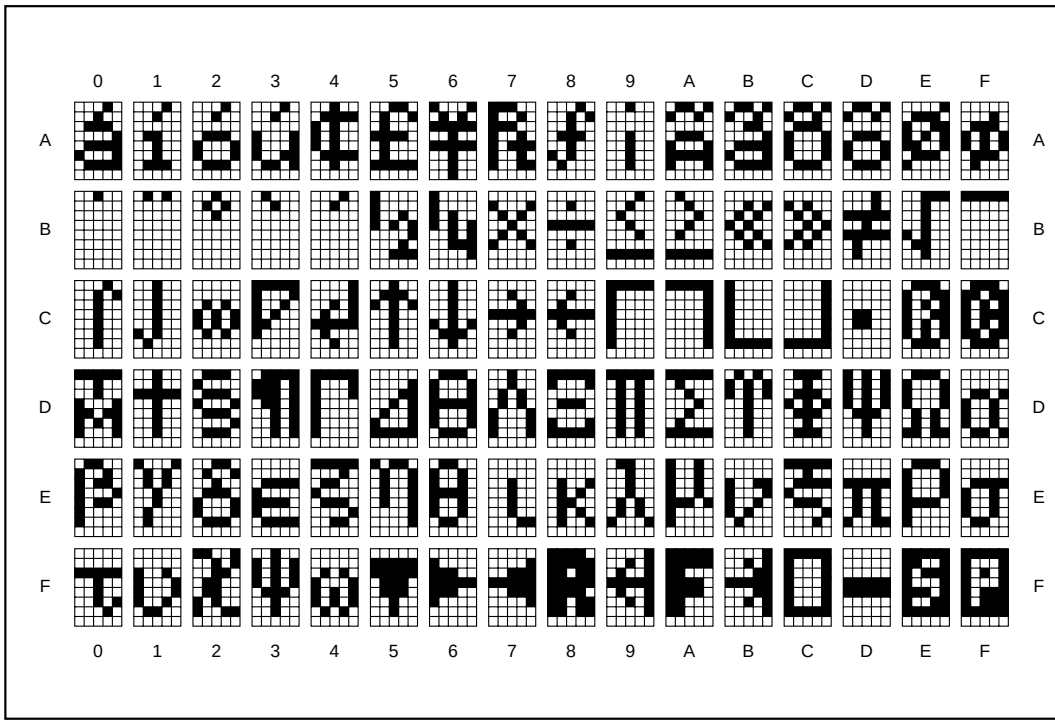

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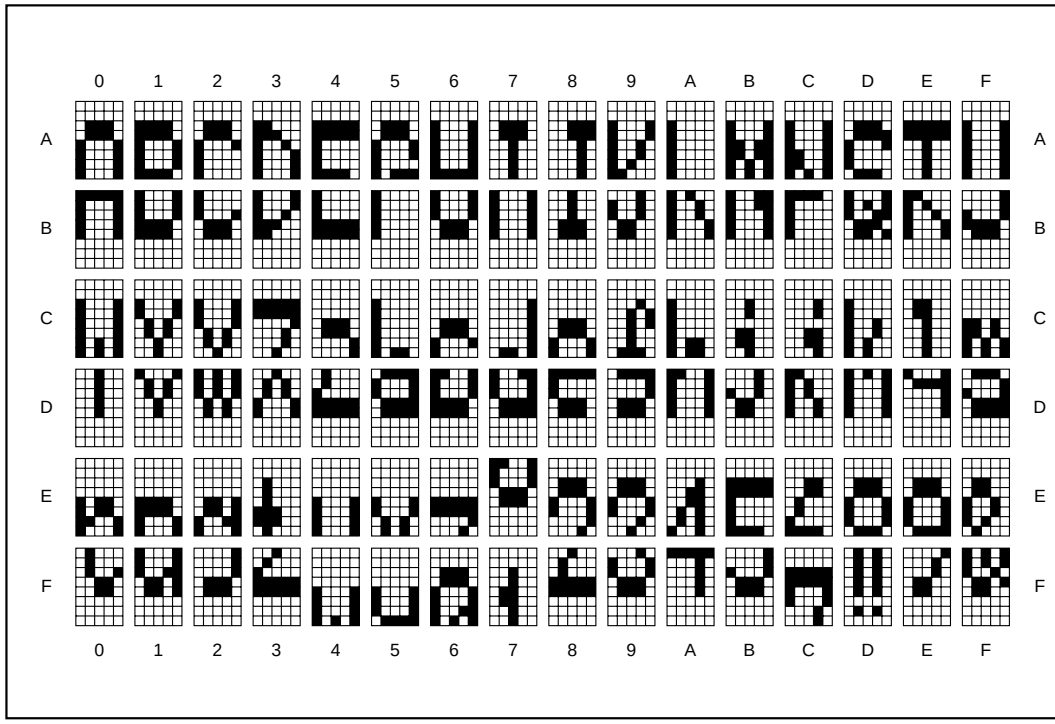

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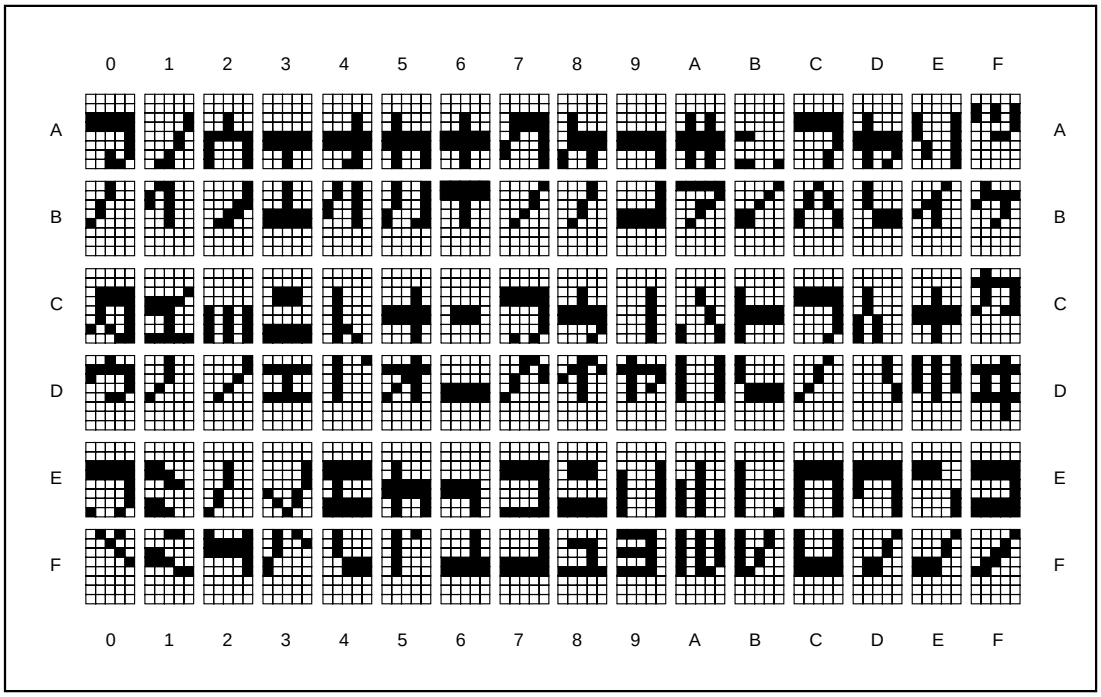

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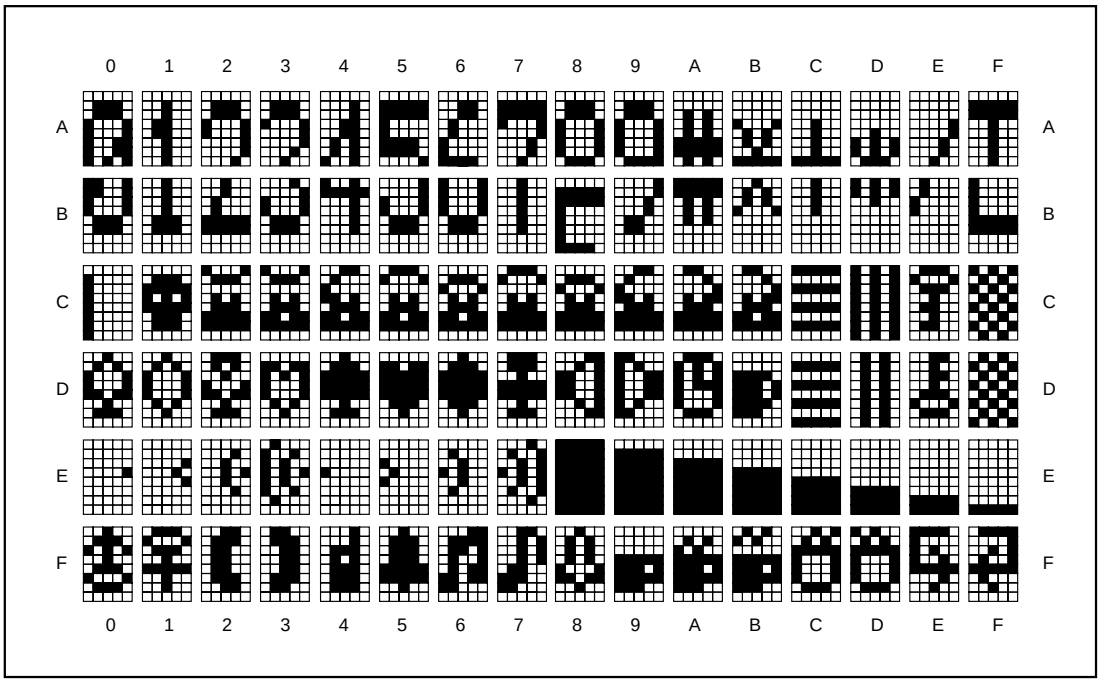

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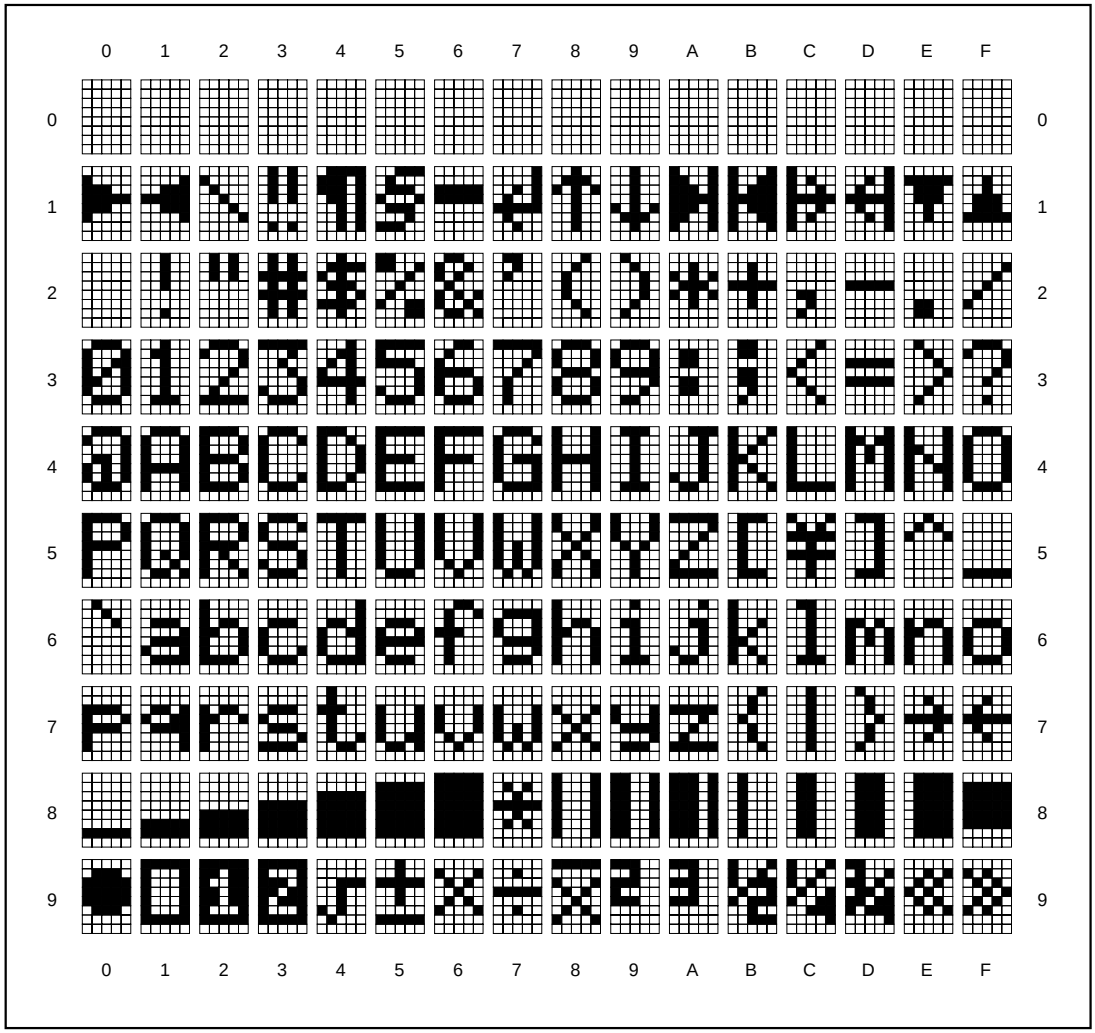

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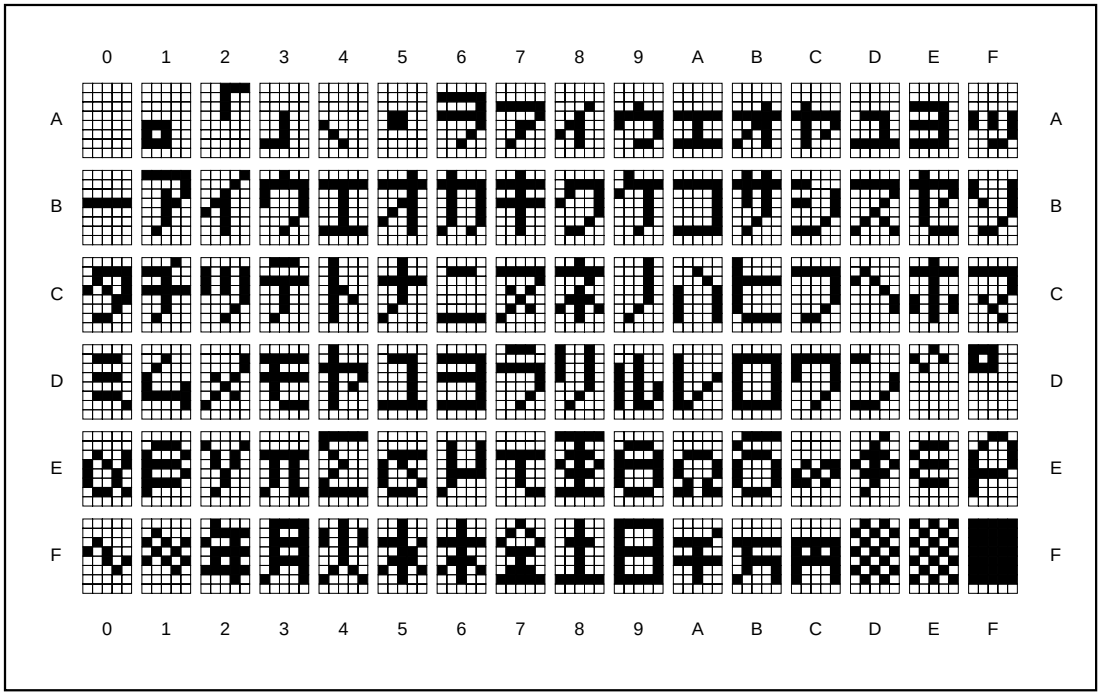

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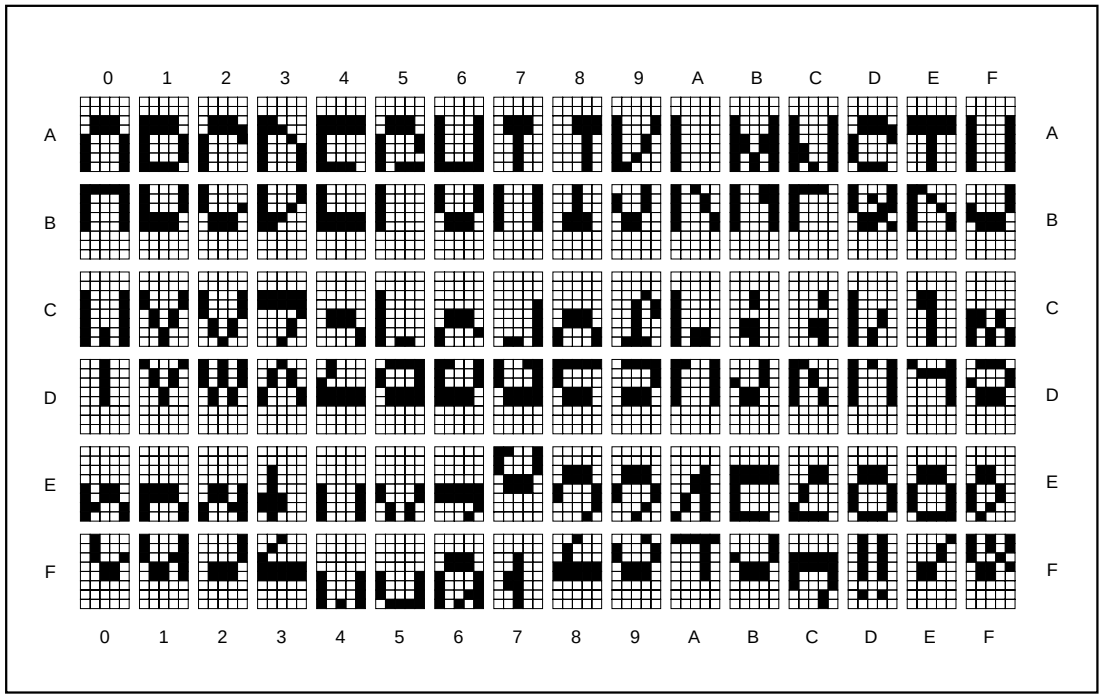

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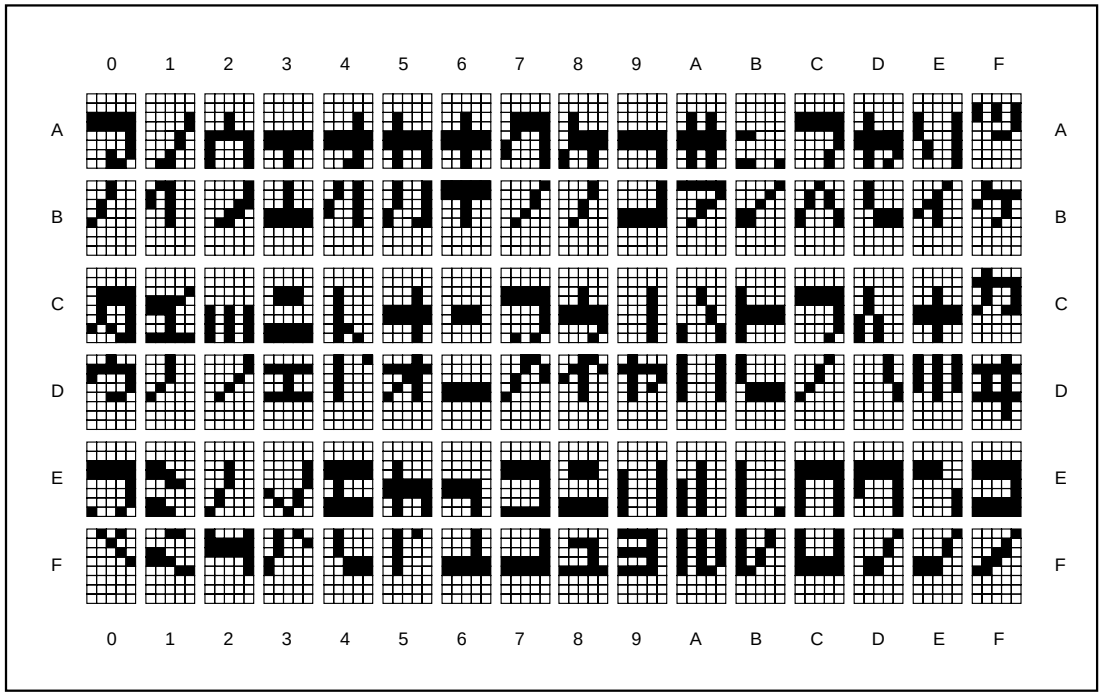

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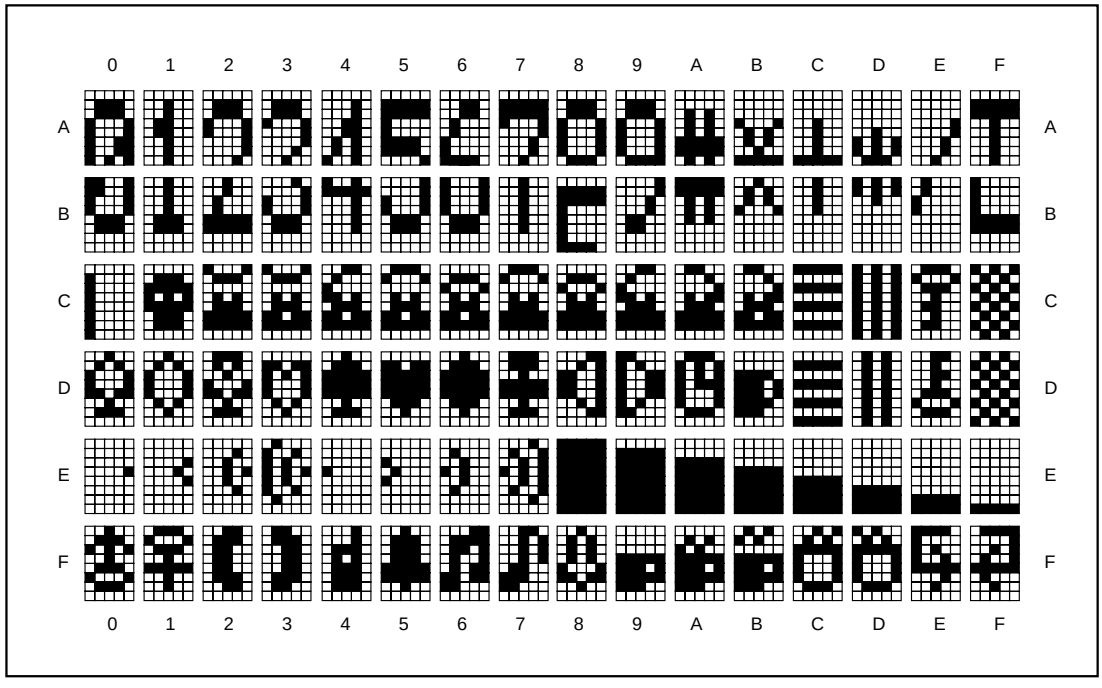
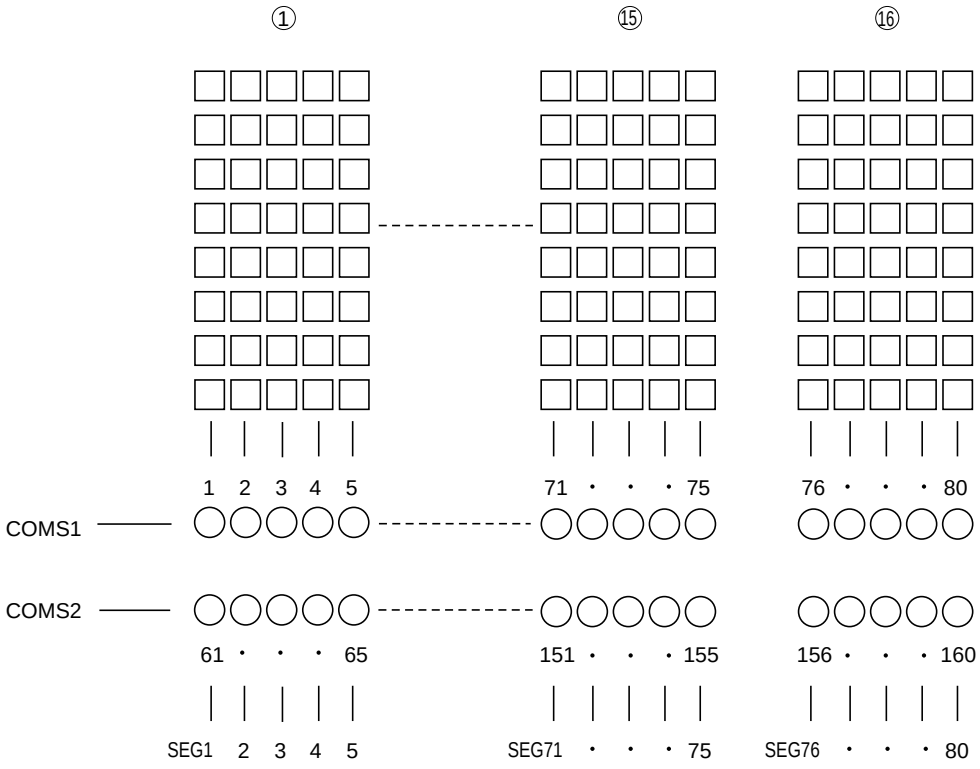


Character code	RAM Address (CGRAM selection: RE = 1)		CGRAM data (character pattern) D7 D0								Character display SEG
00H	(00H to 07H)	0	*	*	*	0	1	1	1	1	
02H	(10H to 17H)	1	*	*	*	1	0	0	0	0	
04H	(20H to 27H)	2	*	*	*	1	0	0	0	0	
		3	*	*	*	0	1	1	1	1	
		4	*	*	*	0	0	0	0	1	
		5	*	*	*	0	0	0	0	1	
		6	*	*	*	1	1	1	1	0	
		7	*	*	*	0	0	0	0	0	
01H	(08H to 0FH)	8	*	*	*	0	0	1	0	0	
03H	(18H to 1FH)	9	*	*	*	0	0	1	0	0	
05H	(28H to 2FH)	A	*	*	*	0	1	1	1	0	
		B	*	*	*	0	1	1	1	0	
		C	*	*	*	0	1	1	1	0	
		D	*	*	*	1	1	1	1	1	
		E	*	*	*	1	1	1	1	1	
		F	*	*	*	0	0	0	0	0	

Unused — Character data

1: Display
0: No display



RAM address [RE = 1]		Bits for symbol							
		D7							D0
60H to 6FH	0	BONF	IORH	*	1	2	3	4	5
	1	BONF	IORH	*	6	7	8	9	10
	:				:				
	F	BONF	IORH	*	76	77	78	79	80
70H to 7FH	0	BONF	IORH	*	81	82	83	84	85
	1	BONF	IORH	*	86	87	88	89	90
	:				:				
	F	BONF	IORH	*	156	157	158	159	160

D7 (BONF)	D6 (IORH)	Function
0	*	No blink
1	0	D4 to D0 blink in black-and-white reverse form.
1	1	The bits of “1” out of D4 to D0 blink.

f_{BLINK} : 1 to 2Hz

Static Icon RAM

The SED1240 series can display static icons in the standby mode.
Each of 10 icons can be set in respect of ON/OFF and blink by using the pins of COMSA to SEGSA to J. The relation between static icon functions and static icon RAM write data is shown below.

RAM address [RE = 0]	SI data								Display
	D7	D6	D5	D4	D3	D2	D1	D0	[□ · · · OFF ■ · · · ON]
00H									SEGSA B C D E
	✳	✳	✳	0	0	0	0	0	□ □ □ □ □
	✳	✳	✳	0	0	0	0	1	□ □ □ □ ■
	✳	✳	✳	0	0	0	1	0	□ □ □ ■ □
	✳	✳	✳	1	1	1	1	1	■ ■ ■ ■ ■
01H									SEGSF G H I J
	✳	✳	✳	0	0	0	0	0	□ □ □ □ □
	✳	✳	✳	0	0	0	0	1	□ □ □ □ ■
	✳	✳	✳	0	0	0	1	0	□ □ □ ■ □
	✳	✳	✳	1	1	1	1	1	■ ■ ■ ■ ■

For static icons, blink ON/OFF control can be exerted independently for each pin.

RAM address [RE = 0]	ISB data VS pin								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
02H	✳	✳	✳	SEGSA	SEGSB	SEGSC	SEGSD	SEGSE	Blink 1 = ON 0 = OFF
03H	✳	✳	✳	SEGSF	SEGSG	SEGSH	SEGSI	SEGSJ	

The following table shows a static icon ON/OFF function and static icon blink control.

RAM address [RE = 0]	SI data								Display
	D7	D6	D5	D4	D3	D2	D1	D0	[□ · · · OFF ■ · · · ON]
00H	✳	✳	✳	1	0	1	1	0	SEGSA B C D E
02H	✳	✳	✳	0	1	0	1	0	■ □ ■ ■ □
									f_{BLINK}
									■ ■ ■ □ □

f_{BLINK}: 1 to 2Hz

<Cautions for static icon operation>

- Be sure to write static icon data when the oscillating circuit is on. If the data is written when the oscillating circuit is off (Sleep Mode), previous display may remain and instantaneous lighting may occur.
- To perform resetting on the $\overline{RES}$ terminal except at the time of turning on power, turn off the static icon and blinking in advance, then turn off the oscillating circuit. If resetting is performed when the static icon or blinking is on, instantaneous lighting may be caused by stopping of the oscillating circuit.

Electronic Volume RAM

The SED1240 series is provided with an electronic volume function that permits controlling the liquid crystal drive voltage V_5 and adjusting the density of liquid crystal display. The electronic volume function can select one of 32 states of the liquid crystal drive voltage by writing 5-bit data into the electronic volume RAM.

When a V_5 voltage regulating built-in resistor is used, this function can attain a wider adjustment if the resistor ratio set command is used together.

The relation between electronic volume set RAM addresses and write data is shown below.

Function	RAM address [RE=0]	Electronic volume data								State	V_{EV}
		D7	D6	D5	D4	D3	D2	D1	D0		
Electronic volume	08H	✳	✳	✳	0	0	0	0	0	0	V_{REG-0}
		✳	✳	✳	0	0	0	0	1	1	$V_{REG-\alpha}$
		✳	✳	✳	0	0	0	1	0	2	$V_{REG-2\alpha}$
						. . .				. . .	
		✳	✳	✳	1	1	1	0	1	29	$V_{REG-29\alpha}$
		✳	✳	✳	1	1	1	1	0	30	$V_{REG-30\alpha}$
		✳	✳	✳	1	1	1	1	1	31	$V_{REG-31\alpha}$
	09H	✳	✳	✳	✳	T4	T2	T1	T0	–	For test

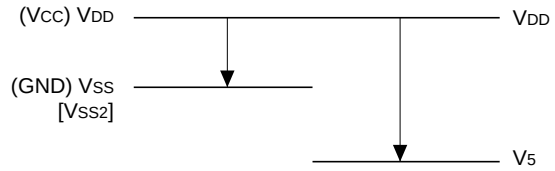
✳ :Unused

α :$\alpha = V_{REG}/150$

Note :Address"09H"(RE=0)isusedfortest.Don'tuseit.

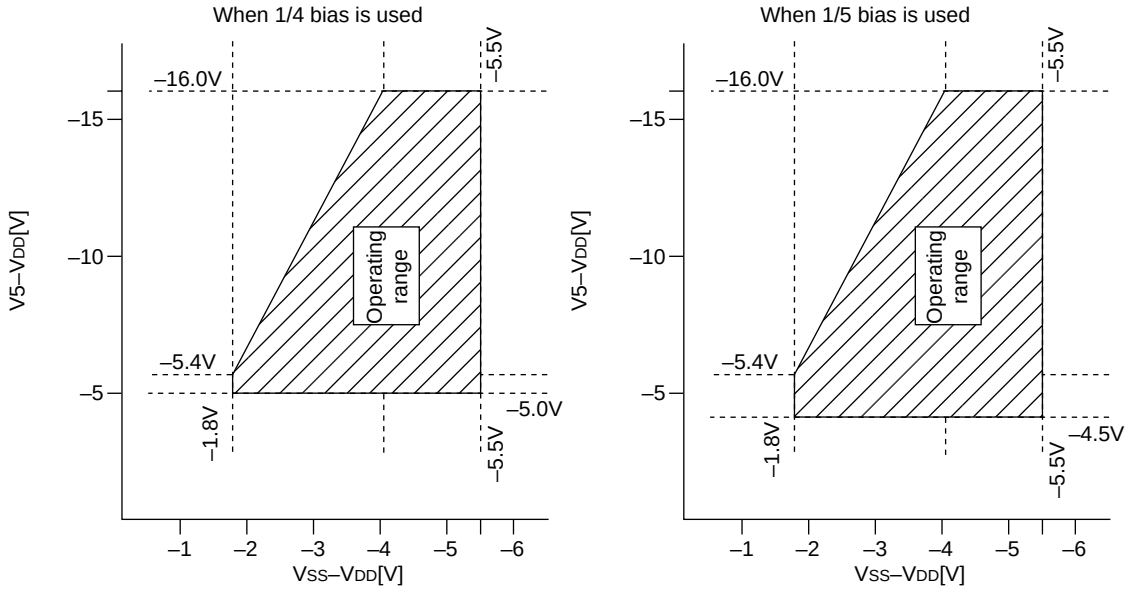
ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Standard value	Unit
Supply voltage (1)		V_{SS}	–7.0 to +0.3	V
Supply voltage (2)		V_{SS2}	–7.0 to +0.3	V
	Double boosting		–7.0 to +0.3	
	Triple boosting		–6.0 to +0.3	
Supply voltage (2)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{str}	–55 to +100	°C
	Bare chip		–65 to +125	



Notes: 1. All the voltage values are based on V_{DD} = 0 V.
2. The voltages of V_1, V_2, V_3, and V_4 must always meet the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ and the condition of $V_{DD} \geq V_5 \geq V_{OUT}$, $V_{DD} \geq (V_{SS}, V_{SS2}) \geq V_{OUT}$.
3. If the LSI is used exceeding the absolute maximum ratings, it may result in permanent destruction. It is desirable to use the LSI in the condition of electric characteristics at ordinary operation. If this condition is exceeded, a malfunction may be caused to the LSI, having a bad effect on its reliability.

● Operating voltage range for V_{SS} system (V_{SS} and V_{SS2}) and V_5 system (V_5)
Set the V_{SS2} to ensure that the V_{OUT} does not exceed the following operating voltage range:
It applies when an external power supply is used. When using an internal power supply, make sure to set V_{SS} in such that V_{OUT} may not exceed the operating voltage range of V_5 system given below.



DC CHARACTERISTICS

[V_{SS} = –5.5 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item		Symbol	Condition		min	typ	max	Unit	Applicable pin
Supply voltage (1)	Recommended operation	V_{SS}	—		–3.6 –5.5	—	–2.4 –1.8	V	V_{SS} *1
Supply voltage (2)	Recommended operation	V_{SS2}	—		–3.6 –5.5	—	–2.4 –1.8	V	V_{SS2} *2 *9
Supply voltage (3)	Recommended operation	V_5	When 1/4 bias used		–16.0	—	–5.0	V	V_5 *2
			When 1/5 bias used		–16.0	—	–4.5	V	
		V_1, V_2	—		0.6×V_5	—	V_{DD}	V	V_1, V_2
		V_3, V_4	—		V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage (1)		V_{IHC}	V_{SS} = –2.4V to –1.8V		0.1×V_{SS}	—	V_{DD}	V	*3
Low-level input voltage (1)		V_{ILC}			V_{SS}	—	0.9×V_{SS}	V	
High-level input voltage (2)		V_{IHC}	V_{SS} = –5.5V to –2.4V		0.2×V_{SS}	—	V_{DD}	V	
Low-level input voltage (2)		V_{ILC}			V_{SS}	—	0.8×V_{SS}	V	
Input leak current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*3
Liquid crystal driver ON resistance		R_{ON}	Ta=25°C ΔV=0.1V	V_5=–7.0V	—	20	40	KΩ	COM,SEG *4
Static current consumption		I_{DDQ}	—		—	0.1	5.0	µA	V_{DD}
Dynamic current consumption	I_{DD}	During display	V_5=–6V no load		—	—	80	µA	V_{DD} *5
		At standby	Oscillation ON, power OFF		—	—	20	µA	V_{DD} *6
		At sleep	Oscillation OFF, power OFF		—	—	5	µA	V_{DD}
		During access	fcyc=200KHZ		—	—	500	µA	V_{DD} *7
Input pin capacity		C_{IN}	Ta=25°C	f=1MHZ	—	5.0	8.0	pF	*3

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Frame frequency	f_{FR}	Ta=25°C V_{SS}=–3.0V	70	100	130	Hz	*10
External clock frequency	f_{CK}	2-line display (SED1242)	—	28.8	—	KHz	*10 *11
	f_{CK}	3-line display (SED1241)	—	41.6	—	KHz	*10 *11
	f_{CK}	4-line display (SED1240)	—	54.4	—	KHz	*10 *11

Item	Symbol	Condition	min	typ	max	Unit	Applicable pin
Minimum reset pulse width	t_{RW}	—	10	—	—	µs	*8
Reset start time	t_{RES}	—	—	—	50	ns	*8

Dynamic system

Item		Symbol	Condition	min	typ	max	Unit	Applicable pin
Built-in power supply	Input voltage	V_{SS2}	Double boosting	–5.5	—	–1.8	V	V_{SS2}
			Triple boosting	–5.5	—	–1.8		
	Boosting output voltage	V_{OUT}	Double boosting	–11.0	—	—	V	V_{OUT}
			Triple boosting	–16.5	—	—		
	Voltage regulating circuit operating voltage	V_{OUT}	—	–16.5	—	–5.4	V	V_{OUT}
	Voltage follower operating voltage	V_5	—	–16.0	—	–4.5	V	V_5 *12
	Reference voltage	V_{REG}	Ta = 25°C –0.05%/°C	–2.06	–2.0	–1.94	V	—

*1: The wide operating voltage range is guaranteed except the case where a sudden voltage change occurs during MPU access.
In the low-supply voltage data holding characteristic, it is applied in the sleep mode and MPU access cannot be guaranteed

*2: At triple boosting, take care about supply voltage V_{SS2} so that it may not exceed the V_5 operating voltage range.

*3: D0 to D5, D6 (SCL), D7 (SI), A0, $\overline{RES}$, $\overline{CS}$, $\overline{WR}$ (E), P/S, IF. C86. $\overline{CK}$

*4: This is a resistance value when a voltage of 0.1 V is applied between output pins SEGn, SEGSn, COMn, and COMSn, and each power pin (V_1, V_2, V_3, V_4). This is specified within the range of operating voltage (2).

$$R_{ON} = 0.1\ V / \Delta I$$

(ΔI: A current flowing when 0.1 V is applied between the power supply and the output)

*5: Applies under the following conditions:
- No access from MPU during all characters 'H' display
- The built-in circuit and oscillating circuit are operating.
- CGRAM unused, HPM = 0 specified, V_{SS} = -3.0

*6: Applies under the following conditions:
- Standby mode
- ALl the built-in power circuit off
- Display off
- Oscillating circuit on

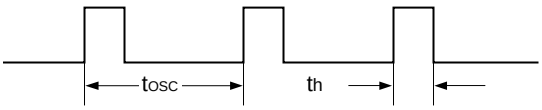
*7: Indicates that fcyc is used for writing at all times. The current consumption during access is approximately proportional to the access frequency (fcyc).

*8: Specifies the $\overline{RES}$ signal minimum pulse width. To perform resetting, it is necessary to input the pulse having a width of t_{RW} or more. Original, the method for reset case 1 is used, but the method for reset case 2 can also be used if the reset start time condition of t_{RES} or less is satisfied.

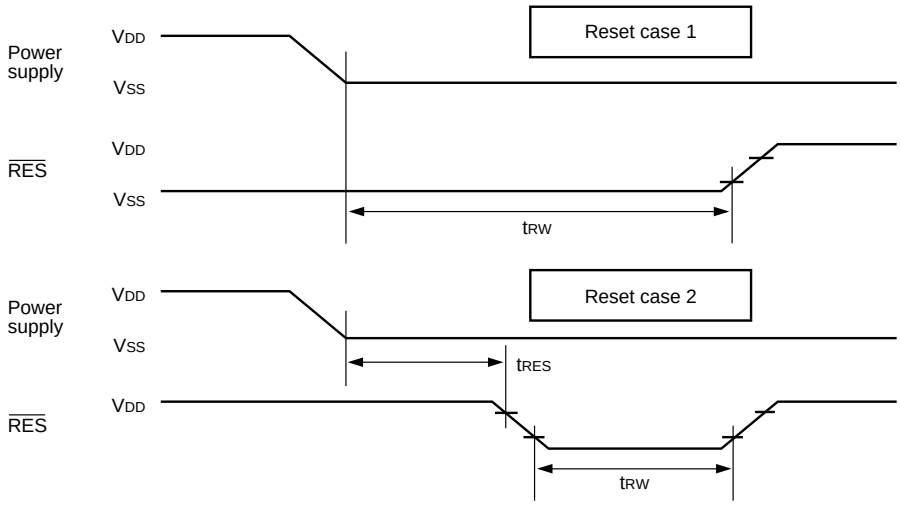
*9: The boosting circuit performs boosting, using voltage between the V_{DD} and V_{SS2} as source voltage. Check the V_{SS2} input voltage to ensure that it does not exceed V_{OUT} absolute maximum rating, or the operating voltage range of the V_{SS} system (V_{SS}) and V_5 system (V_5).

*10: Frequency f_{OSC} of the internal circuit drive oscillating circuit and boosting clock fBST vary according to the type. The following shows the relationship between the oscillating circuit f_{OSC} and boosting clock f BST:
- f_{OSC} = (number of digits) × (1/duty) × f_{FR}
- f_{BST} = (1/2) × (1/number of digits) × f_{OSC}

*11: Enter the following input when performing operations by the external clock, without using the built-in oscillating circuit:
- Duty = (th/t_{OSC}) × 100 = 20 to 30%
- f_{OSC} = 1/t_{OSC}



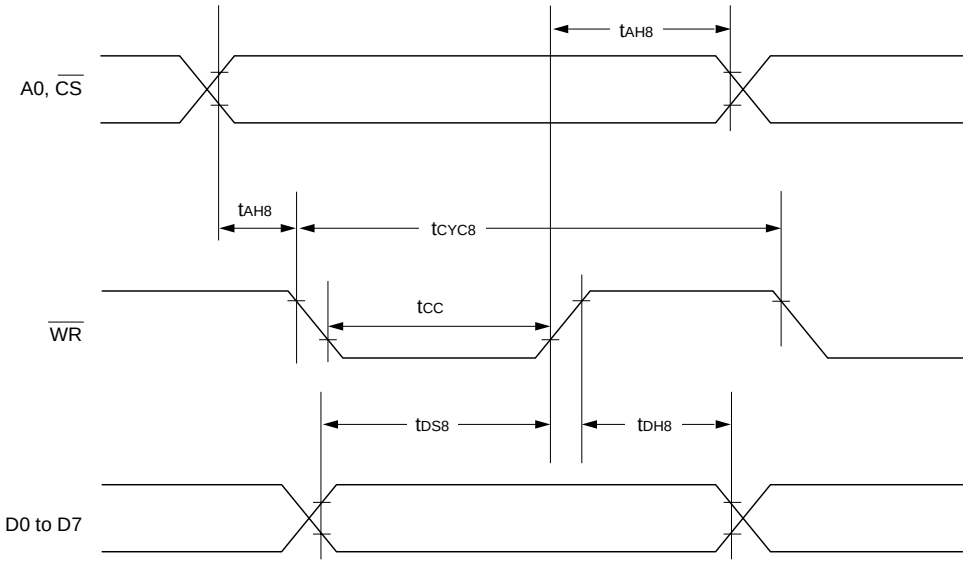
*12: Adjust the V_5 voltage regulating circuit within the voltage follower operating voltage range.



* All timing are specified on the basis of 20% and 80% of V_{SS}.

AC CHARACTERISTICS

System Bus Write Characteristics I (80 series MPU)



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	300	–	ns
Control pulse width (WR)		tCC	–	60	–	ns
Data setup time	D0 to D7	tDS8	–	60	–	ns
Data hold time		tDH8	–	50	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

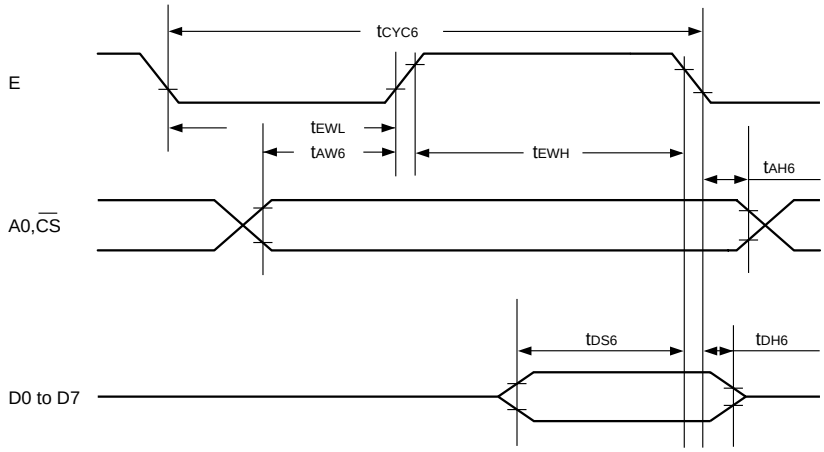
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	500	–	ns
Control pulse width (WR)		tCC	–	100	–	ns
Data setup time	D0 to D7	tDS8	–	100	–	ns
Data hold time		tDH8	–	50	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
Address hold time	A0, CS	tAH8	–	30	–	ns
Address setup time		tAW8	–	60	–	ns
System cycle time	WR	tCYC8	–	1000	–	ns
Control pulse width (WR)		tCC	–	200	–	ns
Data setup time	D0 to D7	tDS8	–	200	–	ns
Data hold time		tDH8	–	50	–	ns

*1: At the fall and rise time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of VSS.
*3: The same timing is not required for A0 and CS. Input signals so that A0 and CS may satisfy tAW8 and tAH8 respectively.

System Bus Write Characteristics II (68 series MPU)



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	300	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	60	–	ns
Data hold time		tDH6	–	50	–	ns
Enable H pulse width	E	tEWH	–	60	–	ns
Enable L pulse width	E	tEWL	–	60	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C unless otherwise specified]

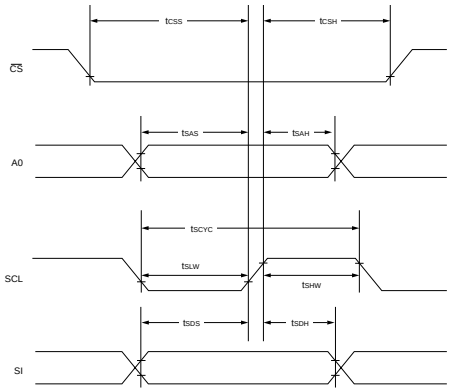
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	500	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	100	–	ns
Data hold time		tDH6	–	50	–	ns
Enable H pulse width	E	tEWH	–	100	–	ns
Enable L pulse width	E	tEWL	–	100	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C unless otherwise specified]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System cycle time	A0, $\overline{CS}$	tCYC6	–	1000	–	ns
Address setup time		tAW6		60	–	ns
Address hold time		tAH6		30	–	ns
Data setup time	D0 to D7	tDS6	–	200	–	ns
Data hold time		tDH6	–	50	–	ns
Enable H pulse width	E	tEWH	–	200	–	ns
Enable L pulse width	E	tEWL	–	200	–	ns

*1: tCYC6 indicates the cycle of the E signal in the $\overline{CS}$ active state.
It is necessary to secure tCYC6 after $\overline{CS}$ becomes active.
*2: For the rise and fall time of input signals, set 15 ns or less.
*3: Every timing is specified on 20% and 80% of VSS.
*4: The same timing is not required for A0 and $\overline{CS}$. Input signals so that A0 and $\overline{CS}$ may satisfy tAW6 and tAH6 respectively.

Serial Interface



[VSS = –5.5 V to –4.5 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	700	–	ns
SCL "H" pulse width		tSHW	–	250	–	ns
SCL "L" pulse width		tSLW	–	250	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	250	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	500	–	ns

[VSS = –4.5 V to –2.4 V, Ta = –30 to 85°C]

Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	1000	–	ns
SCL "H" pulse width		tSHW	–	300	–	ns
SCL "L" pulse width		tSLW	–	300	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	300	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	700	–	ns

[VSS = –2.4 V to –1.8 V, Ta = –30 to 85°C]

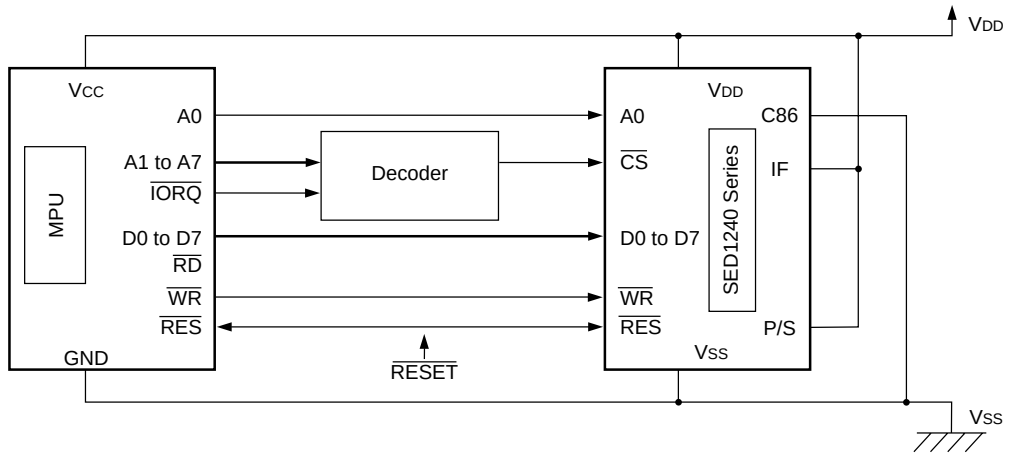
Item	Signal	Symbol	Measuring condition	Min.	Max.	Unit
System clock cycle	SCL	tSCYC	–	2000	–	ns
SCL "H" pulse width		tSHW	–	300	–	ns
SCL "L" pulse width		tSLW	–	300	–	ns
Address setup time	A0	tSAS	–	50	–	ns
Address hold time		tSAH	–	500	–	ns
Data setup time	SI	tSDS	–	50	–	ns
Data hold time		tSDH	–	50	–	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS	–	150	–	ns
		tCSH	–	900	–	ns

*1: For the rise and fall time of input signals, set 15 ns or less.
*2: Every timing is specified on 20% and 80% of VSS.
*3: To validate a command or data immediately before the rise of $\overline{CS}$, tCSH must be satisfied at the latch timing of D0 data. If $\overline{CS}$ is started at another data latch timing, the previous command or data will not be input.

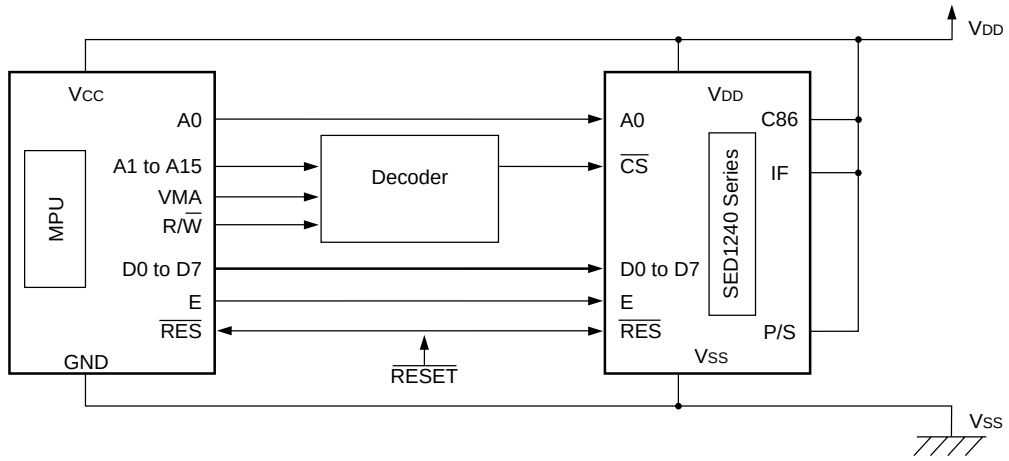
MPU INTERFACE CONNECTION EXAMPLES (FOR REFERENCE)

The SED1240 series can be connected to the 80 series MPU or 68 series MPU. Furthermore, it can be operated with less signal lines if the serial interface is used.
When an MPU bus, port, etc. are put into high-impedance for a certain period by RESET, input RESET into this machine after the input to the SED1240 series becomes definitive.

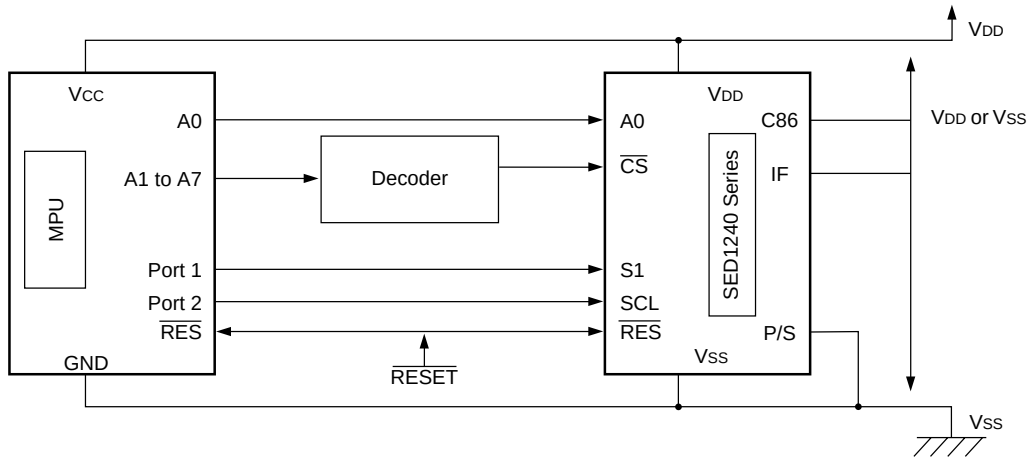
80 Series MPU



68 Series MPU

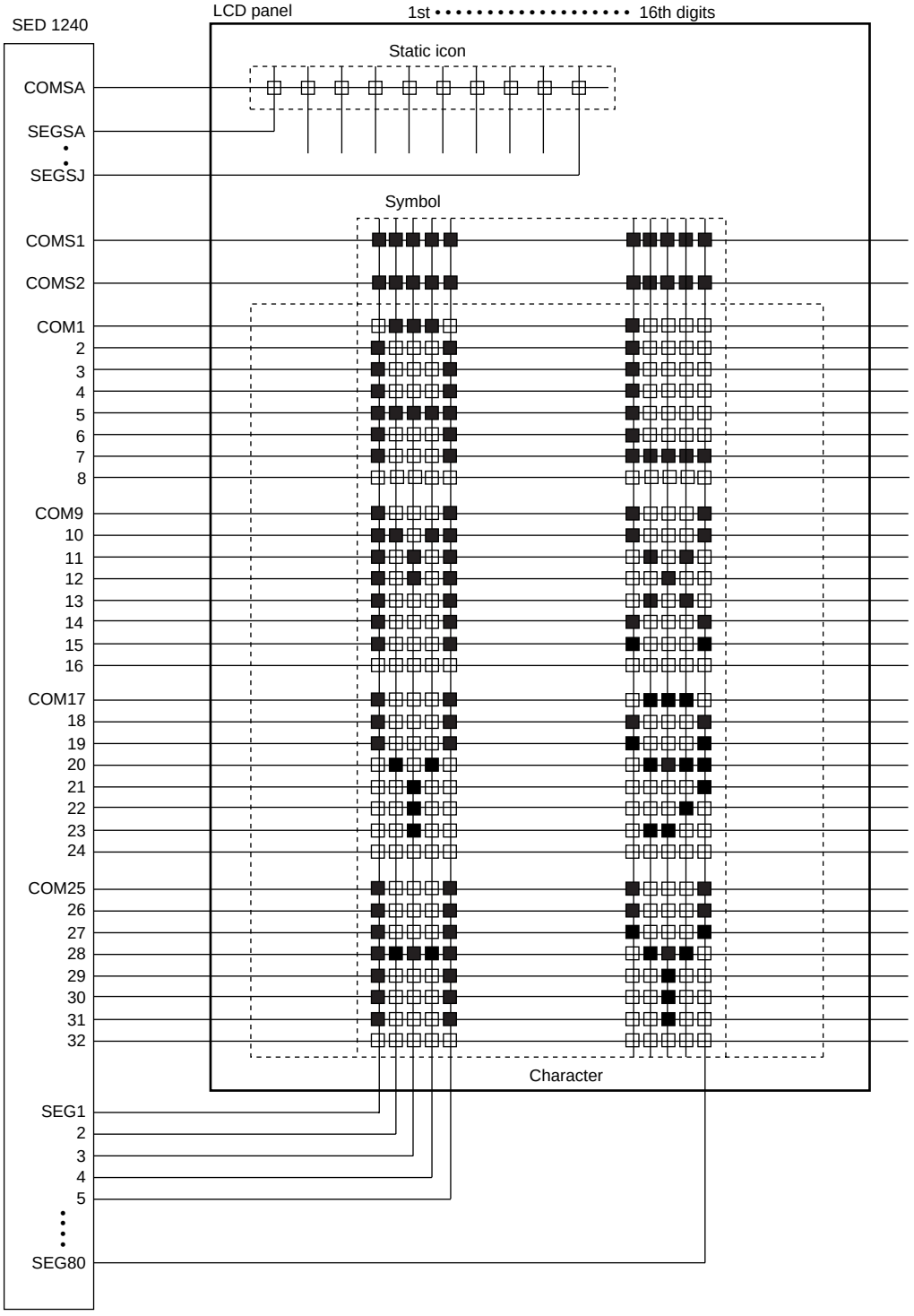


Serial Interface

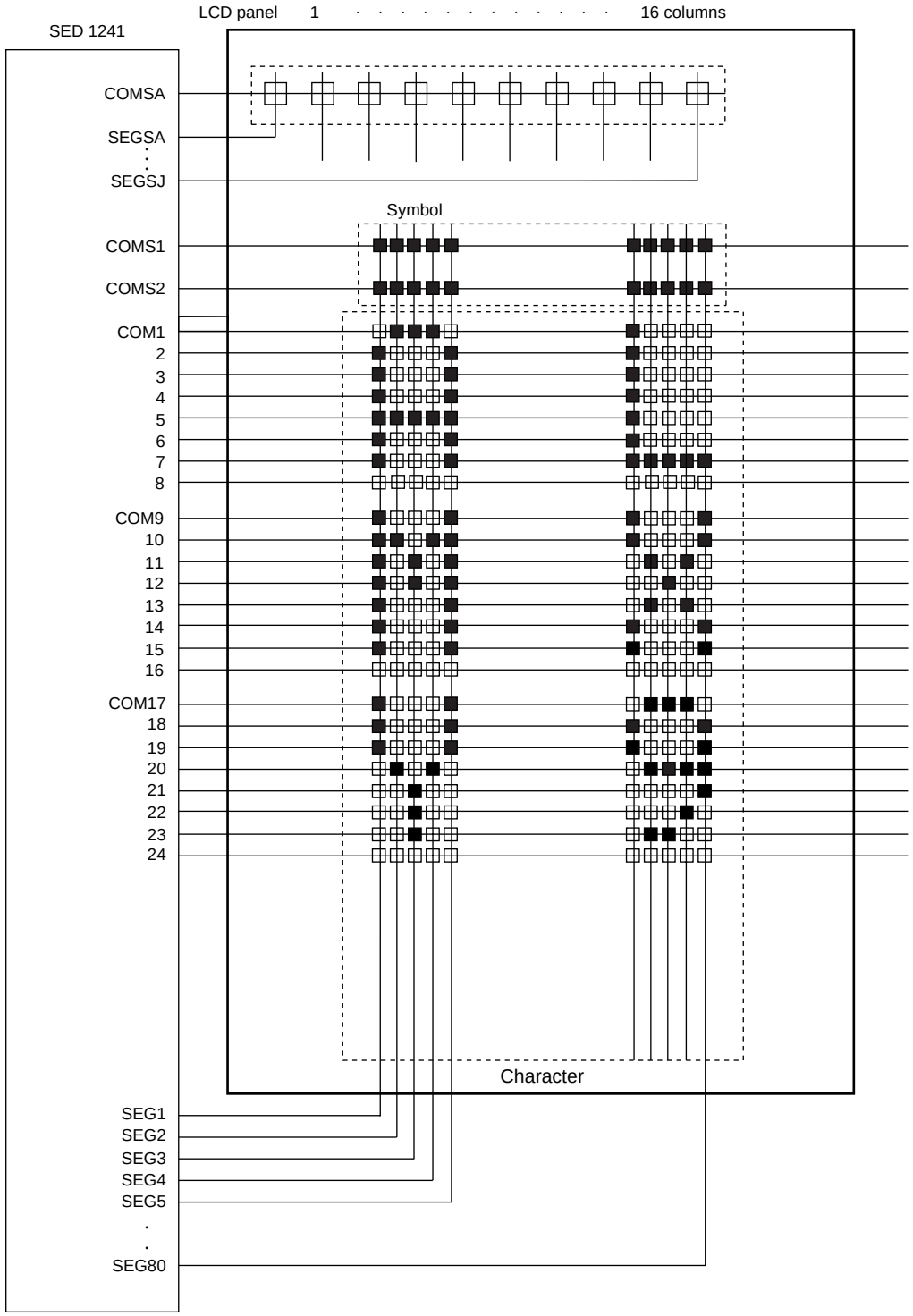


INTERFACE WITH LCD CELL (FOR REFERENCE)

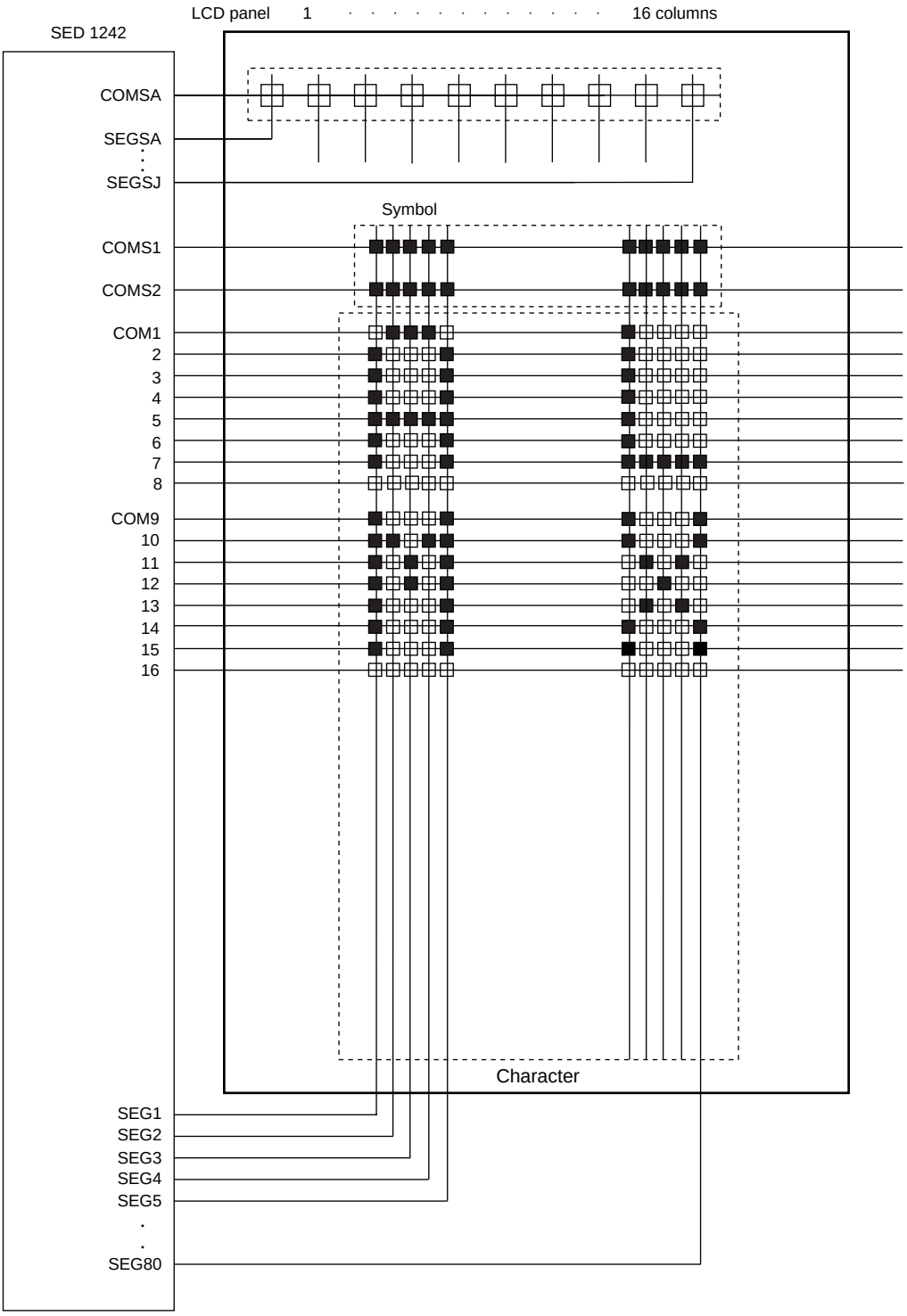
[16 digits × 4 line 5 × 8 dots + symbol]



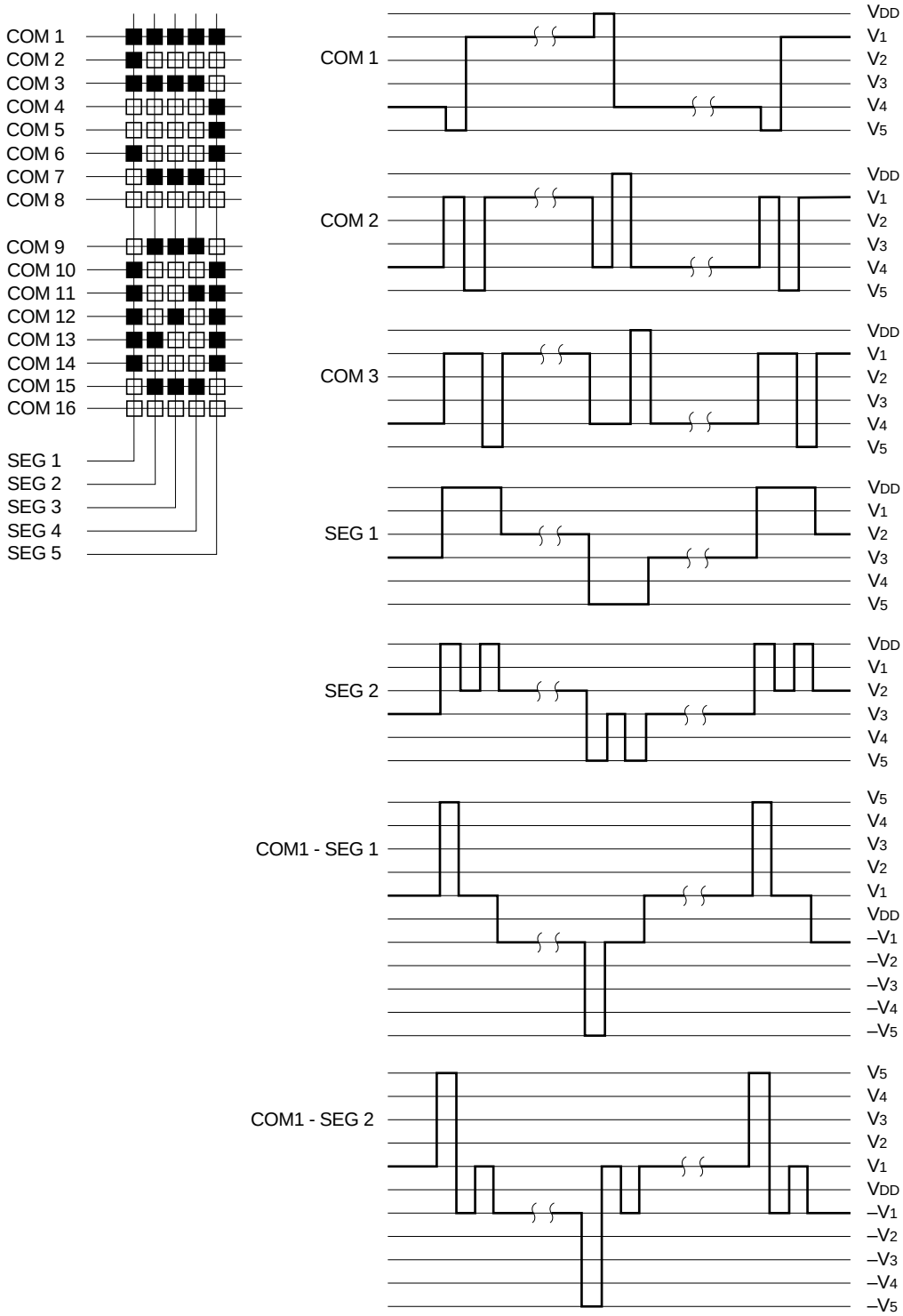
[16 digits × 3 line 5 × 8 dots]



[16 digits × 2 line 5 × 8 dots]



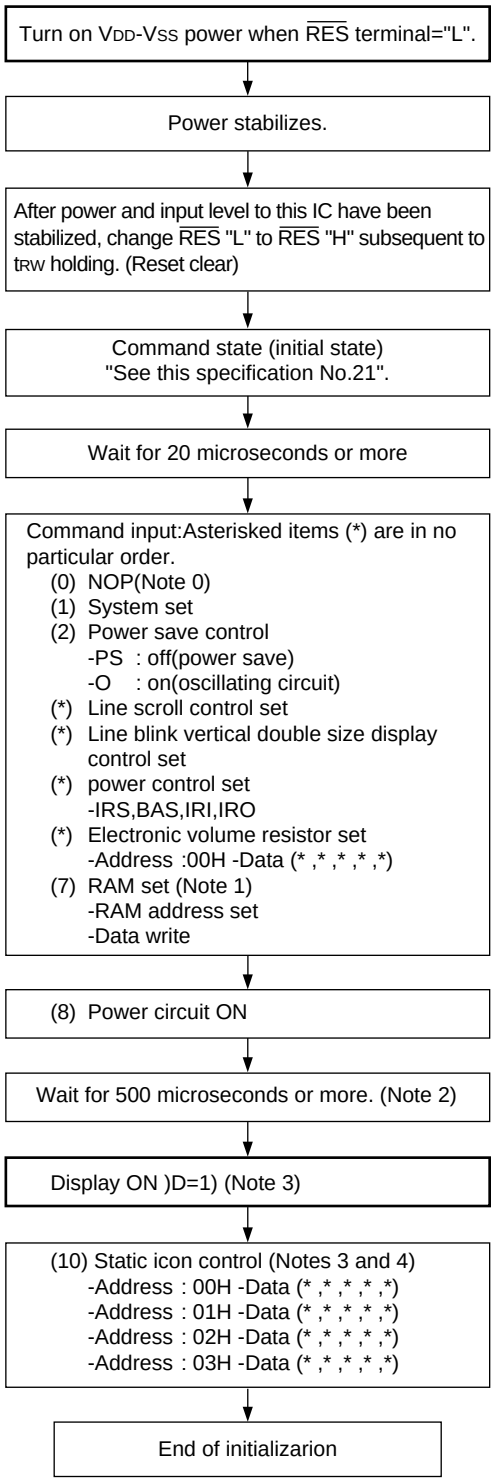
LIQUID CRYSTAL DRIVE WAVEFORM (B WAVEFORM)



Example of Setting the Instructions (Reference)

(1) Initialization

This IC has no power-on reset function when power is turned on. Accordingly, the IC internal status is indefinite when the power has been turned on. Be sure to initialize the system. If electric charge remains in the smoothing capacitor connected between the liquid crystal drive voltage output terminal (V_1 to V_5) and V_{DD} terminal, such a trouble as temporary blackening will occur when power is turned on. To avoid such a trouble, follow the steps given below:



Note 0 : (0) is a NOP command. This command has a function to clear the test mode. After resetting, it is recommended to execute this command several times before starting input. It is also recommended to execute it on a periodic basis at a proper position of the insutruction.

Note 1: (7) denotes RAM initialization. Set the contents to be displayed in the beginning. For items not to be displayed (RAM clear), use the following steps:

- DDRAM - write 20H (character code).
- CGRAM - write 00H (data "0").
- Symbol register - write 00H (data "0").

The RAM data is unspecified at the time of RES input (after power is turned on). If the data "0" is not written at this stage, unexpected display may occur to the unset position.

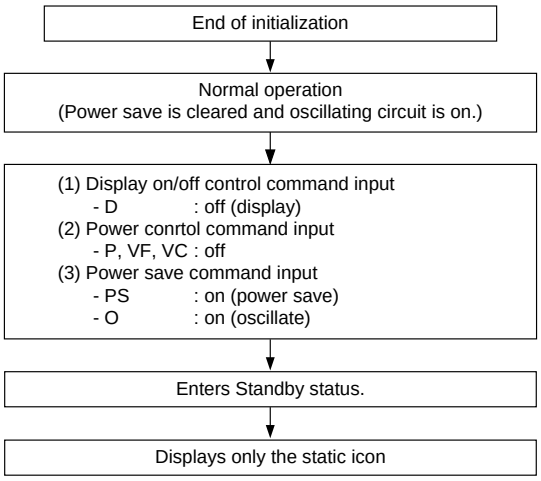
Note 2: Defined by the rising characteristics of the boosting circuit, power regulating circuit and voltage and follower circuit, time setting varies according to the external capacity. So be sure to make confirmation by external capacity, and set this time.

Note 3: The dynamic drive system display lamp is lit up by the display on/off command when it is on. The static icon lamp is lit by the static icon control command. So to light up the lamp simultaneously with start of display, execute the display on/off control command and static icon control within one frame.

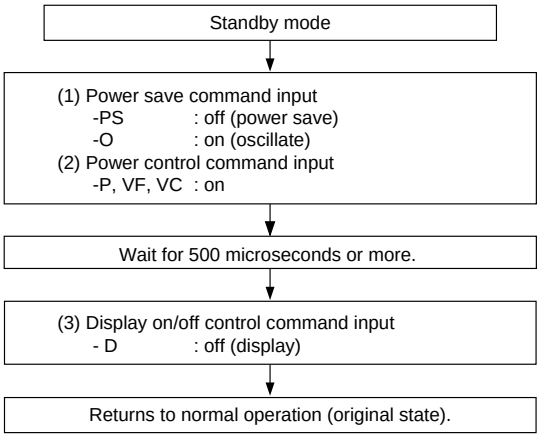
Note 4: Static icon control must be operated when the oscillating circuit is on. (This is mandatory.)

Note 5: (0) to (8) must be performed when display is off.

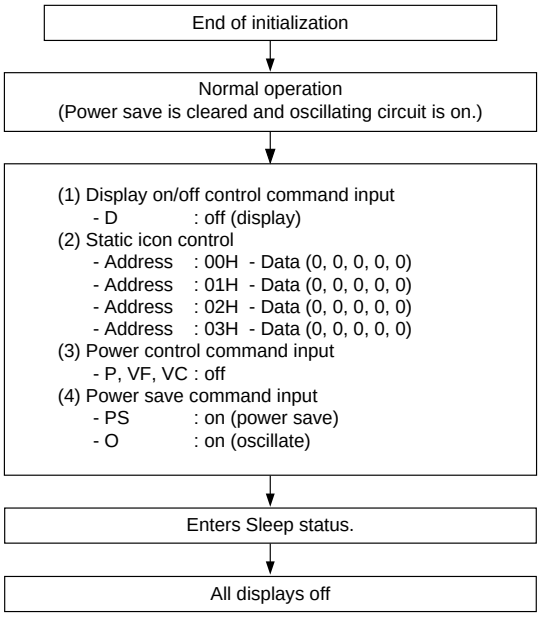
(2-1) Setting the Standby mode



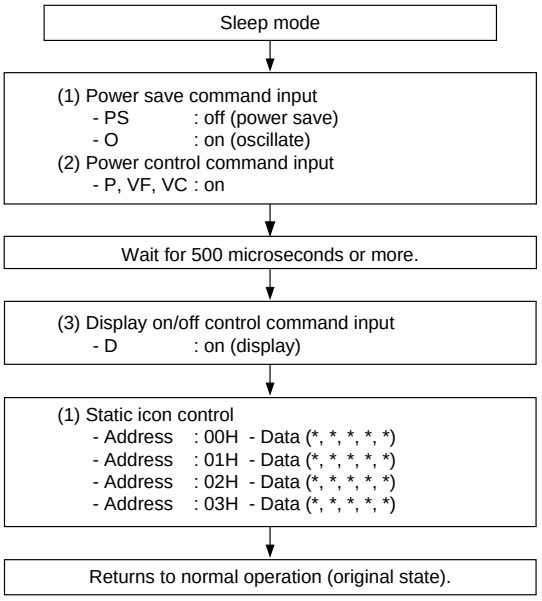
(2-1) Resetting the Standby mode



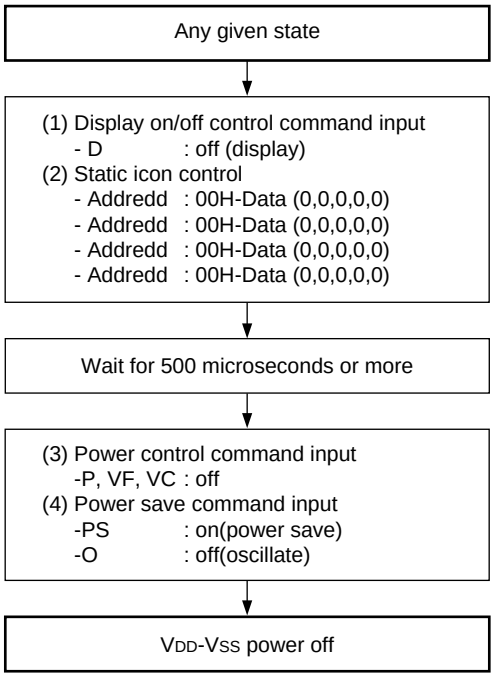
(3-1) Setting the Sleep mode



(3-1) Resetting the Sleep mode



(4) Power off sequence
Similar to the case of power on sequence, if this IC power is turned off when the built-in power is on, power supply to the built-in liquid crystal drive circuit may continue for a very little time, adversely affecting the liquid crystal panel display quality. To prevent this, strictly follow the power off sequence.



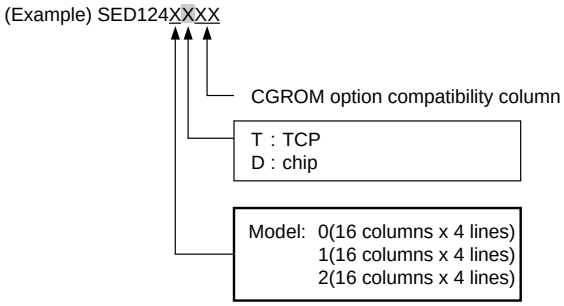
Note: This IC is configured as a logic circuit with a power supply of V_{DD}–V_{SS} which controls the LCD power supply V_{DD}–V_5 driver. Therefore, if the power supply V_{DD}–V_{SS} is shut down while voltage remains in the LCD power supply V_{DD}–V_5, the driver (COM and SEG) may output an uncontrolled voltage. When shutting the power off, be sure to observe the following operation procedure.

- Turn the internal power supply off, confirm that the voltage levels of the internal voltage follower outputs V_1, V_2, V_3 and V_4 have dropped below the LCD panel threshold voltage values, then turn the power of this IC (V_{DD}–V_{SS}) off.

OPTIONS LIST

The SED 1240 series has the following options. Options are available exclusively for users. Please contact our Sales Department.

○ The following shows how to define the name of the product compatible with options:



Character Generator ROM (CGROM) Specifications

The SED1240 series is provided with a character generator ROM for up to 544 types of characters. Each character size is of a structure of 5×7 (8) dots.

This CGROM is designed as a masked ROM, and is compatible with the CGROM for exclusive use of the user. For the standard CGROM, see the Character Font Table.

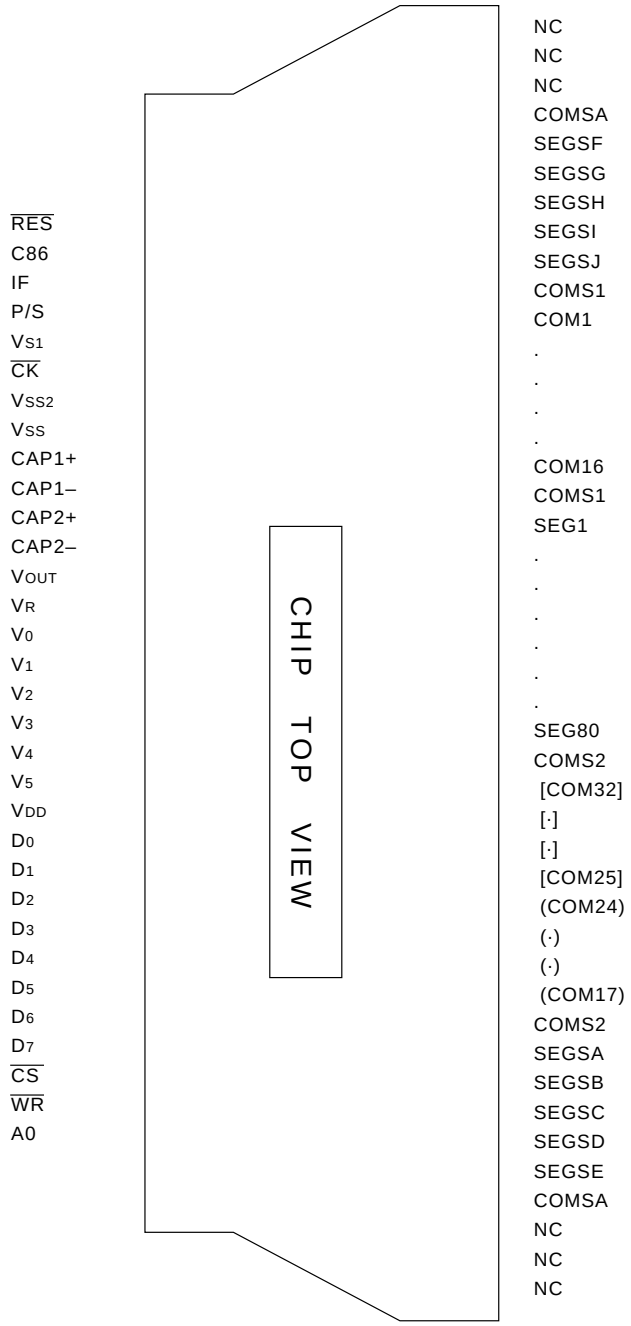
TCP Specifications

The SED1240 series is compatible with the TCP specifications exclusive to the user, in addition to our standard TCP. Please contact our Sales Department for information.

EXAMPLE OF TCP ARRANGEMENT

Note: The following does not specify the TCP external view.

REFERENCE

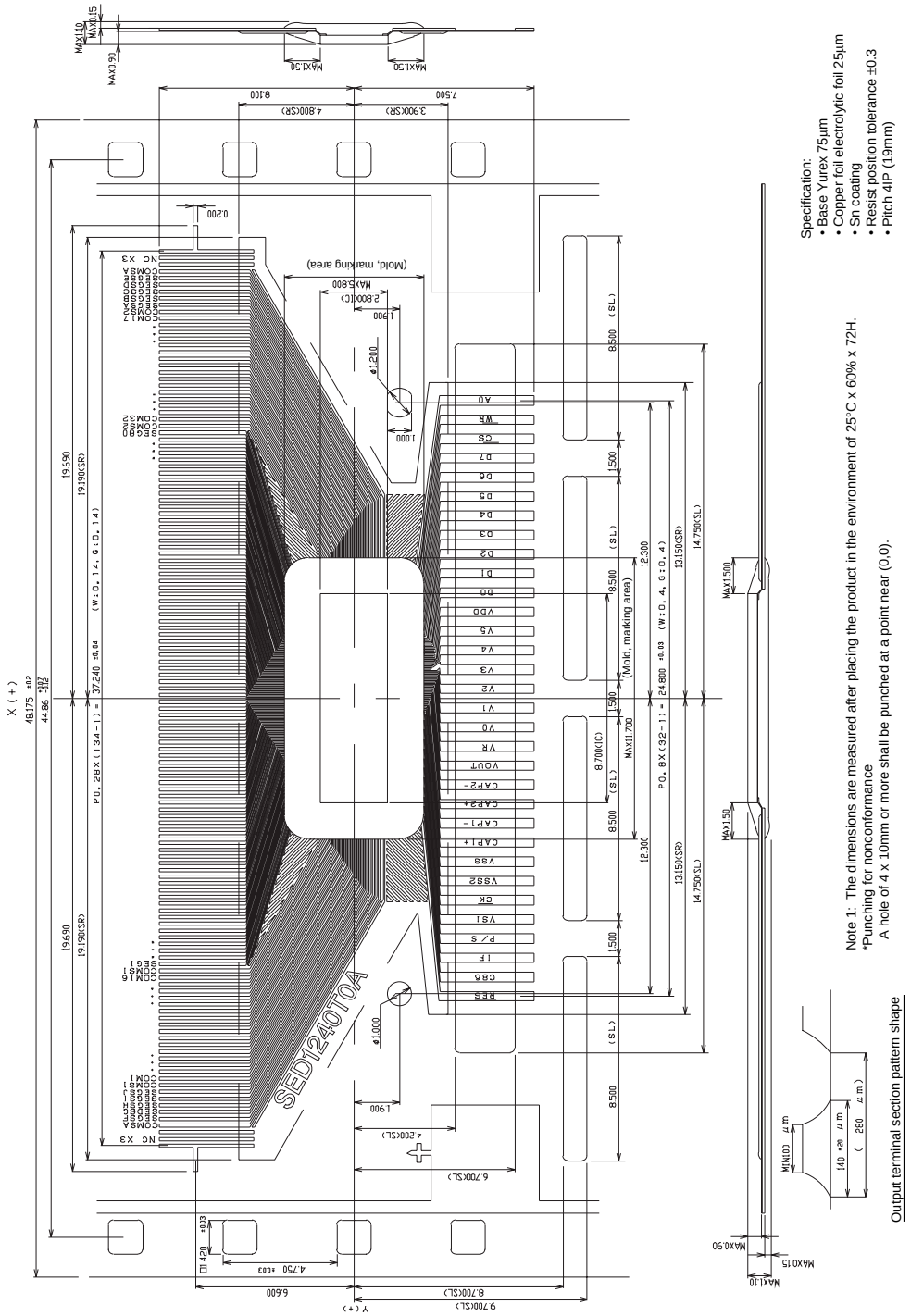


SED1240TXX: COM1 to 16, (COM17 to 24) and [COM25 to 32] are used.
SED1241TXX: COM1 to 16 and (COM17 to 24) are used. [COM25 to 32] is for NC.
SED1242TXX: COM1 to 16 is used. (COM17 to 24) and [COM25 to 32] are for NC.

EXAMPLE OF TCP

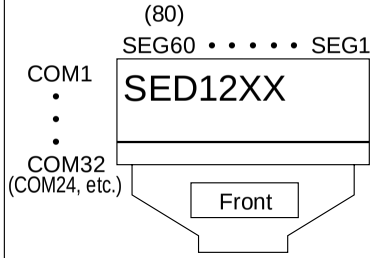
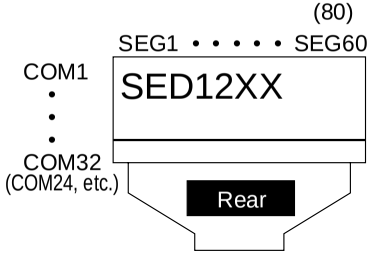
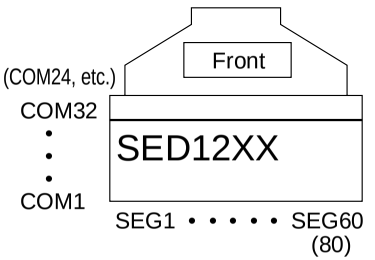
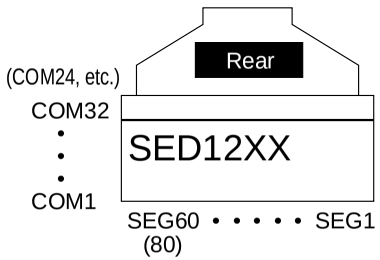
TCP External View

REFERENCE



SED1220/1225/1240 Example of System Setup Depending on Mount Direction

Reference

	① Case1 (Chip Front)	② Case2 (Chip Rear)	③ Case3 (Chip Front)	④ Case4 (Chip Rear)
				
SED1220	• Unable to correspond with commands. • Only able to correspond with custom fonts.	○ System set • S = 0	○ System set • S = 1	• Unable to correspond with commands. • Only able to correspond with custom fonts.
SED1225	○ System set • S1 = 0 • S2 = 1 (Horizontally-reversed)	○ System set • S1 = 0 • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 0	○ System set • S1 = 1 (Vertically-reversed) • S2 = 1 (Horizontally-reversed)
SED1240	○ System set • CS = 0 • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order (as it is reversed in the unit of character).	○ System set • CS = 0 • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 0	○ System set • CS = 1 (COM-reversed) • SS = 1 (SEG-reversed) However, the input of DDRAM address of "SED12XX" from the first digit of the first line shall be 3FH and 3EH, in this order.

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