3. SED152A Series

Contents

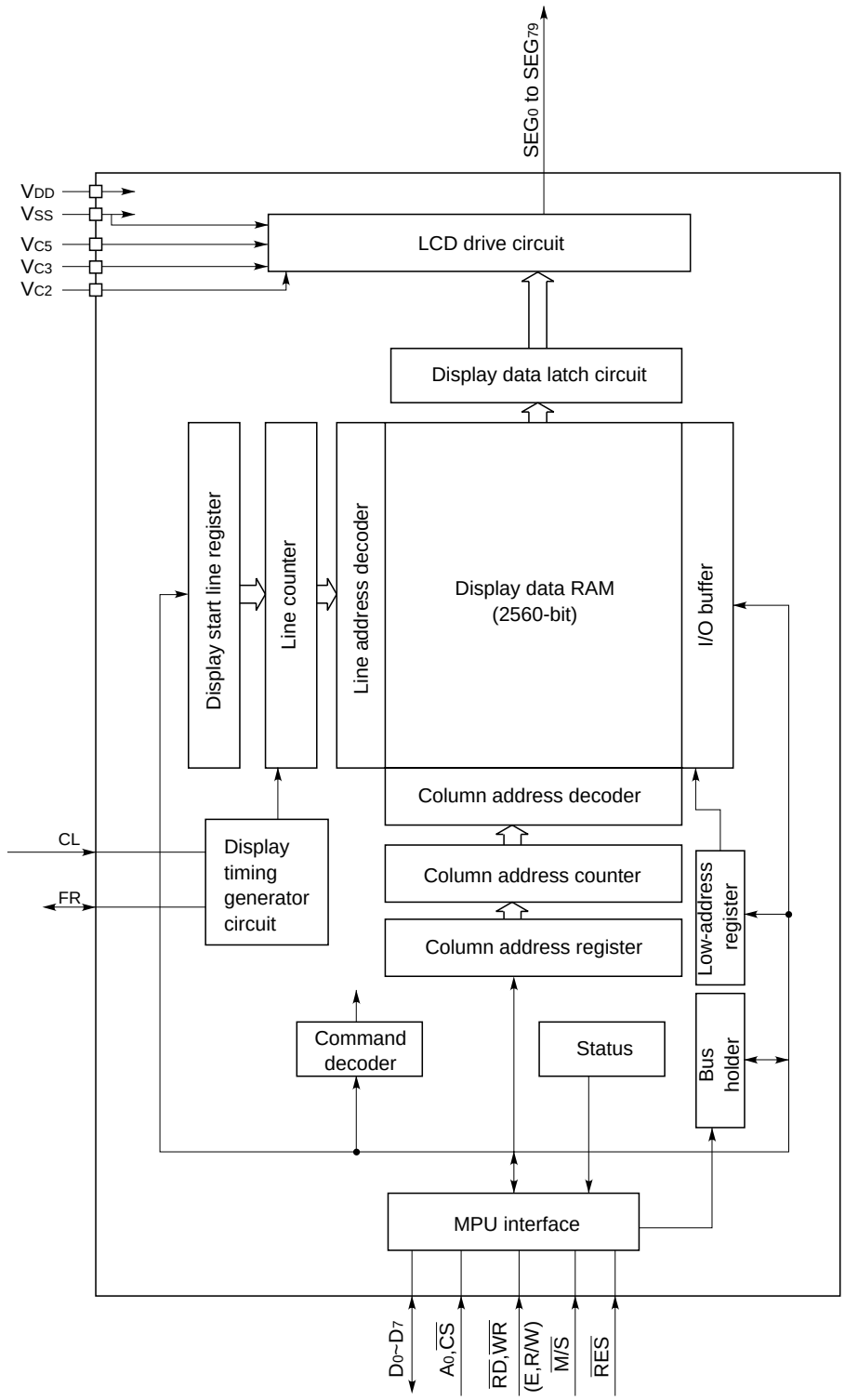
OVERVIEW

The SED152A family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The SED1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- 32 × 80 bit RAM
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  V_{DD} – V_{SS}: 2.4V to 6.0 V
  V_{C5} – V_{SS}: 3.5V to 6.0 V
- Low-power CMOS
- Al-pad chip

BLOCK DIAGRAM

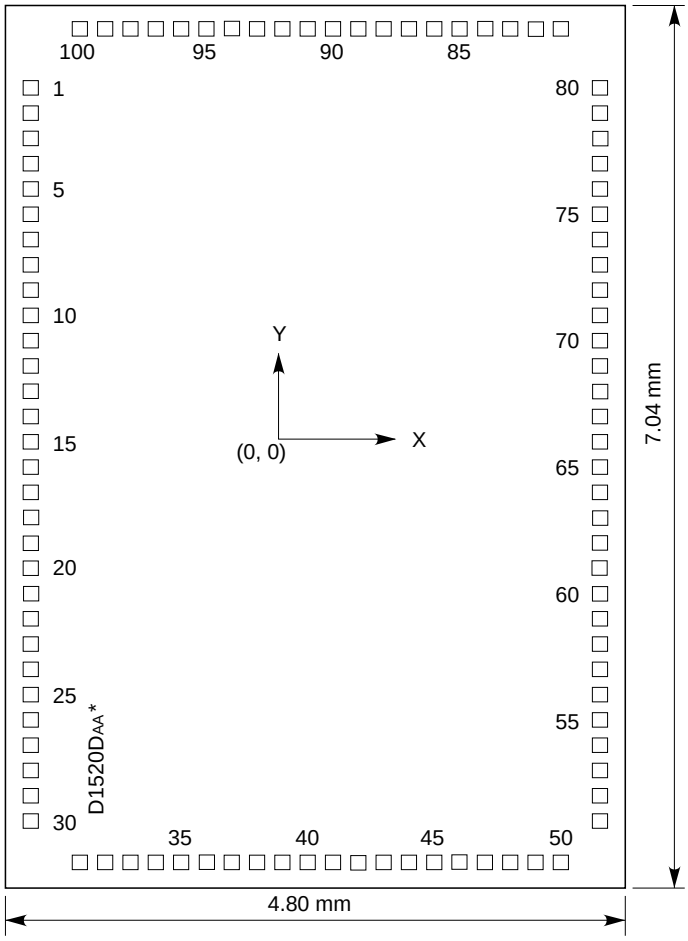


PAD

Pad Arrangement

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 µm



PAD ARRANGEMENT

SED152AD Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	$\overline{A0}$	4641	5048
74	$\overline{CS}$	4641	5247
75	$\overline{CL}$	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{DD}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{SS}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	VC2	2499	6884
91	VC3	2300	6884
92	VC5	2100	6884
93	SEG79	1901	6884
94	SEG78	1701	6884
95	SEG77	1502	6884
96	SEG76	1302	6884
97	SEG75	1103	6884
98	SEG74	903	6884
99	SEG73	704	6884
100	SEG72	504	6884

PIN DESCRIPTION

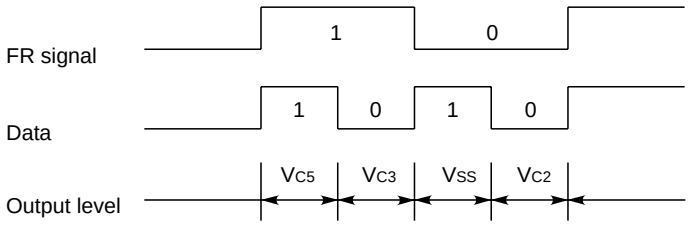
(1) Power Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_{C5}, V_{C3}, V_{C2}	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$

(2) System Bus Connection Pins

D7 to D0 *1	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. Low level (0): D0 to D7 are display control data. High level (1): D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⊓⊔⊓ the 68-series MPU is initialized, and when it goes ⊔⊓⊔ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. An address bus signal is usually decoded by use of chip select signal.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active low. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$) $\overline{WR}$ (R/$\overline{W}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.
FR	Input. This is an input pin of LCD AC signals, and connected to the FR pin of common driver.
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{C5}, V_{C3}, V_{C2}, V_{SS} is selected by the combination of display RAM contents and FR signal. 

BLOCK DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type
   The SED152A series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).
   When the $\overline{CS}$ signal is high, the SED152A series is disconnected from the MPU bus and set to stand by. (However, the reset signal is entered regardless of the internal setup status.)

Table 1

$\overline{RES}$ signal input level	MPU type	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	80-series	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	68-series	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7

Data transfer

The SED152A drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.
In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.
This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	80 MPU		68 MPU	Function
A0	$\overline{RD}$	$\overline{WR}$	R/$\overline{W}$	
1	0	1	1	Read display data
1	1	0	0	Write display data
0	0	1	1	Read status
0	1	0	0	Write to internal register (command)

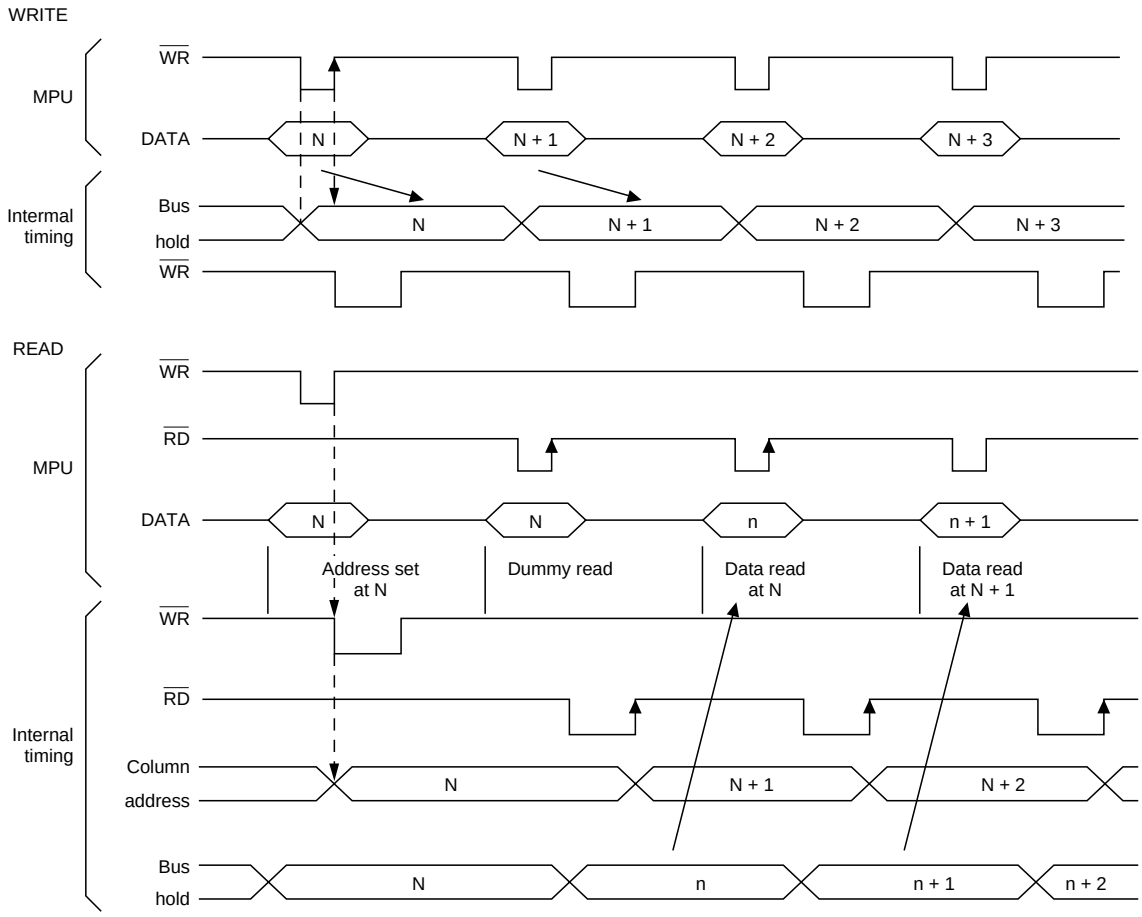


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 3. The contents of the page register are set by the Set Page Register command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 3.

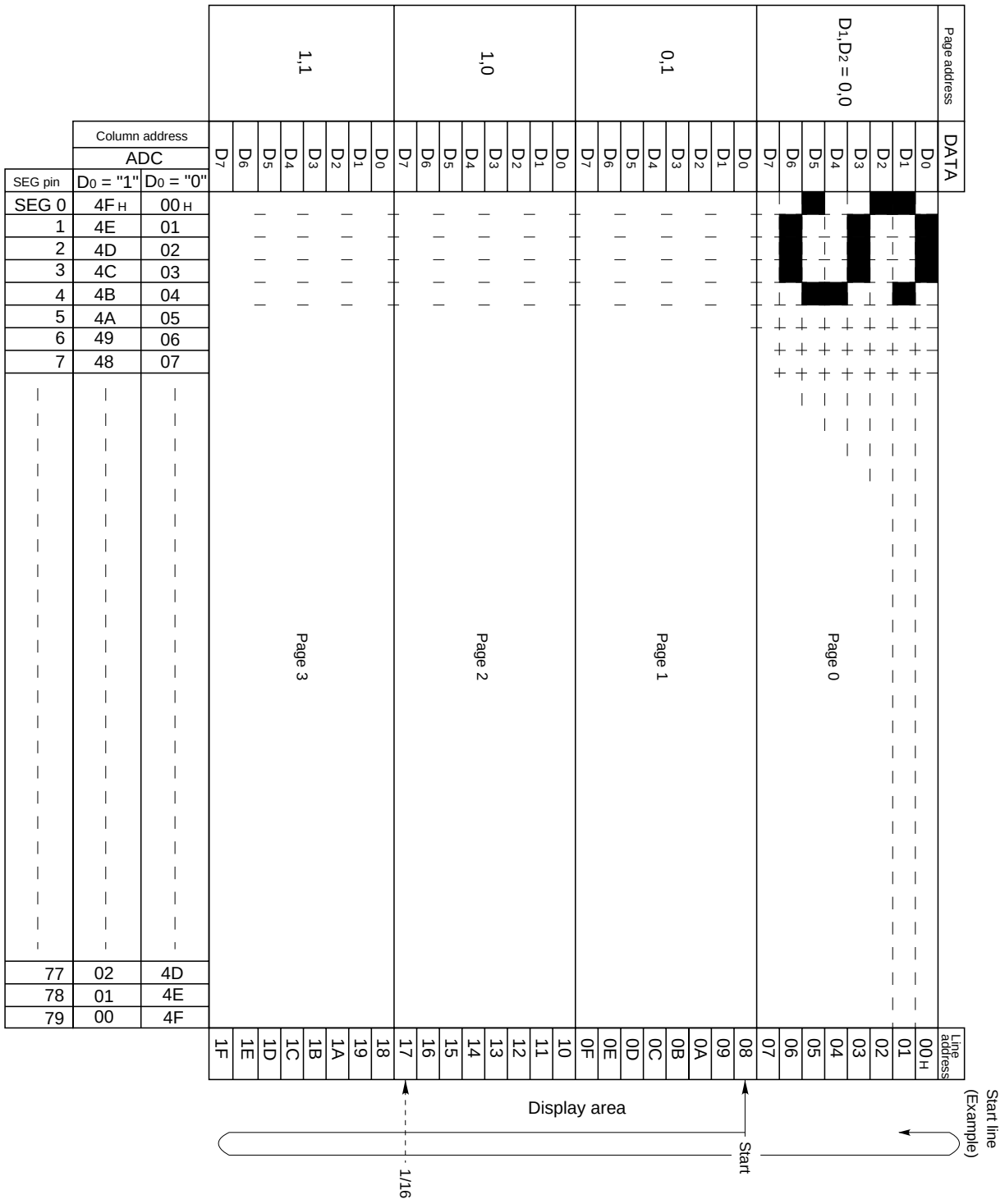
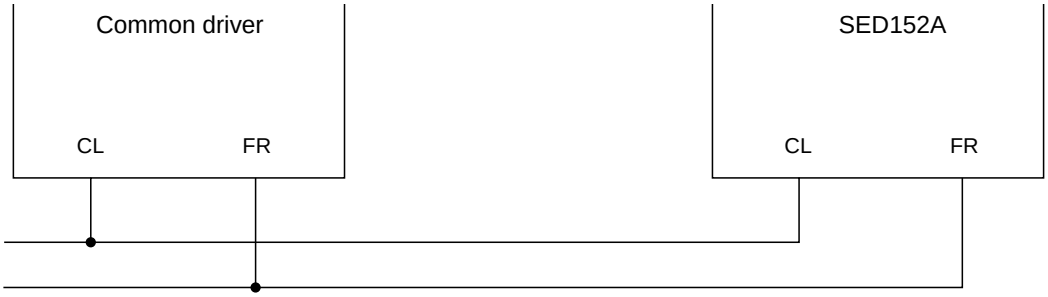


Figure 2 Display Data RAM Addressing

Display Timing Generation Circuit

The master clock CL and the frame signal FR generate internal timing. The master clock CL causes the line counter to operate, which synchronizes with the line counter. Therefore, the master clock CL and the frame signal FR input signals of the same phases as those of the CR and FR signals of the common driver, respectively.



Display Data Latch Circuit

The display data latch circuit is a latch that temporarily memorizes the display data to be output to the liquid crystal drive circuit from the display data RAM for each common period. Display ON/OFF and Display All Lamps ON/OFF commands control the data in this latch. Therefore, data in the display data RAM are never to be modified.

Liquid Crystal Drive Circuit

This circuit comprises 80 sets of multiplexers to generate four-value level for the liquid crystal drive. Various combinations of display data in the display data latch and the FR signals output the liquid crystal waveforms as shown in Fig. 3.

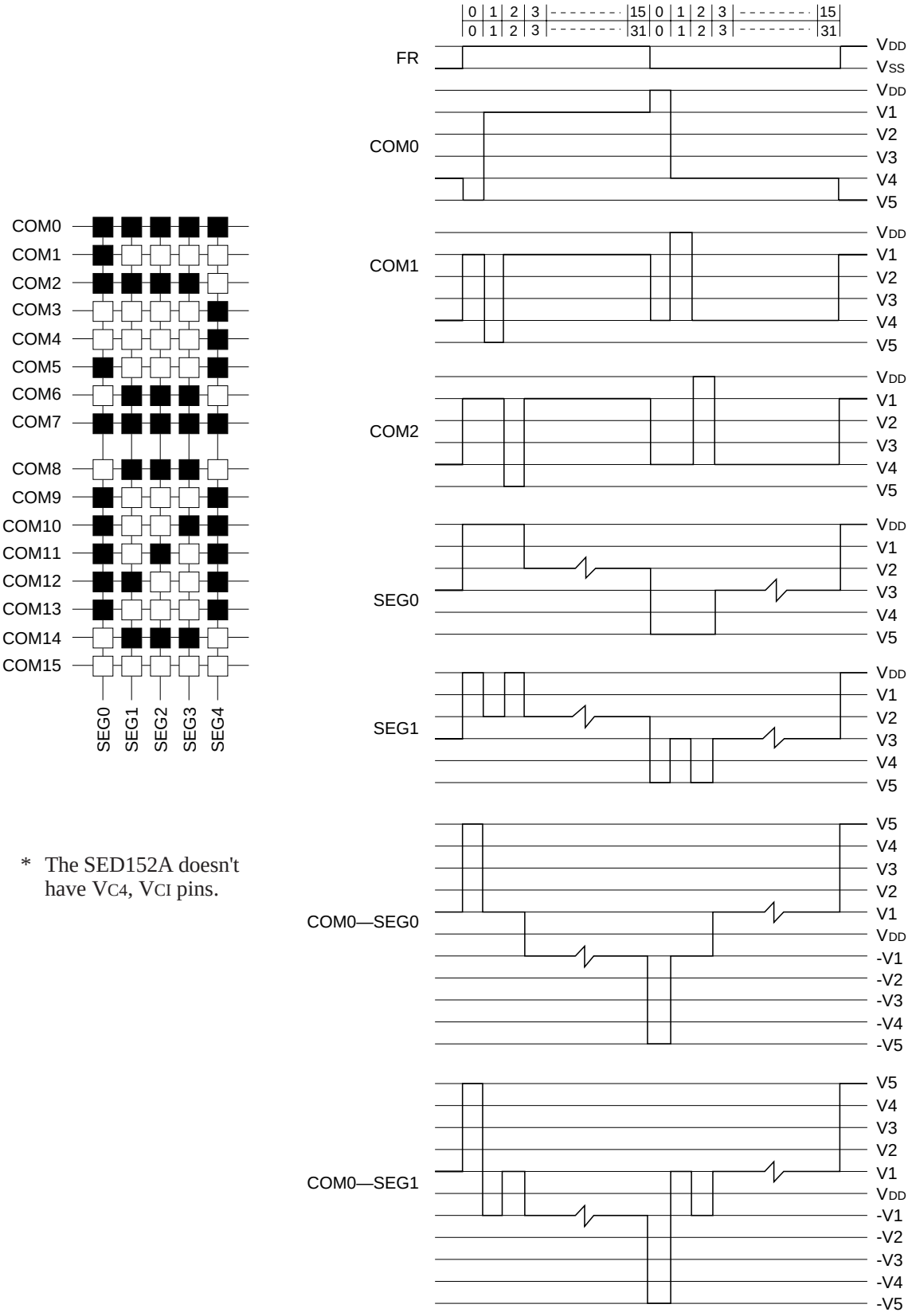
Reset Circuit

This circuit detects the $\overline{RES}$ input rise or fall edge and performs initialization.
$\overline{RES}$ input is level-sensed, then, as shown in Table 1, the MPU interface mode is selected.

When connecting to MPU, the output port of MPU is used and the reset signal is input through software. Otherwise, the circuit is connected to the reset terminal of MPU and the ⎍ reset signal via the inverter is input for 80-system MPU, and the ⎏ reset signal for the 68-system MPU.
$\overline{RES}$ input causes initialization of SEDI52A, and initialization of the MPU is performed at the same time. Failure of initialization by the $\overline{RES}$ terminal upon applying power may lead to a status that cannot be released.
If the reset command is used, items 2 and 5 of the following initial settings are to be executed:

Status in Initial Setting

1. Display OFF
2. To set the display start line register on the first line.
3. Display All Lamps OFF
4. To set the column address counter to address 0.
5. To set the page address counter to the third page.
6. ADC select: normal rotation (ADC command = "0", ADC status flag "1")
7. Read/Modify/Write OFF



* The SED152A doesn't have V_{C4}, V_{CI} pins.

Figure 4 LCD drive waveforms example

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
All-display ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The SED152A identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

This command loads the display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

This command loads the page address register.

A_1	A_0	Page Address
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	(E) $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

All Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: All display on
D=0: All display off

Read-Modify-Write

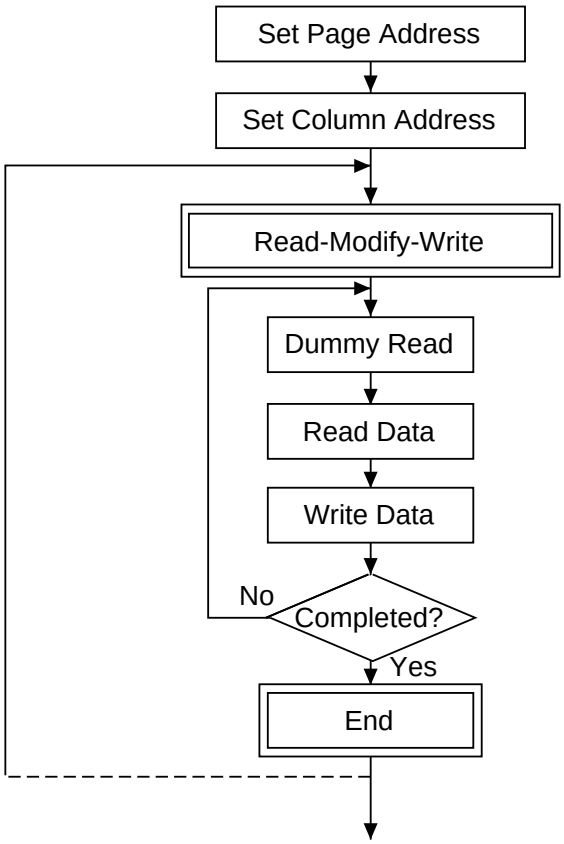
A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

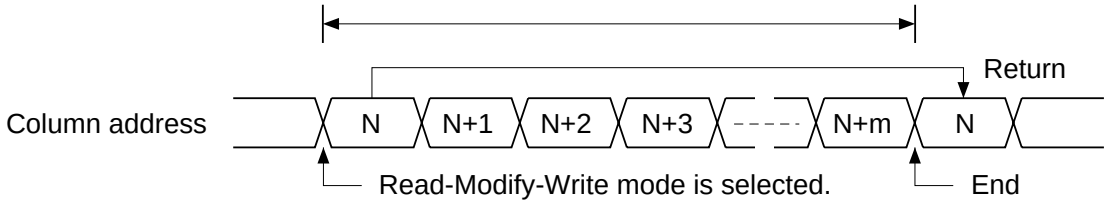
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

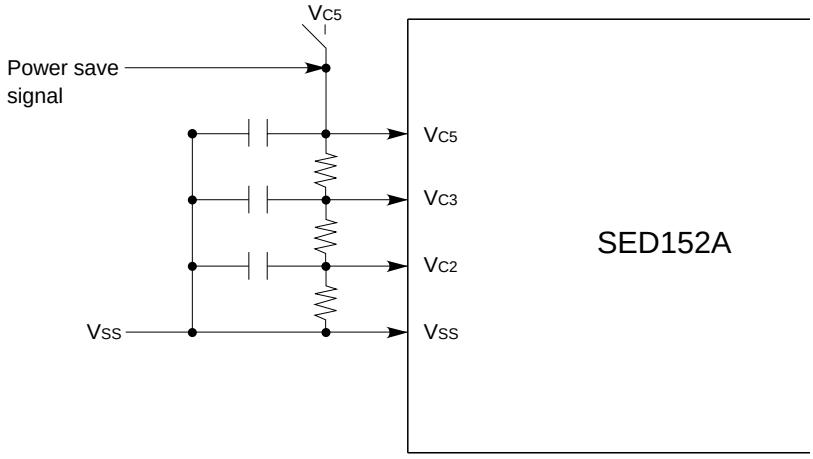
This command clears
- the display start line register.
- and set page address register to 3 page.

  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{C5}	–0.3 to +7.0	V
Supply voltage (3)	V_{C3}, V_{C2}	–0.3 to V_{C5}+3	V
Input voltage	V_{IN}	–0.3 to V_{DD} +0.3	V
Output voltage	V_O	–0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	–40 to +85	deg. C
Storage temperature	T_{stg}	–55 to +125	deg. C

Notes: 1. All voltages are specified relative to V_{SS} = 0 V.
2. The following relation must be always hold
$V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{DD}			4.5	5.0	5.5	V	V_{DD} *1
	Allowable				2.4	—	6.0		
Operating voltage (2)	Allowable	V_{C5}			3.5	—	6.0	V	V_{C5} *2
	Allowable	V_{C3}			0.5×V_{C5}	—	V_{C5}	V	V_{C3}
	Allowable	V_{C2}			V_{SS}	—	0.5×V_{C5}	V	V_{C2}
High-level input voltage		V_{IH}			0.8×V_{DD}	—	V_{DD}	V	*3
		V_{IL}			V_{SS}	—	0.2×V_{DD}	V	*3
		V_{OH1}	I_{OH} = –1 mA		0.8×V_{DD}	—	V_{DD}	V	*4
		V_{OH2}	V_{DD} = –2.7 V I_{OH} = –0.5mA		0.8×V_{DD}	—	V_{DD}	V	*4
Low-level input voltage		V_{OL1}	I_{OL} = 1 mA		V_{SS}		0.2×V_{DD}	V	*4
		V_{OL2}	V_{DD} = 2.7 V I_{OL} = 0.5 mA		V_{SS}		0.2×V_{DD}	V	*4
Input leakage current		I_{L1}			–1.0	—	1.0	µA	*5
Output leakage current		I_{L2}			–3.0	—	3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25 deg. C	V5 = 6.0 V	—	1.3	3.0	kΩ	SEG0 to 79, *7
				V5 = 3.5 V	—	2.5	6.0		

(continued)

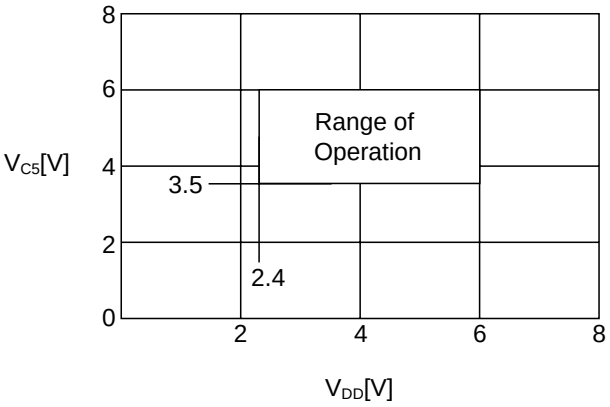
DC Characteristics (Cont'd)

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition	Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Static current dissipation		I_{SSQ}	$\overline{CS}$ = CL = FR = V_{DD}	—	0.01	1.0	µA	V_{SS}
Dynamic current dissipation	During display	I_{SS} (1)	V_{DD} = 5 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	2.0	5.0	µA	V_{SS} *8
			V_{DD} = 3.0 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	1.5	4.5	µA	V_{SS} *8
	During access	I_{SS} (2)	V_{DD} = 5 V t_{cyc} = 200 KHz	—	300	500	µA	V_{SS} *9
			V_{DD} = 3.0 V t_{cyc} = 200 KHz	—	150	300		
Input pin capacitance		C_{IN}	Ta = 25 deg. C, f = 1 MHz	—	5.0	8.0	pF	All input pins

Notes: 1. Although this equipment is capable of withstanding a wide range of operating voltage, it is not designed for withstanding a sudden voltage change while accessing the MPU.

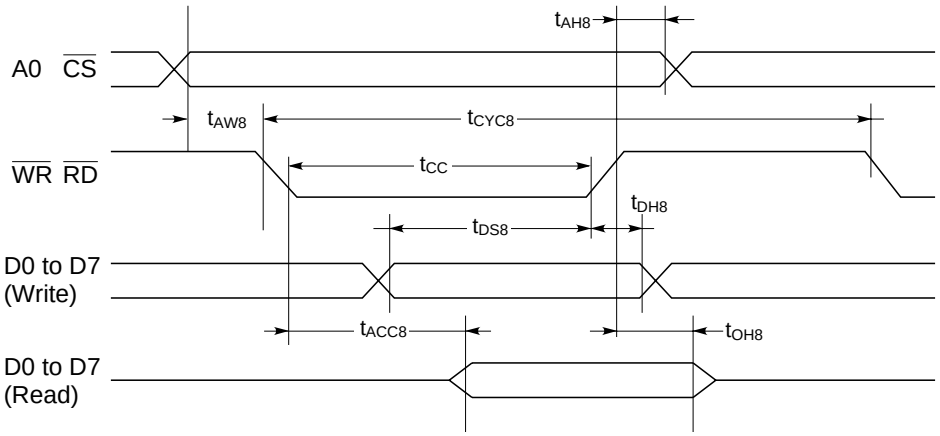
2. Ranges of Operating Voltage for V_{DD} and V_{C5} Systems



3. D0 to D7, A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, (E), $\overline{WR}$, (R/$\overline{W}$), C_L, and FR terminals.
4. D0 to D7 terminals.
5. A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), and C_L terminals.
6. FR, D0 to D7 (in high impedance status) terminals.
7. These are resistance values obtained when voltage of 0.1 V is applied between the output terminals (SEG) and the respective power terminals (V_{C3}, V_{C2}). These are defined within the range of the operating voltage.
8. This is current consumed by a single IC, not including current required by the LCD panel capacity or by the wiring capacity.
9. This indicates current consumption at the time the pattern of vertical stripes is always wrapped in by the tcyc. Current consumption while accessing roughly proportionate to the tcyc for access. If not accessed, only I_{SS1} is relevant.

Timing Characteristics

- System Bus Read/Write Characteristic 1 (80-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 CS	t_{AH8} t_{AW8}	—	10 20	— —	ns ns
System cycle time		WR RD	t_{CYC8}	—	1000	—	ns
Control pulse width	Write		t_{CC}	—	100	—	ns
	Read				200	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	80 10	— —	ns ns
RD access time Output disable time			t_{ACC8} t_{OH8}	C_L = 100 pF	— 10	180 90	ns ns

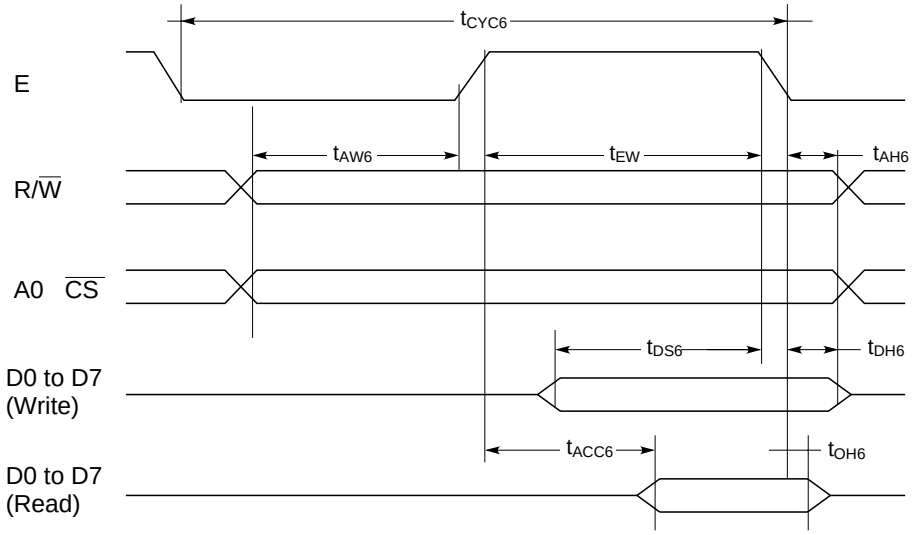
(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 CS	t_{AH8} t_{AW8}	—	20 40	— —	ns ns
System cycle time		WR RD	t_{CYC8}	—	2000	—	ns
Control pulse width	Write		t_{CC}	—	200	—	ns
	Read				400	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	160 20	— —	ns ns
RD access time Output disable time			t_{ACC8} t_{OH8}	C_L = 100 pF	— 20	360 180	ns ns

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• System Bus Read/Write Characteristic 2 (68-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	t_{CYC6}	—	1000	—	ns
Address set-up time Address hold time			t_{AW6} t_{AH6}	—	20 10	— —	ns ns
Data set-up time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	80 10	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L = 100 pF	10	90 180	ns ns
Enable pulse width	Write	E	t_{EW}	—	100	—	ns
	Read				200	—	ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

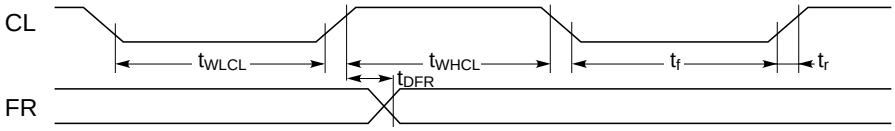
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	t_{CYC6}	—	2000	—	ns
Address set-up time Address hold time			t_{AW6} t_{AH6}	—	40 20	— —	ns ns
Data set-up time Data hold time		D0 to D7	t_{DS6} t_{DH6}	—	160 20	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L = 100 pF	20	180 360	ns ns
Enable pulse width	Write	E	t_{EW}	—	200	—	ns
	Read				400	—	ns

Notes: 1 "t_{CYC6}" represents the cycle of signal E when $\overline{CS}$ = "L". If $\overline{CS}$ = "H" → "L", it is necessary to secure t_{CYC6} after $\overline{CS}$ = "L" is attained.

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Display Control Input Timing



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

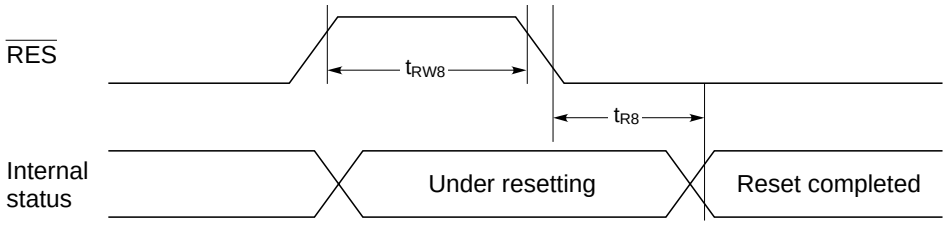
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	35	—	—	µs
High-level pulse width		tWHCL	—	35	—	—	µs
Rise time		tr	—	—	30	150	ns
Fall time		tf	—	—	30	150	ns
FR delay time	FR	tDFR	—	–2.0	0.2	2.0	µs

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	70	—	—	µs
High-level pulse width		tWHCL	—	70	—	—	µs
Rise time		tr	—	—	60	300	ns
Fall time		tf	—	—	60	300	ns
FR delay time	FR	tDFR	—	–4.0	0.4	4.0	µs

Note: All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Reset Input Timing (80-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

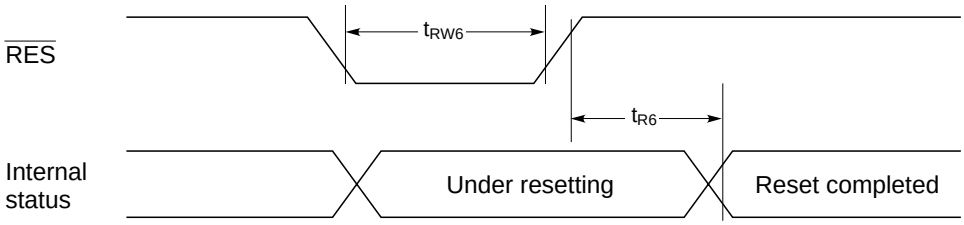
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R8}		2.0	—	—	µs
Reset "H" pulse width	RES	t_{RW8}		1.0	—	—	µs

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R8}		4.0	—	—	µs
Reset "H" pulse width	RES	t_{RW8}		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of V_{DD}.

• Reset Input Timing (68-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R6}		2.0	—	—	µs
Reset "L" pulse width	RES	t_{RW6}		1.0	—	—	µs

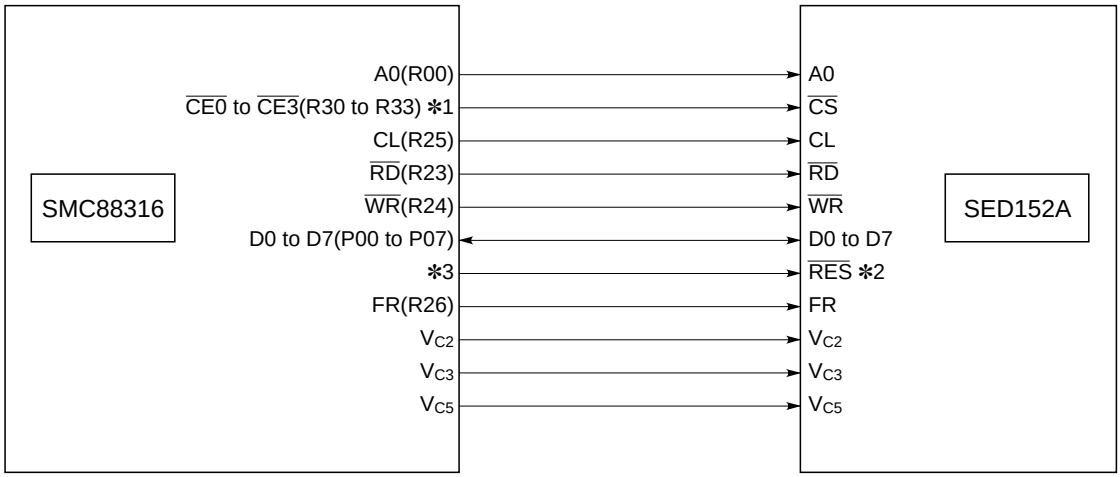
(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_{R6}		4.0	—	—	µs
Reset "L" pulse width	RES	t_{RW6}		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of V_{DD}.

CONNECTION EXAMPLE

MPU Interface (MPU example: SMC88316)



Notes: 1 See SMC88316 technical Manual for the signals of SMC88316.
2 The reset input for 80-system MPU interface of SED152A is the opposite phase of that for the reset input of SMC83315.
3 For the reset input of SED152A, we recommend that you use the output port of SMC88316 and send the reset signals through software.

EXAMPLE OF CONNECTIONS TO LIQUID CRYSTAL PANEL