6. SED1540 Series

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OVERVIEW

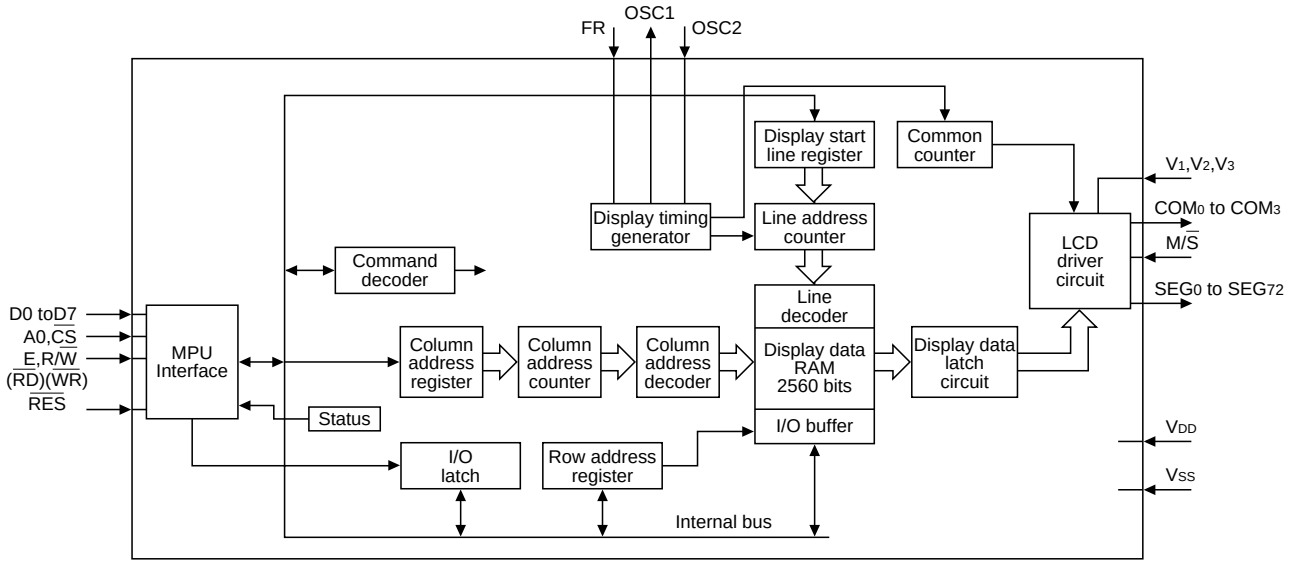
The SED1540 is a segment LCD driver intended for use with medium size LCD panels.
The driver generates LCD drive signals from data supplied by an MPU over a high speed, 8-bit bus, 4-bit bus and stored in its internal display RAM.
The SED1540 incorporates innovative circuit design strategies, to achieve very low power consumption at a wide range of operating voltages, and a rich command set. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

FEATURES

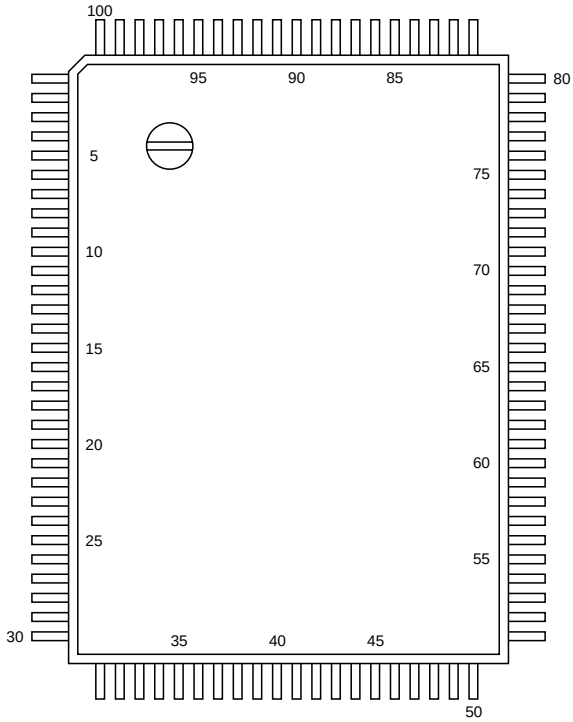
- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Rich command set
- 73 segment drive outputs
- 4 common drive outputs
- Selectable 1/3 or 1/4 duty cycle
- Low power consumption -70 μW maximum
- Wide range of supply voltages, V_{SS} –2.4 V to –7.0 V
- Implemented in CMOS
- Choice of packages
  - —SED1540F0A : 100-pin QFP
  - —SED1540D0A : Aluminum pad chip
  - —SED1540D0B : Gold bump chip

Clock Source	f_{CL}	Frame Frequency
External clock	4 kHz	85/64 Hz
Internal osc.	18 kHz	375/281 Hz

BLOCK DIAGRAM



PACKAGE OUTLINE



PIN OUT

For chip pad locations see section 4.3, Mechanical Specifications.

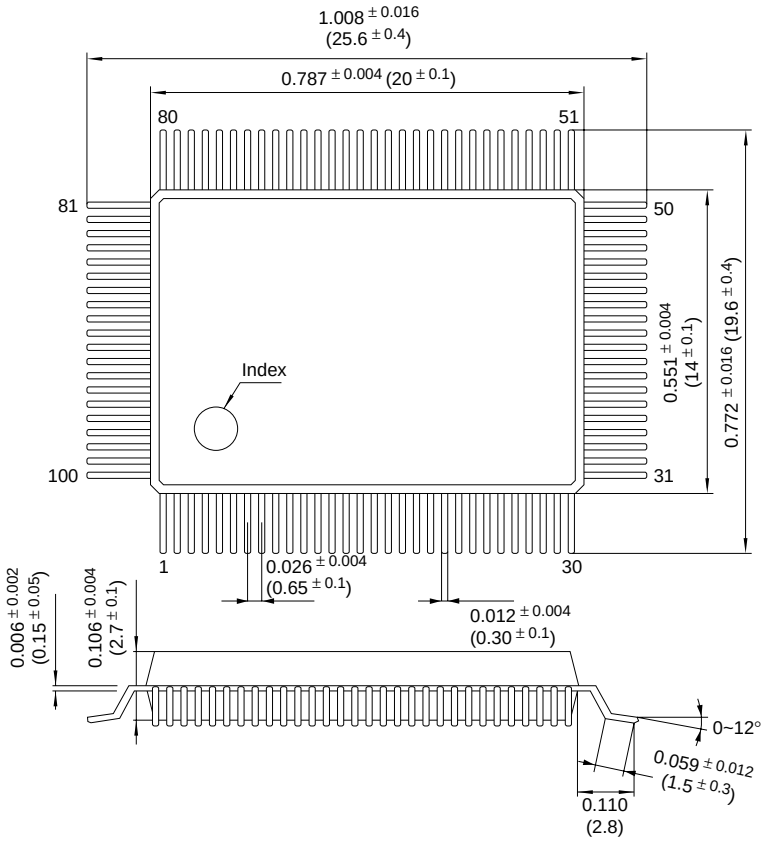
Number	Name	Number	Name	Number	Name	Number	Name
1	SEG71	26	SEG46	51	SEG21	76	E ($\overline{RD}$)
2	SEG70	27	SEG45	52	SEG20	77	R/$\overline{W}$ ($\overline{WR}$)
3	SEG69	28	SEG44	53	SEG19	78	V_{SS}
4	SEG68	29	SEG43	54	SEG18	79	DB0
5	SEG67	30	SEG42	55	SEG17	80	DB1
6	SEG66	31	SEG41	56	SEG16	81	DB2
7	SEG65	32	SEG40	57	SEG15	82	DB3
8	SEG64	33	SEG39	58	SEG14	83	DB4
9	SEG63	34	SEG38	59	SEG13	84	DB5
10	SEG62	35	SEG37	60	SEG12	85	DB6
11	SEG61	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	V_{DD}
13	SEG59	38	SEG34	63	SEG9	88	$\overline{RES}$
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V3
16	SEG56	41	SEG31	66	SEG6	91	$\overline{CS}$
17	SEG55	42	SEG30	67	SEG5	92	NC
18	SEG54	43	SEG29	68	SEG4	93	M/$\overline{S}$
19	SEG53	44	SEG28	69	SEG3	94	V2
20	SEG52	45	SEG27	70	SEG2	95	V1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	SEG72

Duty	Pin	
	98	99
1/4	COM2	COM3
1/3	NC	COM2

Mechanical Specifications

SED1540F0A Flat Pack

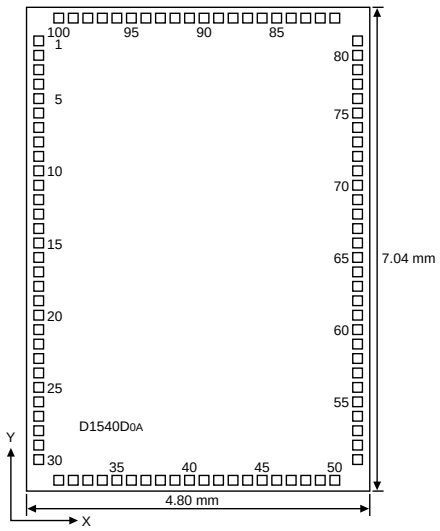
Dimensions: inches (mm)



SED1540D Chip Dimensions

Aluminum pad
- Die size: 4.80 mm × 7.04 mm × 0.525 mm
- Pad size: 100 × 100 µm

Gold bump
- Minimum bump pitch: 199 µm
- Bump height: 20 µm +10/–5 µm
- Bump size: 132 × 111 µm ±20 µm



Pad		X	Y
Number	Name		
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
Number	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
Number	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	OSC1	4641	5247
75	OSC2	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/$\overline{W}$ ($\overline{WR}$)	4641	5846
78	VSS	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V3	2499	6884
91	$\overline{CS}$	2300	6884
92	NC	2100	6884
93	M/$\overline{S}$	1901	6884
94	V2	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	SEG72	504	6884
—	—	—	—
—	—	—	—

PIN DESCRIPTION

System Bus Interface

D0 – D7:
8-bit, tri-state, bi-directional I/O bus
A0:
Data/command select input
- A0=0: Display control data on D0–D7
- A0=1: Display data D0–D7

$\overline{RES}$:
Reset and interface configuration input. The driver is reset on any edge of $\overline{RES}$.
After reset the SED1540F is in the following state
- Display off
- Display startline register: Line 1
- Static drive off
- Column address counter: 0
- Page address register: 0
- Duty cycle: 1/4
- ADC: Forward (ADC command D0 = "0". ADC status flag "1")
- Read-modify-write OFF

In addition the MPU interface is configured by the level of $\overline{RES}$ as given in the table below

$\overline{RES}$	Interface	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
High	68 MPU	↑	↑	↑	↑	↑
Low	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

$\overline{CS}$: Active low chip select input
E or $\overline{RD}$:
- $\overline{RES}$ = 1: Enable clock input
- $\overline{RES}$ = 0: Active low read input. Taking both **$\overline{CS}$** and $\overline{RD}$ inputs low causes the driver to drive the MPU bus.

R/$\overline{W}$ or $\overline{WR}$:
- $\overline{RES}$ = 1: Read/write input
- $\overline{RES}$ = 0: Active low write strobe input. Data is latched into the driver on the falling edge of **$\overline{WR}$**.

LCD Interface

M/$\overline{S}$:
Master/slave driver select input.
- M/$\overline{S}$=1: Master
- M/$\overline{S}$=0: Slave
  The operation is different in master and slave mode as given in the table below.

M/S	COM output	OSC1	OSC2	FR
1	Valid	Input	Output	Output
0	Valid*	NC	Input	Input

Note: Using FR to synchronise master and slave drivers will produce in phase COM outputs.

FR:
LCD AC drive signal input/output.
- M/$\overline{S}$ = 1: Output
- M/$\overline{S}$ = 0: Input

SEG0 to SEG72:
LCD segment (column) driver outputs. The output levels of these pins are given in the table below.

FR	Data	
	1	0
1	V_{DD}	V_2
0	V_3	V_1

COM0 to COM13:
LCD common (row) driver outputs. The output levels of these pins depend on FR and the output of the common counter and are given in the table below.

FR	Counter	
	1	0
1	V_3	V_1
0	V_{DD}	V_2

Oscillator

OSC1:
- M/$\overline{S}$ = 1: Connect the internal oscillator feedback register, R_f, to this pin.
- M/$\overline{S}$ = 0: Leave open.

OSC2:
- M/$\overline{S}$ = 1: Connect the internal oscillator feedback resistor, R_f, to this pin.
- M/$\overline{S}$ = 0: Clock input.

Power Supply

V_{DD}:
+5 V input (0 V ground)
V_{SS}:
0 V ground (-5 V input)
V_1, V_2, V_3:
LCD driver power supply. These voltages must conform to the following relation
$V_{DD} \geq V1 \geq V2 \geq V3$

BLOCK DESCRIPTION

System Bus

Data transfer

The SED1540F driver uses the A0, E (or $\overline{RD}$) and R/W (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table below.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers, all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example, when the MPU executes a read cycle to access display RAM, the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

By using an MPU data bus I/O latch the display data RAM access timing is determined by the driver cycle time, t_{cyc}, not by the RAM access time. In general this strategy leads to faster data transfers between the driver and the MPU.

If the MPU access frequency is likely to exceed $1/t_{cyc}$, then the designer has the choice of inserting NOPs into the access loop or polling the driver, by reading the busy flag, to see if it will accept new data or instructions.

This means that a dummy read cycle has to be executed at the start of every series of reads.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

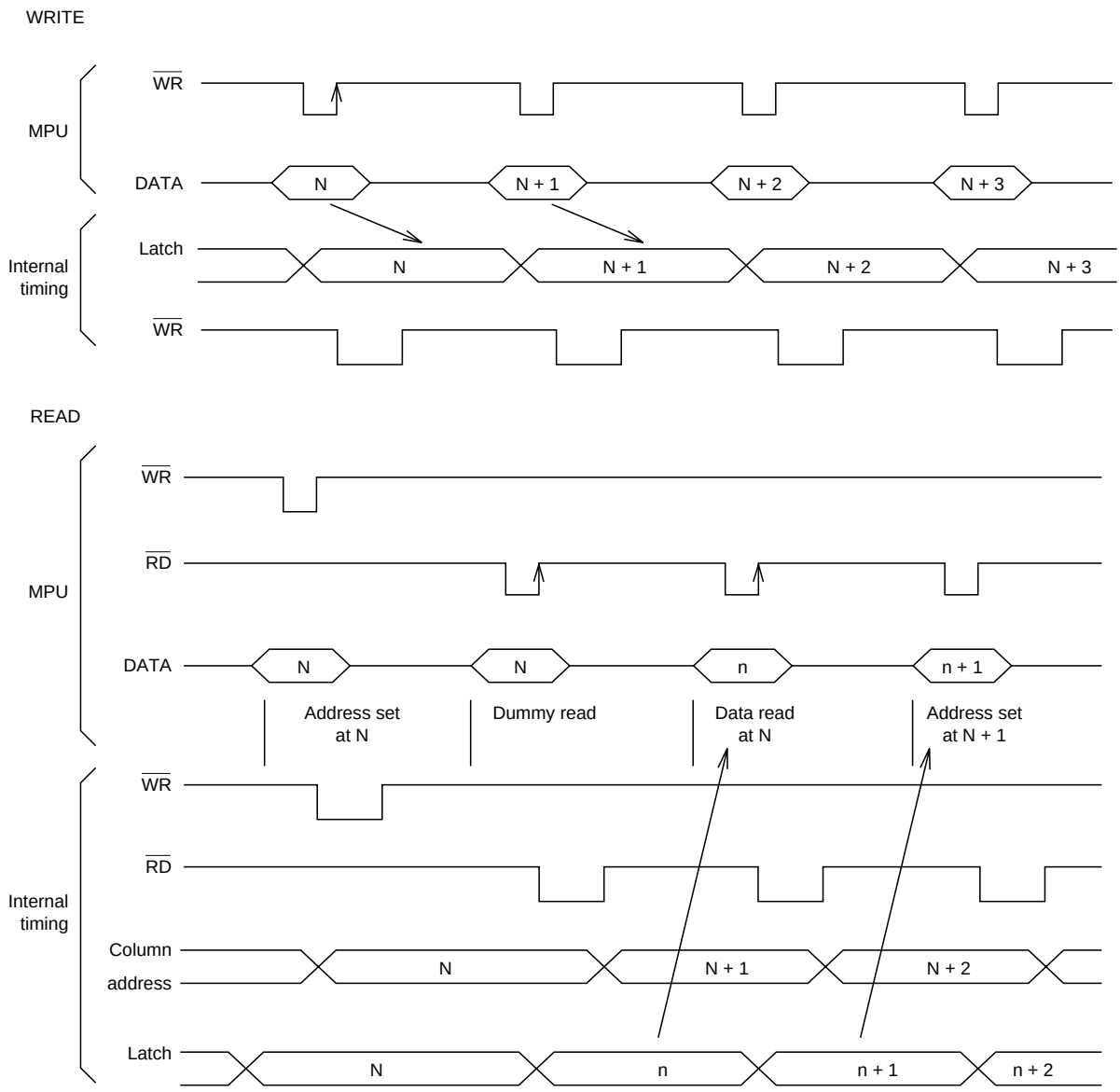


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1540 is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the "Set Display Start Line" command (see section 3).
The contents of the display start-line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data in display data RAM being transferred to the segment driver ciruits.

Column Address Counter

The column address counter is a 7-bit presettable counter which supplies the column address (see figure 2) for MPU accesses to the display data RAM. The counter is incremented by one every time the driver receives a Read or Write Display Data Command.
Addresses above 50 H are invalid, and the counter will not increment past this valu. The contents of the column address conter are set with the Set Column Address command.

Page Register

The page register is a 2-bit register which supplies the page address (see figure 2) for MPU accesses to the display data RAM. The contents of the Page Register are set by the Set Page Register Command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in figure 2.

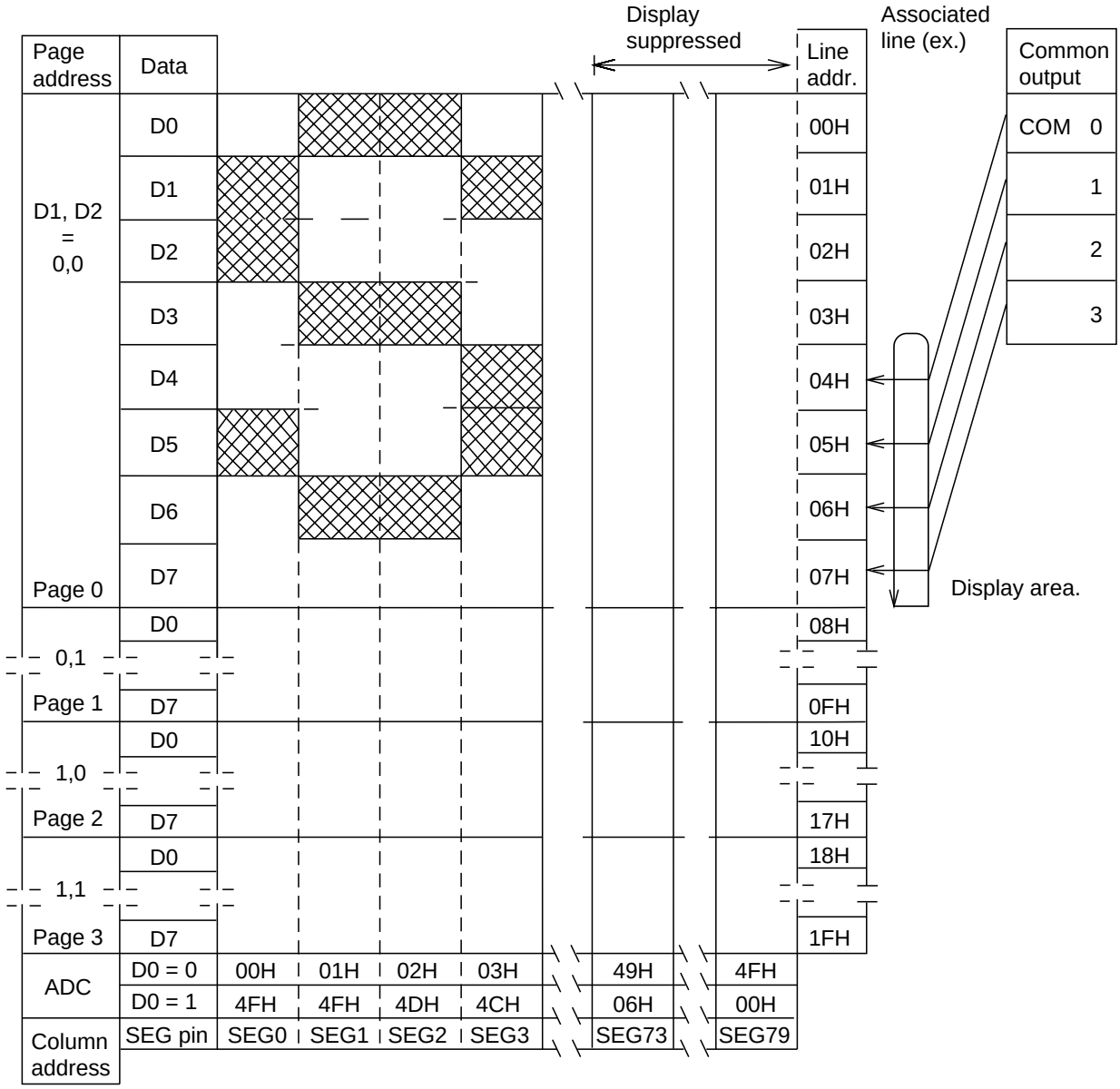


Figure 2 Display Data RAM Addressing

Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock CL. The "Select Duty Cycle" command selects a duty cycle of 1/3 or 1/4.

Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the "Display ON/OFF" and "Static Driver ON/OFF" commands.

LCD Drive Circuit

The LCD driver circuitry generates the 77 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

Display Timing Generator

This circuit generates the internal display timing signal using the basic clock OSC1, and the frame signal, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. OSC1 is used to lock the line counter to the system line scan rate.

Oscillation Circuit

The oscillator is a low power RC oscillator whose frequency of oscillation is determined by the value of the feedback resistor R_f or an externally generated 50% duty cycle clock input via OSC1. If a slave SED1540F is used, its OSC2 input is connected to the OSC2 output of the master driver.

Reset Circuit

This circuit senses both the edge and the level of the signal at the $\overline{RES}$ pin and uses this information to

- Initialization status

1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 0.
6. 1/4 duty is selected.
7. Forward ADC is selected (ADC command D0 is 0 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.

When the Reset command is issued, initialization items 2, 4 and 5 above are executed.

As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.

If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF *
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 72)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: busy 0: Ready ADC 1: Forward 0: Reverse ON/OFF 1: Display off 0: Display on RESET 1: being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: Forward, 1: Reverse
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/4, 0: 1/3
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address register by 1 druing write only.
End	0	1	0	1	1	1	0	1	1	1	0	Read modify write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Sets the display start line register to line 1, and sets the column address counter and page address register to 0.

* The Power Save mode is selected if the static drive is turned ON when the display is OFF.

Command Description

Display ON/OFF

Table 3 is the command table. The SED1540 identifies a data bus using a combination of A0 and R/$\overline{W}$ ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.
D=1: Display ON
D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The BUSY bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver n.
- The ON/OFF bit indicates the current status of the display.
  ON/OFF=1: Display OFF
  RESET=0: Display ON
- The RESET bit indicates whether the driver is executing a reset or is in normal operating mode.
  RESET=1: Currently executing reset command
  RESET=0: Normal operation

Write Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM at a location specified by the contents of the column address and page address registers, and increments the column address register by one.

Read Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O buffer with display data from the display data RAM location specified by the contents of the column address and page address registers and increments the column address register.
After loading a new address into the column address register, one dummy read is required before valid data is obtained.

Select ADC

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

Selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICS and routing of traces during printed circuit board design. See figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

Sets the duty cycle of the LCD drive.
D=1: 1/4 duty cycle
D=0: 1/3 duty cycle

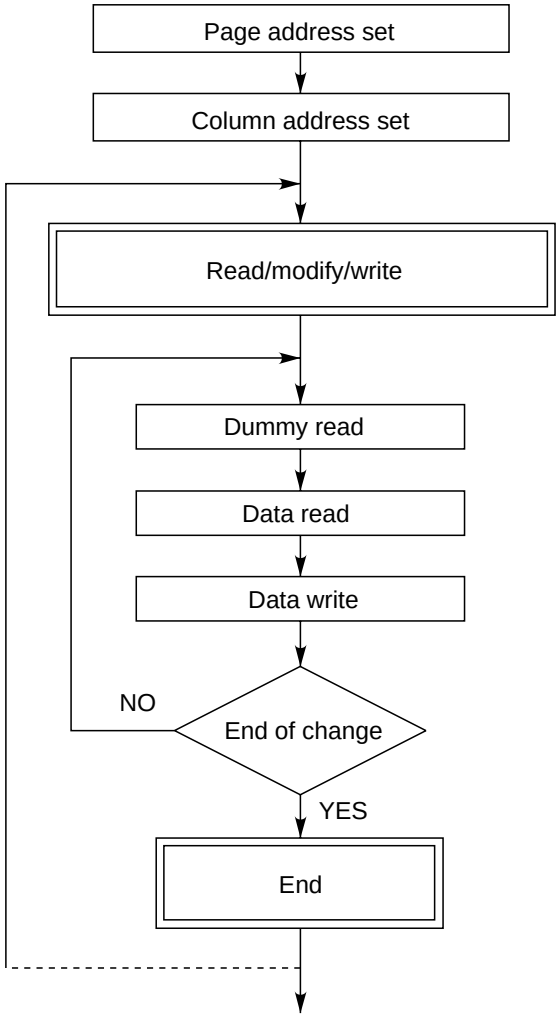
Read-Modify-Write

This command is used in combination with the End command. Once the Read-Modify-Write command is entered, the column address is incremented by 1 only by the display data write command but not incremented by the display data read command. This status is kept until the End command is entered.
When the End command is entered, the column address is returned to the column address when the Read-Modify-Write command is entered. This function can reduce the load of MPU when it repeatedly changes data of the specific display area such as a blinking cursor.

A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

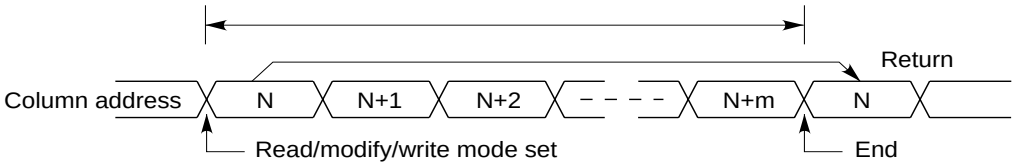
* Any command other than data read and write can be used during the Read-Modify-Write mode. However, the Column Address Set command cannot be used.

Sequence when the cursor is displayed



End

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH



Cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the read-modify-write command.

Reset

This command resets the display start line register, column address counter, and page address register to their initial status. This command does not affect on the display data RAM. For details, see the Reset circuit of the functional block explanation.

The counter and registers are reset after the Reset command has been entered.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

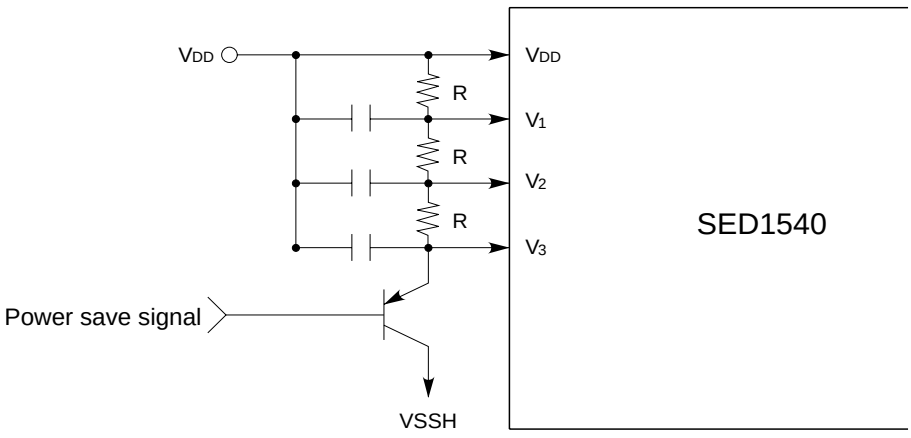
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (compound command)

The system enters the power save state by switching the static drive on in the display off state, reducing the consumed current almost to static current. The internal state in the power save state is as follows:

- The LCD drive is stopped, and the segment and common drivers output the V_{DD} level.
- Oscillating external clock entry is inhibited, and OSC2 becomes floating.
- The display data and the operation mode are held.

The power save state can be canceled by switching the display on or static drive off.
When the LCD drive voltage level is supplied by an externally-equipped resistance dividing circuit, the current flowing through the resistor must be cut by means of the power save signal.



SPECIFICATIONS

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage (1)		V_{SS}	–8.0 to +0.3	V
Supply voltage (2)		V_3	–15.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3	V3 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Power dissipation		P_D	250	mW
Operating temperature		T_{opr}	–40 to +85	deg. C
Storage temperature	QFP	Tstg	–65 to +150	deg. C
	chip		–55 to +125	
Soldering temperature × time (at lead)		T_{sol}	260, 10	deg. C, s

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must always hold $V_{DD} \geq V_1 \geq V_2 \geq V_3$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

(Ta = –20 to 75 deg. C, V_{DD} = 0 V)

Parameter		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_3			–11.0	—	–3.5	V	V_3, See note 10.
	Allowable				–11.0	—	–2.7		
	Allowable	V_1			0.6×V_3	—	V_{DD}	V	V_1
	Allowable	V_2			V_3	—	0.4×V_3	V	V_2
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		See note 3
Low-level input voltage		V_{ILT}			V_{SS}	—	V_{SS}+0.8	V	See note 2
		V_{ILC}			V_{SS}	—	0.8×V_{SS}		See note 3
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	See note 4
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		See note 5
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		OSC2
Low-level output voltage		V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	See note 4
		V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		See note 5
		V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		OSC2
Input leakage current		I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current		I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistor		R_{ON}	Ta = 25 deg. C	V_3 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 72, COM0 to 3. See note 11.
				V_3 = –3.5 V	—	10.0	50.0		
Static current dissipation		I_{DD0}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}

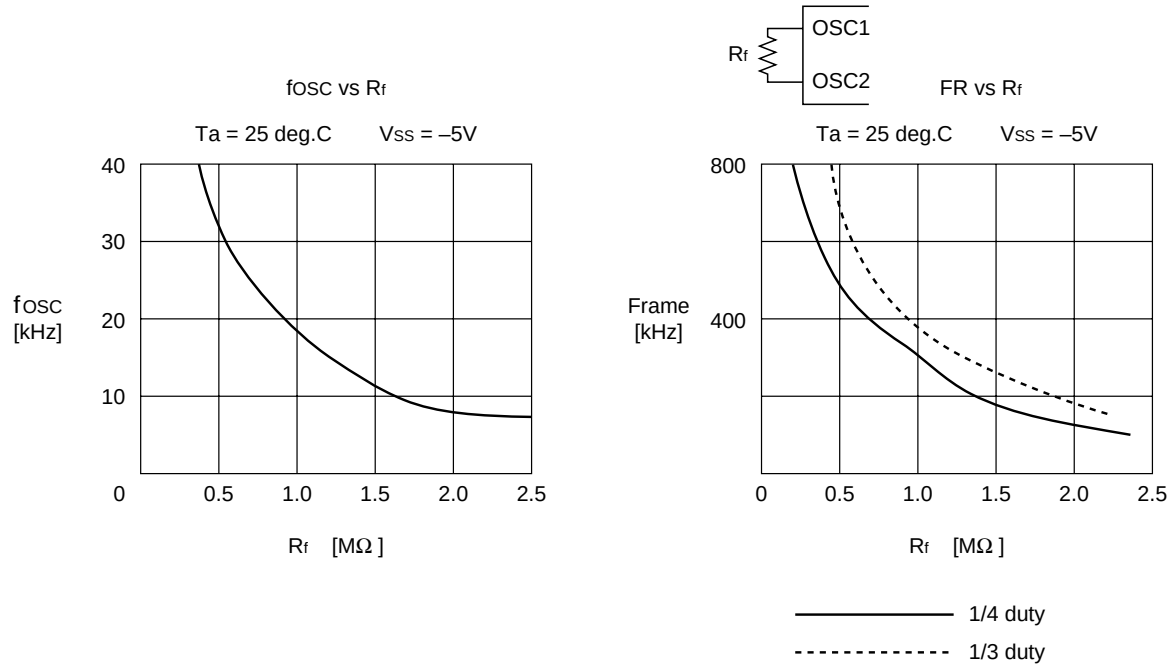
DC Characteristics (Cont'd)

(Ta = –20 to 75 deg. C, V_{DD} = 0 V)

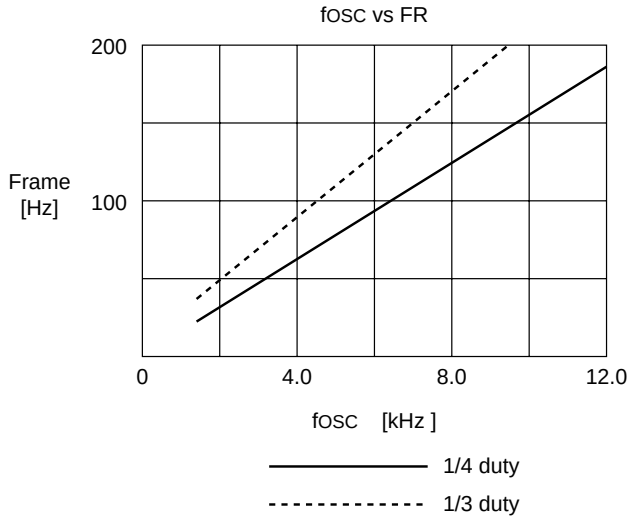
Parameters	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Dynamic current dissipation	I_{DD} (1)	During display	f_{OSC} = 4 kHz	—	1.5	4.0	µA	V_{DD}
		V_3 = –5.0 V	R_f = 1 MΩ	—	9.5	15.0		
	I_{DD} (2)	During assess fcyc = 200 kHz		—	300	500		See note 8.
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	R_f = 1.0 MΩ ±2%, Vss=-5.0V		15	18	21	kHz	See note 9.
		R_f = 1.0 MΩ ±2%, Vss=–5.0V		11	16	21		
Reset time	t_R			1.0	—	1000	µS	$\overline{RES}$

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL and M/$\overline{S}$, $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write access at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V_1, …, V_2) and output (COM, SEG) pins. All voltages within specified operating voltage range.

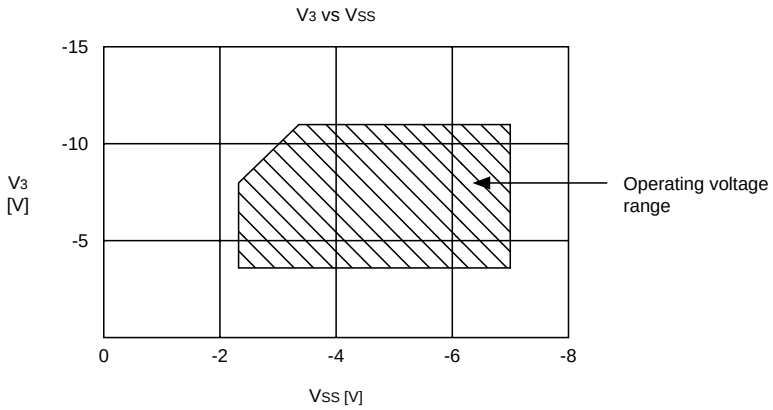
Relationship between f_{OSC}, f_{FR} and R_f



Relationship between f_{CL} and FR

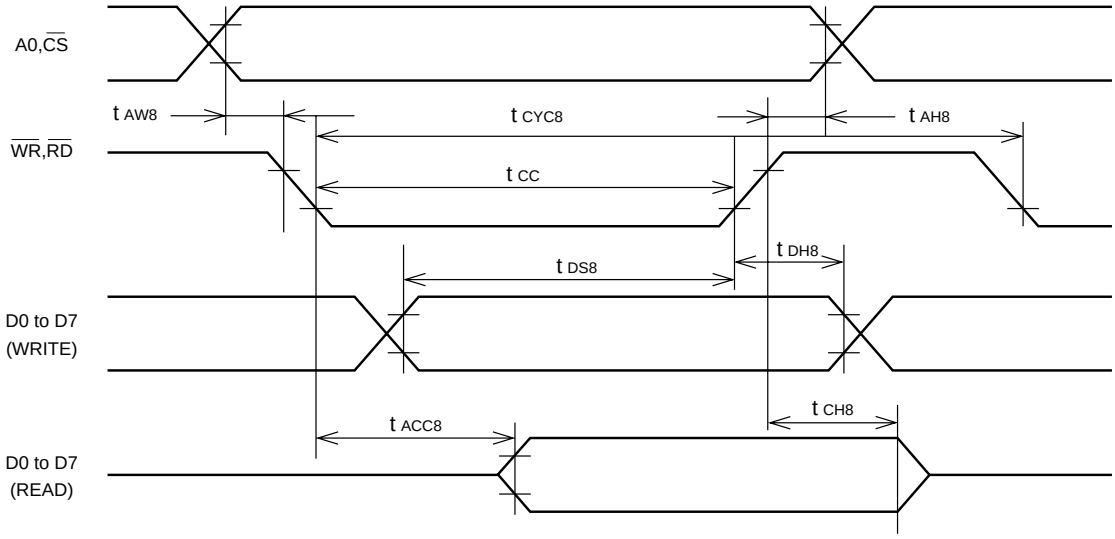


Operating bounds on Vss and V3



AC Characteristics

- MPU Bus Read/Write I (80-family MPU)

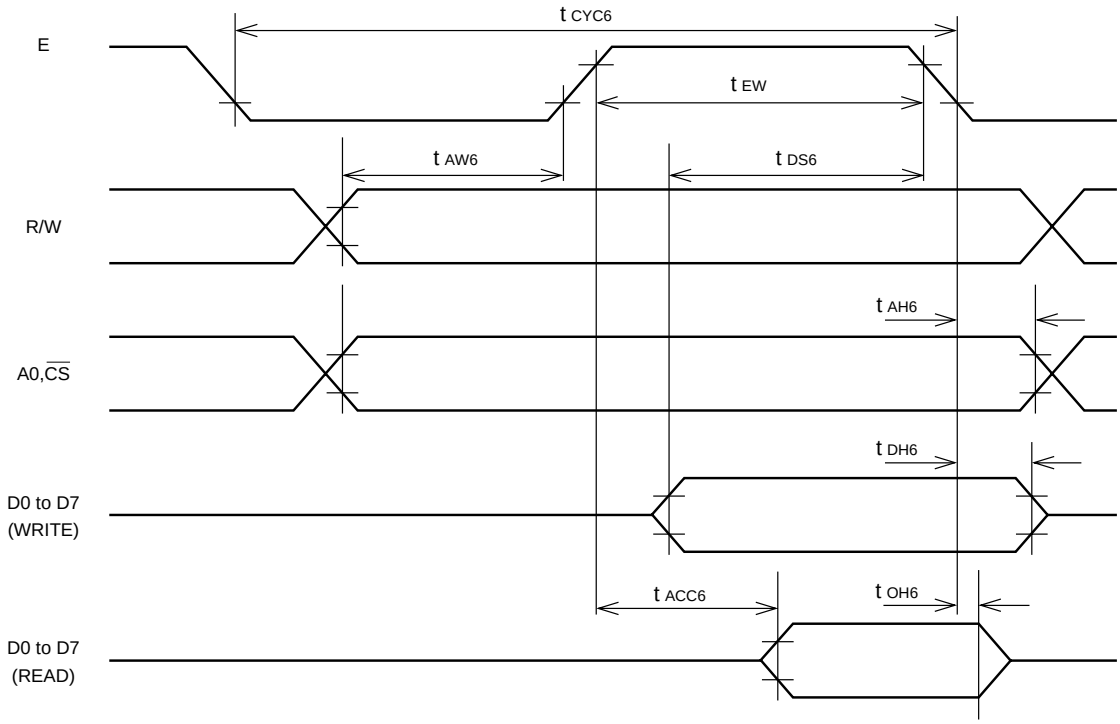


(Ta = –20 to 75 deg. C, Vss = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		10	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		20	—	ns	
System cycle time	t_{CYC8}		1000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	t_{CC}		200	—	ns	
Data setup time	t_{DS8}		80	—	ns	D0 to D7
Data setup time	t_{DH8}		10	—	ns	
$\overline{RD}$ access time	t_{ACC8}	C_L = 100 pF	—	90	ns	
Output disable time	t_{CH8}		10	60	ns	

Notes: 1. All parameter values for a Vss of –3.0 V are about 100% up of their value for a Vss of –5.0 V.
2. All inputs must have a rise and fall time of less than 15 ns.

• MPU Bus Read/Write II (68-family MPU)

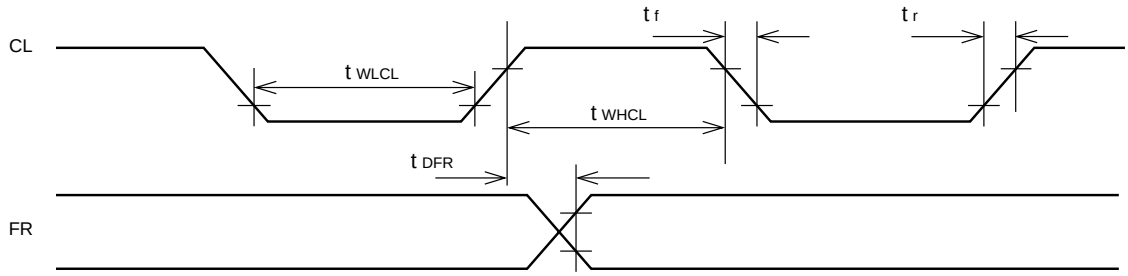


(Ta = –20 to 75 deg. C, Vss = –5 V ±10%)

Parameters		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		t_{CYC6}		1000	—	ns	A0, $\overline{CS}$, R/W
Address setup time		t_{AW6}		20	—	ns	
Address hold time		t_{AH6}		10	—	ns	
Data setup time		t_{DS6}		80	—	ns	D0 to D7
Data hold time		t_{DH6}		10	—	ns	
Output disable time		t_{OH6}	C_L = 100 pF	10	60	ns	
Access time		t_{ACC6}		—	90	ns	
Enable pulse width	Read	t_{EW}		100	—	ns	E
	Write			8	—	ns	

Notes: 1. t_{cyc6} is the cycle time of $\overline{CS}$.E, not the cycle time of E.
2. All parameter values for a Vss of –3.0 V are about 100% up of their value for a Vss of –5.0 V.
3. All inputs must have a rise and fall time of less than 15 ns.

• Display Control Signal Timing



Input

(Ta = –20 to 75 deg. C, Vss = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	t_{WLCL}		35	—	—	µs	CL
High-level pulse width	t_{WHCL}		35	—	—	µs	
Rise time	t_r		—	30	150	ns	
Fall time	t_f		—	30	150	ns	
FR delay time	t_{DFR}		–2.0	0.2	2.0	µs	FR

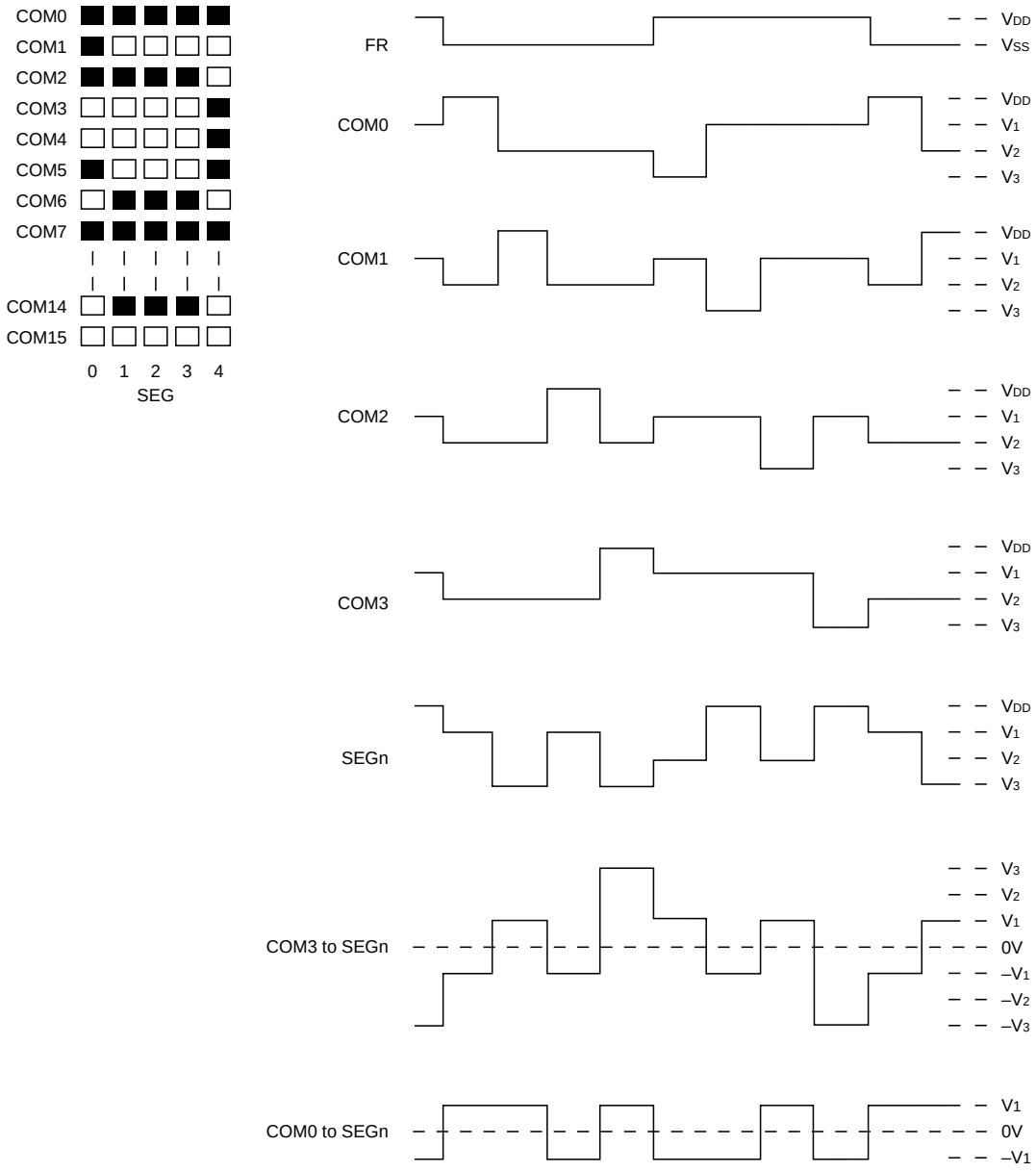
Output

(Ta = –20 to 75 deg. C, Vss = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	C_L = 100 pF	—	0.2	0.4	µs	FR

Notes: 1. The listed input t_{DFR} applies to the SED1540 in slave mode. The listed output t_{DFR} applies to the SED1540 in master mode.
2. All parameter values for a Vss of –3.0 V are about 100% up of their value for a Vss of –5.0 V.

Example Drive Waveforms (1/3 Bias, 1/4 duty)



APPLICATION NOTES

The Oscillator

The external feedback resistor, Rf, is connected as shown in figure 3.

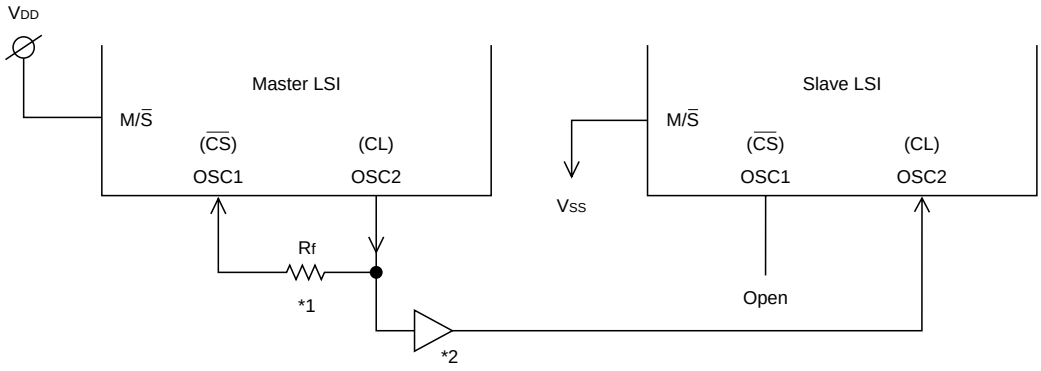
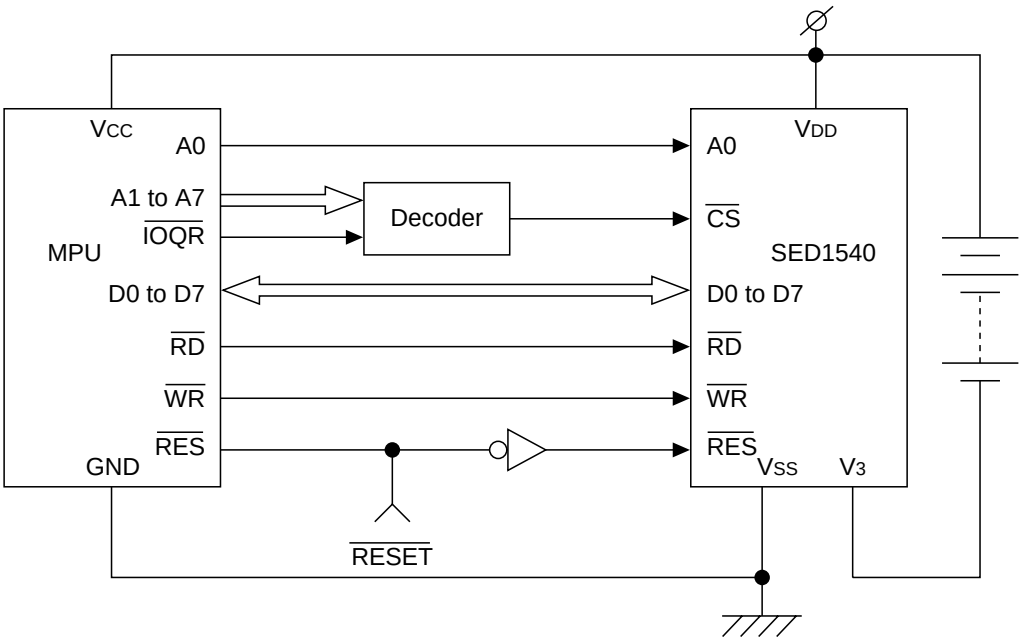


Figure 3 External Rf Connection

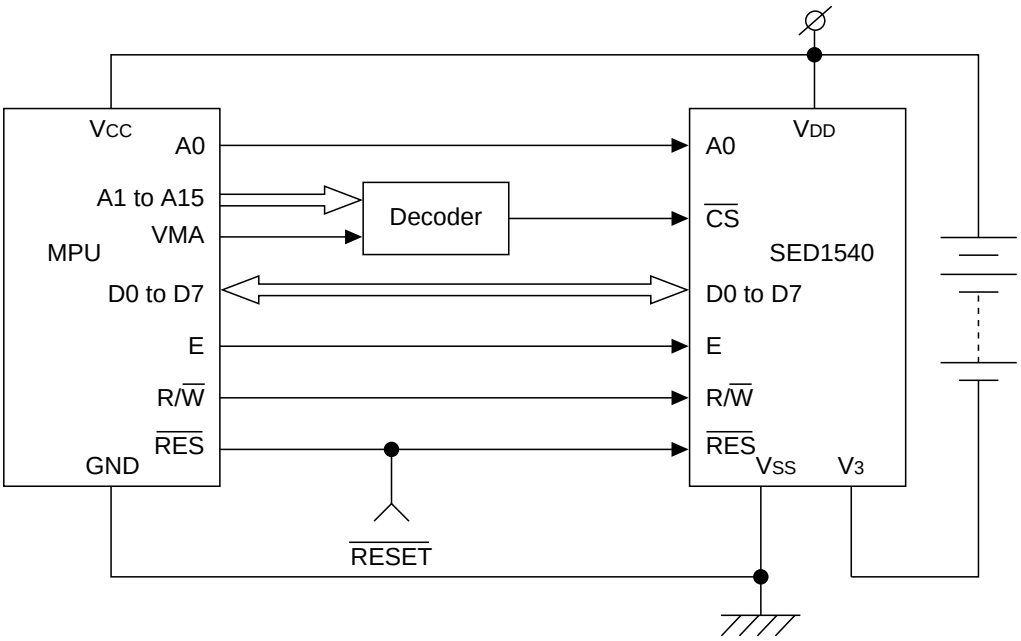
Notes: 1. Parasitic capacitance in the feedback loop will decrease fOSC. The leads of the feedback resistor, Rf, must be kept as short as possible. It may be necessary to reduce Rf to keep fOSC within its specified limits.
2. If a system has two or more slave drivers, a CMOS buffer will be required.

MPU Interface Configuration

80 Family MPU

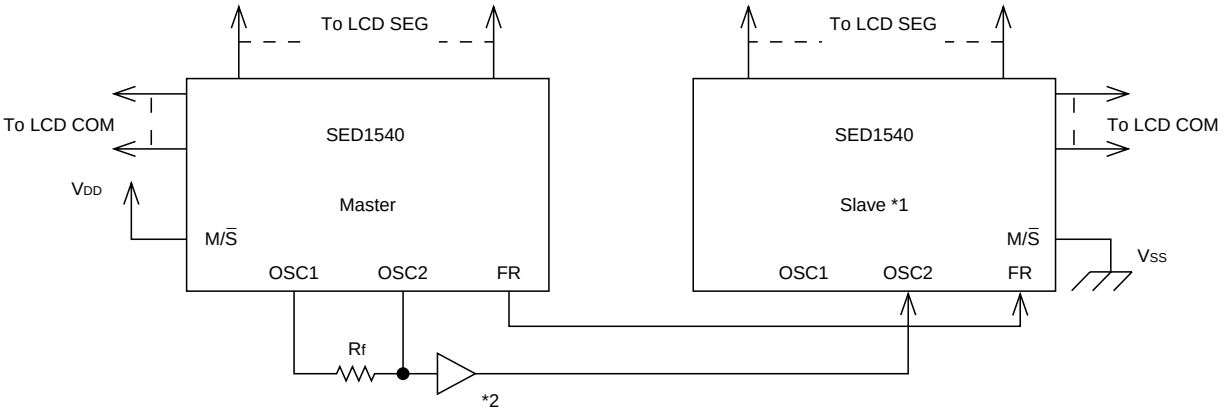


68 Family MPU

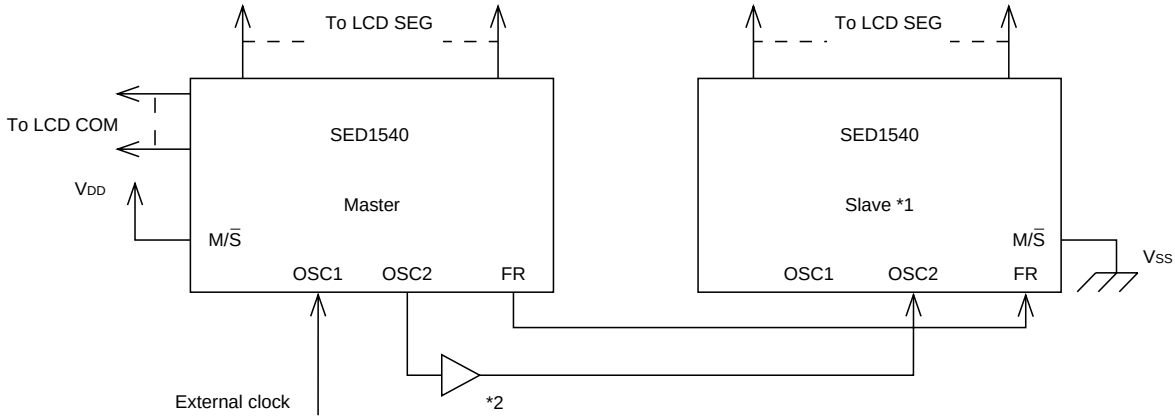


LCD Drive Interface Configuration

SED1540 - SDE1540 (Internal Oscillator)



SED1540 - SED1540 (External clock)



Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

Panel Interface Configuration