9. SED1570 Series

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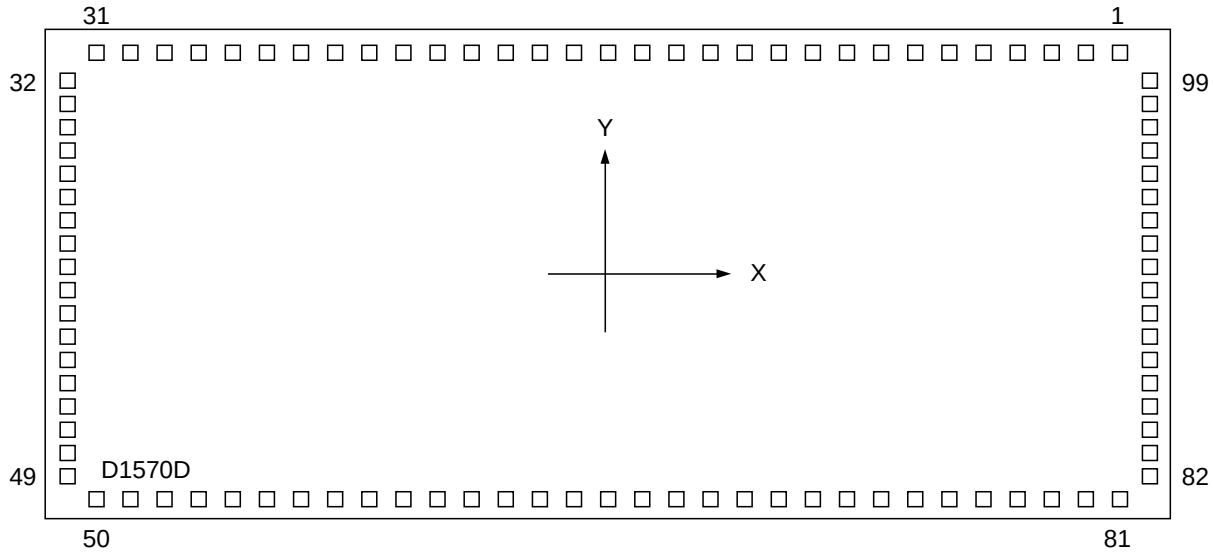
GENERAL DESCRIPTION

The SED1570 is an 80 output segment (column) driver with an internal display RAM. This drive is suitable for driving a dot matrix LCD panel; from a mid-range capacity dot matrix LCD panel to a CGA class dot matrix LCD panel. This device is used with the SED1635.
The display data is stored in the internal display RAM and an LCD panel drive signal is generated. As a result, this device allows configuration of an ultra low power display system since the display data is not transferred unless the display is changed.
In addition, the logic power is low voltage; a wide range of applications is possible.

FEATURES

- Display duty cycle: 1/64 – 1/200
- LCD driver output: 80 out
- Internal display RAM: 200 × 80 bits
- Slim chip
- Ultra low power consumption
- Power $V_{DD} - V_{SS}$ 2.7 V to 5.5 V
  $V_{DD} - V_{EE}$ 8.0 V to 20 V
- High speed and low power date transfer by the 4-bit bus enables chain method
- Non-bias display off function
- Output shift direction-pin selection
- Adjustable LCD power offset bias for V_{DD} level
- Package Chip SED1570D0A (Al pad)
  SED1570D0B (Au bump)

PAD DIMENSIONS



Chip Size	8.04 mm × 3.51 mm
Pad Center Size	100 µm × 100 µm
Pad Pitch	170 µm (Min.)
Chip Thickness	400 µm ±25 µm (Al Pad)
Bump Size	92 µm × 82 µm
Pump Pitch	170 µm (Min.)
Chip Thickness	525 µm
Bump Height	17~28 µm (reference)

PAD COORDINATES

SED1570 Pad Center Coordinates (Al-pad)

Unit: μm

PAD No	PIN Name	X	Y
1	X 75	3640	1595
2	X 76	3432	1595
3	X 77	3224	1595
4	X 78	3016	1595
5	X 79	2808	1595
6	X 80	2600	1595
7	EIO2	2340	1595
8	V_{DD}	2080	1595
9	SHL	1820	1595
10	D_0	1560	1595
11	D_1	1300	1595
12	D_2	1040	1595
13	D_3	780	1595
14	YD	520	1595
15	V_{EE}	260	1595
16	V_5	0	1595
17	V_3	–260	1595
18	V_2	–520	1595
19	V_0	–780	1595
20	FR	–1040	1595
21	XSCL	–1300	1595
22	$\overline{DOFF}$	–1560	1595
23	LP	–1820	1595
24	V_{SS}	–2080	1595
25	EIO1	–2340	1595
26	X 1	–2600	1595
27	X 2	–2808	1595
28	X 3	–3016	1595
29	X 4	–3224	1595
30	X 5	–3432	1595
31	X 6	–3640	1595
32	X 7	–3862	1452
33	X 8	–3862	1282
34	X 9	–3862	1112
35	X 10	–3862	942
36	X 11	–3862	772
37	X 12	–3862	602
38	X 13	–3862	432
39	X 14	–3862	262
40	X 15	–3862	92

PAD No	PIN Name	X	Y
41	X 16	–3862	–78
42	X 17	–3862	–248
43	X 18	–3862	–418
44	X 19	–3862	–588
45	X 20	–3862	–758
46	X 21	–3862	–928
47	X 22	–3862	–1098
48	X 23	–3862	–1268
49	X 24	–3862	–1438
50	X 25	–3641	–1595
51	X 26	–3406	–1595
52	X 27	–3171	–1595
53	X 28	–2936	–1595
54	X 29	–2701	–1595
55	X 30	–2466	–1595
56	X 31	–2231	–1595
57	X 32	–1996	–1595
58	X 33	–1761	–1595
59	X 34	–1526	–1595
60	X 35	–1291	–1595
61	X 36	–1056	–1595
62	X 37	–821	–1595
63	X 38	–586	–1595
64	X 39	–351	–1595
65	X 40	–116	–1595
66	X 41	119	–1595
67	X 42	354	–1595
68	X 43	589	–1595
69	X 44	824	–1595
70	X 45	1059	–1595
71	X 46	1294	–1595
72	X 47	1530	–1595
73	X 48	1765	–1595
74	X 49	2000	–1595
75	X 50	2235	–1595
76	X 51	2470	–1595
77	X 52	2705	–1595
78	X 53	2940	–1595
79	X 54	3175	–1595
80	X 55	3410	–1595

PAD No	PIN Name	X	Y
81	X 56	3645	–1595
82	X 57	3862	–1438
83	X 58	3862	–1268
84	X 59	3862	–1098
85	X 60	3862	–928
86	X 61	3862	–758
87	X 62	3862	–588
88	X 63	3862	–418
89	X 64	3862	–248
90	X 65	3862	–78
91	X 66	3862	92
92	X 67	3862	262
93	X 68	3862	432
94	X 69	3862	602
95	X 70	3862	772
96	X 71	3862	942
97	X 72	3862	1112
98	X 73	3862	1282
99	X 74	3862	1452

(Au-bump) Unit: μm

PAD No	PIN Name	X	Y
1	X 75	3640	1601
2	X 76	3432	
3	X 77	3224	
4	X 78	3016	
5	X 79	2808	
6	X 80	2600	
7	EIO2	2340	
8	V_{DD}	2080	
9	SHL	1820	
10	D_0	1560	
11	D_1	1300	
12	D_2	1040	
13	D_3	780	
14	YD	520	
15	V_{EE}	260	
16	V_5	0	
17	V_3	–260	
18	V_2	–520	
19	V_0	–780	
20	FR	–1040	
21	$\overline{XSCL}$	–1300	
22	$\overline{DOFF}$	–1560	
23	LP	–1820	
24	V_{SS}	–2080	
25	EIO1	–2340	
26	X 1	–2600	
27	X 2	–2808	
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53	X 28	–2936	
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55	X 30	–2466	
56	X 31	–2231	
57	X 32	–1996	
58	X 33	–1761	
59	X 34	–1526	
60	X 35	–1291	
61	X 36	–1056	
62	X 37	–821	
63	X 38	–586	
64	X 39	–351	
65	X 40	–116	
66	X 41	119	
67	X 42	354	
68	X 43	589	
69	X 44	824	
70	X 45	1059	
71	X 46	1294	
72	X 47	1530	
73	X 48	1765	
74	X 49	2000	
75	X 50	2235	
76	X 51	2470	
77	X 52	2705	
78	X 53	2940	
79	X 54	3175	
80	X 55	3410	

PAD No	PIN Name	X	Y
81	X 56	3645	–1601
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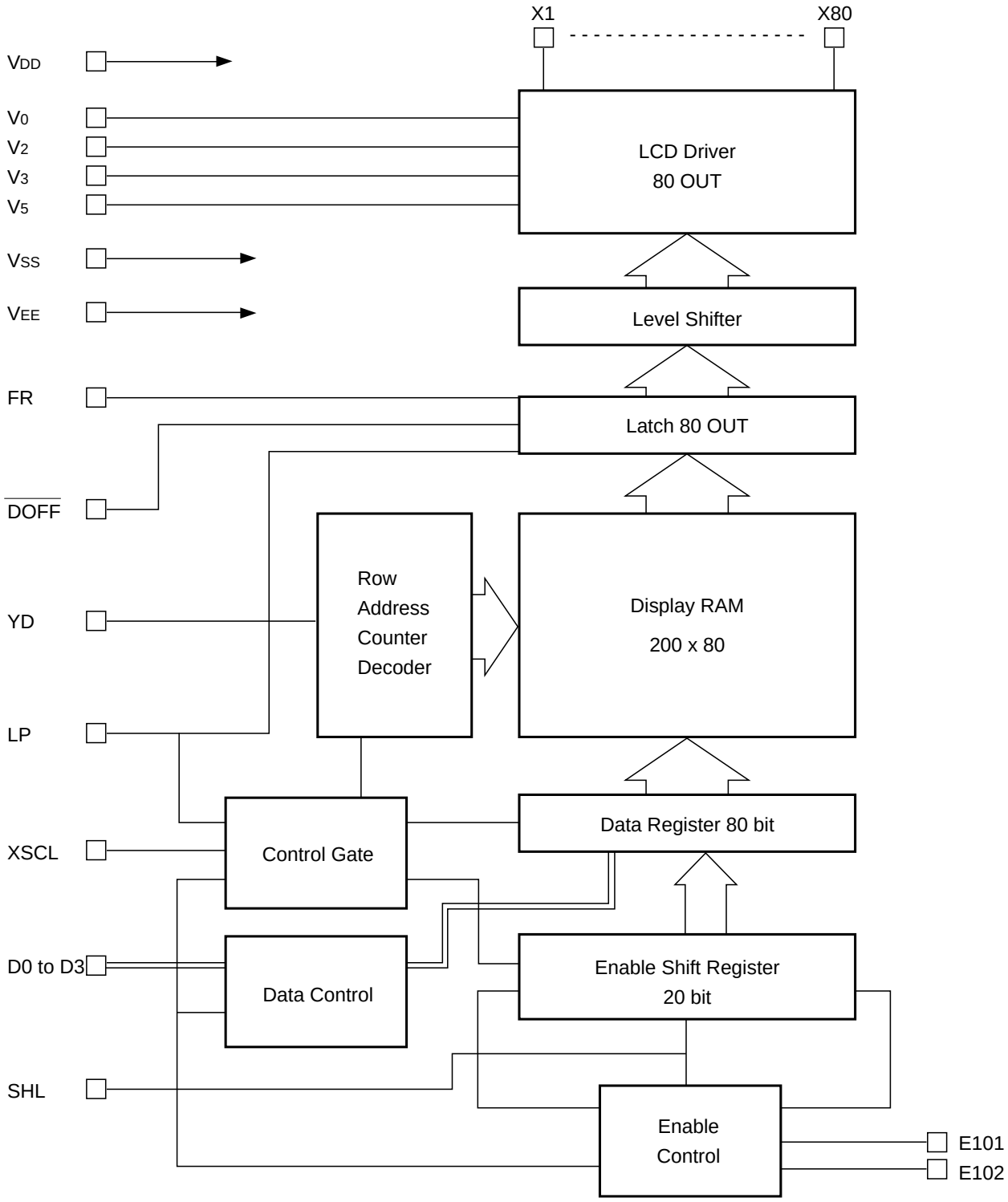
83	X 58		–1268
84	X 59		–1098
85	X 60		–928
86	X 61		–758
87	X 62		–588
88	X 63		–418
89	X 64		–248
90	X 65		–78
91	X 66		92
92	X 67		262
93	X 68		432
94	X 69		602
95	X 70		772
96	X 71		942
97	X 72		1112
98	X 73		1282
99	X 74		1452

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>X1 – X80</td><td>O</td><td>LCD drive segment (column) output
The output changes with the LP's trailing edge.</td><td>80</td></tr>
<tr><td>D_0 – D_3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input
Reads the display data (D_0 – D_3) into the data register with a trailing edge.</td><td>1</td></tr>
<tr><td>LP</td><td>I/O</td><td>Display data latch clock input
• The display RAM data (specified by the low address shift register) is read into the latch with a leading edge, and the LCD display data is output.
• For a specified low address, the contents of the write register are written in the display RAM. (At Data transfer mode)
• Resets the enable control circuit.</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
• Configured by SHL.
• Output is reset to "H" by LP input. When the 80 bit display data is read, the output falls to "L" automatically.
• To connect in cascade format, connect these pins to the next level EIO.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction and input/output select input
• If the display data is entered in the input (D_3, D_2, D_1, D_0) in the order of (a1, a2, a3, a4) (b1, b2, b3, b4) … (t1, t2, t3, t4), the relationship of the display data and the segment output is as given in the table below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="14">Xn (SEG output)</th><th colspan="2">EIO</th></tr>
<tr><th>80</th><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>…</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a1</td><td>a2</td><td>a3</td><td>a4</td><td>b1</td><td>b2</td><td>…</td><td>s3</td><td>s4</td><td>t1</td><td>t2</td><td>t3</td><td>t4</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>t4</td><td>t3</td><td>t2</td><td>t1</td><td>s4</td><td>s3</td><td>…</td><td>b2</td><td>b1</td><td>a4</td><td>a3</td><td>a2</td><td>a1</td><td>I</td><td>O</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input
In the "L" level, the segment output is forced to the V0 level.
The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD AC drive signal input</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Scan start input
• Rests the low address counter decoder.
• The number of scanned lines (number of low addresses) for the display RAM is determined by the number of LP pulses, which are input in one YD cycle.</td><td>1</td></tr>
<tr><td>V_0, V_2, V_3, V_5</td><td>Power supply</td><td>LCD drive power input
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$</td><td>4</td></tr>
<tr><td>V_{EE}</td><td>Power supply</td><td>LCD drive power input V_{DD} – V_{EE}</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power input
V_{DD}: connect to the system V_{CC} pin.
V_{SS}: connect to the system GND.</td><td>2</td></tr>
</table>

BLOCK DIAGRAM



BLOCK DESCRIPTION

Enable Shift Register

The order of the display data latched is reversed by the SHL input.

Enable Control and Data Control

If the enable signal is disabled (EIO = "H"), the internal clock signal and the data bus are fixed to "L". This is a power-save mode.
To use multiple segment drivers, connect in cascade format the EIO pin of each driver, and connect the EIO pin of the first driver to the "V_{SS}" pin.
The enable control circuit automatically detects when the 80 bit data has been read and automatically transfers the enable signal. As a result, a control signal by a control LSI is not necessary.

Display RAM

This is a static RAM (200 × 80 bits) that stores the LCD data.
The display RAM data (80 bit) for the low address is read out to the latch with the trailing edge of the LP signal. In addition, with the trailing edge of the LP signal, the contents of the data register is moved to the write register. The contents of the write register are then written in the display RAM area for the low address. The low address is then incremented.
If the XSCL signal does not come in after the trailing edge of the LP signal, the mode is changed to the self-refresh mode. The write register does not write data in the display RAM and the low address is incremented. The mode is then changed to the read out mode to read the next line.

Low Address Counter Decoder

This selects a line of the display RAM in sequence. This decoder catches the "H" of the YD signal at the trailing edge of the LP signal, and resets the low address counter. It then initialize the selected address of the display RAM. In a normal operation, the decoder is incremented after the writing operation into the display RAM. (The writing operation is caused by the trailing edge of the LP signal.) In the self-refresh mode, the decoder is incremented without the writing operation into the display RAM.

Data Register

This 80 bit register controls the write operation into the display RAM. The data is written in the display RAM with the trailing edge of the LP signal. In the self-refresh mode, the data is not written in the display RAM.

Control Circuit

The control circuit detects the self-refresh mode, allows the write register to write the data into the display RAM, and controls and low address count signal.

Latch

This reads the 80 bit data for the low address of the display RAM with the trailing edge of the LP signal, and sends the output signal to the level shifter.

Level Shifter

This is the level interface circuit that converts the signal voltage level from $V_{DD} – V_{SS}$ to $V_{DD} – V_{EE}$ (LCD driver power).

LCD Driver

The LCD driver outputs the LCD driver voltage.
The table below shows the relationship between the display signals ($D_3 – D_0$), LCD AC-drive wave form (FR) and the segment output voltage.

$\overline{DOFF}$	$D_0 – D_3$	FR	X Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_0

Self-Refresh Function

Setting self-refresh mode

The self-refresh mode functions as follows: if the displayed contents do not change, there is no transfer of the display data from the display controller to the SED1570. The SED1570 automatically detects this and power-down is displayed.

The SED1570 is set to the self-refresh mode by maintaining the shift clock (XSCLK) in the "L" level for 1 horizontal display period (LP signal cycle) after the row data for 1 line has been input. The SED1570 checks the mode (whether or not the mode is changed to the self-refresh mode) every 1 horizontal display period. During 1 horizontal display period in which XSCL stops working, the display data is not written into the SED1570 display RAM.

To stop XSCL, terminate display data (D0 – D3) transfer from the display controller (because of the power down), and set XSCL to "H" or "L". At this time, the display control must periodically send the LP, YD, and FR signals to the SED1570 the same way as when data is transferred. The SED1570 inputs these signals, reads the display data periodically from the internal display RAM and refreshes the display.

The display-off function is available in the self-refresh mode.

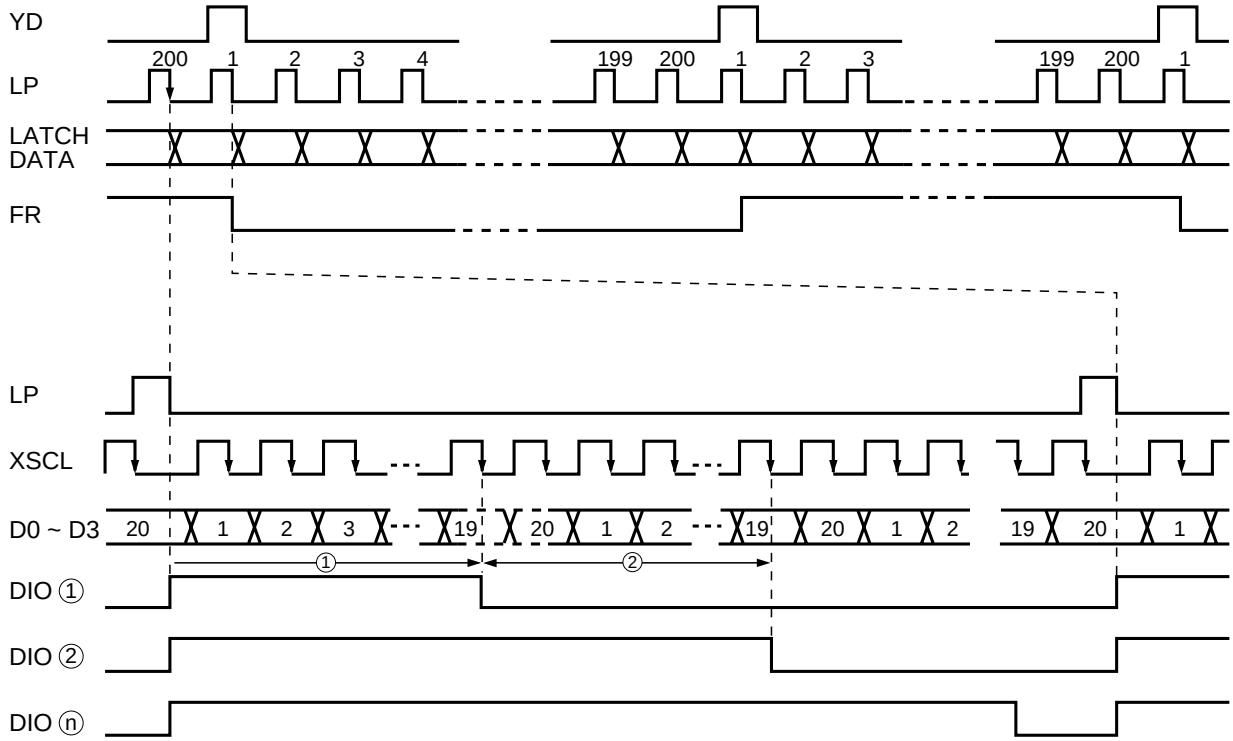
Canceling self-refresh mode

The self-refresh mode is canceled as follows: The display controller inputs the shift clock (XSCL) into the SED1570 for one horizontal display period or longer. This should be down with the trailing edge of the LP signal and in the data transfer timing. After the mode is canceled, the line data, which has been sent in the horizontal display period, is written in the display RAM at the time of the next trailing edge of the LP signal.

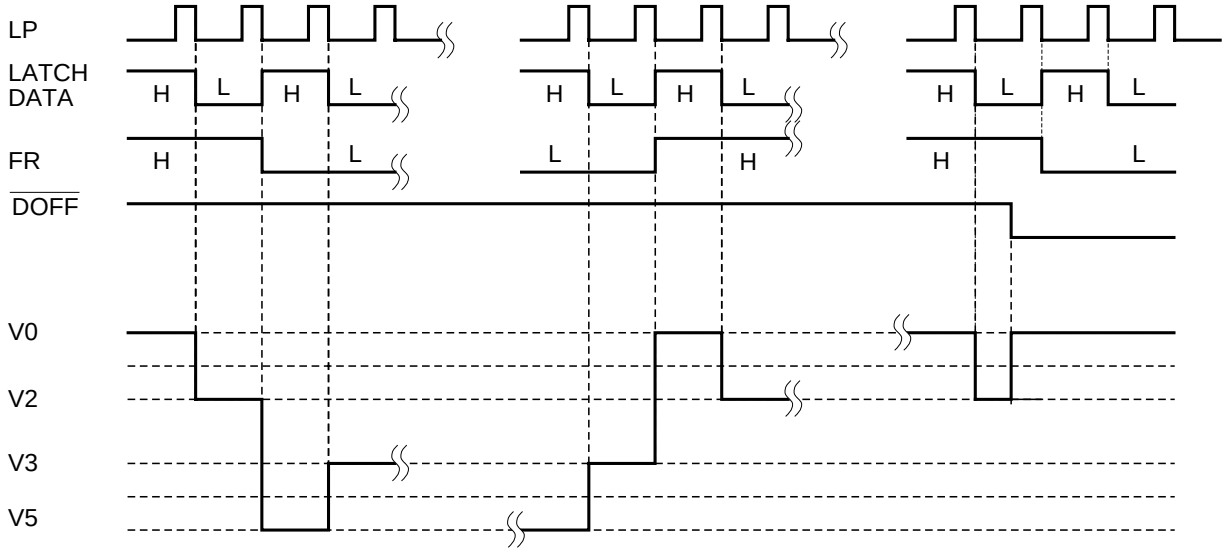
If the SED1570s are connected in cascade format, the self-refresh modes of all SED1570s are not canceled unless the appropriate number of the XSCL clocks for the cascaded SED1570s are entered.

Timing Diagram

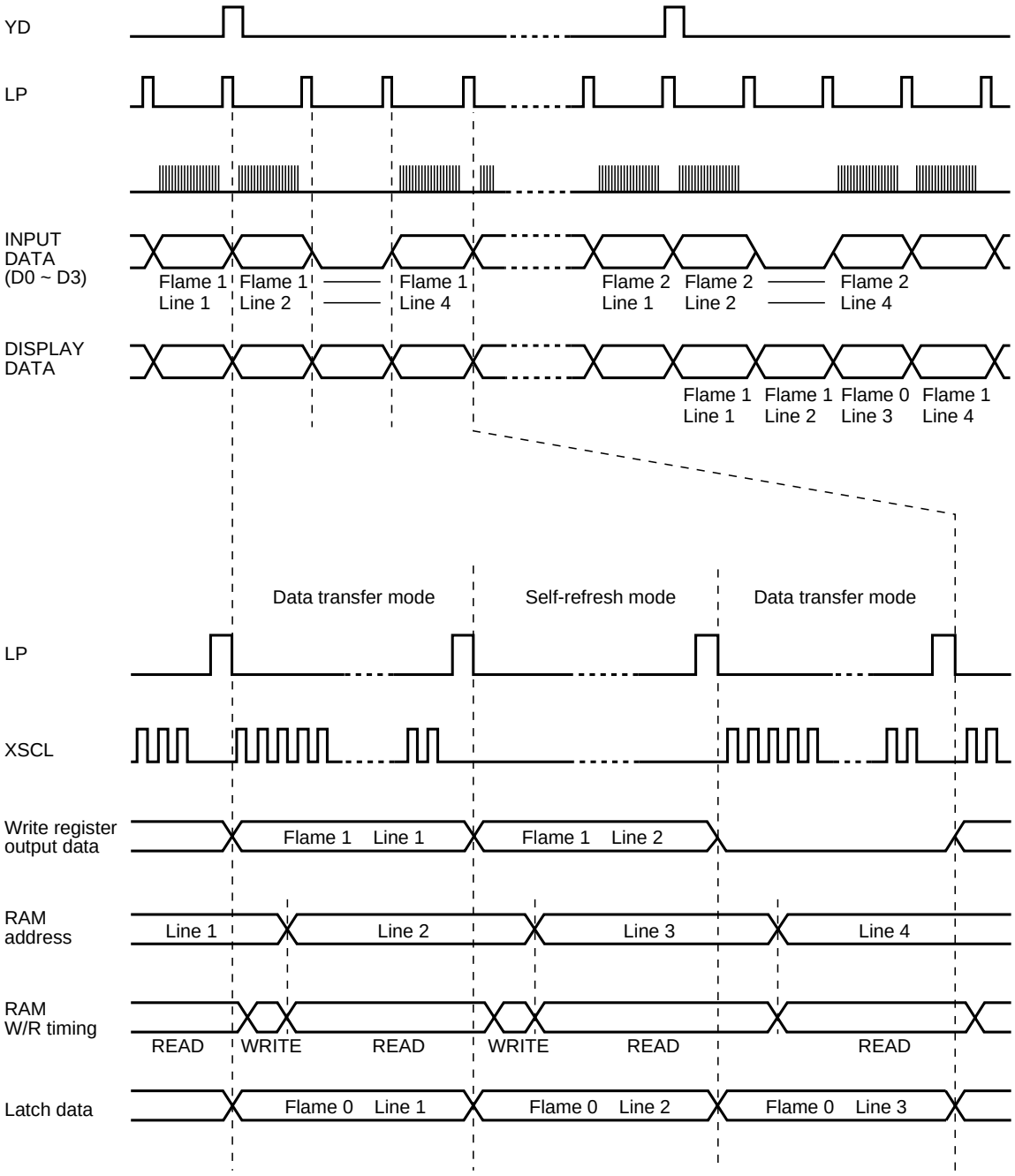
Sample of 1/200 duty



① ~ ⓝ serial conection number of Driver IC



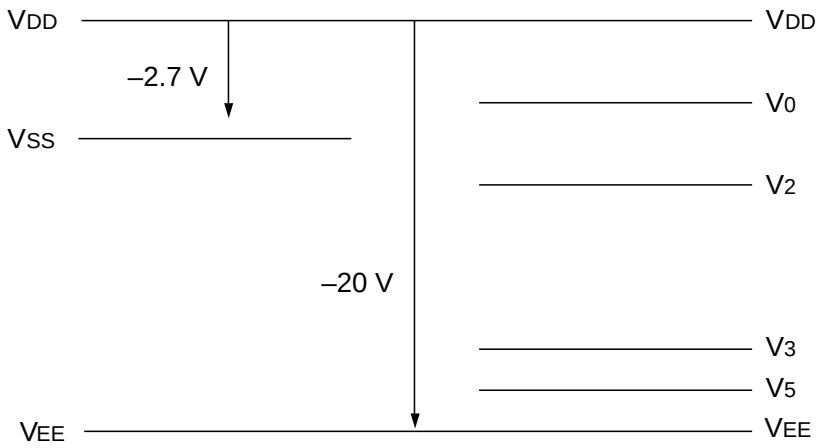
Self-refresh mode timing



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V_{EE}	–22.0 to +0.3	V
Supply voltage 3	V_0, V_2, V_3, V_5	V_{EE} –0.3 to V_{DD} +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I01	20	mA
Operating temperature	Topr	–40 to +85	deg. C
Storage temperature 1	Tstg1	–65 to +150	deg. C
Storage temperature 2	Tstg2	–55 to +100	deg. C

Notes: 1. All voltages are given relative to V_{DD} = 0 V.
2. For storage temperature 1 – Plastic package
For storage temperature 2 – TAB mounted
3. V_0, V_2, V_3, and V_5 must satisfy the condition
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$



4. If the logic power is being floated or if the Vss voltage exceeds -2.5 Vdc during LCD power-on, the LSI chips may be damaged permanently. Take care not to damage the chips especially in the system power on/off sequence.

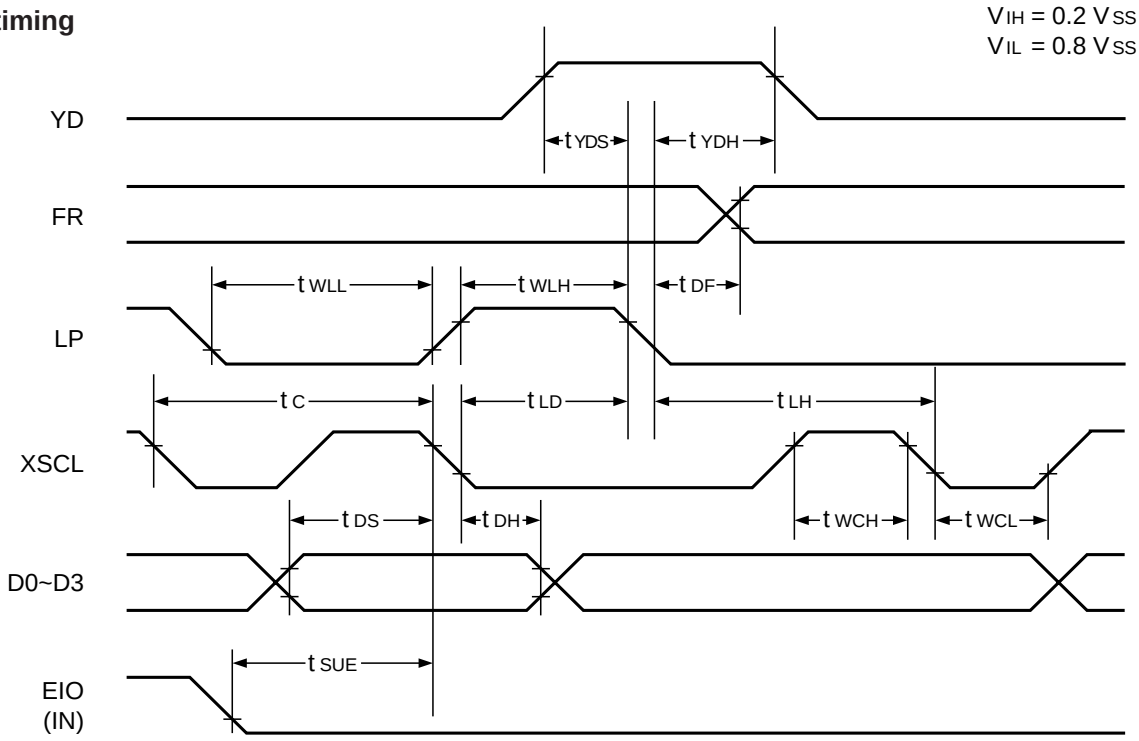
ELECTRICAL CHARACTERISTICS
DC Characteristics

V_{DD} = V_0 = 0 V, V_{SS} = –5.0 V ±10%, Ta = –40 to 85°C

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin
Supply voltage (1)		V_{SS}			–5.5	–5.0	–2.7	V	V_{SS}
Recommended operation voltage		V_{EE}	V_{SS} = –2.7 to –5.5V		–20.0		–8.0	V	V_{EE}
Supply voltage (2)		V_0	Recommended value		V_{DD} –2.5		V_{DD}	V	V_0
Supply voltage (3)		V_2	Recommended value		2/9 V_{EE}			V	V_2
Supply voltage (4)		V_3	Recommended value				7/9 V_{EE}	V	V_3
Supply voltage (5)		V_5	Recommended value		V_{EE}		V_{EE} +2.5	V	V_5
Input high voltage		V_{IH}	V_{SS} = –2.7 to –5.5V		0.2•V_{SS}			V	EIO1, EIO2, FR, D0 to D3, YD, LP, SHL, DOFF, XSCL
Input low voltage		V_{IL}					0.8•V_{SS}	V	
Output high voltage		V_{OH}	V_{SS} = –2.7	I_{OH} = –0.6mA	V_{DD} –0.4			V	EIO1, EIO2
Output low voltage		V_{OL}	to –5.5 V	I_{OL} = 0.6mA			V_{DD} +0.4	V	
Input leakage current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$				2.0	µA	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O leakage current		$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$				5.0	µA	EIO1, EIO2
Static current		I_{SS}	V_5 = –20.0 to –10.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}				25	µA	V_{SS}
On resistance		R_{SEG}	ΔV_{ON} = 0.5 V, V_0 = V_{DD}, V_3 = 7/9•V_{EE}, V_2 = 2/9•V_{EE} V_{EE} = V_5 = –14.0 V			1.0	1.4	KΩ	X1 to X80
Average current consumption (1)	Data transfer mode	I_{DDT}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 4.0 MHz f_{LP} = 14 kHz, f_{FR} = 70 Hz Checkered pattern, non-burden V_{DD} = V_0 = 0V V_2 = –4 V V_3 = –16 V, V_{EE} = V_5 = –20 V			0.3	0.8	mA	V_{DD}
	Self-refresh mode	I_{DDS}	f_{XSCL} = 0 Hz = V_{SS} Another place is same as I_{DDT} item			70	200	µA	
Average current consumption (2)		I_{EE}	V_{SS} = –5.0 V, V_0 = 0.0 V V_2 = –4 V, V_3 = –16 V I_{EE} = V_5 = –20.0 V Another place is same as I_{DDT} item			25	70	µA	V_{EE}
Input capacitance		C_I	Freq. = 1 MHz, Ta = 25°C Simple substance of CHIP				8	pF	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O capacitance		$C_{I/O}$					15	pF	EIO1, EIO2

AC Timing

Input timing



V_{SS} = –5.0 V ±10%, Ta = –40 to 85°C

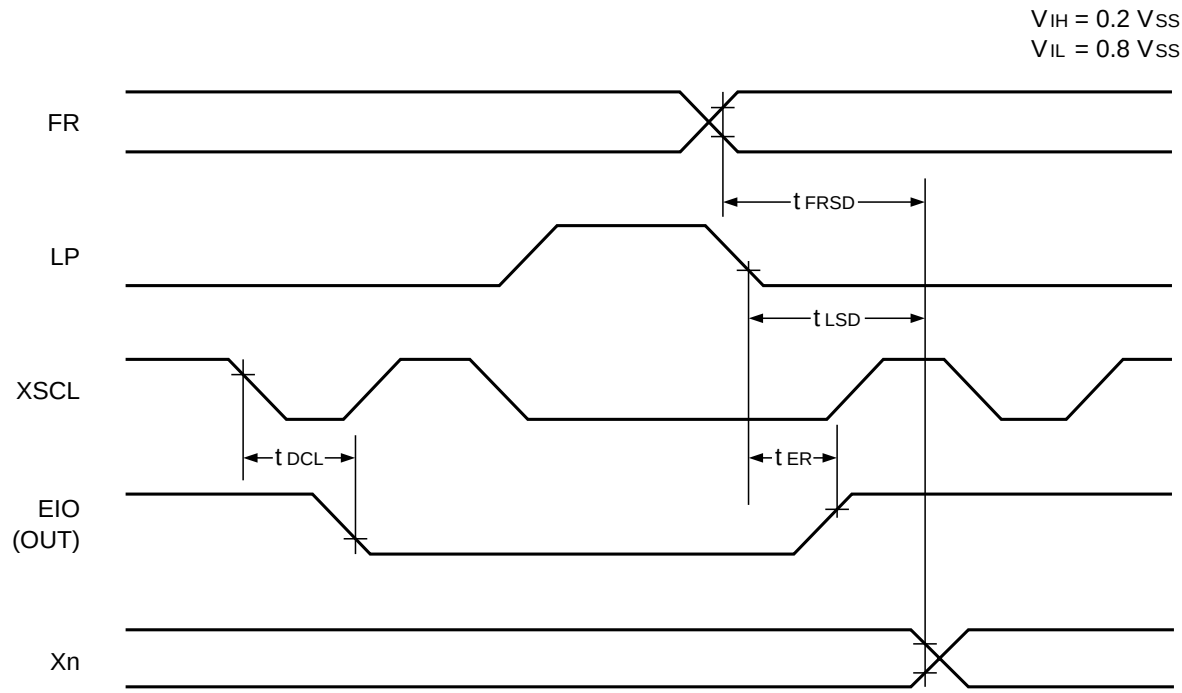
Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		150		ns
XSCL high level pulse width	t_{WCH}		30		ns
XSCL low level pulse width	t_{WCL}		30		ns
Data setup time	t_{DS}		20		ns
Data hold time	t_{DH}		15		ns
XSCL ↓ → LP ↓	t_{LD}		10		ns
LP ↓ → XSCL ↓	t_{LH}		70		ns
LP high level pulse width	t_{WLH}	*	40		ns
LP low level pulse width	t_{WLL}		600		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		35		ns
YD setup time	t_{YDS}		40		ns
YD hold time	t_{YDH}		40		ns
Rise/fall time	t_r, t_f			30	ns

V_{SS} = –4.5 V to –2.7 V, Ta = –40 to 85°C

Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		250		ns
XSCL high level pulse width	t_{WCH}		70		ns
XSCL low level pulse width	t_{WCL}		70		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		50		ns
XSCL ↓ → LP ↓	t_{LD}		80		ns
LP ↓ → XSCL ↓	t_{LH}		140		ns
LP high level pulse width	t_{WLH}	*	75		ns
LP low level pulse width	t_{WLL}		1200		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		50		ns
YD setup time	t_{YDS}		80		ns
YD hold time	t_{YDH}		80		ns
Rise/fall time	t_r, t_f			30	ns

*: Recommended t_{WLH} value = t_C

Output Timing



V_{DD} = –5.0 ±10%, V_{EE} = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF			90	ns
EIO output delay time	t_{DCL}	(EIO)	V_{SS} = –2.7 V		55	ns
LP → Xn output delay time	t_{LSD}	C_L = 100 pF			400	ns
FR → Xn output delay time	t_{FRSD}				400	ns

V_{DD} = –4.5 V to –2.7 V, V_{EE} = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF			150	ns
EIO output delay time	t_{DCL}	(EIO)	V_{SS} = –2.7 V		95	ns
LP → Xn output delay time	t_{LSD}	C_L = 100 pF			800	ns
FR → Xn output delay time	t_{FRSD}				800	ns

LCD DRIVER POWER SUPPLY

Generating LCD Drive Voltages

To obtain individual voltage levels for LCD driver, register-split the potential between V_{EE} – V_{DD} and drive the LCD with the voltage follower using the operation amplifier. When using an operation amplifier, V_0 and V_{DD}, V_5 and V_{EE} are separated.

However, if the potential of V_0 is lower than V_{DD} potential or V_5 is higher than V_{EE} and the potential difference increases, the LCD driver capability decreases. To avoid this, set V_{DD} and V_0 or V_5 and V_{EE} within 0 V to 2.5 V. If an operation amplifier is not used, connect V_0 and V_{DD}, V_5 and V_{EE}.

If there are direct resistors on the V_{EE} (V_{DD}) power line, voltage falls in V_{EE} (V_{DD}) at the LSI power pins. This is caused by I_{DD} (I_{EE}) at the time of signal change. As a result, the relationship ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$) for intermediate potential of LCD can not be maintained and the LSI may be damaged.

To insert a protective resistor, the voltage must be stabilized according to the capacity.

System Power-up

This LSI has high LCD drive voltage. As a result, if the logic power is being floated or if the V_{SS} voltage is kept above –2.5Vdc and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

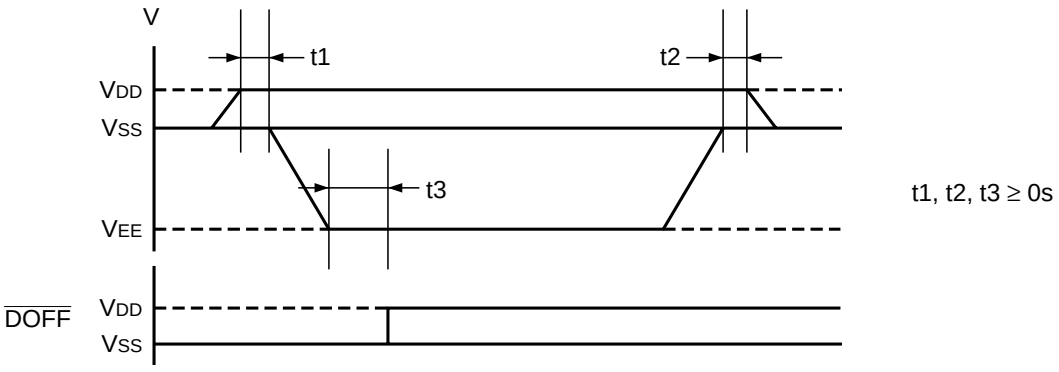
Until the LCD drive voltage is stabilized, use the display off function ($\overline{DOFF}$) to set the potential of the LCD drive output to V0 level.

Follow the sequence given below when turning the power on/off.

To turn on the power – Turn on the logic power
→ Turn the LCD driver on.
(On turn them on simultaneously.)

To turn off the power – Turn off the LCD driver
→ Turn off the logic power.
(Or turn them off simultaneously.)

To avoid excess current, insert the high-speed fuse in series with the LCD power. Select the appropriate value for a protective resistor according to the capacity of a LCD cell.



EXAMPLE OF APPLICATION

Constitution of LCD