12. SED15A6 Series

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1. DESCRIPTION

The SED15A6 series is a single-chip liquid crystal display (=LCD) driver for dot-matrix LCDs that can be connected directly to a microprocessor (=MPU) bus. It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.
The use of the on-chip DDRAM of 65×102 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.
The SED15A6 series does not need external operation clock for DDRAM read/write operations, and has a on-chip LCD power supply circuit featuring very low current consumption with few external components, and moreover has a on-chip CR oscillator circuit.
And the SED15A6 does not need smoothing capacitor on the LCD power supply.
Consequently, the SED15A6 series can be realize a high-performance handy display system with a minimum current consumption and the fewest components.

2. FEATURES

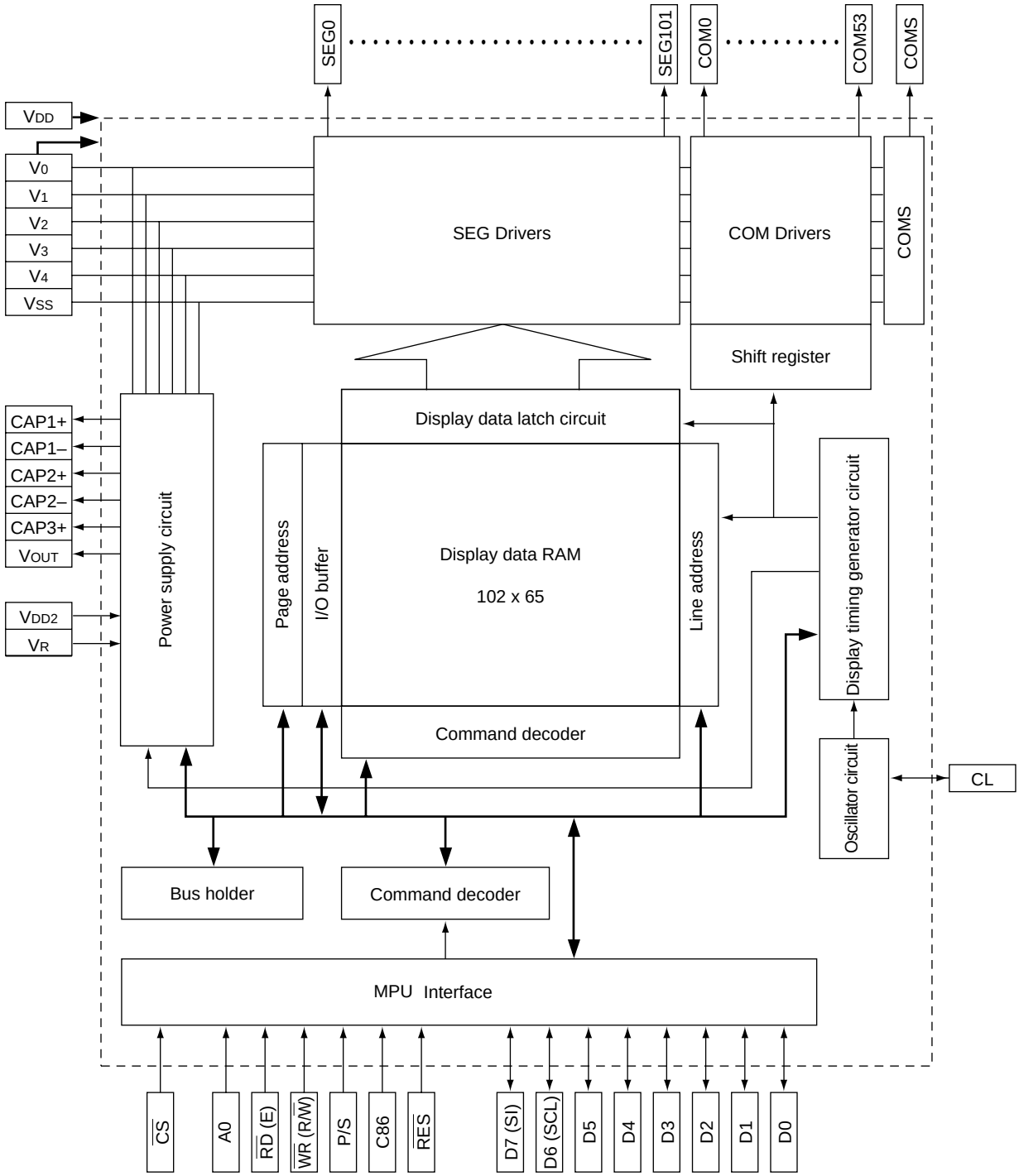
- Direct display of RAM data through the display data RAM.
- RAM bit data : "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity 65×102 = 6630 bits
- Display driver circuits
  SED15A6*** : 55 common output and 102 segment outputs
- High-speed 8-bit MPU interface(The chip can be connected directly to the 8080 series MPUs and the 6800 series MPUs)
- High-speed Serial interface are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, common driver direction select, V_0 voltage regulation internal resistor ratio set.
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit(with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  - High-accuracy voltage adjustment circuit (Thermal gradient –0.1%/°C)
  - V_0 voltage divider resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- Component that can be omitted (you may omit the smoothing capacitor on the voltage follower).
- CR oscillator circuit equipped internally(external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used(an example)
  SED15A6D$_{0B}$ (79μA)
  Condition : V_{DD}–V_{SS} = 1.8V, V_{DD2}–V_{SS} = 3.3V, V_0–V_{SS} = 9.0V, triple boosting, all white is displayed, Ta = 25°C
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply : V_{DD}–V_{SS} = 1.8V to 3.6V
  Boost reference voltage : V_{DD2}–V_{SS} = 1.8V to 5.0V
  Liquid crystal drive power supply : V_0–V_{SS} = 4.5V to 9.0V
- Wide range of operating temperatures : -40 to +85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- There chip not designed for resistance to light or resistance to radiation.

Series Specifications

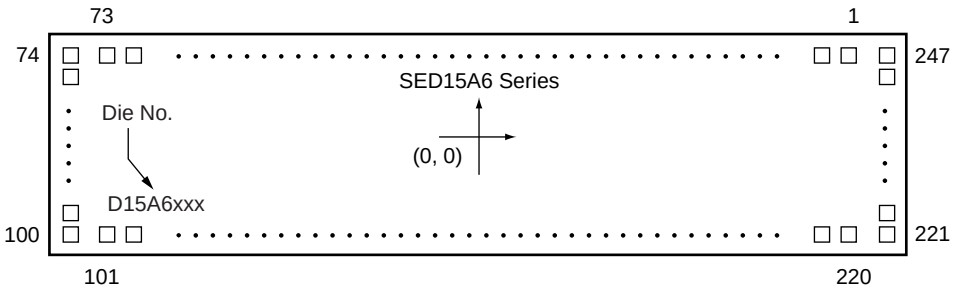
Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Power supply specification	Shipping Forms
SED15A6D$_{0B}$	1/55	1/6,1/8	102	55	–0.1%/°C	Built-in power supply is only used	Bare Chip
*SED15A6D$_{1B}$	1/55	1/6,1/8	102	55	–0.1%/°C	V_0 or V_{OUT} External supply voltage follower is used	Bare Chip
*SED15A6D$_{2B}$	1/55	1/6,1/8	102	55	–0.1%/°C	External power supply is only used	Bare Chip
SED15A6T$_0$	1/55	1/6,1/8	102	55	–0.1%/°C		TCP

* : Being planned

3. BLOCK DIAGRAM



4. PIN DIMENSIONS



		Size X	Size Y	Unit
Chip Size		9.93	2.15	mm
Chip Thickness		0.625		mm
Bump Pitch		70 (Min.)		μm
Bump Size	PAD No.1 to 73	85	85	μm
	PAD No.74	85	74	μm
	PAD No.75 to 99	85	45	μm
	PAD No.100	85	74	μm
	PAD No.101 to 220	52	85	μm
	PAD No.221	85	74	μm
	PAD No.222 to 246	85	45	μm
	PAD No.247	85	74	μm
Bump Height		17 (Typ.)		μm

SED15A6*** Pad Center Coordinates

Units: μm

PAD No.	Pin Name	X	Y
1	(NC)	4570	921
2	TEST0	4449	
3	TEST1	4300	
4	V_{SS}	4151	
5	TEST2	4030	
6	TEST3	3910	
7	$\overline{RES}$	3789	
8	$\overline{CS}$	3668	
9	V_{SS}	3547	
10	$\overline{WR}$(R/$\overline{W}$)	3427	
11	$\overline{RD}$(E)	3306	
12	V_{DD}	3185	
13	CL	3065	
14	A0	2944	
15	D7(SI)	2823	
16	D6(SCL)	2703	
17	D5	2582	
18	D4	2461	
19	D3	2340	
20	D2	2220	
21	D1	2099	
22	D0	1978	
23	V_{DD}	1858	
24	V_{DD}	1737	
25	V_{DD}	1616	
26	V_{DD2}	1496	
27	V_{DD2}	1375	
28	V_{DD2}	1254	
29	V_{DD}	1133	
30	P/S	1013	
31	C86	892	
32	V_{SS}	771	
33	TEST4	651	
34	TEST5	474	
35	TEST6	297	
36	V_{SS}	120	
37	V_{SS}	0	
38	V_{SS}	–121	
39	TEST7	–298	
40	TEST8	–475	
41	TEST9	–652	
42	TEST10	–828	
43	V_{OUT}	–949	
44	V_{OUT}	–1070	
45	V_{OUT}	–1190	
46	V_{SS}	–1311	
47	V_R	–1432	
48	V_0	–1553	
49	V_1	–1673	
50	V_2	–1794	

PAD No.	Pin Name	X	Y
51	V_3	–1915	921
52	V_4	–2035	
53	CAP2+	–2156	
54	CAP2+	–2277	
55	(NC)	–2397	
56	(NC)	–2518	
57	(NC)	–2639	
58	(NC)	–2760	
59	(NC)	–2880	
60	CAP2–	–3001	
61	CAP2–	–3122	
62	(NC)	–3242	
63	(NC)	–3363	
64	(NC)	–3484	
65	(NC)	–3604	
66	CAP1+	–3725	
67	CAP1+	–3864	
68	CAP1–	–3967	
69	CAP1–	–4087	
70	CAP3+	–4208	
71	CAP3+	–4329	
72	V_{OUT}	–4449	
73	(NC)	–4570	
74	(NC)	–4808	926
75	COMS		842
76	COM26		771
77	COM25		701
78	COM24		631
79	COM23		561
80	COM22		491
81	COM21		421
82	COM20		351
83	COM19		281
84	COM18		210
85	COM17		140
86	COM16		70
87	COM15		0
88	COM14		–70
89	COM13		–140
90	COM12		–210
91	COM11		–281
92	COM10		–351
93	COM9		–421
94	COM8		–491
95	COM7		–561
96	COM6		–631
97	COM5		–701
98	COM4		–771
99	COM3		–842
100	(NC)		–926

PAD No.	Pin Name	X	Y
101	(NC)	–4623	–921
102	(NC)	–4545	
103	COM2	–4467	
104	COM1	–4389	
105	COM0	–4312	
106	(NC)	–4234	
107	(NC)	–4156	
108	(NC)	–4079	
109	(NC)	–4001	
110	SEG0	–3923	
111	SEG1	–3846	
112	SEG2	–3768	
113	SEG3	–3690	
114	SEG4	–3613	
115	SEG5	–3535	
116	SEG6	–3457	
117	SEG7	–3380	
118	SEG8	–3302	
119	SEG9	–3224	
120	SEG10	–3146	
121	SEG11	–3069	
122	SEG12	–2991	
123	SEG13	–2913	
124	SEG14	–2836	
125	SEG15	–2758	
126	SEG16	–2680	
127	SEG17	–2603	
128	SEG18	–2525	
129	SEG19	–2447	
130	SEG20	–2370	
131	SEG21	–2292	
132	SEG22	–2214	
133	SEG23	–2136	
134	SEG24	–2059	
135	SEG25	–1981	
136	SEG26	–1903	
137	SEG27	–1826	
138	SEG28	–1748	
139	SEG29	–1670	
140	SEG30	–1593	
141	SEG31	–1515	
142	SEG32	–1437	
143	SEG33	–1360	
144	SEG34	–1282	
145	SEG35	–1204	
146	SEG36	–1127	
147	SEG37	–1049	
148	SEG38	–971	
149	SEG39	–893	
150	SEG40	–816	

Units: µm

PAD No.	Pin Name	X	Y
151	SEG41	–738	–921
152	SEG42	–660	
153	SEG43	–583	
154	SEG44	–505	
155	SEG45	–427	
156	SEG46	–350	
157	SEG47	–272	
158	SEG48	–194	
159	SEG49	–117	
160	SEG50	–39	
161	SEG51	39	
162	SEG52	117	
163	SEG53	194	
164	SEG54	272	
165	SEG55	350	
166	SEG56	427	
167	SEG57	505	
168	SEG58	583	
169	SEG59	660	
170	SEG60	738	
171	SEG61	816	
172	SEG62	893	
173	SEG63	971	
174	SEG64	1049	
175	SEG65	1127	
176	SEG66	1204	
177	SEG67	1282	
178	SEG68	1360	
179	SEG69	1437	
180	SEG70	1515	
181	SEG71	1593	
182	SEG72	1670	
183	SEG73	1748	
184	SEG74	1826	
185	SEG75	1903	
186	SEG76	1981	
187	SEG77	2059	
188	SEG78	2136	
189	SEG79	2214	
190	SEG80	2292	
191	SEG81	2370	
192	SEG82	2447	
193	SEG83	2525	
194	SEG84	2603	
195	SEG85	2680	
196	SEG86	2758	
197	SEG87	2836	
198	SEG88	2913	
199	SEG89	2991	
200	SEG90	3069	

PAD No.	Pin Name	X	Y
201	SEG91	3146	–921
202	SEG92	3224	
203	SEG93	3302	
204	SEG94	3380	
205	SEG95	3457	
206	SEG96	3535	
207	SEG97	3613	
208	SEG98	3690	
209	SEG99	3768	
210	SEG100	3846	
211	SEG101	3923	
212	(NC)	4001	
213	(NC)	4079	
214	(NC)	4156	
215	(NC)	4234	
216	COM27	4312	
217	COM28	4389	
218	COM29	4467	
219	(NC)	4545	
220	(NC)	4623	
221	(NC)	4808	–926
222	COM30		–842
223	COM31		–771
224	COM32		–701
225	COM33		–631
226	COM34		–561
227	COM35		–491
228	COM36		–421
229	COM37		–351
230	COM38		–281
231	COM39		–210
232	COM40		–140
233	COM41		–70
234	COM42		0
235	COM43		70
236	COM44		140
237	COM45		210
238	COM46		281
239	COM47		351
240	COM48		421
241	COM49		491
242	COM50		561
243	COM51		631
244	COM52		701
245	COM53		771
246	COMS		842
247	(NC)		926

5. PIN DESCRIPTION

Power supply pins

Name	I/O	Description	Number of pins
V_{DD}	Supply	Power supply. Connect to MPU power pin V_{CC}.	5
V_{DD2}	Supply	Externally-input reference power supply for booster circuit.	3
V_{SS}	Supply	This is a 0V terminal connected to the system GND.	7
V_0, V_1, V_2 V_3, V_4	Supply	Multi-level power supply for LCD drive. The voltages are determined by LCD cell.The voltages should maintain the following relationship : $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$. When on-chip power supply circuit turns on, V_0 voltage are generated, and the following voltages are generated to V_1 to V_4. Either voltage can be selected by LCD bias set command.	5

	SED15A6***
V_1	5/6 • V_0, 7/8 • V_0
V_2	4/6 • V_0, 6/8 • V_0
V_3	2/6 • V_0, 2/8 • V_0
V_4	1/6 • V_0, 1/8 • V_0

LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1- pins.	2
CAP1–	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP1+ pins.	2
CAP2+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP2– pins.	2
CAP2–	O	Boosting capacitor negative connection pin. Capacitor is connected across CAP2+ pins.	2
CAP3+	O	Boosting capacitor positive connection pin. Capacitor is connected across CAP1– pins.	2
V_{OUT}	O	Booster output. Capacitor is connected across V_{SS} or V_{DD2}.	4
V_R	I	Voltage adjustment pin. Provides V_0 voltage using external resistors. When internal resistors are used, this pin cannot be used. Operable only when the built-in resistor for V_0 adjustment is not used. [V_0 resistance ratio is (D2, D1, D0) = (1.1.1)] This pin is disabled when the built-in resistor for V_0 adjustment is used. This pin must be open in this case.	1

System bus connection pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SL)
(SCL)</td><td>I/O</td><td>8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus.
When the serial interface is selected (P/S=LOW) ;
D7 : Serial data input (SI)
D6 : Serial clock input (SCL)
At this time, D0 through D5 will go under the Hz mode.
When the chip selects are in non-active state, D0 through D7 will go under the Hz mode.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Control/data flag input.
A0=HIGH : The data on D7 to D0 is display data.
A0=LOW : The data on D7 to D0 is control data.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip select input. Data input is enable when $\overline{CS}$ is low.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When $\overline{RES}$ is caused to go low, initialization is executed.
A reset operation is performed at the signal level.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When connected to an 8080-series MPU ;
This is active-LOW. This pin is connected to the $\overline{RD}$ signal of the 8080-series MPU. While this signal is low, SED15A6 series data bus in an output status.
• When connected to an 6800-series MPU ;
This is active-HIGH. This is used as an enable clock input pin of the 6800-series MPU.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When connected to an 8080-series MPU ;
This is active-LOW. This pin is connected to the $\overline{WR}$ signal of the 8080-series MPU. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
• When connected to an 6800-series MPU ;
This is the read/write control signal input .
R/$\overline{W}$=HIGH : Read.
R/$\overline{W}$=LOW : Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface selection pin.
C86=HIGH : 6800-series MPU interface
C86=LOW : 8080-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input selection pin.
P/S=HIGH : Parallel data input
P/S=LOW : Serial data input
The following applies depending on the P/S status :
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D7 to D0</td><td>$\overline{RD}$, $\overline{WR}$</td><td>–</td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
In serial mode, no data can be read from DDRAM.
When P/S=LOW,D5 to D0 are HZ. D5 to D0 may be HIGH, LOW or Open, and moreover A0, $\overline{RD}$, $\overline{WR}$, C86 may be HIGH or LOW.</td><td>1</td></tr>
</table>

LCD driver pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I</td><td>This pin is used for enabling or disabling the built-in oscillation circuit for the display clock.
CL = HIGH: Built-in oscillation circuit is enabled.
CL = LOW: Built-in oscillation circuit (external input) is disabled.
Select CL = LOW to turn the external clock off.
When using the built-in oscillation circuit, select CL = HIGH (V_{DD}).</td><td>1</td></tr>
<tr><td>SEG0
to SEG101</td><td>O</td><td>These pins output the signal for the segment drive of LCD.
One of V_0, V_2, V_3 and V_{SS} levels is selected depending on a given combination of display RAM data and internal FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">Internal FR signal</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reversing display</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_0</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_0</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0
to COM53</td><td>O</td><td>These pins output the signal for the common drive of LCD.
Following number of pins are assigned to SED15A6*$_{**}$.
<table>
<tr><th>Model</th><th>COM</th><th>Number of COM pins</th></tr>
<tr><td>SED15A6*$_{**}$</td><td>COM0~COM53</td><td>54</td></tr>
</table>
One of V_0, V_1, V_4 and V_{SS} levels is selected depending on a given combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{SS}</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_0</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{SS}</td></tr>
</table></td><td>54</td></tr>
<tr><td>COMS</td><td>O</td><td>They are COM pins exclusively used for the indicator.
Both pins output the same signal.
They must be made open when not used.</td><td>2</td></tr>
</table>

Test pins

Name	I/O	Description	Number of pins
TEST0 to 10	I/O	These are terminals for IC chip testing. They are set to OPEN.	11

Total : 220 pins for the SED15A6*$_{**}$.

Note and caution

• If control signal from MPU is Hz,an over-current may flow through the IC. A protection is required to prevent the Hz signal at the input pins.

6. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED15A6 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). Through selecting the P/S pin polarity to the HIGH or LOW, it is possible to select either 8-bit parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH:Parallel Input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW:Serial Input	$\overline{CS}$	A0	–	–	–	SI	SCL	–

– : Must always be HIGH or LOW

Parallel interface

When the parallel interface has been selected (P/S =HIGH), then it is possible to connect directly to either an 8080-series MPU or a 6800-series MPU (as shown in Table 2) by selecting C86 pin to either HIGH or LOW.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH:6800-series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW:8080-series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

Moreover, the SED15A6 series identifies the data bus signal according to A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$)signals, as shown in Table 3.

Table 3

Common	6800-series	8080-series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	1	0	Writes control data (command)

Serial interface

When the serial interface has been selected (P/S=LOW) then when the chip is in active state($\overline{CS}$=LOW) the serial data input (SI) and the serial clock input (SCL) can be received.

The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether the serial data input is display data or command data; when A0=HIGH, the data is display data, and when A0=LOW then the data is command data.

The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.

Figure 1 is a serial interface signal chart.

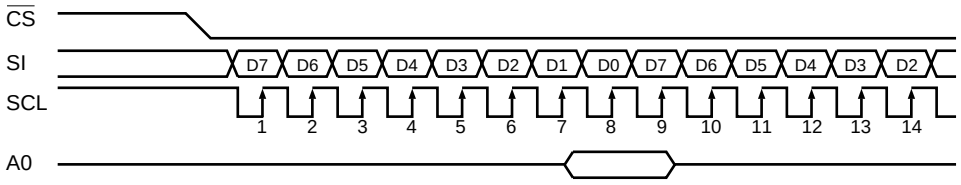


Figure 1

* When the chip is inactive, the shift register and the counter is reset to the initial state.
* Data read is not available as long as the serial interface is selected.
* Reasonable care must be exercised so that SCL signal may not be exposed undesirable effects resulting from, for instance, terminal reflection of wiring or external noises. Before using the signal, it is recommended to test the signal in actual system.

Chip select input

The MPU interface (either papallel or serial) is enabled only when $\overline{CS}$=LOW.
When the chip select is inactive, D7 to D0 enter a high impedance state, and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When the serial interface is selected, the shift register and the counter are reset.

Access to DDRAM and internal registers

In accessing the DDRAM and the internal registers of the SED15A6 series,the MPU is required to satisfy the only cycle time (t_{CYC}),and is not needed to consider the wait time. Accordingly, it is possible to transfer data at higher speed.
In order to realize the higher speed accessing, the SED15A6 series can perform a type of pipeline processing between LSIs using bus holder of internal data bus when data is sent from/to the MPU. For example, when the MPU writes data to the DDRAM, once the data is stored in the bus holder, then it is written to the DDRAM before the next data write cycle. And when the MPU reads the contents of the DDRAM, the first data read cycle (dummy read cycle) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. Thus,there is a certain restriction in the DDRAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

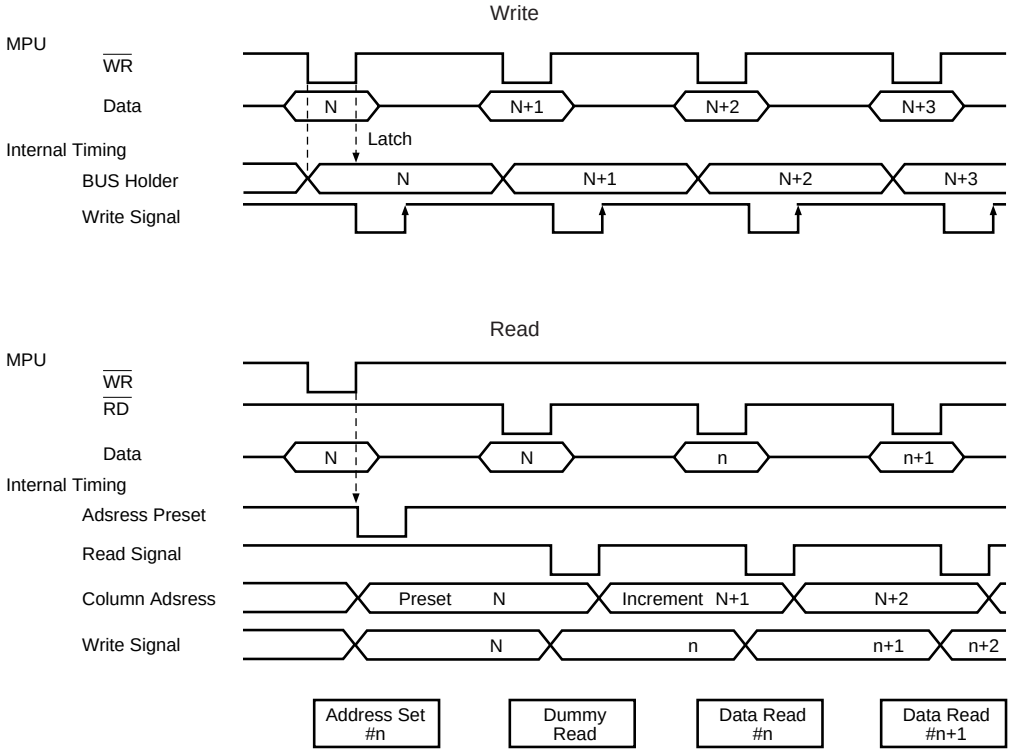


Figure 2

DDRAM

DDRAM and page/column address circuit

The DDRAM stores pixel data for LCD. It is a 65-row (8 page by 8 bit + 1) by 102-column addressable array. As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD common direction. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

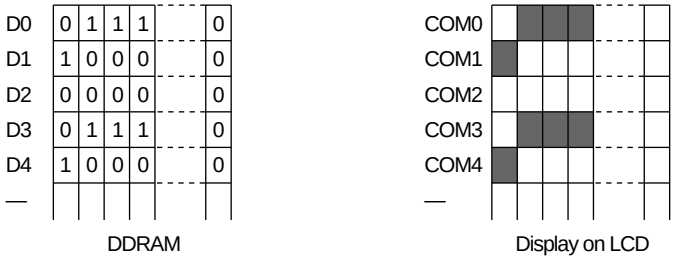


Figure 3

Page address circuit

Each pixel can be selected when page address and column address are specified(refer to Figure 5).
The MPU issues Page address set command to change the page and access to another page. Page address 8 (D3,D2,D1,D0 = 1,0,0,0) is DDRAM area dedicate to the indicator, and display data D0 is only valid.
The DDRAM column address is specified by Column address set command.The specified column address is automatically incremented by +1 when a Display data read/write command is entered. After the last column address (65H) ,column address returns to 00H and page address incremented by +1 (refer to Figure 4). After the very last address (column = 65H,page = 7H),both column address and page address return to 00H (column address = 00H, page address = 0H).

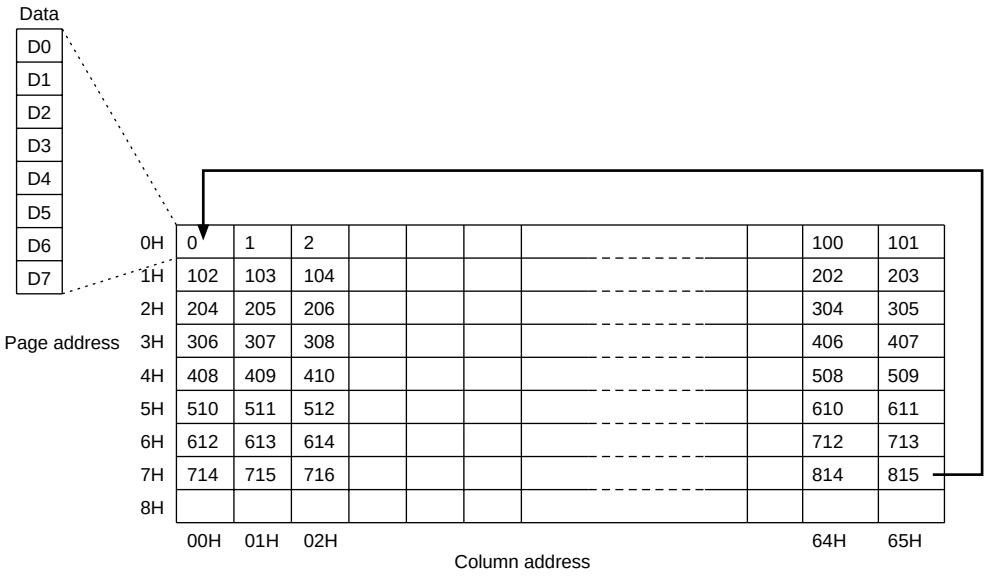


Figure 4

Column address circuit

Designate the column side address of the indication data RAM as shown in Fig. 5, using the column address setting command. Since the designated column address increments (+1) each time an indication data•read/write command is input, the MPU can make access to the indication data in succession.
Also, as shown in Fig. 4, after an access has been made to the final column address (65H), the column address will return to (00H) and the page address will be automatically incremented (by +1). Thanks to this feature, it is possible to write continuous data being divided between adjoining pages. Furthermore, after accesses have been made to the final addresses of both of the page and column (column = 65H and page = 7H), both of the column address and the page address returns to (00H).
(The page will not increment to "8H". Therefore, be careful when executing "read•modify•write" processes.)
Also, as shown in Table 4, the correlation between the column address of the indication data RAM and the segment output can be reversed by use of the ADC command (segment driver direction select command). Thanks to this feature, IC layout limitations when constituting an LCD module can be lessened.

Table 4

Column Address	00H	01H	02H		63H	64H	65H
Normal Direction	SEG0	SEG1	SEG2		SEG99	SEG100	SEG101
Reverse Direction	SEG101	SEG100	SEG99		SEG2	SEG1	SEG0

Line address circuit

The line address circuit specifies the line address (as shown Figure 5) relating to the COM output when the contents of the DDRAM are displayed. The display start line address, what is normally the top line of the display, can be specified by Display start line address set command. And Common driver direction select command can be used to reverse the relationship between the DDRAM line address and common output. For example, as is shown in Table 5, the display start line address corresponds to the COM0 output when the common driver direction is normal, or the COM53 output when common driver direction is reversed.And the display area is followed by the higher number line addresses in ascending order from the display start line address, corresponding to the duty cycle. This allows flexible IC layout during LCD module assembly.
If the display start line address is changed dynamically using the Display start line address set command,then screen scrolling and page swapping can be performed.

Table 5 (at display start line address=1CH)

Line Address	1CH	1DH		3FH	00H		11H	12H
Normal Direction	COM0	COM1		COM35	COM36		COM52	COM53
Reverse Direction	COM53	COM52		COM18	COM17		COM1	COM0

Display data latch circuit

The display data latch circuit is a latch temporarily stored the display data that is output to the LCD driver circuit from the DDRAM.
Display ON/OFF command, Display normal/reverse command, and Displayd all points ON/OFF command control only the data within the latch,and do not change the data within the DDRAM.

Display data RAM

The display data RAM stores pixel data for the LCD. It is a 102-column × 65-row addressable array as shown in Figure 5.

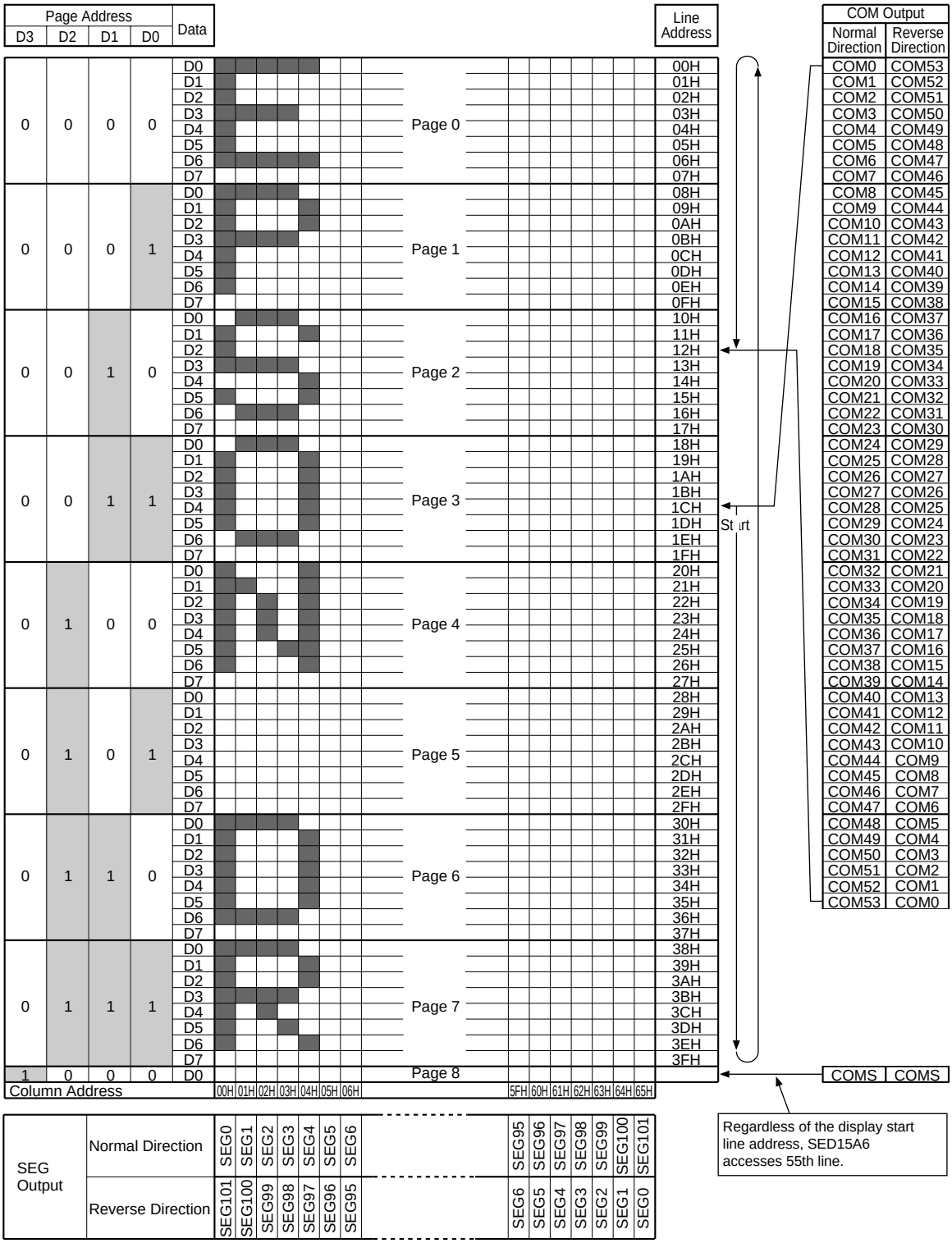


Figure 5

Oscillation circuit

The SED15A6 series generates display clocks using its built-in CR oscillation circuit. The built-in oscillation circuit is enabled when CL = HIGH is selected and the power save mode is turned off.

You can stop operation of the CR oscillation circuit by selecting CL = LOW. Display clock can be externally entered via CL pin (when external clock is turned off, CL pin must be placed in LOW).

Table 6

CL	Operation
HIGH	Built-in CR oscillation circuit is enabled.
LOW	Built-in CR oscillation circuit is turned off [display clock is turned off].
Clock input	External clock input mode

Table 7 shows relationship between frequency of external clock (f_{CL}), frequency of built-in clock circuit (f_{OSC}) and f_{FR}.

Since CL pin is used for resetting the built-in CR clock circuit, it must satisfy the f_{CL} requirements given in the "DC Characteristics".

Table 7

Item		f_{FR} computation formula
SED15A6***	When built-in oscillation circuit is used	$f_{FR}=f_{OSC} / (55\times8)$ [Hz]
	When external clock input is used	$f_{FR}=f_{CL} / (55\times16)$ [Hz]

Display timing generator circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit, and generates COM scan signal and the LCD AC signal (dual-frame AC driver waveform).

LCD driver circuits

These are multiplexers outputting the LCD panel driving 4-level signal which level is determined by a combination of display data, COM scan signal, and LCD AC signal (FR). Figure 6 shows an example of SEG and COM output waveforms.

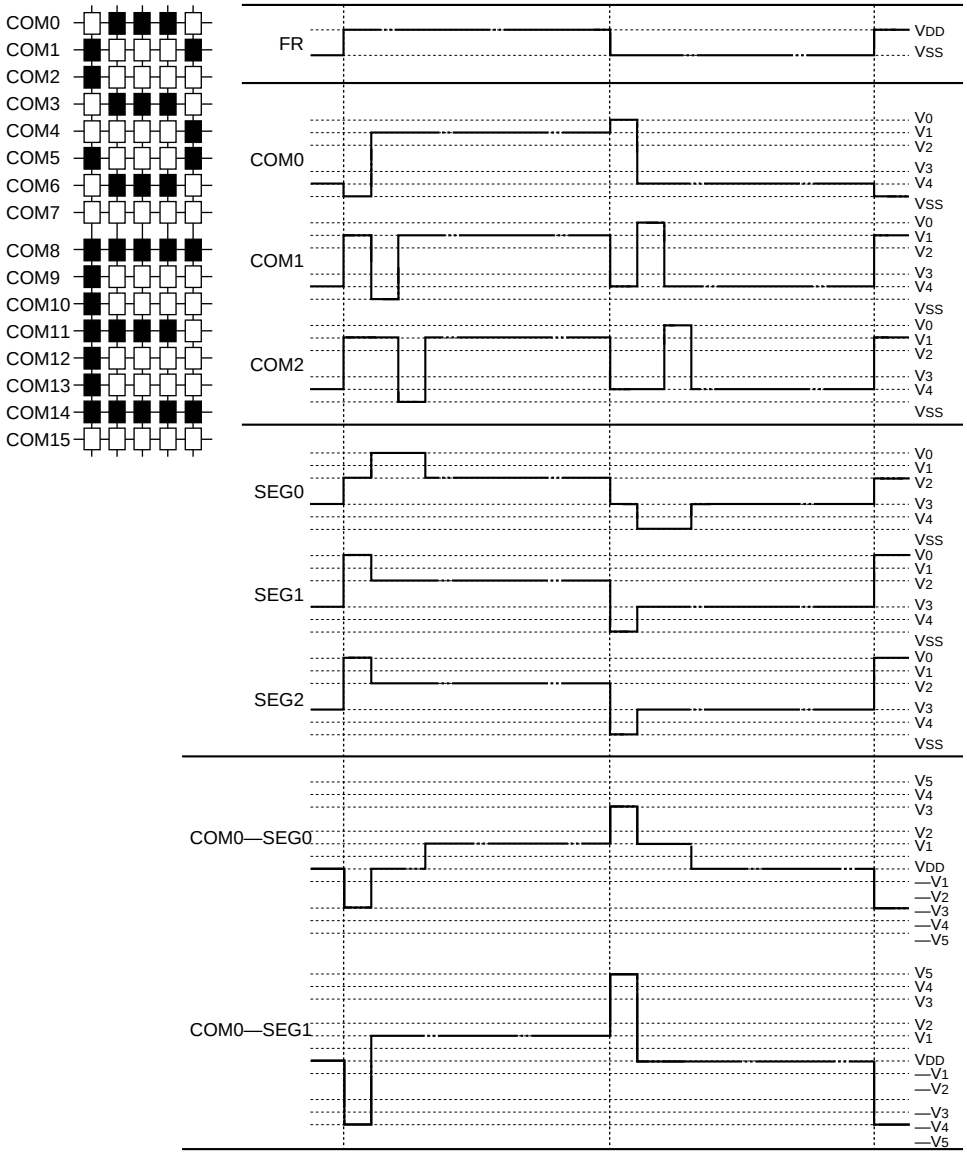

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
V0
V1
V2
V3
V4
V5
COM0—SEG0
COM0—SEG1
—V1
—V2
—V3
—V4
—V5

Figure 6

Power supply circuit

The power supply circuit generates the voltage to drive the LCD panel at low power consumption.
The power supply circuit consists of a booster circuit, voltage regulator circuit, and voltage follower circuit, and is controlled by Power control set command. Using this command, the booster circuit, the voltage regulator circuit, and the voltage follower circuit can be independently turned ON or OFF. Consequently, the external power supply and part of internal power supply circuit functions can be used simultaneously. Table 8 shows reference combinations.
Table 8 lists the functions controllable from 3 bits data of the power control set command. And, Table 9 shows sample combinations of the bits.
Select the models depending on the state of use.

Table 8

Item	State	
	"1"	"0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 9

Usage	Model	D2	D1	D0	Booster circuit.	V adjusting circuit.	V/F circuit.	External voltage entered.	Pins on booster circuit
Built-in power supply alone is used	*1	1	1	1	ON	ON	ON	V_{DD2}	Used
V adjusting and	*2	0	1	1	OFF	ON	ON	V_{OUT} *4	OPEN
V/F circuits alone are used V/F circuit alone is used	*2	0	0	1	OFF	OFF	ON	V_0 *4	OPEN
External power supply alone is used	*3	0	0	0	OFF	OFF	OFF	V_0 to V_4 *4	OPEN

* Pins on the booster circuits denote CAP1+, CAP1–, CAP2+, CAP2– and CAP3+ pins.
* Although other combinations than the above are available, they are not pragmatic and thus not recommendable.
*1: SED15A6D0B *2: SED15A6D1B *3: SED15A6D2B
*4: V_{DD2} is recommended to short-circuit to V_{DD}

Booster circuit

Using the booster circuit, it is possible to produce Quad/Triple/Double boosting of the V_{DD2}–V_{SS} voltage level.
Quad boosting : If capacitor are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, between CAP3+ and CAP1-, between V_{OUT} and V_{DD2}, the potential between V_{DD2} and V_{SS} is boosted to quadruple toward the positive side and it is output at V_{OUT} pin.
Triple boosting : If capacitor are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, between V_{OUT} and V_{DD2}, and jumper between CAP3+ and V_{OUT}, the triple boosted voltage appears at V_{OUT} pin.
Double boosting : If capacitor are inserted between CAP1+ and CAP1-, between V_{OUT} and V_{DD2}, open CAP2-, and jumper between CAP2+, CAP3+ and V_{OUT}, the double boosted voltage appears at V_{OUT} pin.
The boosted voltage relationships are shown in Figure 7.

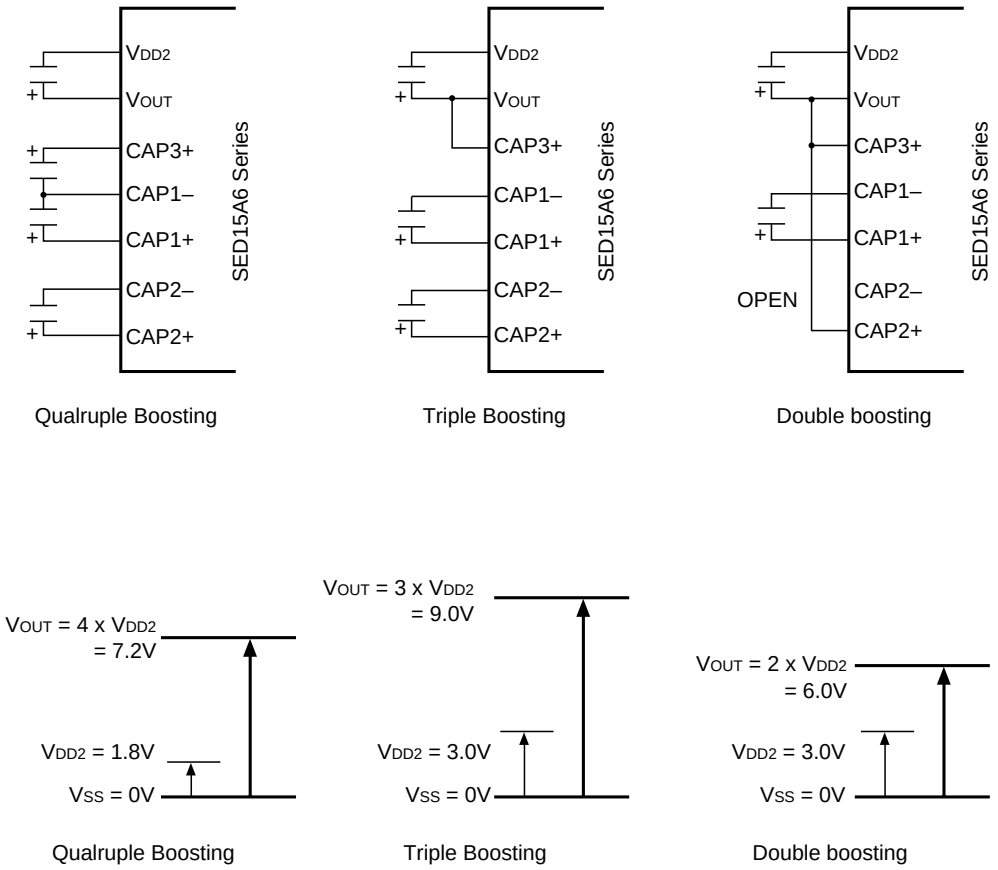


Figure 7

*V_{DD2} voltage must be set so that V_{OUT} voltage does not exceed the absolute maximun rated value.
*The Capacitance depend on the load of the LCD panel to be driven. Set a value that LCD driver voltage may be stable (reference value = 1.0 to 4.7µF).

Voltage regulator circuit

The boosting voltage occurring at the V_{OUT} pin is sent to the voltage regulator, and the V_0 voltage (LCD driver voltage) is output.
Because the SED15A6 series has the high-accuracy constant voltage source, the 32-level electronic volume function and the internal resistor for the V_0 voltage regulator (= V_0-resistor), it is possible to construct a high-accuracy voltage regulator circuit without external component. And V_0 voltage can be adjusted by commands only to adjust the LCD contrast.

The V_0 voltage can be calculated using the following equation within the range of $V_0 < V_{OUT}$.

$$V_0 = (1+Rb/Ra) \cdot V_{EV}$$
$$= (1+Rb/Ra) \cdot (1-\alpha/200) V_{REG} \quad \text{(Expression A-1)}$$
$$V_{EV} = (1-\alpha/200) \cdot V_{REG}$$

V_{REG} is the on-chip constant voltage as shown in Table 10 at Ta=25°C.

Table 10

Model	V_{REG}	Thermal Gradient
SED15A6D**	1.2V	–0.1%/°C

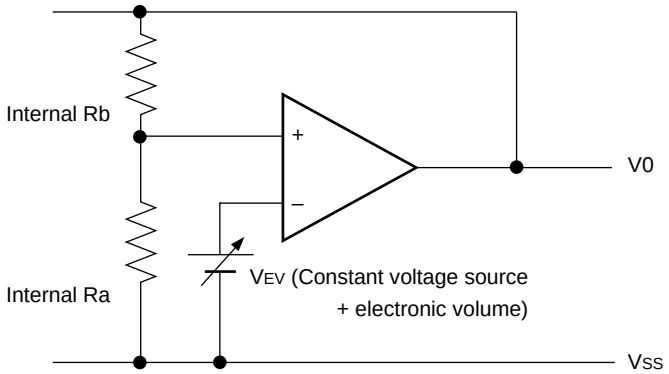


Figure 8

α is a value of the electronic volume, and can be set to one of 32-states by Electronic volume command setting the 5-bit data in the electronic volume register.Table 11 shows the value of α.

Table 11

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	0	3
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Rb/Ra is the V0-resistor ratio, and can be set to one of 7-states by V0-resistor ratio set command setting the 3-bit data in the V0-resistor ratio register. Table 12 shows the value of (1+Rb/Ra) ratio (reference value).

Table 12

			1+Rb/Ra
D3	D2	D1	SED15A6 (Typ.)
0	0	0	5.45
0	0	1	5.71
0	1	0	6.00
0	1	1	6.32
1	0	0	6.67
1	0	1	7.06
1	1	0	7.50
1	1	1	External resistor can be used.

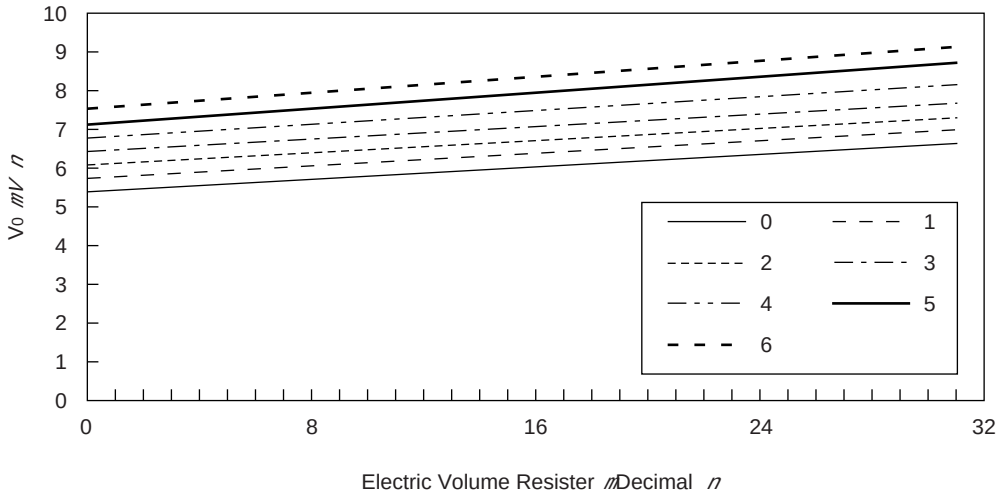


Figure 9 The V0 voltage as a function of the V0 voltage regulator internal resister internal resistor and the electronic volume register [Ta=25°C]

<Setup example : When setting Ta = 25C and V_0 = 7V on an SED15A6*** model with temperature gradient of –0.1% /˚C>

From Figure 9 and expression A-1, the following setting will be employed.

Table 13

Content	Resistors							
	D7	D6	D5	D4	D3	D2	D1	D0
Resistance ratio of V_0 adjusting built-in resistors	0	0	1	0	0	0	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 14 shows V_0 voltage variable range and its variable step available from the electronic volume function when the above setting is employed.

Table 14

V_0	Min.		Typ.		Max.	Unit
Variable range	6.41[80H]	to	7.0[90H]	to	7.58[9FH]	[V]
Variable step			37.92			[mV]

[ ]: Commands selected from the electronic volume.

When external resistor is used (when the built-in resistor for V_0 adjustment is not used)

It is also possible to select a supply voltage V_0 for LCD without using the built-in V_0 voltage adjusting resistors (resistance ratio select command [27H] for the built-in V_0 voltage adjusting resistors) by adding a resistor across V_{SS} and V_R as well as V_R and V_0. In this case too, using the electronic volume allows you to control LCD V_0 through the command and, thus, adjust contrast of LCD display.

Voltage V_0 is given by the following expression when external resistance values Ra' and Rb' are specified in the range of $V_0 < V_{OUT}$:

$$V_0 = (1+Rb/Ra)\cdot V_{EV}$$
$$= (1+Rb/Ra)\cdot(1-\alpha/200)V_{REG} \quad \text{(Expression B-1)}$$
$$V_{EV} = (1-\alpha/200)\cdot V_{REG}$$

V_{REG} represents the constant voltage source on the IC. Its value at Ta = 25°C is constant as shown in Table 10.

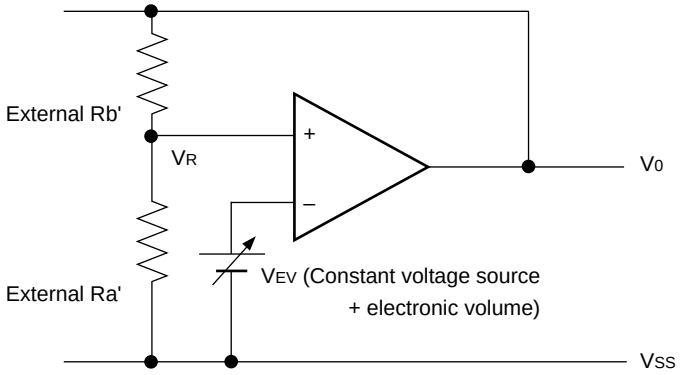


Figure 10

<A setting example: When setting Ta = 25C and V_0 = 7V on an SED15A6*** model with temperature gradient =–0.1% C>
When the intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0) are selected from the electronic volume, the following is given by expression B-1 since α = 15 and V_{REG} = 1.2V (Expression B-2).

$V_0 = (1+Rb'/Ra') \cdot (1-\alpha/200) \cdot V_{REG}$

$7V = (1+Rb'/Ra') \cdot (1-15/200) \cdot 1.2$ (Expression B-2)

If you select 5 μA for the current conducted to Ra' and Rb', the following expression is derived:

$Ra' + Rb' = 1.4M\Omega$ (Expression B-3)

Thus, the following is derived from expressions B-2 and B-3:

$Rb' / Ra' = 5.31$

$\therefore Ra' = 220k\Omega, \quad Rb' = 1180k\Omega$

Table 14 shows the command selected from the electronic volume. Table 16 lists V_0 voltage variable range and variable steps available from the electronic volume function.

Table 15

Content	Resistors							
	D7	D6	D5	D4	D3	D2	D1	D0
Resistance ratio of built-in V_0 voltage adjusting resistors	0	0	1	0	0	1	1	1
Electronic volume	1	0	0	1	0	0	0	0

Table 16

V_0	Min.		Typ.		Max.	Unit
Variable range	6.45[80H]	to	7.0[90H]	to	7.64[9FH]	[V]
Variable step			38.4			[mV]

[ ]: Commands selected from the electronic volume.

When using external resistors (When using variable resistors in stead of the built-in V_0 voltage adjusting resistors)

Adding external variable resistors to the above mentioned external resistors allows you to select an LCD drive voltage V_0 through fine tuning of Ra' and Rb'. In this case too, using the electronic volume function permits you to control an LCD voltage through the command and, thus, adjust contrast of the LCD display.
You can determine the V_0 voltage from the following expression when fine adjustment of Ra' and Rb' is done by specifying resistance values of external resistors R1 and R2 (variable resistors) and R3 within the range of $|V_0| < |V_{OUT}|$:

$V_0 = \{1+(R3+R2-\Delta R2) / (R1+\Delta R2)\} \cdot V_{EV}$

$= \{1+(R3+R2-\Delta R2) / (R1+\Delta R2)\} \cdot (1-\alpha/200) \cdot V_{REG}$ (Expression C-1)

$[V_{EV} = (1-\alpha/200) \cdot V_{REG}]$

Where, V_{REG} is the constant voltage source in the IC and its value remains at a constant level as shown in Table 10.

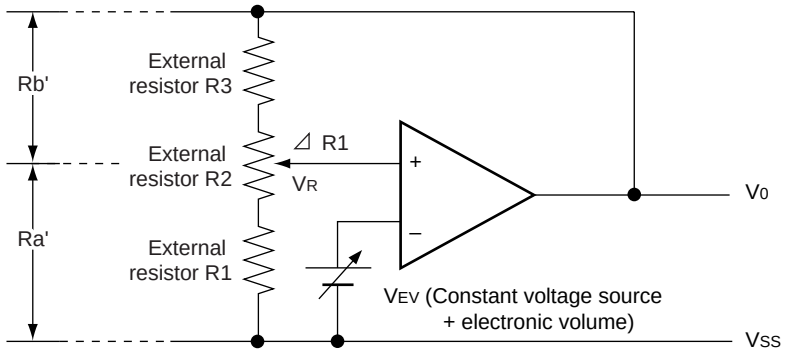


Figure 11

<A setting example: When setting Ta = 25C and V_0 = 5 to 9V on an SED15A6*** model with Temperature gradient = –0.1% C>
α = 15 and V_{REG} = 1.2V when intermediate resistor values (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0) are selected from the electronic volume. Thus, using expression C-1, you can select V_0 = 9V when $\Delta R2 = 0\Omega$ in the following manner:

9V ={1+(R3+R2) / R1} • (1–15/200) • 1.2
R3 + R2=7.11 • R1 (Expression C-2)

If you select 5 uA for the current to be conducted across V_0 and V_{SS} when V_0 = 7V, sum of resistance of R1, R2 and R3 can be derived as shown below:

R1 + R2 + R3 = 1.4MΩ (Expression C-3).

From expressions C-2 and C-3, R1 = 1.4MΩ/8.11=173KΩ.
And, you can select V = 5V when $\Delta R2 = R2$ through the following computation:

5V = ={1+R3/(R1+R2) } • (1–15/200) • 1.2
R3/(R1 + R2) = 3.5 (Expression C-4).

R2 = 137@ and R3 = 1.09 MΩ are derived from expressions C-2, C-3 and C-4.
Table 15 lists the commands used, and Table 17 shows V_0 voltage variable voltage range and variable steps available from the electronic volume.

Table 17

V_0	Min.		Typ.		Max.	Unit
Variable range	6.39[80H]	to	7.0[90H]	to	7.57[9FH]	[V]
Variable step			38.1			[mV]

[ ]: Commands selected from the electronic volume.

* When using the built-in V_0 voltage adjusting resistors or the electronic volume function, both of the voltage adjustment circuit and the voltage follower circuit must be activated, as a minimum requirement, by the power control set command. When the booster is circuit is turned off, necessary voltage must be supplied from V_{OUT}.
* V_R pin is enabled only when the built-in V_0 voltage adjusting resistors are not used. V_R pin must be made open when these resistors are used.
* Since V_R pin has a higher input impedance, appropriate noise protection measures must provided including cutting the wiring distance shorter or using shielded wire.

Voltage Follower Circuit

The V_0 voltage is divided to generate the V_1, V_2, V_3 and V_4 voltages by on-chip resistor circuit. And the V_1, V_2, V_3 and V_4 voltages are impedance-converted by voltage follower, and provide to LCD driver circuit.
LCD bias ratio can be selected by LCD bias set command which is 1/6 bias or 1/8 bias for SED15A6 series.

On-chip Power Supply Turn Off Sequence

Before turning the built-in power supply off, to discharge the remaining electric charge of LCD panel and power supply PIN etc., it is recommended to turn on the power save mode employing the following command sequence. You can also turn the built-in power supply off by initializing it using RES pin or the reset command. Here, of SED15A6D0B with built-in power supply being only used, LOW level signal entering RES pin discharges V_{OUT}, thereby introducing shorting across V_{OUT}–V_{DD2} and V_0–V_{SS}. Of SED15A6D1B/SED15A6D2B with external power supply being used, discharge the electric charge by short-circuiting the external power supply to V_{SS} when the power supply is off or power is being saved. (V_{OUT} and V_0 electric charge discharging functions are not in the IC)

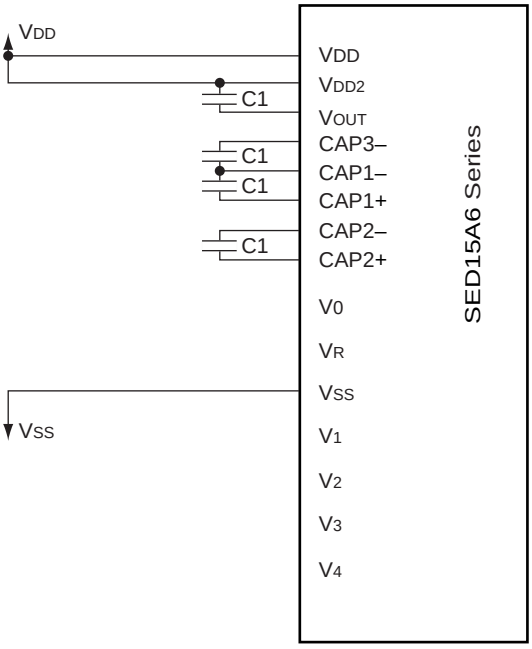
Table 18

Sequence	Contents (command and state)	Command address								
		D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power save command (composite command)
	↓									
Step2	Display all points on	1	0	1	0	0	1	0	1	
	↓									
End	Built-in power OFF	0	0	1	0	1	0	0	0	

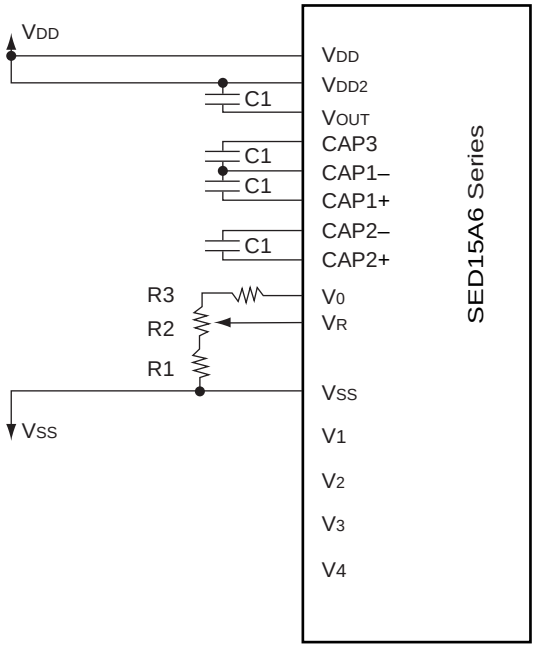
Sample Circuits

1. When the booster, voltage adjustment and V/F circuits are all used [SED15A6D0B]

(1) When built-in V_0 voltage adjusting resistors are used (When $V_{DD2} = V_{DD}$ is boosted 4 times)

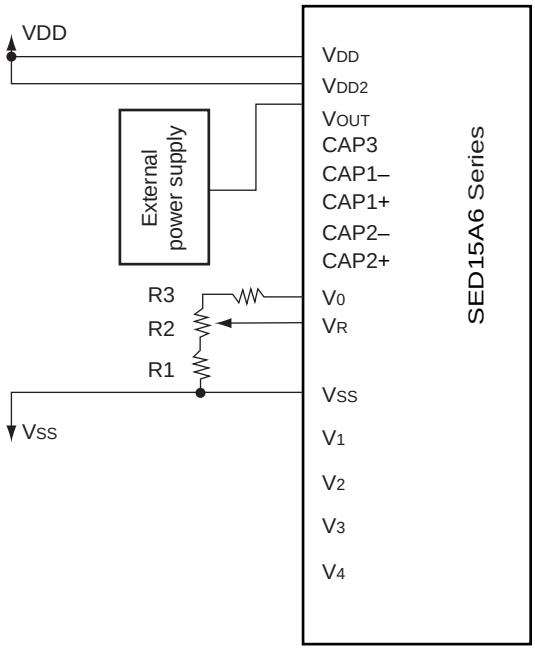


(2) When built-in V_0 voltage adjusting resistors are not used (When $V_{DD2} = V_{DD}$ boosted 4 times)

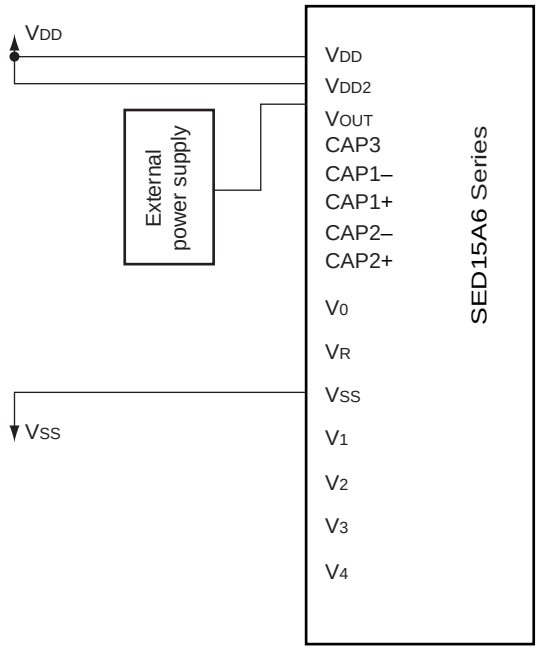


2. When the voltage adjustment and V/F circuits alone are used

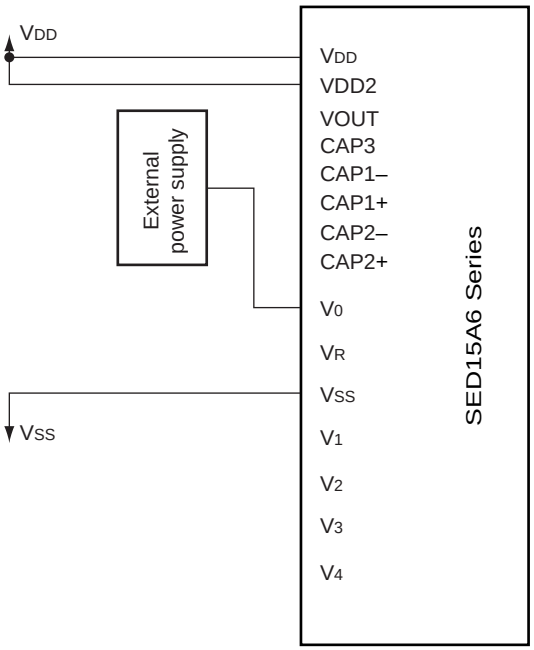
(1) When built-in V_0 voltage adjusting resistors are not used [SED15A6D1B]



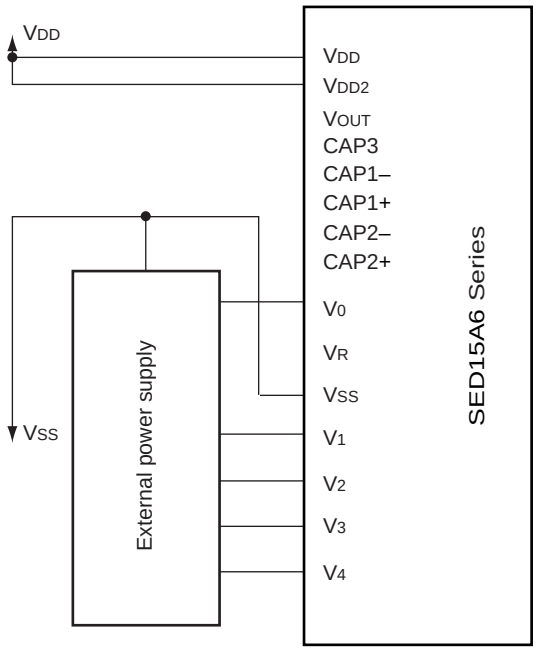
(2) When built-in V_0 voltage adjusting resistors are used Voltage Follower Circuit [SED15A6D1B]



3. When V/F circuit alone is used [SED15A6D1B]



4. When built-in power supply is not used[SED15A6D2B]



* Since V_R pin has a higher impedance, wiring distance must be minimized or shielded wire must be used.

Sample setting
When V_0 is varied between 8 and 9V.

Item	Setting	Unit
C1	1.0 to 4.7	μF

Figure 12

Reset Circuit

When pin goes low, $\overline{RES}$ or when Reset command is used, this LSI is initialized.

Initialized states

- Serial interface internal shift register and counter clear
- Power saver mode is entered.
  - Oscillation circuit is stopped.
  - The LCD power supply circuit is stopped.
  - Display OFF
  - Display all points ON (Display all points ON ON/ OFF command D0 = "1")
  - Segment/common driver outputs go to the V_{SS} level.
- Display normal
- Page address=0H
- Column address=0H
- Display start line address=set at the first line
- Segment driver direction=normal
- Common driver direction=normal
- Read modify write OFF
- Power control register (D2, D1, D0) = (0, 0, 0)
- V_0-resistor ratio register (D2, D1, D0) = (0, 0, 0)
- Electronic volume register (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
- LCD power supply bias ratio = 1/6 bias (SED15A6)
- Test mode is released.

*** Voltage short-circuit across V_{OUT} and V_{DD2} as well as Vo and V_{SS} [allowed only when $\overline{RES}$ pin = LOW level].**

When reset is detected, this LSI is set to above initialized states. However it has no effect on contents of DDRAM. As seen in "Microprocessor Interface (Reference Example)", connect $\overline{RES}$ pin to the reset pin of the MPU and initialize the MPU at the same time. The initialization by $\overline{RES}$ pin is always required during power-on.
If the control signal from MPU is HZ, an overcurrent may flow through the LSI. A protection is required to prevent the HZ signal at the input pin during power-on.
In case the SED15A6 series does not use the on-chip LCD power supply circuit, after $\overline{RES}$ pin is turnd LOW to HIGH, the external LCD power supply must be turned on.

7. COMMANDS

The SED15A6 series identifies the data bus by a combination of A0, $\overline{RD}$ (E), $\overline{WD}$(R/$\overline{W}$) signals.
In the 8080-series MPU interface, the command is activated when a low pulse is input to $\overline{RD}$ pin for reading and when a low pulse is input to $\overline{WD}$ pin for writing. In the 6800-series MPU interface, the SED15A6 series enters a read mode when a high level is input to R/$\overline{W}$ pin and a write mode when a low level is input to R/$\overline{W}$ pin, and the command is activated when a high pulse is input to E pin. Therefore, in the command explanation and command table, the 6800-series MPU interface is different from the 8080-series MPU interface in that $\overline{RD}$(E) becomes "1 (H)" in Display data read command. And when the serial interface is selected, the data is input in sequence starting with D7.
Taking the 8080-series MPU interface as an example, commands will be explained below.

Explanation of commands

Display ON/OFF

This command turns the display ON and OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0 1	Display OFF Display ON

When the Display OFF command is executed when in the Display all points ON mode , Power saver mode is entered. See the section on the Power saver for details.

Display normal/reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	Normal:DDRAM Data HIGH =LCD ON voltage Reverse:DDRAM Data LOW =LCD ON voltage

Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

When the Display all points ON command is executed when in the Display OFF mode, Power saver mode is entered. See the section on the Power saver for details.

Page address set

This command specifies the page address of the DDRAM (refer to Figure 5).
Specifying the page address and column address enables to access a desired bit of the DDRAM. After the last column address (65H), page address incremented by +1 (refer to Figure 4). After the very last address (column = 65H, page = 7H), page address return to 0H.
Page address 8H is the DDRAM area dedicate to the indicator, and only D0 is valid for data change.
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0H
							0	0	0	1	1H
							0	0	1	0	2H
								:			:
							0	1	1	1	7H
							1	0	0	0	8H

Column address set

This command specifies the column address of the DDRAM (refer to Figure 5).
The column address is split into tow sections (the upper 3-bits and lower 4-bits) when it is set (fundamentally, set continuously).
Each time the DDRAM is accessed, the column address automatically increments by +1, making it possible for the MPU to continuously access to the display data. After the last column address (65H) ,column address returns to 00H (refer to Figure 4).
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	*	A6	A5	A4	Upper bit address
						0	A3	A2	A1	A0	Lower bit address

*Disabled bit

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	00H
0	0	0	0	0	0	1	01H
0	0	0	0	0	1	0	02H
			:				:
1	1	0	0	1	0	0	64H
1	1	0	0	1	0	1	65H

Display start line address set

This command is used to specify the display start line address of the DDRAM (refer to Figure 5).
If the display start line address is changed dynamically using this command, then screen scrolling, page swapping can be performed.
See the function explanation in “Line address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	00H
					0	0	0	0	0	1	01H
					0	0	0	0	1	0	02H
							:				:
					1	1	1	1	1	0	3EH
					1	1	1	1	1	1	3FH

Segment driver direction select

This command can reverse the correspondence between the DDRAM column address and the segment driver output.
See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Common driver direction select

This command can reverse the correspondence between the DDRAM line address and the common driver output. See the function explanation in “Line address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

*Disabled bit

Display data read

This command reads 8-bit data from the specified DDRAM address. Since the column address is automatically incremented by +1 after each read ,the MPU can continuously read multiple-word data. One dummy read is required immediately after the address has been set. See the function explanation in “Access to DDRAM and internal registers” and “DDRAM and page/column address circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

Display data write

This command writes 8-bit data to the specified DDRAM address. Since the column address is automatically incremented by +1 after each write ,the MPU can continuously write multiple-word data. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

Read modify write

This command is used paired with End command. Once this command is issued, the column address is not incremented by Display data read command, but is incremented by Display data write command. This mode is maintained until End command is issued. When End command is issued, the column address returns to the address it was at when Read modify write command was issued. This function makes it possible to reduce the MPU load when there are the data to change repeatedly in a specified display region, such as blinking cursor.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

*When End command is issued, only column address returns to the address it was at when Read modify write command was issued, but page address does not return. Consequently, Read modify Write mode cannot be used over pages. When you want to maintain the current page address after a read modify write operation done on a column address between the start and the final column address (65H), you must specify the page address again after the operation is over.

*Even if Read modify write mode, other commands besides Display data read/write can also be used. However, Column address set command cannot be used.

The sequence for cursor display

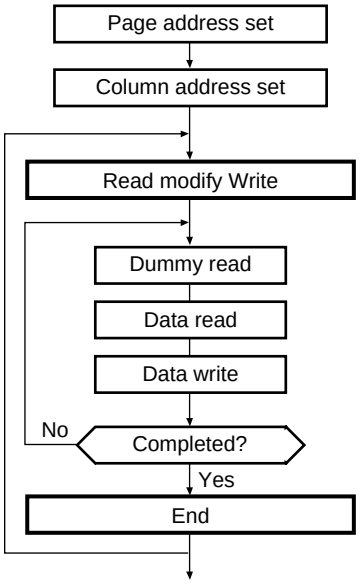


Figure 13

End

This command releases the Read modify write mode, and returns the column address to the address it was when Read modify write command was issued .

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

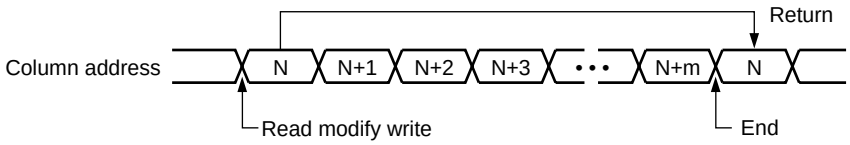


Figure 14

Power control set

This command sets the on-chip power supply function ON/OFF. See the function explanation in “Power supply circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Mode
0	1	0	0	0	1	0	1	0			Booster : OFF
								1			Booster : ON
									0		Voltage regulator : OFF
									1		Voltage regulator : ON
										0	Voltage follower : OFF
										1	Voltage follower : ON

V0-resistor ratio set

This command sets the internal resistor ratio “Rb/Ra” for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in “Power supply circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra : V_0 voltage
0	1	0	0	0	1	0	0	0	0	0	small low
								0	0	1	
								0	1	0	
								0	1	1	↓ ↓
								1	0	0	
								1	0	1	
								1	1	0	large high
								1	1	1	External resistor mode

Electronic volume

This command sets a value of electronic volume "α" for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in "Power supply circuit", for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	α : V0 voltage
0	1	0	1	0	0	0	0	0	0	0	31 low
						0	0	0	0	1	30
						0	0	0	1	0	29
								↓			↓ ↓
						1	1	1	1	0	1
						1	1	1	1	1	0 high

LCD bias set

This command selects the voltage bias ratio required for the LCD. This command is enabled when the voltage follower circuit operates.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Bias SED15A6
0	1	0	1	0	1	0	0	0	1	0	1/8 bias
										1	1/6 bias

Power saver

When the display all points ON command is executed when in the display OFF mode, power saver mode is entered, and the power consumption can be greatly reduced.
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the MPU. The internal states in the power saver mode is as follows:

- The oscillation circuit is stopped.
- The LCD power supply circuit is stopped.
- The LCD driver circuit is stopped and segment/common driver outputs output the V_{SS} level.
- The display data and operation mode before execution of the Power saver command are held, and the MPU can access to the DDRAM and internal registers.

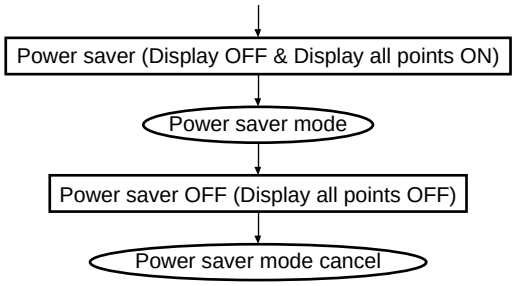


Figure 15

Reset

When this command is issued, this LSI is initialized. This command, however, is not used for introducing short circuit across V_{OUT} and V_{DD2} or V_0 and V_{SS} (only when $\overline{RES}$ pin = LOW). Also note that initialization of the display data RAM does not take place in parallel with initialization of the LSI. See the function explanation in "Reset circuit", for detail.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

When initializing the LSI while power is turned on, reset signal to the $\overline{RES}$ pin is used. This signal cannot be replaced by the reset command.

NOP

Non-operation command

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for LSI chip testing. Please do not use. If the test command is issued by accident, it can be cleared by applying an LOW signal to the pin, or by issuing the Reset command or the Display ON/OFF command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

* Disabled bit

(Note):
The SED15A6 series chip maintain their operating modes ,but excessive external noise,etc.,may happen to change them. Thus in the packaging and system design it is necessary to suppress the noise or take measures to prevent the noise. Moreover, it is recommended that the operating modes are refreshed periodically to prevent the effects of unanticipated noise.

Command Table

Table 19

Command	Code											Function
	A0	XR	XW	D7	D6	D5	D4	D3	D2	D1	D0	
(1)Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display 0:OFF, 1:ON
(2)Display normal/reverce	0	1	0	1	0	1	0	0	1	1	0 1	LCD display 0:normal, 1:reverce
(3)Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	LCD display 0:normal display, 1:all points ON
(4)Page address set	0	1	0	1	0	1	1	address				Sets the DDRAM page address
(5)Column address set Upper 3-bit address	0	1	0	0	0	0	1	*	address			Sets the DDRAM column address
Column address set Lower 4-bit address	0	1	0	0	0	0	0	address				
(6)Display start line address set	0	1	0	0	1	address						Sets the DDRAM display start line address.
(7)Segment driver directuin select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the correspondence between the DDRAM column address and the SEG driver output. 0:normal, 1:reverse
(8)Common driver direction select	0	1	0	1	1	0	0	0 1	*	*	*	Sets the correspondence between the DDRAM line address and the COM driver output. 0:normal, 1:reverse
(9)Display data read	1	0	1	Read data								Reads from the DDRAM.
(10)Display data write	1	1	0	Wtite data								Writes to the DDRAM.
(11)Read modify write	0	1	0	1	1	1	0	0	0	0	0	Column address increment at write:+1, at read:0.
(12)End	0	1	0	1	1	1	0	1	1	1	0	Releases Read modify write mode.
(13)Power control set	0	1	0	0	0	1	0	1	Operating mode			Sets the on-chip power supply circuit operating mode.
(14)V_0-resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Sets the V_0-resistor ratio value.
(15)Electronic volume	0	1	0	1	0	0	Electronic volume value					Sets the electronic volume value.
(16)LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. SED15A6 0:1/8bias, 1:1/6bias
(17)Power saver	-	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Display all points ON
(18)Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(19)NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation
(20)Test	0	1	0	1	1	*	1	*	*	*	*	IC test command. Do not use.

(Note)*:disabled bit

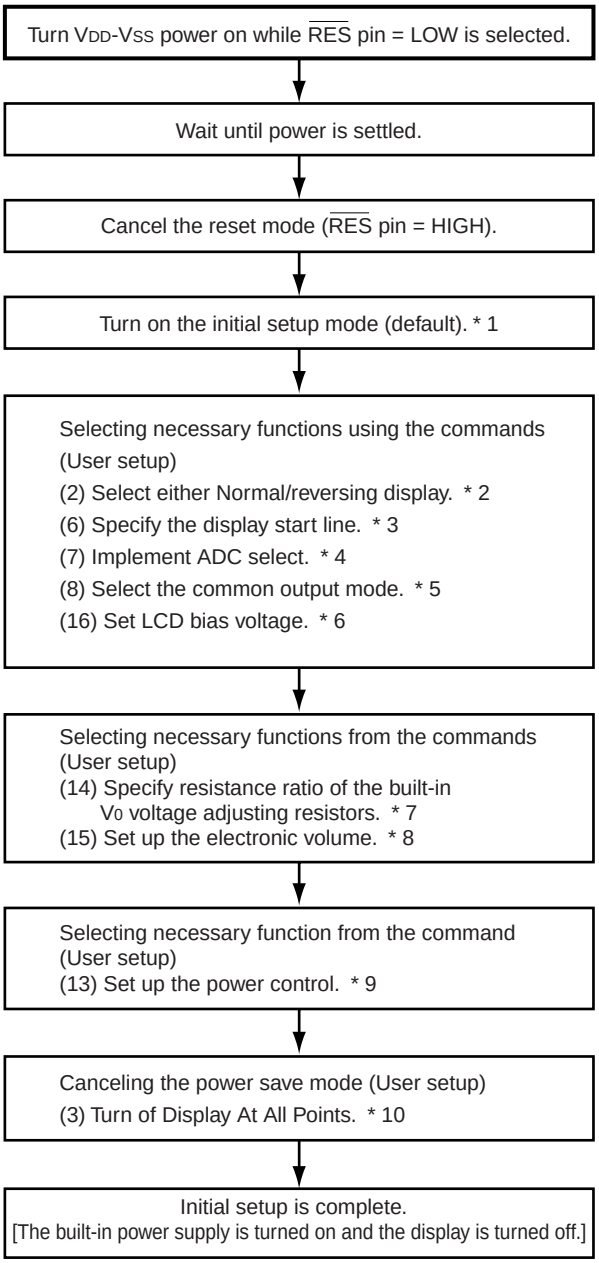
8. AN EXAMPLE OF FUNCTION SETUP USING COMMANDS

Instruction Setup Example

(For your reference)

Note: If charge remains on the smoothing capacitor connected across the LCD drive voltage output pin and V_{DD2} pin, troubles (such as momentary blackening) can occur on the display screen during its powering on process. In order to avoid such troubles, it is recommended to implement the following flow.

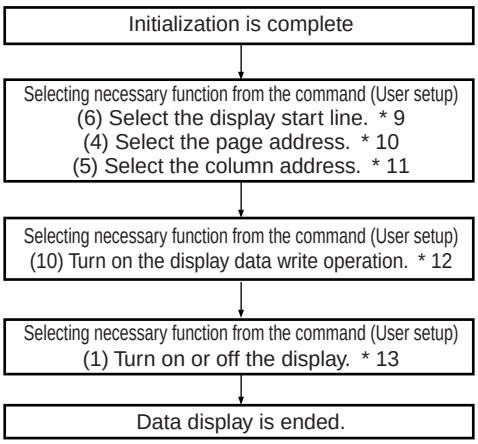
1. When switching to the built-in power supply takes place immediately after powering on:



Note: Reference Items

* 1: Refer to the “Description of Functions; Reset Circuit” .
  In the initial setup mode (default), too, contents of the display data RAM is still uncertain.
* 2: Refer to the “(2) Normal/reversing Display” in the “Description of Commands”.
* 3: Refer to the “(6) Display Line Setup” in the “Description of Commands”.
* 4: Refer to the “(7) ADC Select” in the “Description of Commands”.
* 5: Refer to the “(8) Common Output Mode Select” in the “Description of Commands”.
* 6: Refer to the “(16) LCD Bias Set” in the “Description of Commands”.
* 7: Refer to the “Description of Functions; Power Supply Circuit” and “Description of Commands - (14) Specifying resistance ratio of built-in V0 voltage adjusting resistors”.
* 8: Refer to the “Description of Functions; Power Supply Circuit” and “Description of Commands - (15) Electronic Volume” .
* 9: Refer to the “Description of Functions; Power Supply Circuit” and “Description of Commands - (13) Setting Up Power Control” .
* 10: Refer to the “(17) Power Save” in the “Description of Commands” .

2. Data display

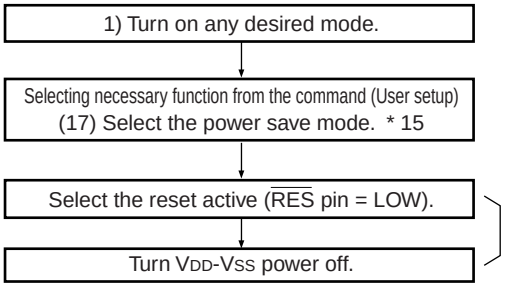


Note: Reference Items

* 9: Refer to the "(6) Setup of Display Start Line" in the "Description of Commands".
* 10: Refer to the "(4) Page Address Set" in the "Description of Commands".
* 11: Refer to the "(5) Column Address Set" in the "Description of Commands".
* 12: Refer to the "(10) Display Data Write" in the "Description of Commands".
* 13: Refer to the "(1) Display Data ON/OFF" in the "Description of Commands".

The all-white display of data should be avoided as much as practicable right after the display mode is turned on (right after the display has been turned on).

3. Powering off * 14

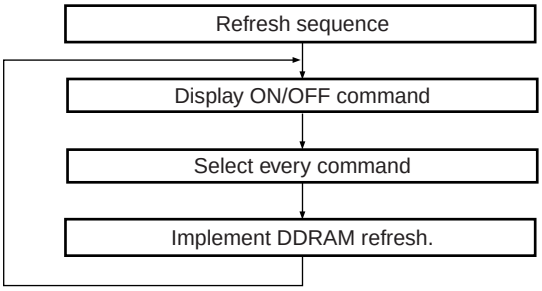


The time (tL) provided between turning on of the reset active and turning off of V_{DD}-V_{SS} power (V_{DD}-V_{SS} = 1.8V) must be longer than the time required for V_0-V_4 potential to go lower (tH) than the threshold voltage set on the LCD (usually 1V).
For "t_H", see the "Reference data" in the following section. If "t_H" is excessively long, it must be cut short by installing a resistor across V_0 and V_{SS}.

Note:

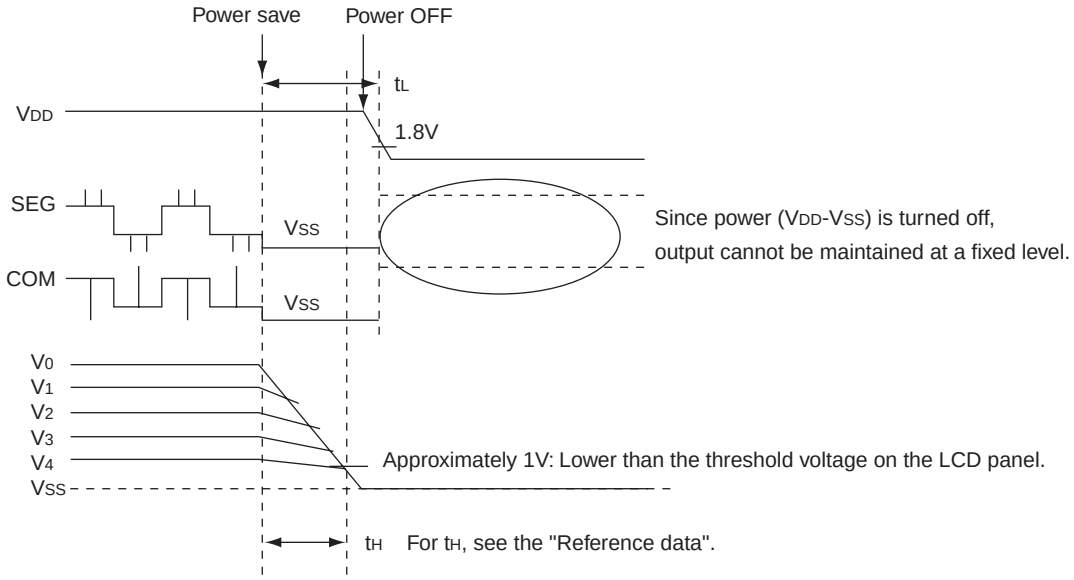
* 14: This IC is provided on the power supply V_{DD}-V_{SS} logic circuit to offer control over the V_0-V_{SS} drivers on the LCD power supply. Thus, if the power supply V_0-V_{SS} is turned off while voltage is still remaining on the LCD power supply V_0-V_{SS}, the drivers (both COM and SEG) can generate uncontrolled output. Make sure to observe the following powering off procedure:
  • Turn off the built-in power supply first, then, after making sure that potential on V_0 to V_4 is lower than the LCD panel threshold voltage, turn the IC power (V_{DD}-V_{SS}) off. Also refer to the "Power Supply Circuit" in the Description of Functions.
* 15: Refer to the "(17) Power Save" in the "Description of Commands".
After entering the power save command, you must implement reset procedure from the $\overline{RES}$ pin before turning off V_{DD}-V_{SS} power.

4. Refresh
It is recommended to implement the refresh sequence on a regular basis.

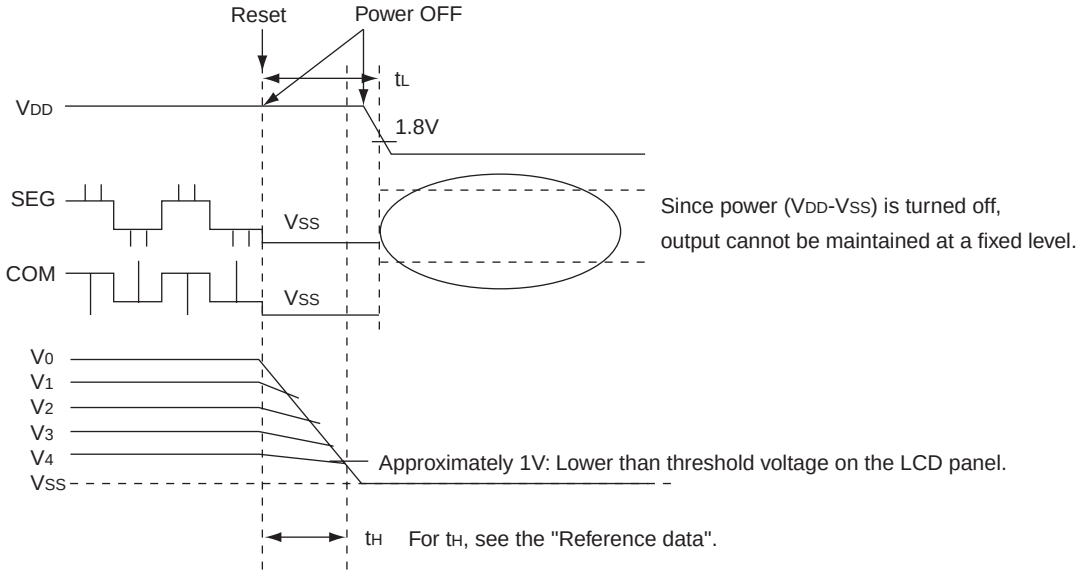


5. Precautions on powering off
<Powering off (V_{DD}-V_{SS}) off>
Turn the power (V_0-V_{SS}) save mode off -> Then, turn the power (V_{DD}-V_{SS}) off.
* The requirement "$t_L > t_H$" must be strictly observed.
* If "$t_L < t_H$", display failures can result.

t_L must be specified on software from MPU.
t_H depends on discharging capability of the drivers. See the "Reference data" in the following section. It also depends on a given LCD panel, thus actual timing must be determined after experimenting on your LCD panel.



<When powering off (V_{DD}-V_{SS}) is not available with the command>
Turn off the reset mode (LCD power (V_0-V_{SS}) system).
-> Then, turn power (V_{DD}-V_{SS}) off.
* The requirement "$t_L > t_H$" must be observed.
* When specifying t_L, measures such as extending fall time of power supply (V_{DD}-V_{SS}) should be considered. t_H depends on the drivers' discharging capability. See the "Reference data" in the following section. It also depends on model of a given LCD panel, thus actual timing must be determined after experimentation on your LCD panel.



6. Reference data
The following data is for your reference alone. t_H is significantly affected by capacity of V_0 pin, thus you must verify appropriateness of a selected t_H on the panel being equipped with the pin.

[Conditions: V_{DD} = 1.8V, voltage is tripled and capacity of the boosting capacitor = 1.0 µF]

When V_0 is under no-load, t_H per voltage is 22 µs. It becomes 220 µs when V_0 = 9V.
Capacity dependency is 1 pF. Δt_H per voltage is 50 ns.

An example: When V_{DD} = 1.8V, V_0 = 8V and V_0 pin capacity [board capacity] (CL) = 100 pF.

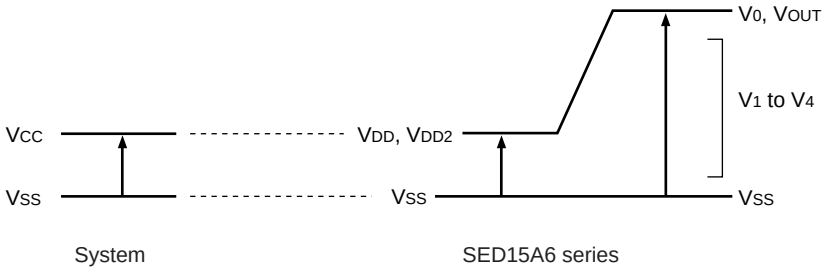
$t_H = 22\mu s \times 8V + 50ns \times 100pF \times 8V = 216\mu s$

9. ABSOLUTE MAXIMUM RATING

Unless otherwise noted, V_{SS} = 0V.

Table 20

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DD}	–0.3 to 0.6	V
Power supply voltage (2)		V_{DD2}	–0.3 to 0.6	V
	Double boosting		–0.3 to 5.0	
	Triple boosting		–0.3 to 3.3	
	Quadruple boosting		–0.3 to 2.5	
Power supply voltage (3)		V_0, V_{OUT}	–0.3 to 10.0	V
Power supply voltage (4)		V_1, V_2, V_3, V_4	–0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	–40 to 85	°C
Storage temperature	TCP	T_{STR}	–55 to 100	°C
	Bare chip		–55 to 125	



Notes and Conditions

1. V_{SS} = 0V is assumed for every voltage indicated above.
2. Voltage V_0, V_1, V_2, V_3, V_4 must always keep up the condition of $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ and $V_{OUT} \geqq V_0 \geqq V_{SS}$.
3. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

10. DC CHARACTERISTICS

Table 21 V_{SS}=0V, V_{DD}=3V±10%, Ta=–40~85°C unless otherwise noted.

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Supply voltage(1)	Recommended operation	V_{DD}	(V_{SS} is used as the reference)	2.7	–	3.3	V	V_{DD} *1
	Operational available	V_{DD}	(V_{SS} is used as the reference)	1.8	–	3.6	V	
Supply voltage(2)	Recommended operation	V_{DD2}	(V_{SS} is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
Supply voltage(3)	Operational available	V_0	(V_{SS} is used as the reference)	4.5	–	9.0		V_0 *2
	Operational available	V_1, V_2	(V_{SS} is used as the reference)	0.6×V_0	–	V_0	V	V_1, V_2
	Operational available	V_3, V_4	(V_{SS} is used as the reference)	V_{SS}	–	0.4×V_0		V_3, V_4
High-level input voltage		V_{IH}		0.7×V_{DD}	–	V_{DD}	V	*3
Low-level input voltage		V_{IL}		V_{SS}	–	0.3×V_{DD}	V	
High-level output voltage		V_{OH}	I_{OH}=–0.5mA	0.7×V_{DD}	–	V_{DD}	V	*4
Low-level output voltage		V_{OL}	I_{OL}=0.5mA	V_{SS}	–	0.3×V_{DD}	V	
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}	–1.0	–	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	–	3.0	µA	*6
LCD driver ON resistance		R_{ON}	V_0=7.0V Ta=25°C	–	2.0	5.0	KΩ	SEGn, COMn *7
Static current consumption		I_{DDQ}	Ta=25°C	–	0.01	5.0	µA	V_{DD},V_{DD2}
Output leak current		I_{0Q}	V_0=7.0V Ta=25°C	–	0.01	15.0	µA	V_0
Input terminal capacitance		C_{IN}	Ta=25°C, f =1MHz		10.0	15.0	pF	
Oscillation frequency	Built-in oscillation	f_{OSC}	Ta=25°C	31.68	35.20	38.72	kHz	*8
	External input	f_{CL}		35.2	70.4	140.8		CL *8

Table 22

Item		Symbol	Condition	Standard value			Unit	Pin used
				Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{DD2}	When voltage is doubled (Vss is used as the reference)	1.8	–	5.0	V	V_{DD2} *1
			When voltage is tripled (Vss is used as the reference)	1.8	–	3.3		
			When voltage is quadrupled (Vss is used as the reference)	1.8	–	2.5		
	Boosted output voltage	V_{OUT}	(Vss is used as the reference)	–	–	10.0		V_{OUT}
	Operating current of voltage adjustment circuit	V_{OUT}	(Vss is used as the reference)	5.0	–	10.0		V_{OUT}
	V/F circuit operating voltage	V_0	(Vss is used as the reference)	4.5	–	9.0		V_0 *9
	Reference voltage	V_{REG}	–0.1%/°C Ta=25°C (Vss is used as the reference)	1.16	1.2	1.24		*10

Note 1: V_{SS} = 0V is assumed for every voltage indicated.

Note 2: Voltages V_0, V_1, V_2, V_3 and V_4 must conform to the requirements that $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS}$ as well as $V_{OUT} \geqq V_0 \geqq V_{SS}$.

Note 3: Operating the LSI is operated beyond the maximum absolute rating can damage it permanently. In the normal operation, it is desirable to use the LSI in compliance with its electric characteristics. If the LSI is used under any conditions conflicting with its electric characteristics, not only its malfunctioning but also serious loss of reliability can result.

◊ Dynamic operating current (1) - When display is turned on with the built-in power supply being disconnected [Ta = 25°C and output under no-load].
Following shows current consumed by entire IC when external power supply is used.

Table 23-1 Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	23	48	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	25	50		

Table 23-2 Display: Checker pattern

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=7.2V	–	26	54	µA	*11
	I_{SS}(1)	V_{DD}=V_{DD2}=1.8V, V_0=9.0V	–	29	57		

◊ Dynamic operating current (2) - When display is turned on with the built-in power supply being connected [Ta = 25°C and output under no-load].

Table 24-1 Display: All-white

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	68	101	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	79	112		

Table 24-2 Display: Checker pattern

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	75	103	µA	*12
	I_{SS}(2)	V_{DD}=1.8V,V_{DD2}=3.3V, V_0=7.2V, and voltage is tripled.	–	87	112		

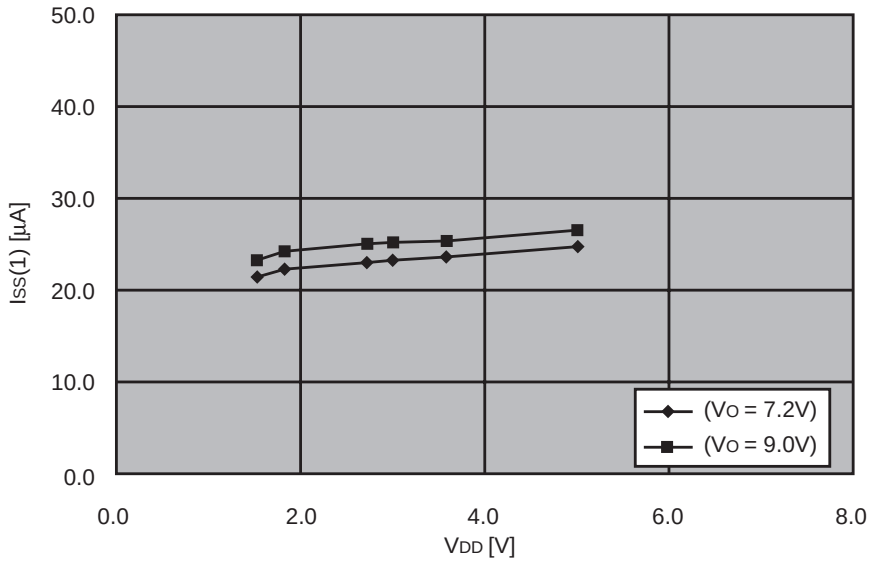
◊ Current consumption in the power save mode [Ta = 25°C and output under no-load]

Table 25

Item	Symbol	Requirement	Min.	Typ.	Max.	Unit	Remarks
SED15A6***	I_{SS}(3)	V_{DD}=V_{DD2}=1.8~3.6V	–	0.01	5	µA	

[Reference data 1]

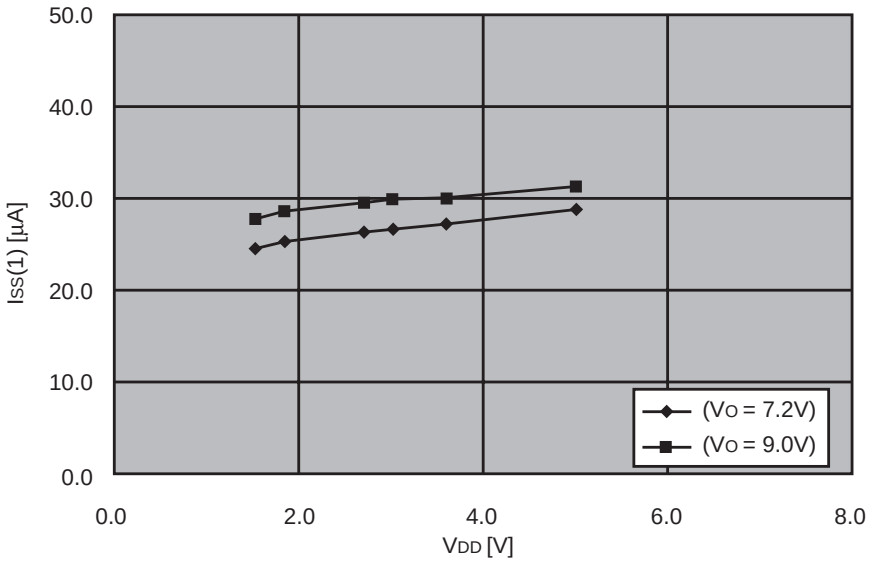
◊ Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (All-white display)



Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}-V_{SS} = 1.8V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: All-white.
Remarks: See * 11.

Figure 16

◊ Dynamic operating current (1) - When LCD display is turned on with external power supply being connected (Checker pattern display)

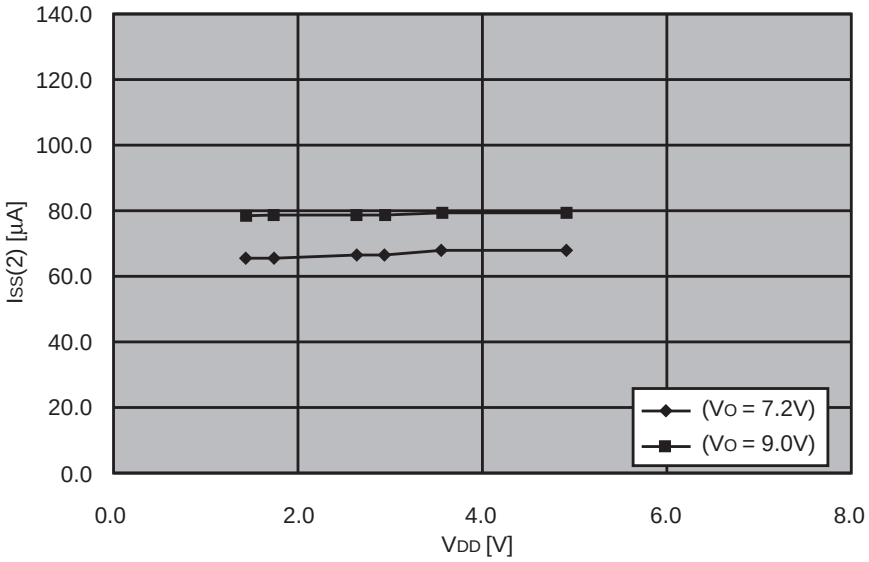


Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}-V_{SS} = 1.8V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: Checker.
Remarks: See * 11.

Figure 17

[Reference data 2]

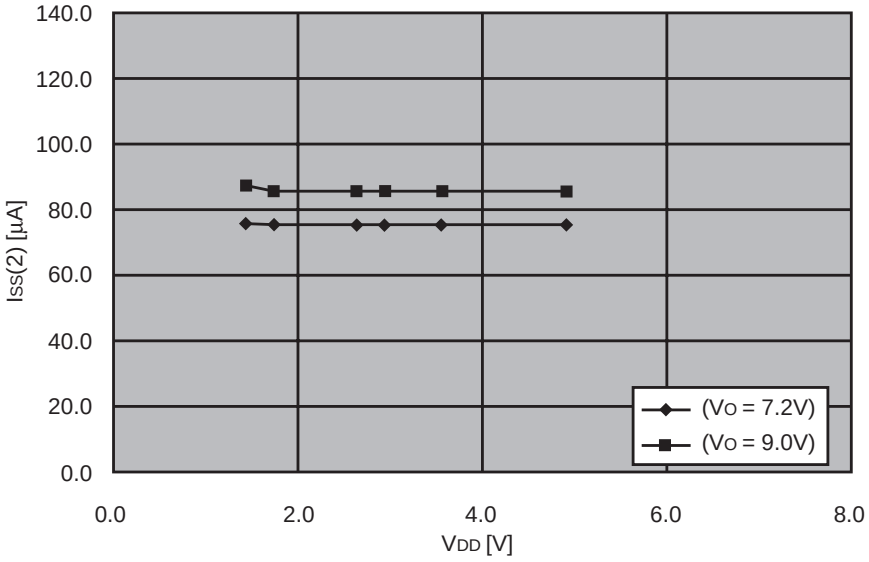
◊ Dynamic operating current (2) - When LCD display is turned on with built-in power supply being connected (All-white display)



Conditions:
Built-in power supply ON
Voltage tripled
V_{DD2}-V_{SS} = 3.3V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: All-white.
Remarks: See * 12.

Figure 18

◊ Dynamic operating current (2) - When LCD display is turned on with built-in power supply being connected (Checker pattern display)

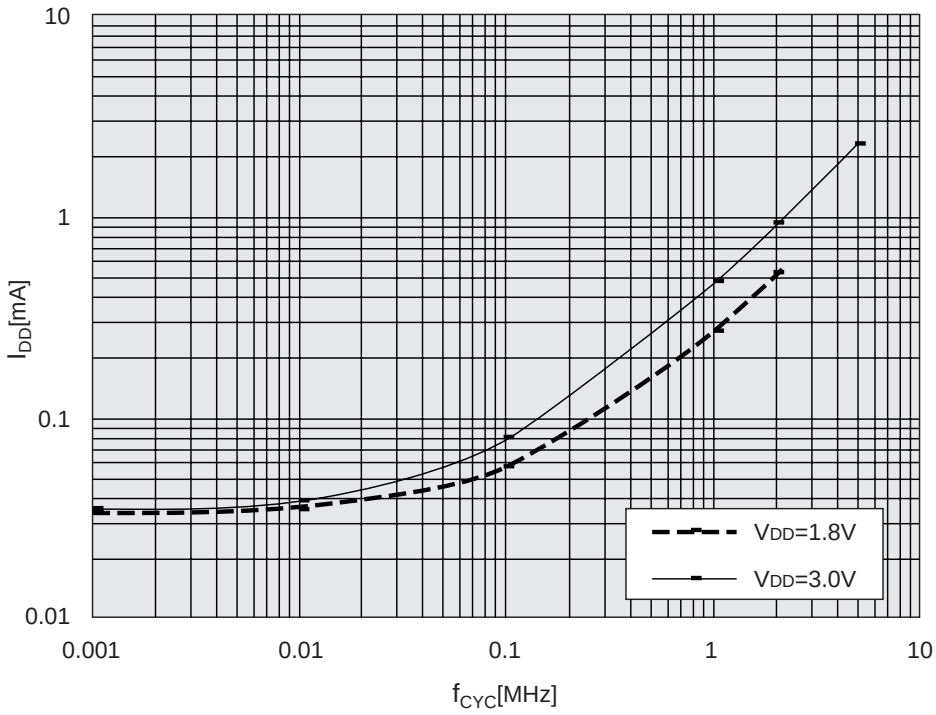


Conditions:
Built-in power supply ON
Voltage tripled
V_{DD2}-V_{SS} = 3.3V
V_{DD}-V_{SS} = 1.8V
V_0-V_{SS} = 7.2V
V_0-V_{SS} = 9.0V
Ta = 25°C
Display pattern: Checker.
Remarks: See * 12.

Figure 19

[Reference data 3]

◊ Dynamic operating current (3) - During an access is being made



This chart shows current consumption when the checker pattern write is constantly implemented in f_{CYC}.
Iss (1) alone is consumed when an access is not taking place.

Conditions:
Built-in power supply OFF
External power supply ON
V_{DD2}–V_{SS}=3.0V
V_0–V_{SS}=9.0V
Ta=25°C

Figure 20

[Reference data 4]
◊ Operating voltage range of V_{DD} and V_0 systems.

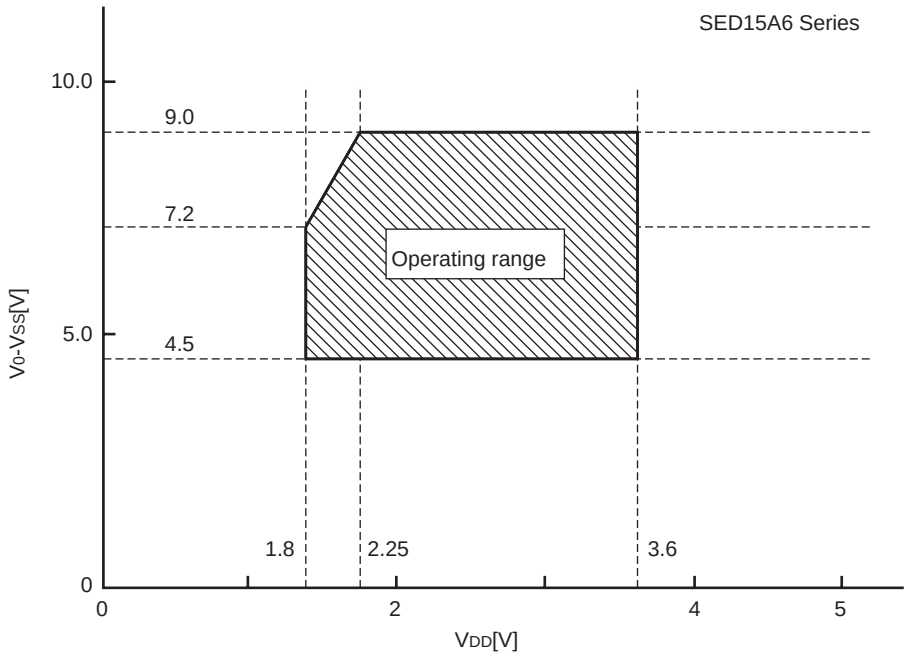


Figure 21

[Reference items]

* 1 : Although wide operating voltage range is warranted, an exemption to it is when an access made by MPU is accompanied with radical voltage fluctuations.
* 2 : See Figure 21 for the operating voltage range of V_{DD} and V_0 systems. It is applicable when an external power supply is used.
* 3 : A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), CS, CL, C86, P/S and $\overline{RES}$ pins. $V_{IH} = 0.8 \times V_{DD}$ to V_{DD}, $V_{IL} = V_{SS}$ to $0.2 \times V_{DD}$ when $V_{DD} = 1.8V$ to 2.7V.
* 4 : D0 to D7 pins. $I_{OH} = -0.25mA$, $I_{OL} = 0.25mA$ when $V_{DD} = 1.8V$ to 2.7V.
* 5 : A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, C86, CL and $\overline{RES}$ pins.
* 6 : It is applicable when D0 to D5, D6 (SCL) and D7 (SI) pins are placed in high impedance.
* 7 : It represents the resistance value to be employed when 0.1V is applied across the output pin SEGn or COMn and respective power terminals (V_1, V_2, V_3 and V4). It must be selected within the operating voltage range (3). $R_{ON} = 0.1V/\Delta I$ (ΔI represents the current conducted when 0.1V is applied when the power supply is turned on).
* 8 : For the relationship between the oscillating frequency and frame frequency, refer to Table 6. External inputs listed in the standard value space are recommended values.
* 9 : Adjustment of the V_0 voltage adjustment circuit must be done within the operating voltage range of the voltage follower circuit.
* 10 : The built-in reference voltage source of the V_0 voltage adjustment circuit. Two types of V_{REG} temperature gradients are supported by the SED15A6; (1) Approximately –0.1%/°C and (2) External input.
* 11/12 : The built-in oscillation circuit is used. It indicates current consumed by the independent IC when the display is turned on. Current consumption of the SED15A6 indicated here is one when the 1/6 bias mode is turned on. It does not includes current consumed due to the LCD panel capacity or wiring capacity (driver output is under no-load). These values are applicable when an access is not made by MPU.
* 12 : These values are applicable when the V_0 voltage adjusting built-in resistors are used on an SED15A6 model with V_{REG} optional temperature gradient of –0.1%/°C.

11. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080-series MPU)

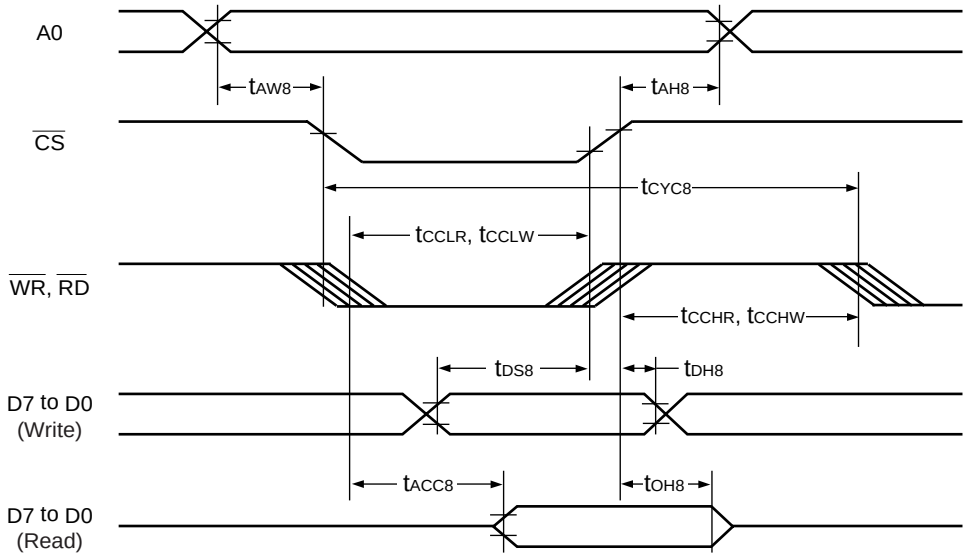


Figure 22

Table 26 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		500	–	
Control LOW pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		100	–	
Control LOW pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		200	–	
Control HIGH pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		100	–	
Control HIGH pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		100	–	
Data setup time	D7 to D0	t_{DS8}		70	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	180	
Output disable time		t_{OH8}		10	100	

Table 27 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		1000	–	
Control LOW pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		150	–	
Control LOW pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		300	–	
Control HIGH pulse width($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		150	–	
Control HIGH pulse width($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		150	–	
Data setup time	D7 to D0	t_{DS8}		120	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	260	
Output disable time		t_{OH8}		10	200	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) $\leqq$ (t_{CYC8}-t_{CCLW}-t_{CCHW}) or (t_r, t_f) $\leqq$ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
*3. t_{CCLW} and t_{CCLR} are specified by the overlap period in which $\overline{CS}$ is "0" and $\overline{WR}$, $\overline{RD}$ are "0".
*4. Timing of A0 is determined by the overlap period in which $\overline{CS}$ is LOW and $\overline{WR}$ and $\overline{RD}$ are LOW, too.

System Bus Read/Write Characteristics 2 (For the 6800-series MPU)

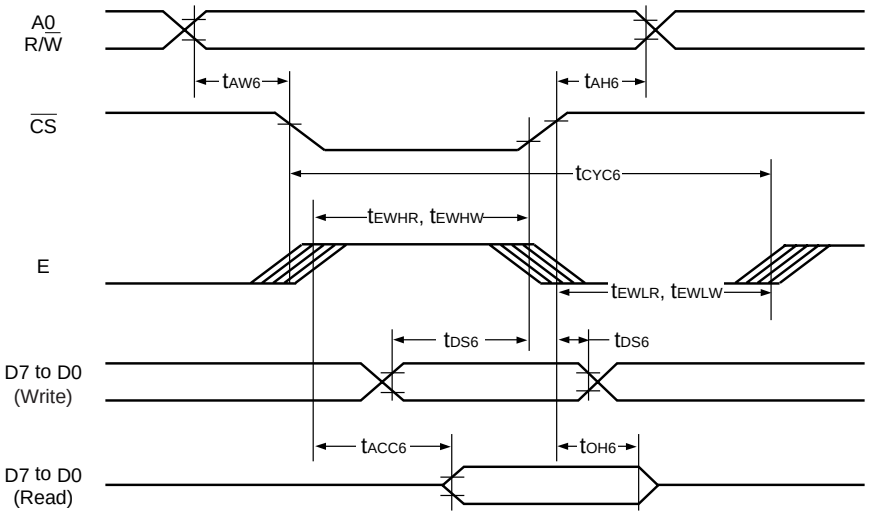


Figure 23

Table 28 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		500	–	
Enable	width	E	t_{EWHW}		100	–	
HIGH pulse width	Read		t_{EWHR}		200	–	
Enable	width		t_{EWLW}		100	–	
LOW pulse width	Read		t_{EWLR}		100	–	
Data setup time		D7 to D0	t_{DS6}		70	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	180	
Output disable time			t_{OH6}		10	100	

Table 29 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		1000	–	
Enable	width	E	t_{EWHW}		150	–	
HIGH pulse width	Read		t_{EWHR}		300	–	
Enable	width		t_{EWLW}		150	–	
LOW pulse width	Read		t_{EWLR}		150	–	
Data setup time		D7 to D0	t_{DS6}		120	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	260	
Output disable time			t_{OH6}		10	200	

* 1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) ≧ (t_{CYC6}-t_{EWHW}-t_{EWLW}) or (t_r, t_f) ≧ (t_{CYC6}-t_{EWHR}-t_{EWLR}).
* 2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
* 3. t_{EWHW} and t_{EWHR} are specified by the overlap period in which $\overline{CS}$ is "0" and E is "1".
* 4. Timing of A_0 is determined by the overlap period in which $\overline{CS}$ is LOW and E is HIGH.

Serial interface

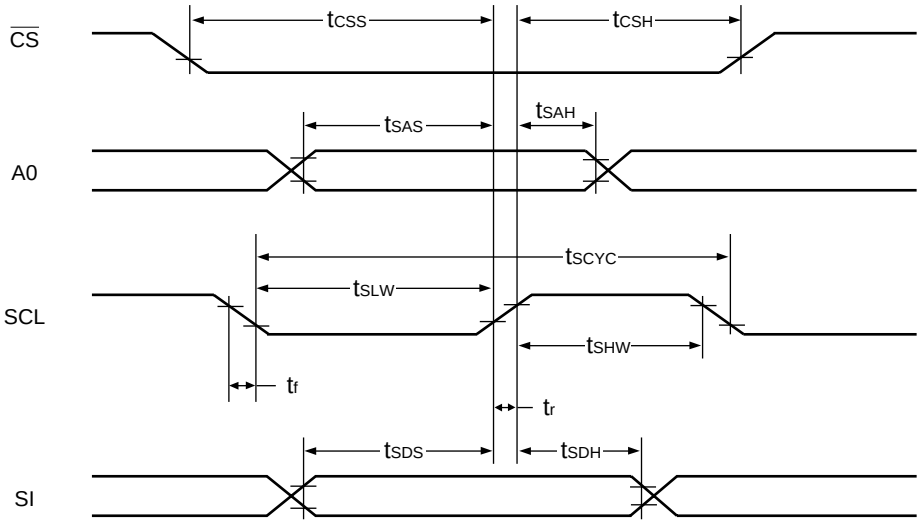


Figure 24

Table 30 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		125	–	ns
Serial clock HIGH pulse width		t_{SHW}		50	–	
Serial clock LOW pulse width		t_{SLW}		50	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		75	–	
		t_{CSH}		75	–	

Table 31 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		200	–	ns
Serial clock HIGH pulse width		t_{SHW}		75	–	
Serial clock LOW pulse width		t_{SLW}		75	–	
Address setup time	A0	t_{SAS}		75	–	
Address hold time		t_{SAH}		75	–	
Data setup time	SI	t_{SDS}		50	–	
Data hold time		t_{SDH}		50	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		100	–	
		t_{CSH}		100	–	

Note : 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Reset timing

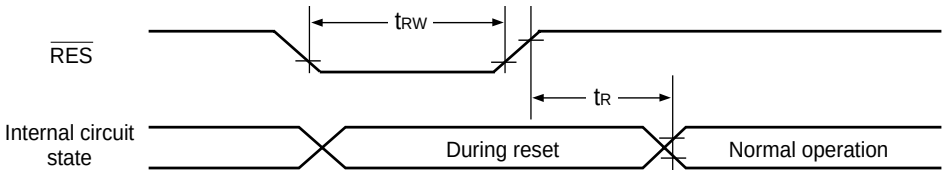


Figure 25

Table 32 [V_{DD}=2.7V to 3.6V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	–	

Table 33 [V_{DD}=1.8V to 2.7V, Ta=–40 to 85°C]

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1500	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1500	–	

Note : 1. The input Signal rise and fall times must be with in 15ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

12. MPU INTERFACE (EXAMPLES)

The SED15A6 series can be directly connected to the 80 series MPU or 68 series MPU. Adding a serial interface allows you to drive the SED15A6 with less number of signal lines.

After initialization is completed from the $\overline{RES}$ pin, make sure that respective input pins on the SED15A6 series are normally controlled.

(1) 80 series MPU

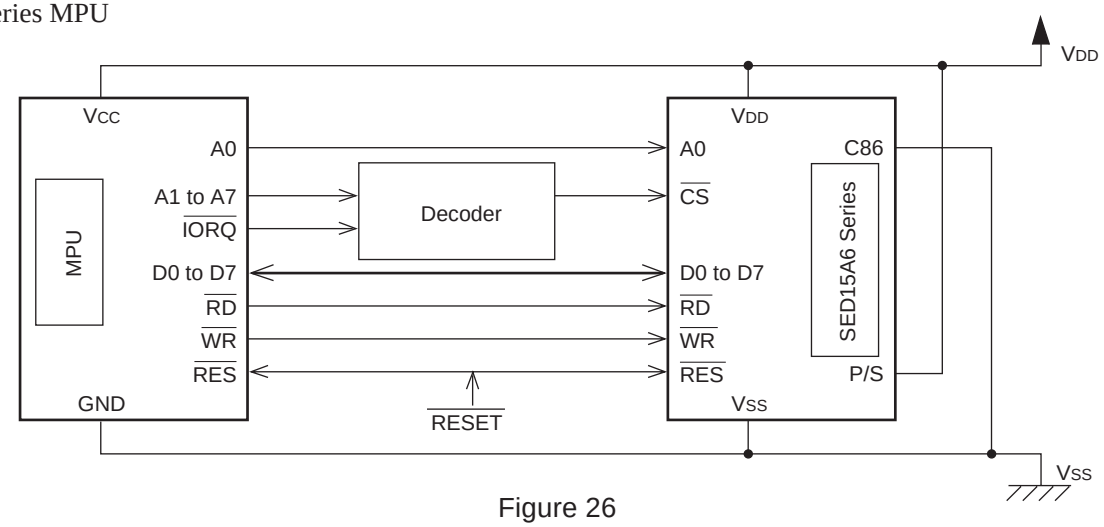


Figure 26

(2) 68 series MPU

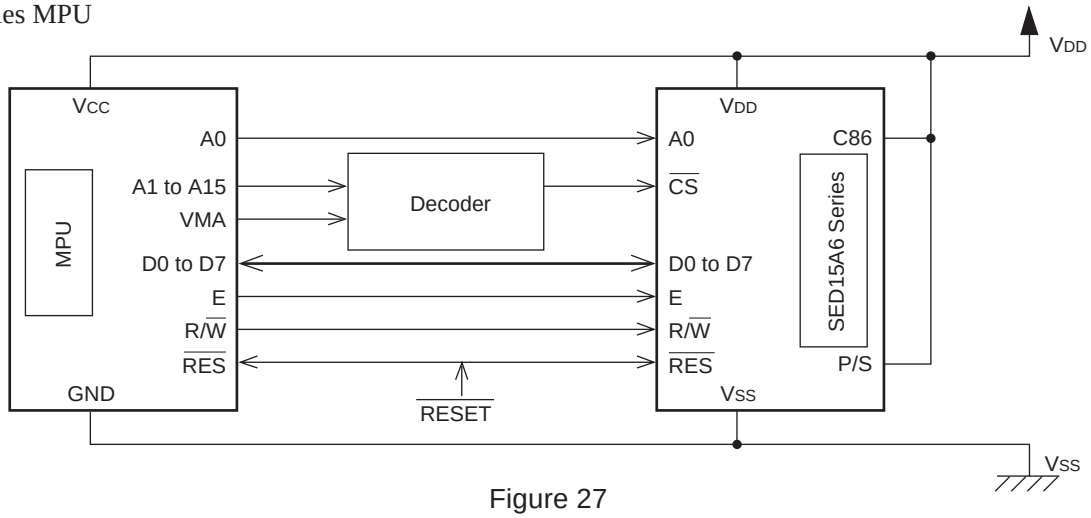


Figure 27

(3) Serial interface

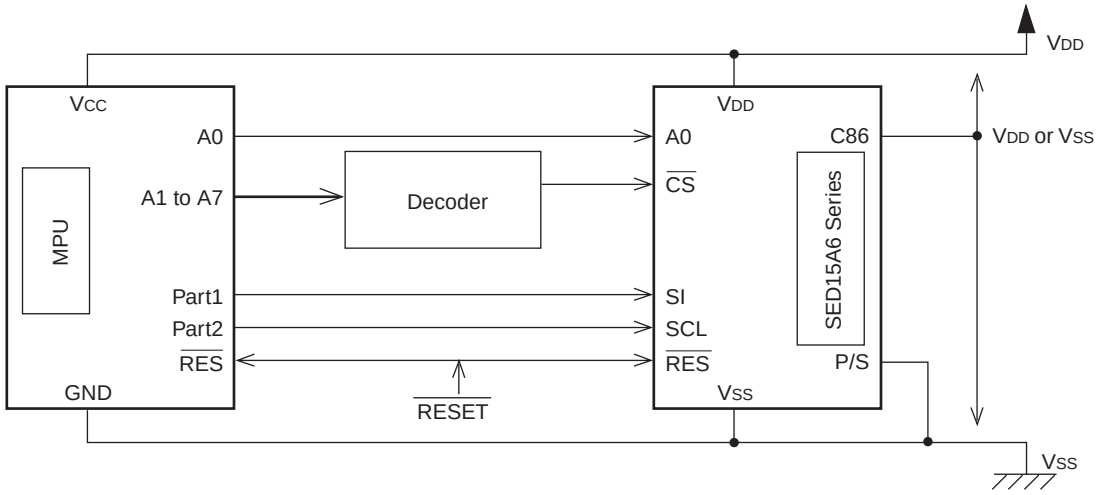


Figure 28