13. SED15B1 Series

Contents

1. DESCRIPTION

The SED15B1 series is a single-chip liquid crystal display (=LCD) driver for dot-matrix LCDs that can be connected directly to a microprocessor (=MPU) bus. It accepts 8-bit parallel or serial display data from a MPU, stores it in an on-chip display data RAM (=DDRAM), and generates a LCD drive signal independent of the MPU clock.
The use of the on-chip DDRAM of 65×132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip DDRAM bits offer high flexibility in graphic display.
The SED15B1 series does not need external operation clock for DDRAM read/write operations, and has a on-chip LCD power supply circuit featuring very low current consumption with few external components, and moreover has a on-chip CR oscillator circuit.
Consequently, the SED15B1 can be realize a high-performance handy display system with a minimum current consumption and the fewest components.

2. FEATURES

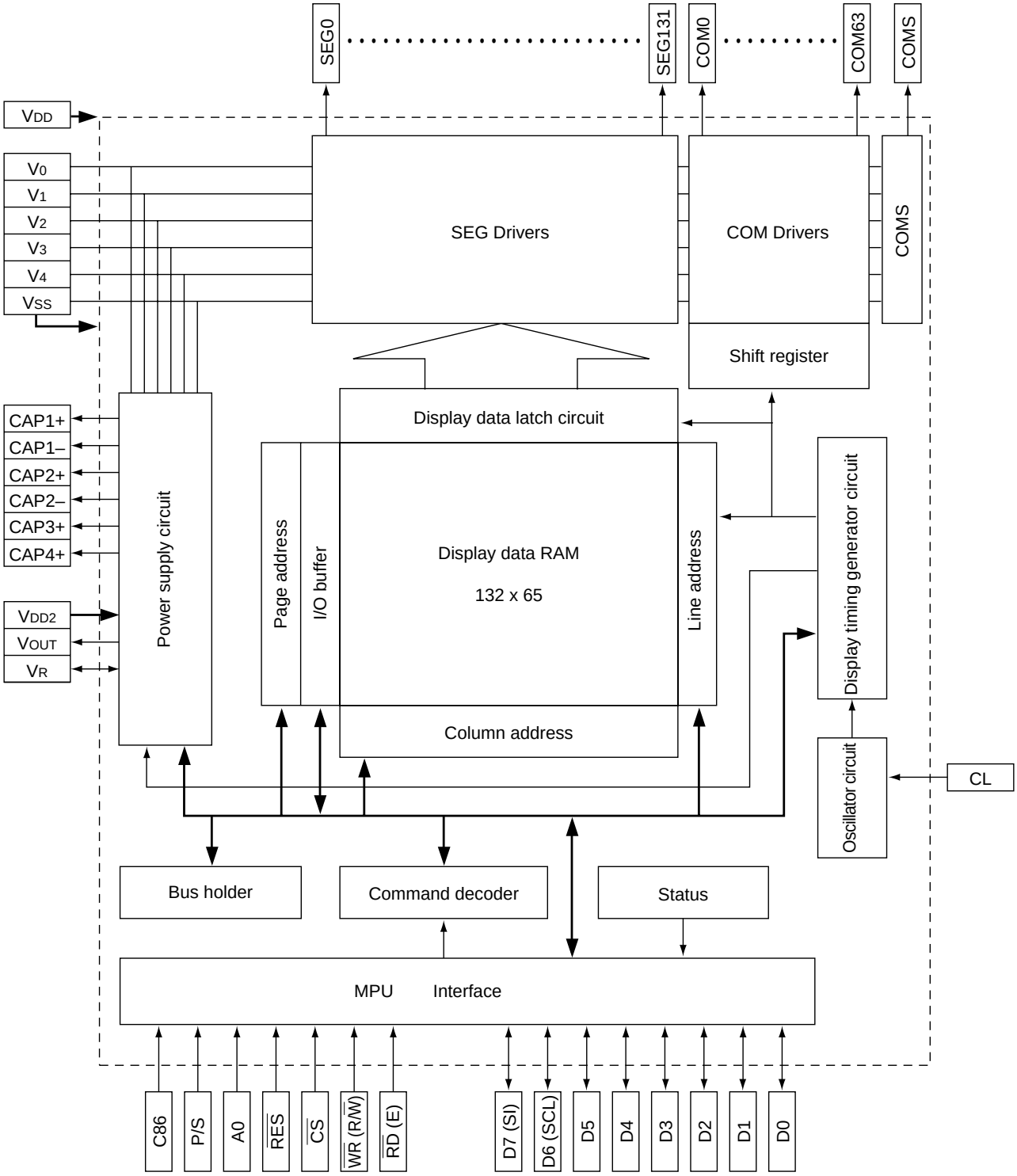
- Direct display by DDRAM :
  Bit data of DDRAM "0" .... a dot of display is OFF
  "1" .... a dot of display is ON
  (at Display normal)
- DDRAM capacity : 65×132=8580bits
- High-speed 8-bit Serial interface/8-bit MPU interface (The chip can be connected directly to both the 8080-series MPUs and the 6800-series MPUs) .
- Many command functions :
  Display ON/OFF, Display normal/reverse, Display all points ON/OFF,
  Page address set, Column address set, Display start line address set,
  Segment/Common driver direction select,
  Display data Read/Write ,Read modify write,
  Power control set, Electronic contrast control, LCD bias set,
  Power saver, Reset
- On-chip low power supply circuit for LCD driving voltage generation
  Booster circuit (with boost ratios of Double/Triple/Quadruple/Quintuple)
  Voltage regulator circuit (with high-accuracy electronic voltage adjustment function)
  Voltage follower (with V_1 to V_4 voltage dividing resistors)
- On-chip CR oscillation circuit (external clock can also be input.)
- Very low power consumption
- Power supply :
  Logic power supply : V_{DD}-V_{SS}=1.7 to 5.5V
  Booster reference supply : V_{DD2}-V_{SS}=1.7 to 5.5V
  LCD driving power supply : V_0-V_{SS}=4.5 to 16.0V
- Wide range of operating temperatures -40 to 85°C
- CMOS process
- Package : Au bump chip and TCP
- These ICs are not designed for strong radio/optical activity proof.

Series Specifications

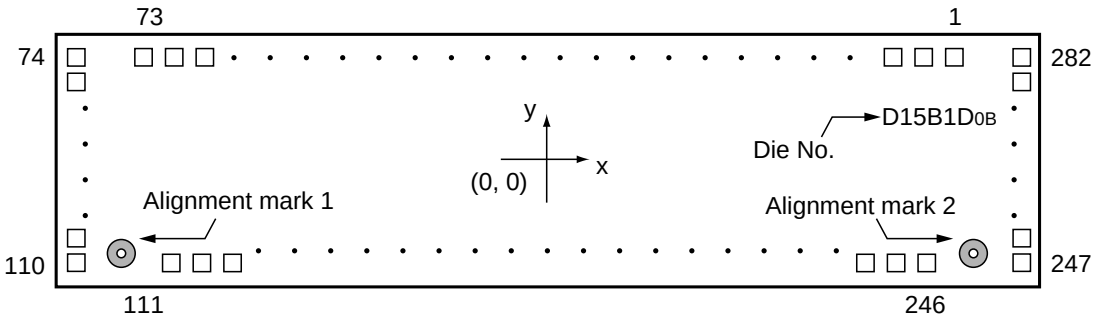
Product Name	Duty	Bias	SEG Dr	COM Dr	V_{REG} Temperature Gradient	Voltage Condition	Shipping Forms
SED15B1D$_{0B}$	1/65	1/9,1/7	132	65	–0.05%/	Internal voltage	Bare Chip
*SED15B1D$_{1B}$	1/65	1/9,1/7	132	65	–0.05%/	V_0 or V_{OUT} external voltage	Bare Chip
*SED15B1D$_{2B}$	1/65	1/9,1/7	132	65	–0.05%/	V_0 ~ V_4 extarnal voltage	Bare Chip
*SED15B1T$_{0*}$	1/65	1/9,1/7	132	65	–0.05%/		TCP

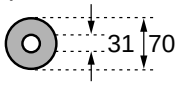
* : Start the development on demands
** : Under development

3. BLOCK DIAGRAM



4. PIN DIMENSIONS



Chip size	10.82mm×2.81mm	
Bump pitch	70µm (Min.)	
Bump size	PAD No.1 to 73	91µm× 91µm
	PAD No.74 to 110	91µm×45.5µm
	PAD No.111 to 246	45.5µm× 91µm
	PAD No.247 to 282	91µm×45.5µm
Bump height	17µm (Typ.)	
Chip thickness	625µm	
Ground bias	VSS	
Alignment mark 1	Center coordinates (µm)	(–4965, –1231)
	Size (µm)	
Alignment mark 2	Center coordinates (µm)	(4947, –1224)
	Size (µm)	

Pad Center Coordinates

Unit: µm

PAD No.	Pin Name	X	Y
1	(NC)	4852	1248
2	(NC)	4722	↓
3	TEST0	4592	
4	TEST1	4462	
5	TEST2	4332	
6	V_{SS}	4202	
7	TEST3	4072	
8	TEST4	3942	
9	TEST5	3812	
10	$\overline{RES}$	3682	
11	$\overline{CS}$	3552	
12	V_{SS}	3422	
13	$\overline{WR}$	3292	
14	$\overline{RD}$	3162	
15	V_{DD}	3032	
16	CL	2902	
17	A0	2772	
18	D7,SI	2642	
19	D6,SCL	2512	
20	D5	2382	
21	D4	2252	
22	D3	2122	
23	D2	1992	
24	D1	1862	
25	D0	1732	
26	V_{DD}	1602	
27	V_{DD}	1472	
28	V_{DD}	1342	
29	V_{DD2}	1212	
30	V_{DD2}	1082	
31	V_{DD2}	952	
32	TEST6	822	
33	V_{DD}	692	
34	P/S	562	
35	C86	432	
36	V_{SS}	302	
37	TEST7	172	
38	TEST8	3	
39	TEST9	–166	
40	V_{SS}	–335	
41	V_{SS}	–465	
42	V_{SS}	–595	
43	(NC)	–725	
44	V_{OUT}	–855	
45	V_{OUT}	–985	
46	V_{OUT}	–1115	
47	(NC)	–1245	
48	TEST10	–1414	
49	TEST11	–1583	
50	TEST12	–1713	↓

PAD No.	Pin Name	X	Y
51	TEST13	–1882	1248
52	V_{SS}	–2051	↓
53	V_R	–2181	
54	V_0	–2311	
55	V_1	–2441	
56	V_2	–2571	
57	V_3	–2701	
58	V_4	–2831	
59	CAP2+	–2961	
60	CAP2+	–3091	
61	CAP2–	–3221	
62	CAP2–	–3351	
63	CAP4+	–3481	
64	CAP4–	–3611	
65	V_{OUT}	–3741	
66	CAP1+	–3871	
67	CAP1+	–4001	
68	CAP1–	–4131	
69	CAP1–	–4261	
70	CAP3+	–4391	
71	CAP3+	–4521	
72	(NC)	–4651	
73	(NC)	–4781	↓
74	(NC)	–5255	1264
75	(NC)	↓	1194
76	COM31		1124
77	COM30		1054
78	COM29		984
79	COM28		913
80	COM27		843
81	COM26		774
82	COM25		703
83	COM24		633
84	COM23		562
85	COM22		492
86	COM21		422
87	COM20		352
88	COM19		282
89	COM18		211
90	COM17		141
91	COM16		71
92	COM15		1
93	COM14		–69
94	COM13		–140
95	COM12		–210
96	COM11		–280
97	COM10		–350
98	COM9		–420
99	COM8		–491
100	COM7	↓	–561

PAD No.	Pin Name	X	Y
101	COM6	–5255	–631
102	COM5	↓	–701
103	COM4		–771
104	COM3		–842
105	COM2		–912
106	COM1		–982
107	COM0		–1052
108	COMS		–1122
109	(NC)		–1193
110	(NC)	↓	–1263
111	(NC)	–4738	–1248
112	(NC)	–4668	↓
113	SEG0	–4598	
114	SEG1	–4528	
115	SEG2	–4458	
116	SEG3	–4388	
117	SEG4	–4317	
118	SEG5	–4247	
119	SEG6	–4177	
120	SEG7	–4107	
121	SEG8	–4037	
122	SEG9	–3966	
123	SEG10	–3896	
124	SEG11	–3826	
125	SEG12	–3756	
126	SEG13	–3686	
127	SEG14	–3615	
128	SEG15	–3545	
129	SEG16	–3475	
130	SEG17	–3405	
131	SEG18	–3335	
132	SEG19	–3264	
133	SEG20	–3194	
134	SEG21	–3124	
135	SEG22	–3054	
136	SEG23	–2984	
137	SEG24	–2913	
138	SEG25	–2843	
139	SEG26	–2773	
140	SEG27	–2703	
141	SEG28	–2633	
142	SEG29	–2562	
143	SEG30	–2492	
144	SEG31	–2422	
145	SEG32	–2352	
146	SEG33	–2282	
147	SEG34	–2211	
148	SEG35	–2141	
149	SEG36	–2071	
150	SEG37	–2001	↓

Unit: µm

PAD No.	Pin Name	X	Y
151	SEG38	–1931	–1248
152	SEG39	–1860	
153	SEG40	–1790	
154	SEG41	–1720	
155	SEG42	–1650	
156	SEG43	–1580	
157	SEG44	–1509	
158	SEG45	–1439	
159	SEG46	–1369	
160	SEG47	–1299	
161	SEG48	–1229	
162	SEG49	–1158	
163	SEG50	–1088	
164	SEG51	–1018	
165	SEG52	–948	
166	SEG53	–878	
167	SEG54	–807	
168	SEG55	–737	
169	SEG56	–667	
170	SEG57	–597	
171	SEG58	–527	
172	SEG59	–456	
173	SEG60	–386	
174	SEG61	–316	
175	SEG62	–246	
176	SEG63	–176	
177	SEG64	–105	
178	SEG65	–35	
179	SEG66	35	
180	SEG67	105	
181	SEG68	175	
182	SEG69	246	
183	SEG70	316	
184	SEG71	386	
185	SEG72	456	
186	SEG73	526	
187	SEG74	597	
188	SEG75	667	
189	SEG76	737	
190	SEG77	807	
191	SEG78	877	
192	SEG79	948	
193	SEG80	1018	
194	SEG81	1088	
195	SEG82	1158	
196	SEG83	1228	
197	SEG84	1299	
198	SEG85	1369	
199	SEG86	1439	
200	SEG87	1509	

PAD No.	Pin Name	X	Y
201	SEG88	1579	–1248
202	SEG89	1650	
203	SEG90	1720	
204	SEG91	1790	
205	SEG92	1860	
206	SEG93	1930	
207	SEG94	2001	
208	SEG95	2071	
209	SEG96	2141	
210	SEG97	2211	
211	SEG98	2281	
212	SEG99	2352	
213	SEG100	2422	
214	SEG101	2492	
215	SEG102	2562	
216	SEG103	2632	
217	SEG104	2703	
218	SEG105	2773	
219	SEG106	2843	
220	SEG107	2913	
221	SEG108	2983	
222	SEG109	3054	
223	SEG110	3124	
224	SEG111	3194	
225	SEG112	3264	
226	SEG113	3334	
227	SEG114	3405	
228	SEG115	3475	
229	SEG116	3545	
230	SEG117	3615	
231	SEG118	3685	
232	SEG119	3756	
233	SEG120	3826	
234	SEG121	3896	
235	SEG122	3966	
236	SEG123	4036	
237	SEG124	4107	
238	SEG125	4177	
239	SEG126	4247	
240	SEG127	4317	
241	SEG128	4387	
242	SEG129	4458	
243	SEG130	4528	
244	SEG131	4598	
245	(NC)	4668	
246	(NC)	4738	
247	(NC)	5248	–1225
248	COM32		–1155
249	COM33		–1085
250	COM34		–1015

PAD No.	Pin Name	X	Y
251	COM35	5248	–944
252	COM36		–874
253	COM37		–804
254	COM38		–734
255	COM39		–664
256	COM40		–593
257	COM41		–523
258	COM42		–453
259	COM43		–383
260	COM44		–313
261	COM45		–242
262	COM46		–172
263	COM47		–102
264	COM48		–32
265	COM49		38
266	COM50		109
267	COM51		179
268	COM52		249
369	COM53		319
270	COM54		389
271	COM55		460
272	COM56		530
273	COM57		600
274	COM58		670
275	COM59		740
276	COM60		811
277	COM61		881
278	COM62		951
279	COM63		1021
280	COMS		1091
281	(NC)		1162
282	(NC)		1232

5. PIN DESCRIPTION

Power supply pins

Name	I/O	Description	Number of pins
V_{DD}	Supply	Power supply. Connect to MPU power pin V_{CC}.	5
V_{DD2}	Supply	Externally-input reference power supply for booster circuit.	3
V_{SS}	Supply	This is a 0V terminal connected to the system GND.	7
V_0, V_1, V_2 V_3, V_4	Supply	Multi-level power supply for LCD drive. The voltages are determined by LCD cell.The voltages should maintain the following relationship : $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$. When on-chip power supply circuit turns on, V_0 voltage are generated, and the following voltages are generated to V_1 to V_4. Either voltage can be selected by LCD bias set command.	5

	SED15B1
V_1	6/7 • V_0, 8/9 • V_0
V_2	5/7 • V_0, 7/9 • V_0
V_3	2/7 • V_0, 2/9 • V_0
V_4	1/7 • V_0, 1/9 • V_0

LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive connection pin.	2
CAP1–	O	Boosting capacitor negative connection pin.	2
CAP2+	O	Boosting capacitor positive connection pin.	2
CAP2–	O	Boosting capacitor negative connection pin.	2
CAP3+	O	Boosting capacitor positive connection pin.	2
CAP4+	O	Boosting capacitor positive connection pin.	2
V_{OUT}	O	Booster output.	4
V_R	I	Voltage adjustment pin. Provides V_0 voltage using external resistors. When internal resistors are used, this pin cannot be used.	1

System bus connection pins

Name	I/O	Description	Number of pins
D7 to D0 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit MPU data bus. When the serial interface is selected (P/S=LOW) ; D7 : Serial data input (SI) D6 : Serial clock input (SCL)	8
A0	I	Control/data flag input. A0=HIGH : The data on D7 to D0 is display data. A0=LOW : The data on D7 to D0 is control data.	1
$\overline{CS}$	I	Chip select input. Data input is enable when $\overline{CS}$ is low.	1
$\overline{RES}$	I	When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1

Pin name	I/O	Description	Number of pins
$\overline{RD}$ (E)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{RD}$ signal of the 8080-series MPU. While this signal is low, SED15B1 series data bus is an output status. • When connected to an 6800-series MPU ; This is active-HIGH. This is used as an enable clock input pin of the 6800-series MPU.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080-series MPU ; This is active-LOW. This pin is connected to the $\overline{WR}$ signal of the 8080-series MPU. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. •When connected to an 6800-series MPU ; This is the read/write control signal input . R/$\overline{W}$=HIGH : Read. R/$\overline{W}$=LOW : Write.	1
C86	I	MPU interface selection pin. C86=HIGH : 6800-series MPU interface C86=LOW : 8080-series MPU interface	1
P/S	I	Serial data input/parallel data input selection pin. P/S=HIGH : Parallel data input P/S=LOW : Serial data input The following applies depending on the P/S status :	1

P/S	Data/Command	Data	Read/Write	Serial Clock
HIGH	A0	D7 to D0	$\overline{RD}$, $\overline{WR}$	
LOW	A0	SI (D7)	Write only	SCL (D6)

In serial mode, no data can be read from DDRAM.
When P/S=LOW,D5 to D0 are HZ. D5 to D0 may be HIGH, LOW or Open, and moreover A0, $\overline{RD}$, $\overline{WR}$, C86 may be HIGH, LOW or Open.

LCD driver pins

Name	I/O	Description	Number of pins
CL	I	External clock input. When external clock is halted, CL must be LOW. If internal clock (on-chip CR oscillation circuit) is selected, CL connected to V_{DD}.	1
SEG0 to SEG131	O	LCD segment driver output.	132
COM0 to COM63	O	LCD common driver output.	64
COMS	O	LCD common driver output for the indicator. When it is not used, it is made open.	2

Test pins

Name	I/O	Description	Number of pins
TEST0 to TEST13	I/O	These are terminals for IC chip testing. Please set to open.	14

Note and caution

• If control signal from MPU is HZ, an over-current may flow through the IC. A protection is required to prevent the HZ signal at the input pins.

6. FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED15B1 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). Through selecting the P/S pin polarity to the HIGH or LOW, it is possible to select either 8-bit parallel data input or 8-bit serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH:Parallel Input	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW:Serial Input	$\overline{CS}$	A0	–	–	–	SI	SCL	–

– : HIGH, LOW or Open

Parallel interface

When the parallel interface has been selected (P/S= HIGH), then it is possible to connect directly to either an 8080-series MPU or a 6800-series MPU (as shown in Table 2) by selecting C86 pin to either HIGH or LOW.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH:6800-series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW:8080-series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

Moreover, the SED15B1 series identifies the data bus signal according to A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Common	6800-series	8080-series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	0	1	0	Writes control data (command)

Serial interface

When the serial interface has been selected (P/S= LOW),only writing display data and control data is possible by four input signals. The serial data input (SI) and serial clock input (SCL) are enabled when $\overline{CS}$ is low. When chip is not selected, the shift register and counter which compose serial interface are reset.
The serial data is read from the serial data input pin in the rising edge of the serial clocks D7,D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether the serial data input is display data or command data; when A0=HIGH, the data is display data, and when A0=LOW then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

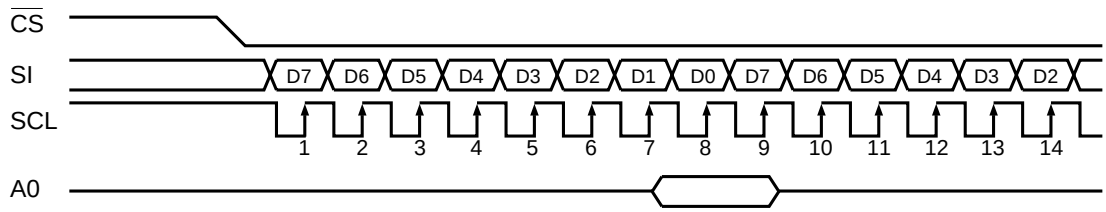


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

Chip select input

The MPU interface (either parallel or serial) is enabled only when $\overline{CS}$=LOW.
When the chip select is inactive, D7 to D0 enter a high impedance state, and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When the serial interface is selected, the shift register and the counter are reset.

Access to DDRAM and internal registers

In accessing the DDRAM and the internal registers of the SED15B1 series, the MPU is required to satisfy the only cycle time (t_{CYC}), and is not needed to consider the wait time. Accordingly, it is possible to transfer data at higher speed.

In order to realize the higher speed accessing, the SED15B1 series can perform a type of pipeline processing between LSIs using bus holder of internal data bus when data is sent from/to the MPU. For example, when the MPU writes data to the DDRAM, once the data is stored in the bus holder, then it is written to the DDRAM before the next data write cycle. And when the MPU reads the contents of the DDRAM, the first data read cycle (dummy read cycle) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. Thus, there is a certain restriction in the DDRAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

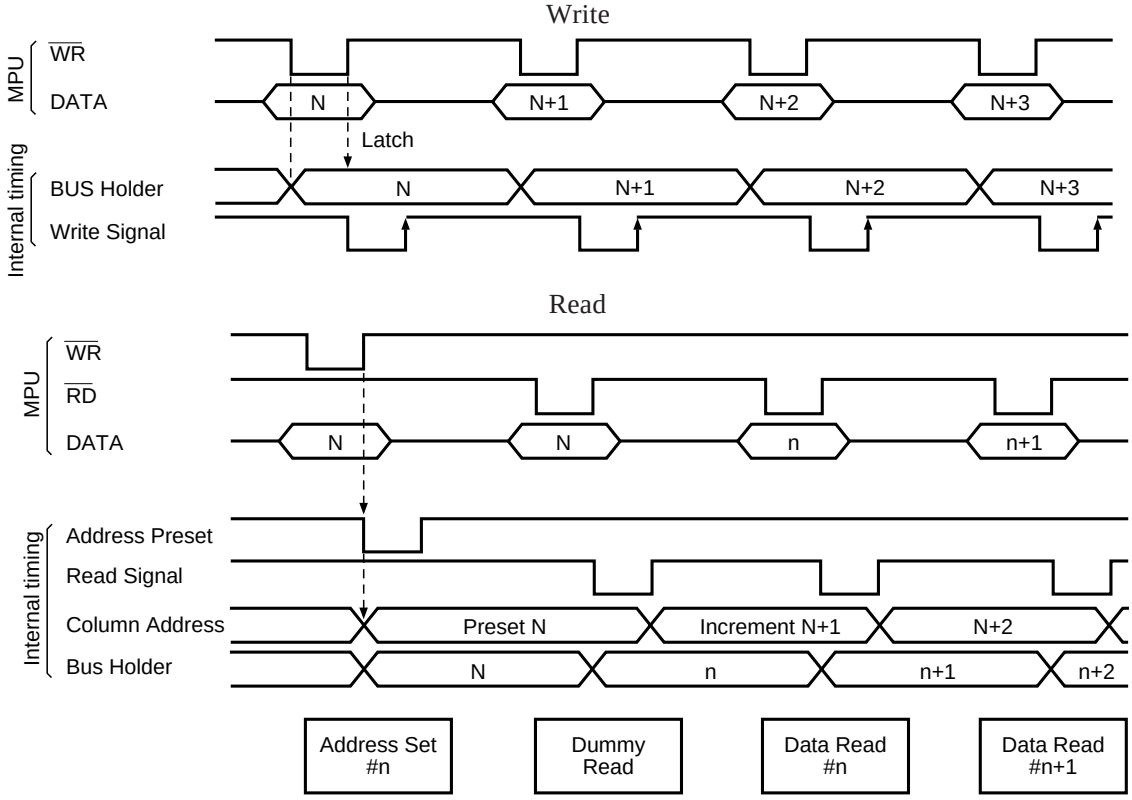


Figure 2

DDRAM and page/column address circuit

The DDRAM stores pixel data for LCD. It is a 65-row (8 page by 8 bit + 1) by 132-column addressable array.

As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD common direction.

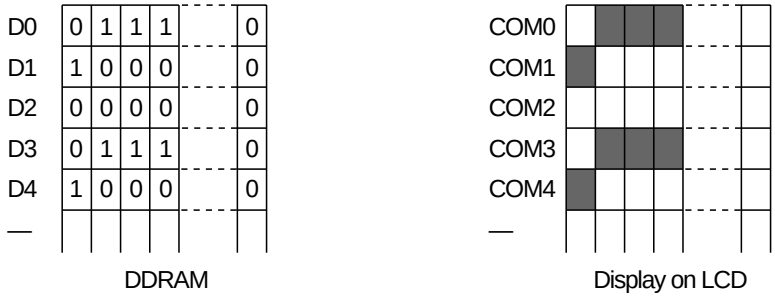


Figure 3

Each pixel can be selected when page address and column address are specified(refer to Figure 5).
The MPU issues Page address set command to change the page and access to another page. Page address 8 (D3,D2,D1,D0 = 1,0,0,0) is DDRAM area dedicate to the indicator, and display data D0 is only valid.
The DDRAM column address is specified by Column address set command. The specified column address is automatically incremented by +1 when a Display data read/write command is entered. After the last column address (83H), column address returns to 00H and page address incremented by +1 (refer to Figure 4). After the very last address (column = 83H,page = 8H),both column address and page address return to 00H (column address = 00H, page address = 0H).

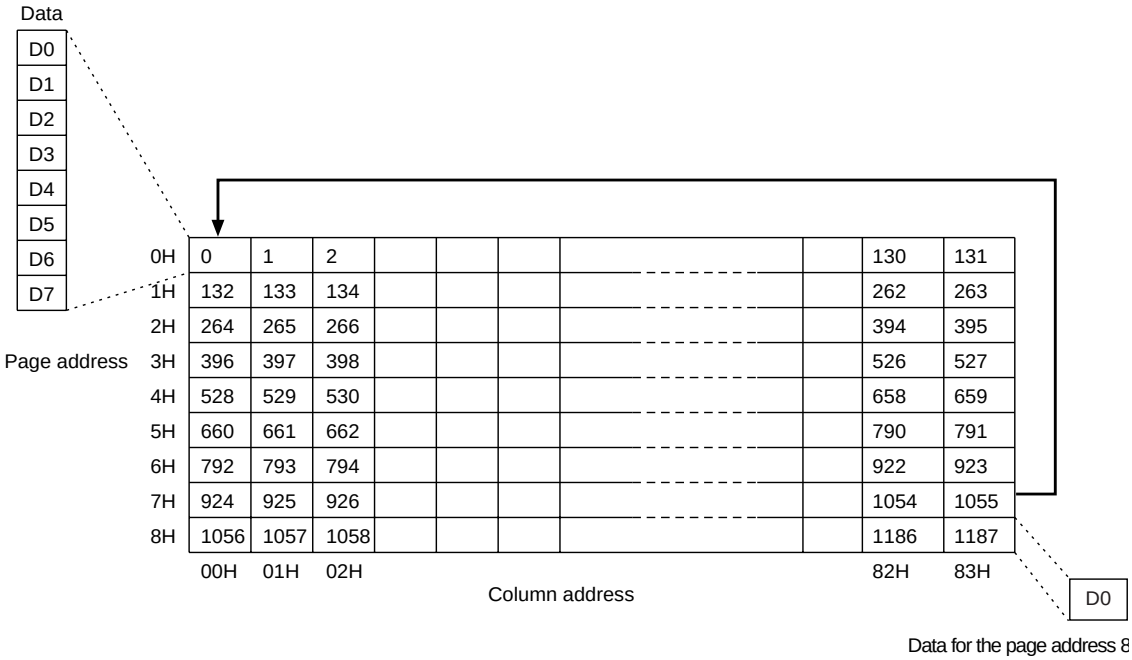


Figure 4

The MPU reads from and writes to the DDRAM through the I/O buffer independent of the LCD controller operation. Therefore, data can be written to the DDRAM at the same time as data is being displayed, without causing the LCD to flicker.

Furthermore, as is shown in Table 4, Segment driver direction select command can be used to reverse the relationship between the DDRAM column address and segment output. This allows flexible IC layout during LCD module assembly.

Table 4

Column Address	00H	01H	02H		81H	82H	83H
Normal Direction	SEG0	SEG1	SEG2		SEG129	SEG130	SEG131
Reverse Direction	SEG131	SEG130	SEG129		SEG2	SEG1	SEG0

Line address circuit

The line address circuit specifies the line address (as shown Figure 5) relating to the COM output when the contents of the DDRAM are displayed. The display start line address, what is normally the top line of the display, can be specified by Display start line address set command. And Common driver direction select command can be used to reverse the relationship between the DDRAM line address and common output. For example, as is shown in Table 5, the display start line address corresponds to the COM0 output when the common driver direction is normal, or the COM63 output when common driver direction is reversed.And the display area is followed by the higher number line addresses in ascending order from the display start line address, corresponding to the duty cycle. This allows flexible IC layout during LCD module assembly.
If the display start line address is changed dynamically using the Display start line address set command,then screen scrolling and page swapping can be performed.

Table 5 (at display start line address=1CH)

Line Address	1CH	1DH		3FH	00H		1AH	1BH
Normal Direction	COM0	COM1		COM35	COM36		COM62	COM63
Reverse Direction	COM63	COM62		COM28	COM27		COM1	COM0

Display data latch circuit

The display data latch circuit is a latch temporarily stored the display data that is output to the LCD driver circuit from the DDRAM.
Display ON/OFF command, Display normal/reverse command, and Displayed all points ON/OFF command control only the data within the latch, and do not change the data within the DDRAM.

Display Data RAM

The display data RAM stores pixel data for the LCD.
It is a 132-columm×65-row addressale array as shown in Figure 5.

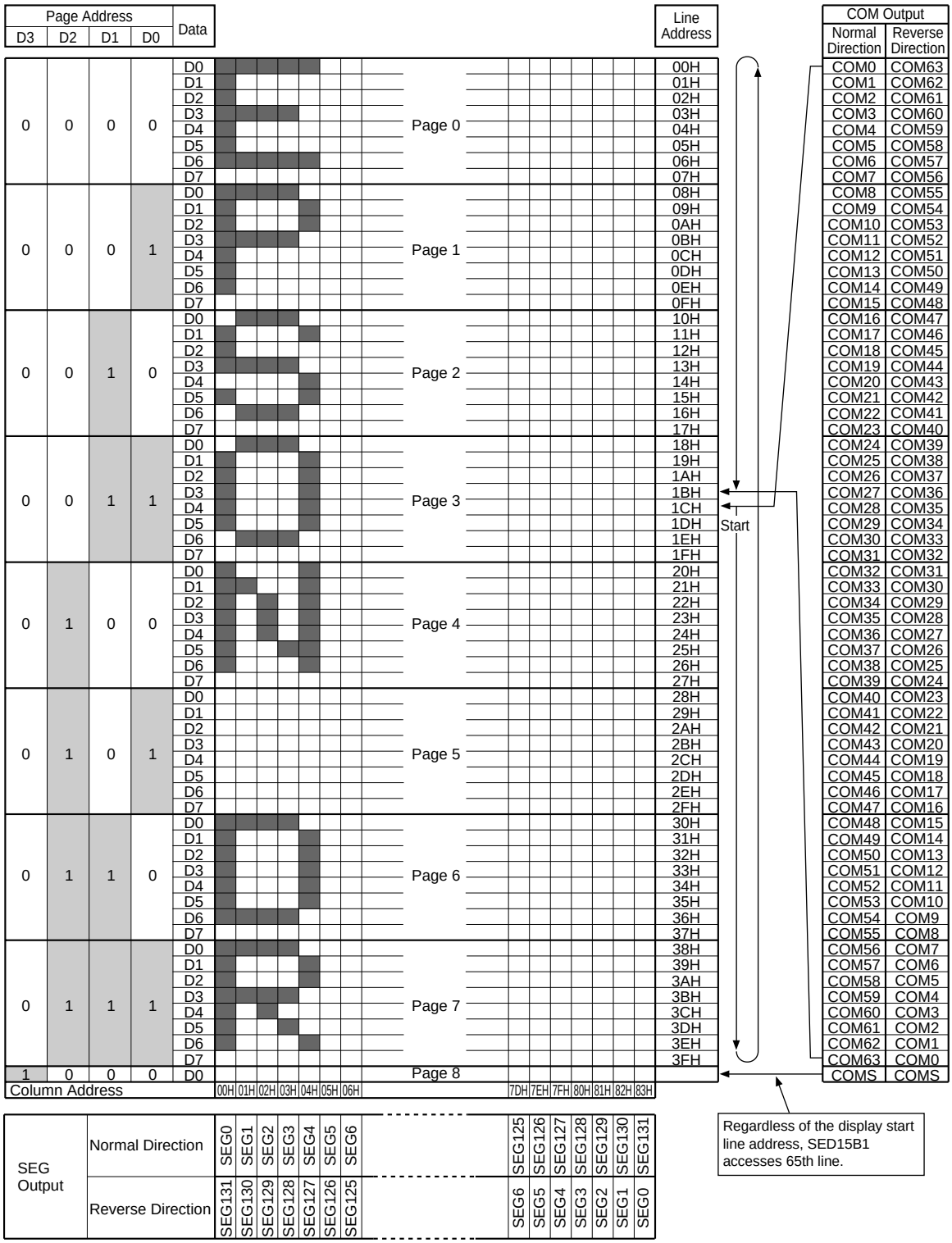


Figure 5

Oscillation circuit

The SED15B1 series has a complete on-chip CR oscillation circuit, and its output is used as the display timing signal source.
The on-chip oscillation circuit is available when CL = HIGH.
And the SED15B1 series is also capable external clock input from CL pin. (When external clock is halted, CL must be LOW.)

Display timing generator circuit

The display timing generator circuit generates the timing signals from the display clocks to the line address circuit and the display data latch circuit. The display data is latched to the display data latch circuit and is output to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates COM scan signal and the LCD AC signal (FR) from the display clocks. As shown in Figure 6, the FR normally generates the 2- frame AC drive waveforms .

2-frame AC drive waveforms

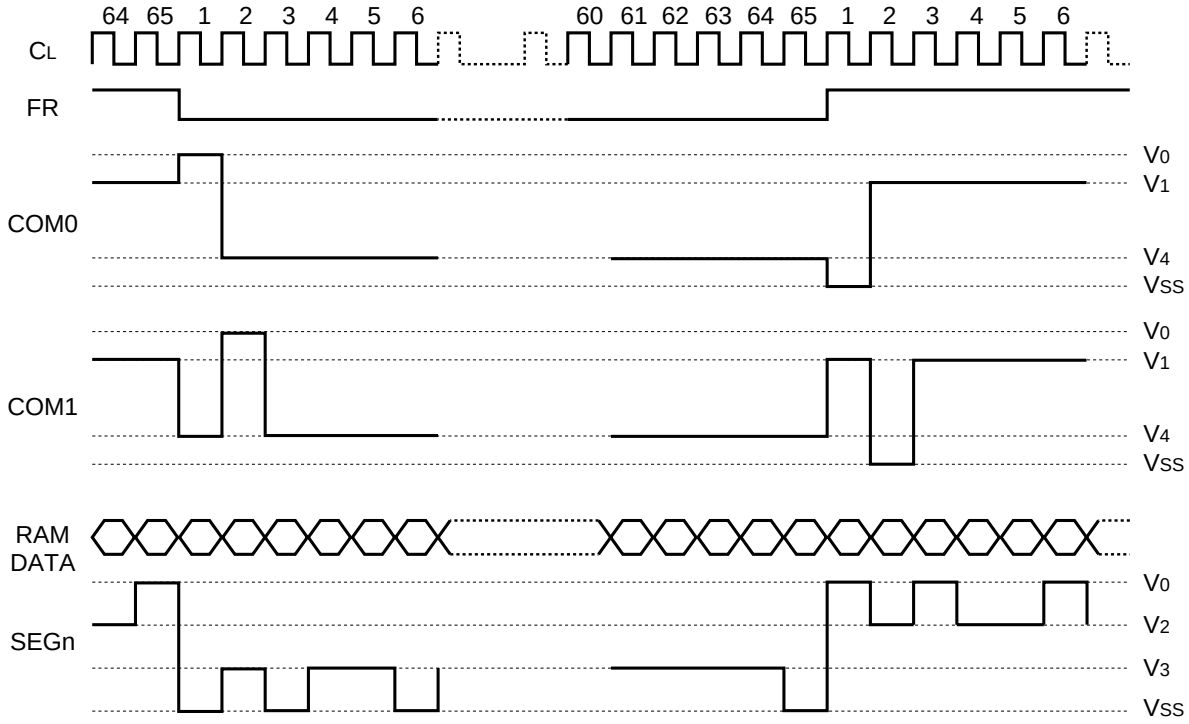


Figure 6

LCD driver circuits

These are multiplexers outputting the LCD panel driving 4-level signal which level is determined by a combination of display data, COM scan signal, and LCD AC signal (FR). Figure 7 shows an example of SEG and COM output waveforms.

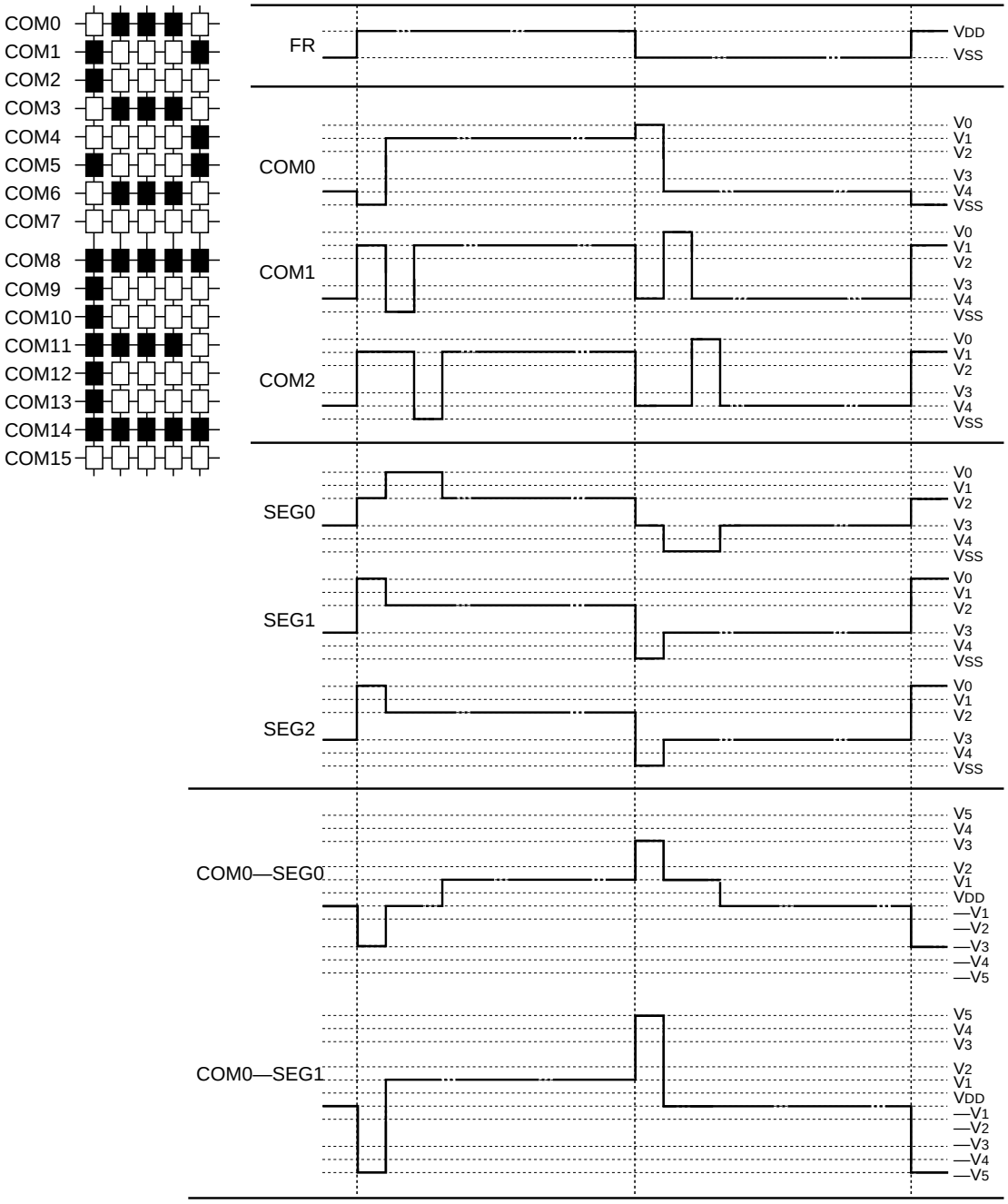


Figure 7

Power supply circuit

The power supply circuit generates the voltage to drive the LCD panel at low power consumption.
The power supply circuit consists of a booster circuit, voltage regulator circuit, and voltage follower circuit, and is controlled by Power control set command. Using this command, the booster circuit, the voltage regulator circuit, and the voltage follower circuit can be independently turned ON or OFF. In the case of using SED15B1D0B which use a booster circuit, voltage regulator circuit, and voltage follower circuit, every circuit is required to be turnend ON or OFF at the same time by Power control set command. In the case of using SED15B1D0B/SED15B1D2B which need the external power supply and use part of on-chip power supply circuit, each must be set the appropriate state as shown in the Table 6.

Table 6

Power supply condition	Product name*2	Booster circuit	Voltage regulator circuit	Voltage follower circuit	External voltage input	Boosting system pin*3
On-chip power supply used	SED15B1D0B	ON	ON	ON	V_{DD2}	Used
Voltage regulator circuit and Voltage follower circuit only	SED15B1D1B	OFF	ON	ON	V_{OUT}	Open
Voltage follower circuit only	SED15B1D1B	OFF	OFF	ON	V_0=V_{OUT}*4	Open
External power supply only	SED15B1D2B	OFF	OFF	OFF	V_0=V_{OUT}*4 V_1 to V_4	Open

*1 Combinations other than those shown in above table are possible but impractical.
*2 Chose the appropriate product according to the power supply condition.
*3 The boosting system pin indicates the CAP+, CAP1–, CAP2+, CAP2–, CAP3+, and CAP4+ pin.
*4 Both V_0 pin and V_{OUT} pin should be connected to external power supply.

Booster circuit

Using the booster circuit, it is possible to produce Quintuple/Quadruple/Triple/Double boosting of the V_{DD2}-V_{SS} voltage level.

Quintuple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP3+ and CAP1–, between CAP4+ and CAP2–, between V_{OUT} and V_{DD2}, the potential between V_{DD2} and V_{SS} is boosted to quintuple toward the positive side and it is output at V_{OUT} pin.

Quadruple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP3+ and CAP1–, between V_{OUT} and V_{DD2}, and jumper between CAP4+ and V_{OUT}, the potential between V_{DD2} and V_{SS} is boosted to quadruple toward the positive side and it is output at V_{OUT} pin.

Triple boosting :
Connect capacitor between CAP1+ and CAP1–, between CAP2+ and CAP2–, between V_{OUT} and V_{DD2}, and jumper between CAP3+, CAP4+ and V_{OUT}, the triple boosted voltage appears at V_{OUT} pin.

Double boosting :
Connect capacitor between CAP1+ and CAP1–, between V_{OUT} and V_{DD2}, open CAP2–, and jumper between CAP2+, CAP3+, CAP4+ and V_{OUT}, the double boosted voltage appears at V_{OUT} pin.

The boosted voltage relationships are shown in Figure 8.

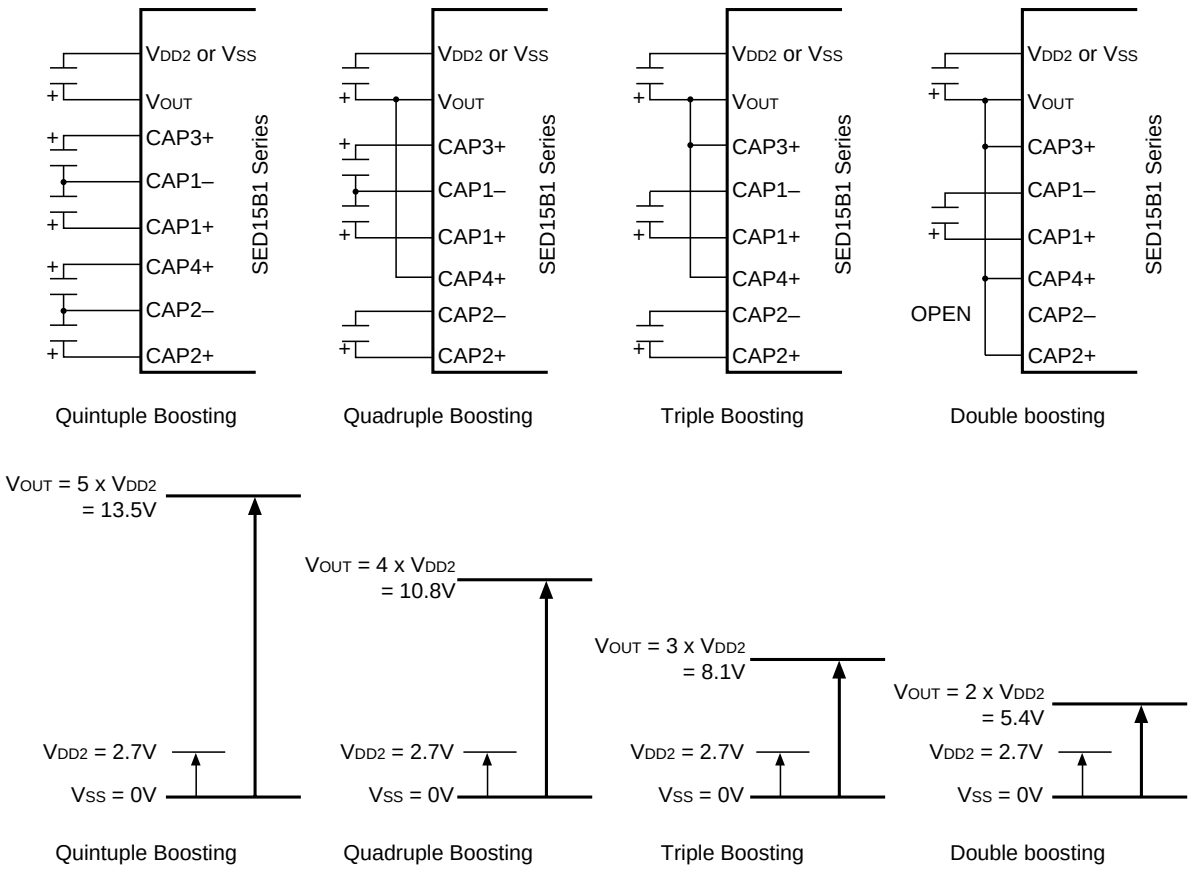


Figure 8

* V_{DD2} voltage must be set so that V_{OUT} voltage does not exceed the absolute maximum rated value.
* The Capacitance depend on the load of the LCD panel to be driven. Set a value that LCD driver voltage may be stable (reference value = 1.0 to 4.7 μF).

Voltage regulator circuit

The boosting voltage occurring at the V_{OUT} pin is sent to the voltage regulator, and the V_0 voltage (LCD driver voltage) is output.
Because the SED15B1 series has the high-accuracy constant voltage source, the 32-level electronic volume function and the internal resistor for the V_0 voltage regulator (= V_0-resistor), it is possible to construct a high-accuracy voltage regulator circuit without external component. And V_0 voltage can be adjusted by commands only to adjust the LCD contrast.
(A) When the V_0-resistor is used.
Through the use of the V_0-resistor and the electronic volume function, V_0 voltage can be controlled by commands only (without adding any external resistors). The V_0 voltage can be calculated using the following equations within the range of $V_0 < V_{OUT}$.

$$V_0 = (1+Rb/Ra) \cdot V_{EV}$$

$$V_{EV} = (1-\alpha/200) \cdot V_{REG} \quad \text{(Equation A-1)}$$

V_{REG} is the on-chip constant voltage as shown in Table 7 at Ta=25°C.

Table 7

Model	V_{REG}	Thermal Gradient
SED15B1***	1.3V	–0.05%/°C

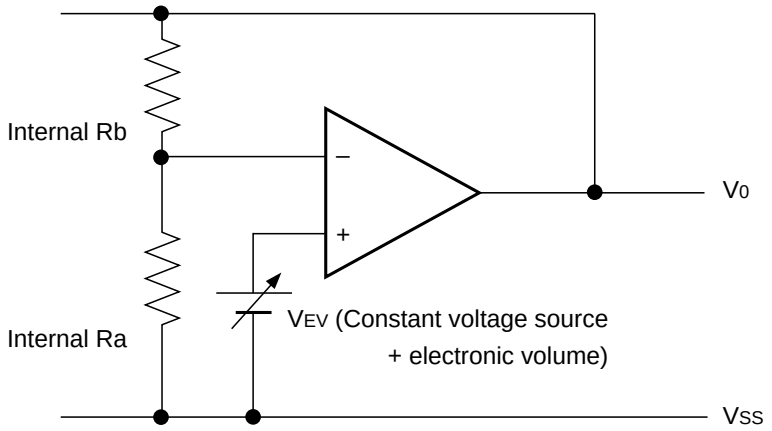


Figure 9

α is a value of the electronic volume, and can be set to one of 32-states by Electronic volume command setting the 5-bit data in the electronic volume register. Table 8 shows the value of α.

Rb/Ra is the V0-resistor ratio, and can be set to one of 7-states by V0-resistor ratio set command setting the 3-bit data in the V0-resistor ratio register. Table 9 shows the value of (1+Rb/Ra) ratio (reference value).

Table 8

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Table 9

			1+Rb/Ra
D3	D2	D1	SED15B1
0	0	0	5.60
0	0	1	5.86
0	1	0	6.15
0	1	1	6.46
1	0	0	6.81
1	0	1	7.20
1	1	0	7.64
1	1	1	External resistor can be used.

Figure 10 shows V0 voltage measured by V0-resistor ratio and electronic voltage at Ta=25°C.

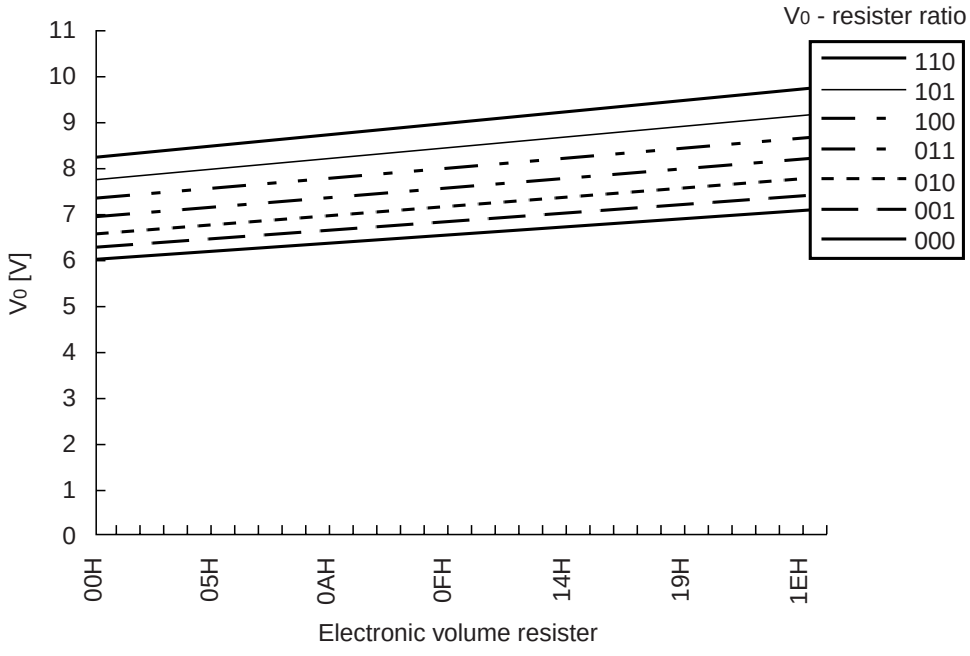


Figure 10

<Setup example>
When selection Ta=25°C and V_0=7V for SED15B1 series on which temperature gradient=–0.05%/°C. Using Figure 10 and equation A-1, the following setup is enabled.

Table 10

Commands	Register							
	D7	D6	D5	D4	D3	D2	D1	D0
V_0-resister ratio set	0	0	1	0	0	0	0	1
Electronic volume	1	0	0	1	0	0	0	1

In this case, the variable range and the notch width of the V_0 voltage is shown as Table 11, as dependent on the electronic volume.

Table 11

V_0	Min.	Typ.	Max.	Units
Variable range	6.44[α=31]	7.05[α=15]	7.62[α=0]	[V]
Notch width		37		[mV]

(B) When external resistors are used. (1)

(The V_0-resistor is not used.)

The V_0 voltage can also be set without using the V_0-resistor by adding resistors Ra' and Rb' between V_{SS} and V_R, and between V_R and V_0, respectively. In this case, the electronic volume command makes it possible to adjust the contrast of the LCD by controlling V_0 voltage. In the range where $V_0 < V_{OUT}$, the V_0 voltage can be calculated using equation B-1 based on the external resistors Ra' and Rb'.

$$V_0=(1+Rb'/Ra')\cdot V_{EV}$$

$$V_{EV}=(1-\alpha/200)\cdot V_{REG} \qquad \text{(Equation B-1)}$$

V_{REG} is the on-chip constant voltage as shown in Table 8 at Ta=25°C.

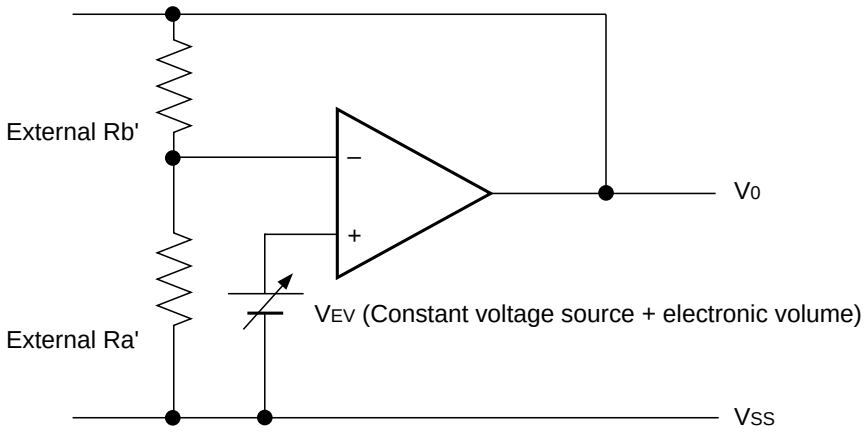


Figure 11

<Setup example>
When selection Ta=25°C and V_0=11V for SED15B1 series on which temperature gradient=–0.05%/°C.
The central value of the electronic volume register is (D5, D4, D3, D2, D1, D0)=(1, 0, 0, 0, 0,), that is α=15.
So, according to equation B-1 and V_{REG}=1.3V, the Rb'/Ra' is shown as follows.

$$V_0 = (1+Rb'/Ra') \cdot (1-\alpha/200) \cdot V_{REG}$$

$$11V = (1+Rb'/Ra') \cdot (1-15/200) \cdot 1.3V \qquad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra'+Rb' = 2.2M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equation B-2 and B-3,

$$Rb'+Ra' = 8.15$$

$$Ra' = 240k\Omega$$

$$Ra' = 1960k\Omega$$

In this case, the variable range and the notch width of the V_0 voltage is, as shown Table 12, as dependent on the electronic volume.

Table 12

V_0	Min.	Typ.	Max.	Units
Variable range	10.01[α=31]	11.0[α=15]	11.9[α=0]	[V]
Notch width		59		[mV]

(C) When external resistors are used. (2)
(The V_0-resistor is not used.)
When the external resistors described above are used, adding a variable resistor as well make it possible to perform fine adjustments on Ra' and Rb', to set the V_0 voltage. In this case, the electronic volume function makes it possible to control the V_0 voltage by commands to adjust the LCD contrast. In the range where $V_0 < V_{OUT}$ the V_0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistors) and R3 settings, where R2 can be subjected to fine adjustments (Δ R2).

$$V_0 = \{1+(R3+R2-\Delta R2)/(R1+\Delta R2)\} \cdot V_{EV}$$

$$= \{1+(R3+R2-\Delta R2)/(R1+\Delta R2)\} \cdot (1-\alpha/200) \cdot V_{REG}$$

$$[\because V_{EV} = (1-\alpha/200) \cdot V_{REG}] \qquad \text{(Equation C-1)}$$

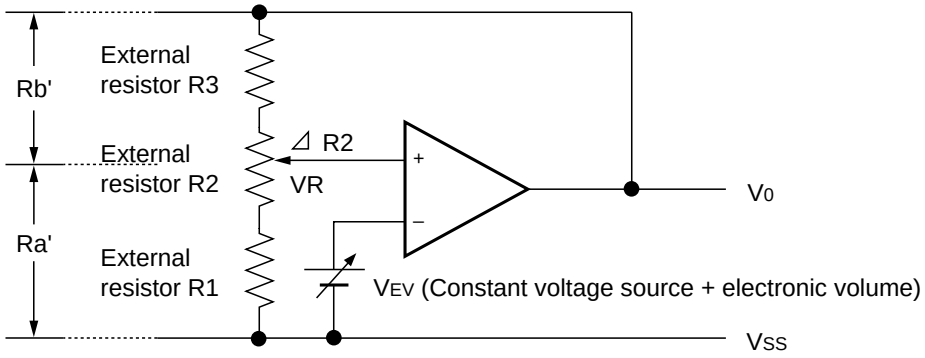


Figure 12

<Setup example>
When selection Ta=25°C and V_0=5V to V_0=9V (using R2) for SED15B1 series on which temperature gradient=–0.05%/°C.
The central value of the electronic volume register is (D5, D4, D3, D2, D1, D0)=(1, 0, 0, 0, 0,), that is α=15.
So, according to equation C-1 and V_{REG}=1.3V, the R1, R2, R3, are shown as follows. (when Δ R2=0Ω at V_0=9V and Δ R2=R2 at V_0=5V)

$$9V = \{1+(R3+R2)/R1\} \cdot (1-15/200) \cdot 1.3V \quad \text{(Equation C-2)}$$

$$5V = \{1+R3/(R1+R2)\} \cdot (1-15/200) \cdot 1.3V \quad \text{(Equation C-3)}$$

Moreover, when the value of the current running through V_0 and V_{SS} is set to 5 μ A at V_0=7V (central value),

$$R1+R2+R3=1.4M\Omega \quad \text{(Equation C-3)}$$

With this, according to equation C-2, C-3 and C-4,

R1=187kΩ
R2=150kΩ
R3=1063kΩ

In this case, if V_0 is set to 7V as central value, Δ R2 becomes 53kΩ
And, the variable range and the notch width of the V_0 voltage is, as shown Table 13, as dependent on the electronic volume. (Δ R2=53kΩ)

Table 13

V_0	Min.	Typ.	Max.	Units
Variable range	6.41[α=31]	7.0[α=15]	7.58[α=0]	[V]
Notch width		37		[mV]

* When the V_0-resistor or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_0-resistor is not used. When the V_0-resistor is used, then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

Voltage Follower Circuit

The V_0 voltage is divided to generate the V_1, V_2, V_3 and V_4 voltages by on-chip resistor circuit. And the V_1, V_2, V_3 and V_4 voltages are impedance-converted by voltage follower,and provide to LCD driver circuit.
LCD bias ratio can be selected by LCD bias set command which is 1/7 bias or 1/9 bias for SED15B1 series.

Power supply turn off sequence

Only SED15B1D_{0B} which is used as on-chip power supply LCD driver, has the faculty of V_{OUT} shorts to V_{DD2} when the $\overline{RES}$ pin is LOW, and V_0 shorts to V_{SS} when the $\overline{RES}$ pin is LOW or reset command is issued. When the on-chip power supply is turned off, it is recommended to be the $\overline{RES}$ pin is LOW., for the purpose of the electric discharge on the LCD panel.
SED15B1D_{0B}/SED15B1D_{2B} which is used as external power supply LCD driver, don't have such a discharge faculty, so that V_{OUT} and V_0 need to short to V_{SS}, when the external power supply turn off or power saver.
See the section on the Command Description for details.

Reference Circuit Examples

Figure 13 ~ 18 shoes reference circuit examples.

(1) When used all of the booster circuit, voltage regulator circuit and V/F circuit [SED15B1D0B]

① Use the voltage regulator with V0-resistor
(Example where VDD=VDD2, with 5 × boosting)

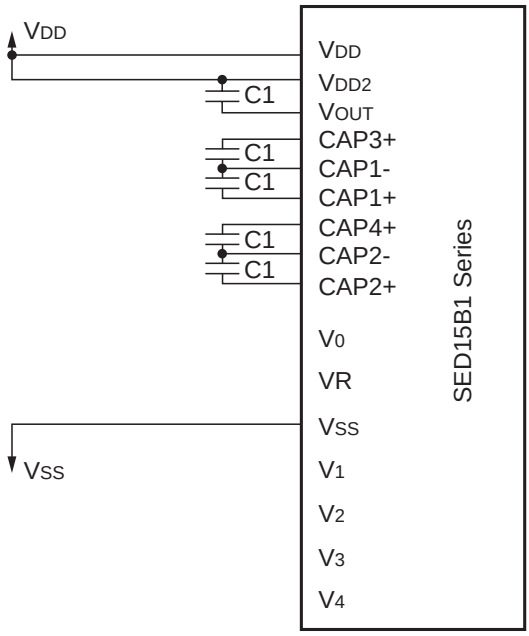


Figure 13

② Use the voltage regulator with external resistor
(Example where VDD=VDD2, with 5 × boosting)

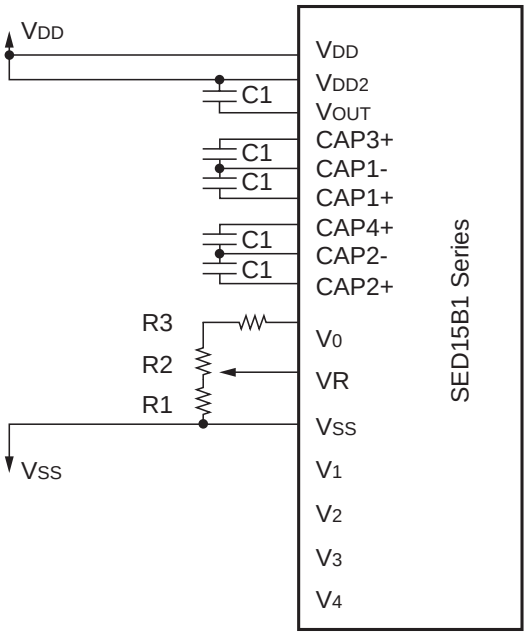


Figure 14

(2) When used only the voltage regulator circuit and V/F circuit [SED15B1D1B]

① Use the voltage regulator with V0-resistor

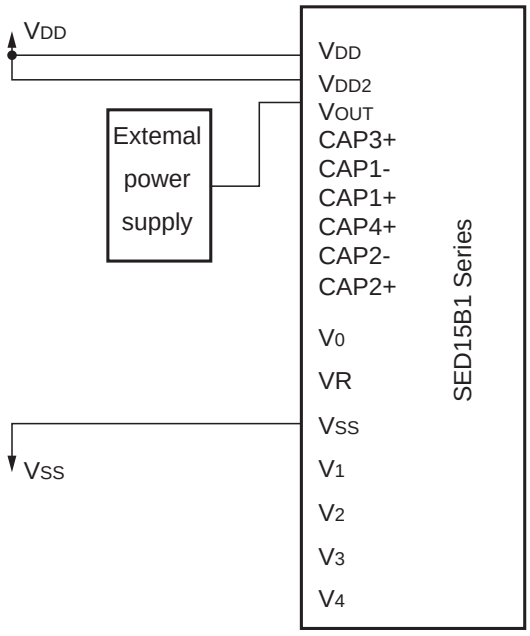


Figure 15

② Use the voltage regulator with external resistor

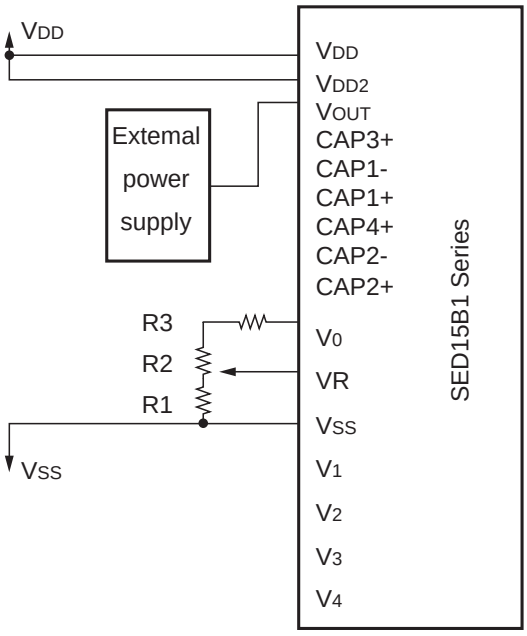


Figure 16

(3) When used only the V/F circuit
[SED15B1D1B]

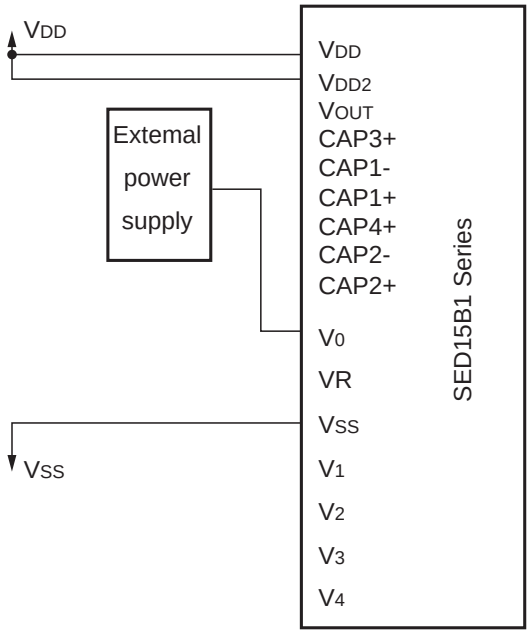


Figure 17

(4) When the on-chip power supply is not used
[SED15B1D2B]

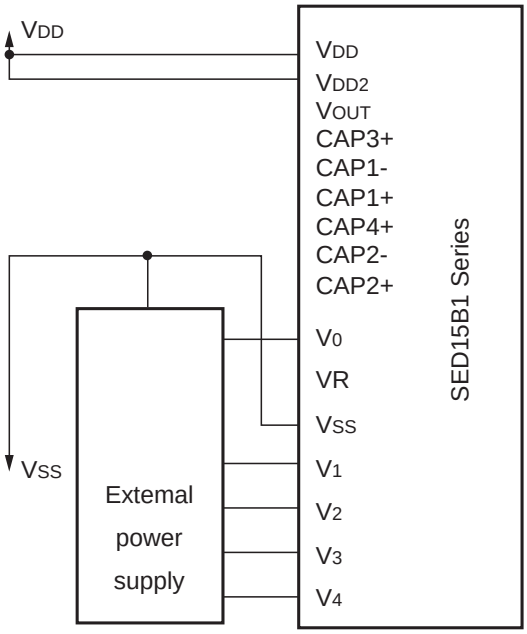


Figure 18

Example of shared reference settings
When V_0 can vary between 8 and 12V

Item	Set value	Units
C_1	1.0 ~ 4.7	µF

Figure 14

* Because the V_R terminal input impedance is high, use short leads and shield lines.

Reset Circuit

When $\overline{RES}$ pin goes low,or when Reset command is used,this LSI is initialized.
Initialized states :

- Serial interface internal shift register and counter clear
- Power saver mode is entered.
  - Oscillation circuit is stopped.
  - The LCD power supply circuit is stopped.
  - Display OFF
  - Display all points ON
  - Segment/common driver outputs go to the V_{SS} level.
- Display normal
- Page address=0H
- Column address=00H
- Display start line address=00H
- Segment driver direction = normal
- Common driver direction = normal
- Read modify write OFF
- Power control register (D2, D1, D0) = (0, 0, 0)
- V_0-resistor ratio register (D2, D1, D0) = (0, 0, 0)
- Electronic volume register (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
- LCD power supply bias ratio = 1/7 bias
- Test mode is released.
- V_0 is shorted to V_{SS} *1
- V_{OUT} is shorted to V_{DD2} *1*2

When reset is detected, this LSI is set to above initialized states. However it has no effect on contents of DDRAM. As seen in "Microprocessor Interface (Reference Example)", connect $\overline{RES}$ pin to the reset pin of the MPU and initialize the MPU at the same time. The initialization by $\overline{RES}$ pin is always required during power-on.
If the control signal from MPU is HZ, an overcurrent may flow through the LSI. A protection is required to prevent the HZ signal at the input pin during power-on.
In case the SED15B1 series does not use the on-chip LCD power supply circuit, $\overline{RES}$ pin must be HIGH when the external LCD power supply is turned on.

*1 This faculty is available only SED15B1D0B.
*2 This faculty is not available by reset command, it is abailable only when hard reset : $\overline{RES}$=LOW is active.

7. COMMANDS

The SED15B1 series identifies the data bus by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals.
In the 8080-series MPU interface, the command is activated when a low pulse is input to $\overline{RD}$ pin for reading and when a low pulse is input to $\overline{WR}$ pin for writing. In the 6800-series MPU interface, the SED15B1 series enters a read mode when a high level is input to R/$\overline{W}$ pin and a write mode when a low level is input to R/$\overline{W}$ pin, and the command is activated when a high pulse is input to E pin. Therefore, in the command explanation and command table, the 6800-series MPU interface is different from the 8080-series MPU interface in that $\overline{RD}$ (E) becomes "1 (H)" in Display data read command. And when the serial interface is selected, the data is input in sequence starting with D7.
Taking the 8080-series MPU interface as an example, commands will be explained below.

Explanation of commands

Display ON/OFF

This command turns the display ON and OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0 1	Display OFF Display ON

When the Display OFF command is executed when in the Display all points ON mode , Power saver mode is entered. See the section on the Power saver for details.

Display normal/reverse

This command can reverse the lit and unlit display without overwriting the contents of the DDRAM.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	Normal:DDRAM Data HIGH =LCD ON voltage Reverse:DDRAM Data LOW =LCD ON voltage

Display all points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the DDRAM. Even when this is done, the DDRAM contents are maintained. This command takes priority over the Display normal/reverse command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

When the Display all points ON command is executed when in the Display OFF mode, Power saver mode is entered. See the section on the Power saver for details.

Page address set

This command specifies the page address of the DDRAM (refer to Figure 5).
Specifying the page address and column address enables to access a desired bit of the DDRAM. After the last column address (83H), page address incremented by +1 (refer to Figure 4). After the very last address (column = 83H, page = 8H), page address return to 0H.
Page address 8H is the DDRAM area dedicate to the indicator, and only D0 is valid for data change.
See the function explanation in "DDRAM and page/column address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0H
							0	0	0	1	1H
							0	0	1	0	2H
								:			:
							0	1	1	1	7H
							1	0	0	0	8H

Column address set

This command specifies the column address of the DDRAM (refer to Figure 5).
The column address is split into two sections (the upper 4-bits and lower 4-bits) when it is set (fundamentally, set continuously).
Each time the DDRAM is accessed, the column address automatically increments by +1, making it possible for the MPU to continuously access to the display data. After the last column address (83H) ,column address returns to 00H (refer to Figure 4).
See the function explanation in "DDRAM and page/column address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper bit address
						0	A3	A2	A1	A0	Lower bit address

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				:				:
1	0	0	0	0	0	1	0	82H
1	0	0	0	0	0	1	1	83H

Display start line address set

This command is used to specify the display start line address of the DDRAM (refer to Figure 5).
If the display start line address is changed dynamically using this command, then screen scrolling, page swapping can be performed.
See the function explanation in "Line address circuit", for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	00H
					0	0	0	0	0	1	01H
					0	0	0	0	1	0	02H
							:				:
					1	1	1	1	1	0	3EH
					1	1	1	1	1	1	3FH

Segment driver direction select

This command can reverse the correspondence between the DDRAM column address and the segment driver output. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Common driver direction select

This command can reverse the correspondence between the DDRAM line address and the common driver output. See the function explanation in “Line address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

*Disabled bit

Display data read

This command reads 8-bit data from the specified DDRAM address. Since the column address is automatically incremented by +1 after each read ,the MPU can continuously read multiple-word data. One dummy read is required immediately after the address has been set. See the function explanation in “Access to DDRAM and internal registers” and “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

Display data write

This command writes 8-bit data to the specified DDRAM address. Since the column address is automatically incremented by +1 after each write ,the MPU can continuously write multiple-word data. See the function explanation in “DDRAM and page/column address circuit”, for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

Read modify write

This command is used paired with End command. Once this command is issued, the column address is not incremented by Display data read command, but is incremented by Display data write command. This mode is maintained until End command is issued. When End command is issued, the column address returns to the address it was at when Read modify write command was issued. This function makes it possible to reduce the MPU load when there are the data to change repeatedly in a specified display region, such as blinking cursor.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

*When End command is issued, only column address returns to the address it was at when Read modify write command was issued, but page address does not return. Consequently, Read modify Write mode cannot be used over pages.
*Even if Read modify write mode, other commands besides Display data read/write can also be used. However, Column address set command cannot be used.

The sequence for cursor display

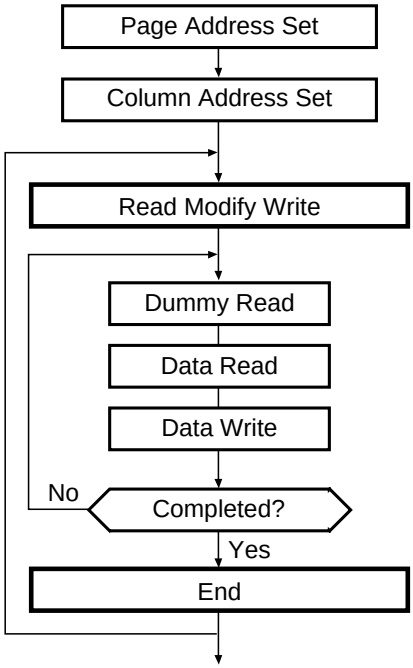


Figure 19

End

This command releases the Read modify write mode, and returns the column address to the address it was when Read modify write command was issued .

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

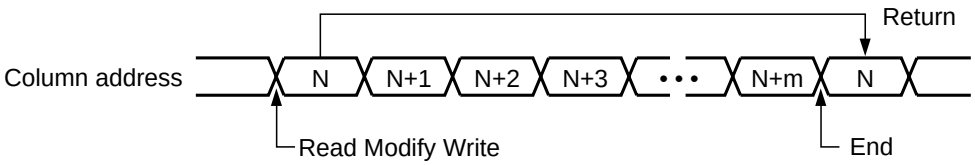


Figure 20

Power control set

This command sets the on-chip power supply function ON/OFF. See the function explanation in “Power supply circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Mode
0	1	0	0	0	1	0	1	0			Booster : OFF
								1			Booster : ON
									0		Voltage regulator : OFF
									1		Voltage regulator : ON
										0	Voltage follower : OFF
										1	Voltage follower : ON

V_0-resistor ratio set

This command sets the internal resistor ratio “Rb/Ra” for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in “Power supply circuit”, for detail.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra : V_0 voltage
0	1	0	0	0	1	0	0	0	0	0	SMALL LOW
								0	0	1	
								0	1	0	
								0	1	1	↓ ↓
								1	0	0	
								1	0	1	
								1	1	0	LARGE HIGH
								1	1	1	External resistor mode

Electronic volume

This command sets a value of electronic volume "α" for the V_0 voltage regulator to adjust the contrast of LCD panel display. See the function explanation in "Power supply circuit", for detail.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	α : V0 voltage	
0	1	0	1	0	0	0	0	0	0	0	31	LOW
						0	0	0	0	1		
						0	0	0	1	0		
								↓			↓	↓
						1	1	1	1	0		
						1	1	1	1	1	0	HIGH

LCD bias set

This command selects the voltage bias ratio required for the LCD. This command is enabled when the voltage follower circuit operates.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Bias SED15B1
0	1	0	1	0	1	0	0	0	1	0	1/9 bias
										1	1/7 bias

Power saver

When the display all points ON command is executed when in the display OFF mode, power saver mode is entered, and the power consumption can be greatly reduced.

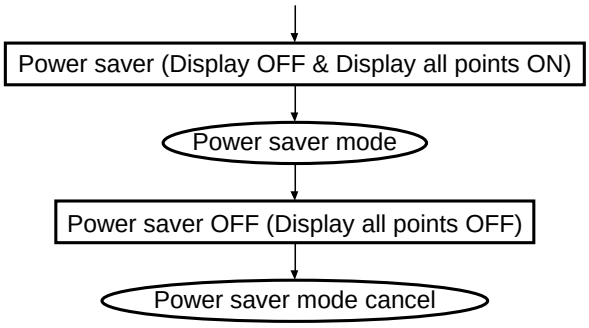


Figure 21

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the MPU. The internal states in the power saver mode is as follows:

- The oscillation circuit is stopped.
- The LCD power supply circuit is stopped.
- The LCD driver circuit is stopped and segment/common driver outputs output the V_{SS} level.
- The display data and operation mode before execution of the Power saver command are held, and the MPU can access to the DDRAM and internal registers.

Reset

This LSI is in initialized by this command. And when SED15B1D0B is used, V0 is shorted to VSS. (Only when $\overline{RES}$= LOW, VOUT is shorted to VSS. So VOUT is not shorted to VSS by this commands.) See the function explanation in "Reset circuit", for detail.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

NOP

Non-operation command

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for LSI chip testing. Please do not use. If the test command is issued by accident, it can be cleared by applying an LOW signal to the $\overline{RES}$ pin, or by issuing the Reset command or the Display ON/OFF command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

* Disabled bit

(Note):
The SED15B1 series chip maintain their operating modes ,but excessive external noise, etc., may happen to change them. Thus in the packaging and system design it is necessary to suppress the noise or take measures to prevent the noise. Moreover, it is recommended that the operating modes are refreshed periodically to prevent the effects of unanticipated noise.

Command Table

Table 14

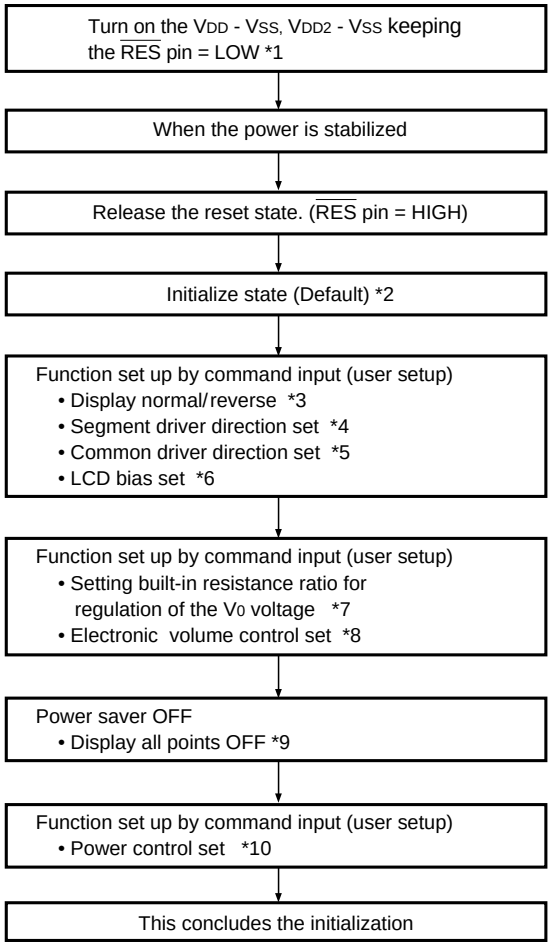
Command	Code											Function
	A0	XR	XW	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display 0:OFF, 1:ON
Display normal/reverce	0	1	0	1	0	1	0	0	1	1	0 1	LCD display 0:normal, 1:reverce
Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	LCD display 0:normal display, 1:all points ON
Page address set	0	1	0	1	0	1	1	address				Sets the DDRAM page address
Column address set Upper 4-bit address	0	1	0	0	0	0	1	address				Sets the DDRAM column address
Column address set Lower 4-bit address	0	1	0	0	0	0	0	address				
Display start line address set	0	1	0	0	1	address						Sets the DDRAM display start line address.
Segment driver directuin select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the correspondence between the DDRAM column address and the SEG driver output. 0:normal, 1:reverse
Common driver direction select	0	1	0	1	1	0	0	0 1	*	*	*	Sets the correspondence between the DDRAM line address and the COM driver output. 0:normal, 1:reverse
Display data read	1	0	1	Read data								Reads from the DDRAM.
Display data write	1	1	0	Write data								Writes to the DDRAM.
Read modify write	0	1	0	1	1	1	0	0	0	0	0	Column address increment at write:+1, at read:0.
End	0	1	0	1	1	1	0	1	1	1	0	Releases Read modify write mode.
Power control set	0	1	0	0	0	1	0	1	Operating mode			Sets the on-chip power supply circuit operating mode.
V_0-resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Sets the V_0-resistor ratio value.
Electronic volume	0	1	0	1	0	0	Electronic volume value					Sets the electronic volume value.
LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. SED15B1 0:1/9bias, 1:1/7bias
Power saver	-	-	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Display all points ON
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation
Test	0	1	0	1	1	*	1	*	*	*	*	IC test command. Do not use.

(Note)*:disabled bit

8. COMMAND DESCRIPTION

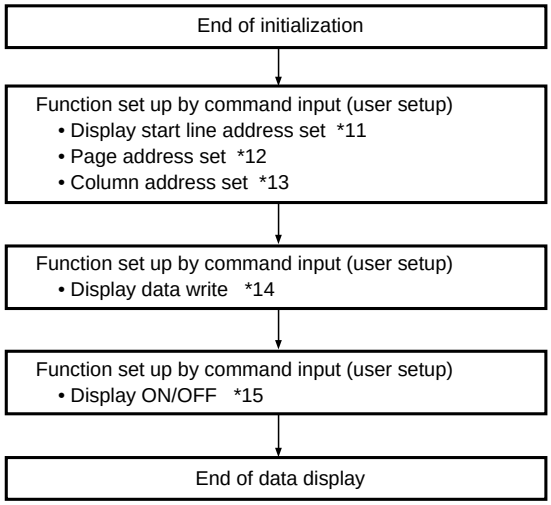
Instruction Setup of SED15B1D0B : Reference

(1) Initialization



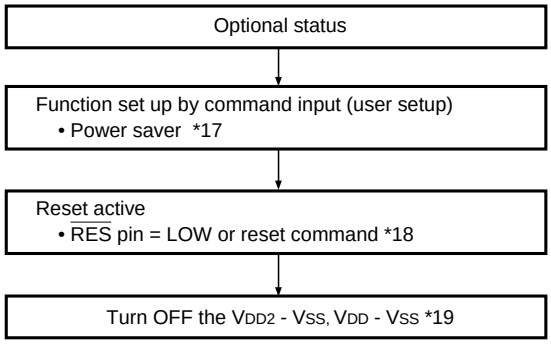
Notes: Refer to respective sections or paragraphs listed below
*1: Description of Timing characteristics; Notes for Power on Sequence
*2: Description of functional; Reset Circuit
*3: Command Description; Display normal/reverse
*4: Command Description; Segment driver direction select
*5: Command Description; Common driver direction select
*6: Command Description; LCD bias set
*7: Description of functions; Power supply circuit & Command description; V0-resistor ratio set
*8: Description of functions; Power supply circuit & Command description; Electronic volume
*9: Command Description; Power saver
*10: Description of functions; Power supply circuit & Command description; Power control set

(2) Data display



Notes: Reference items
*11: Command Description; Display start line address set
*12: Command Description; Page address set
*13: Command Description; Column address set
*14: Command Description; Display data write
*15: Command Description; Display ON/OFF

(3) Power OFF *16



Notes: Reference items
*16: After turning OFF the internal power supply, turn OFF the power supply of this IC.
(Function Description; Power supply circuit)
When the power of this IC is turned OFF with the internal power supply is held in the ON status, since the where the voltage is supplied, even though an only little, to on chip LCD drive circuit is still continued, it is featured to ill affect the display quality of the LCD panel. To avoid this, be sure to observe the power OFF sequence strictly.
*17: Command Description; Power saver
*18: It is recommended to be $\overline{\text{RES}}$ pin=LOW. Only if it is not possible to be $\overline{\text{RES}}$ pin=LOW, ase reset command.
*19: Set the time t_L from reset active to turning off the V_{DD2}/V_{DD} power, longer then the time t_H when the potential of $V_0 \sim V_4$ becomes below the threshold voltage (approximately 1V) of the LCD panel. ($t_L > t_H$) If $t_L < t_H$, an irregular display may occur.
Refer to the < Reference Data > as below. When t_H is too long, insert a resis for between V_0 and V_{SS} to reduce it.

<Reference Data>
Condition: V_{DD}=V_{DD2}=1.8V, Quintuple boosting, Boosting Capacitance 1 µ F,
Set the V_0 voltage to 8V
t_H (µ s) is calculated the following equation.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0$

CL :The capacitance of LCD panel connected between V_0 and V_{SS}
t_{H0} :t_H at the CL=0
Δt_H :t_H when the V_0 drops 1V per the CL=1pF.

This is reference data, so it is needed to estimate a real LCD module since t_H is depends on the V_{DD}/V_{DD2} voltage and the capacitance of LCD panel.

① In case of $\overline{RES}$ pin=LOW

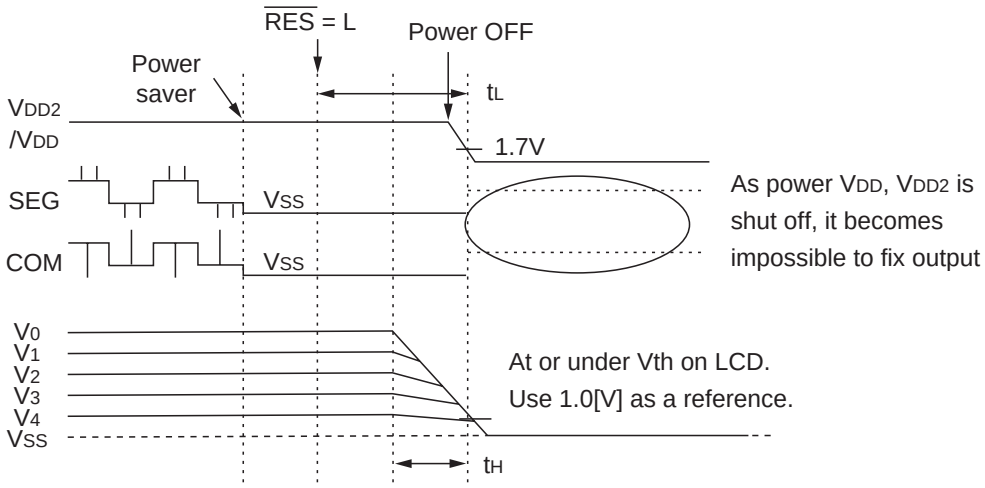


Figure 22

SED15B1D0B has the discharge faculty that is shorted V_{OUT} to V_{DD2}, when $\overline{RES}$ pin=LOW.
As t_{H0}=70(µs/V), Δt_H=0.079(µs/V/nF) by measurement, t_H is calculated as follows, when V_0=7V and CL=100pF.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0 = 70 \times 7 + 0.079 \times 100 \times 7 = 545 \mu s$

② In case of reset command

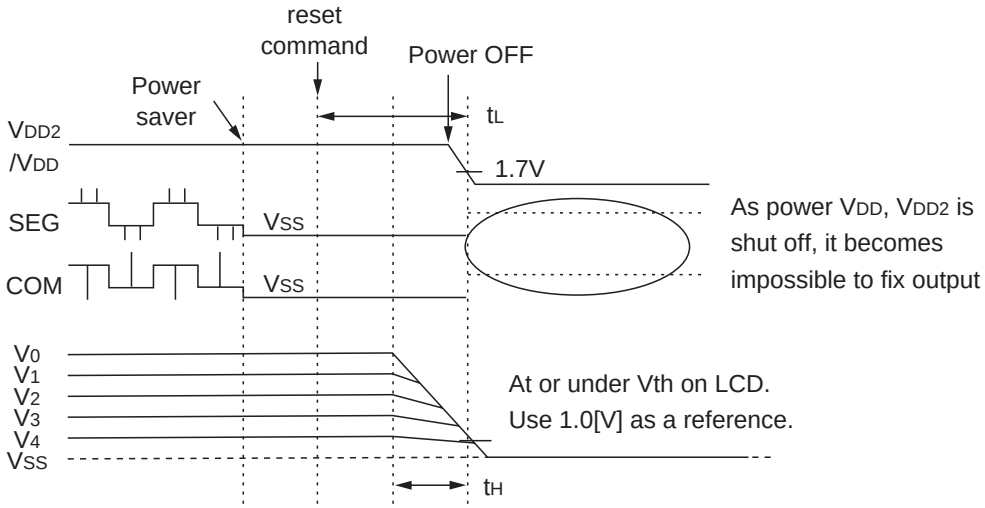


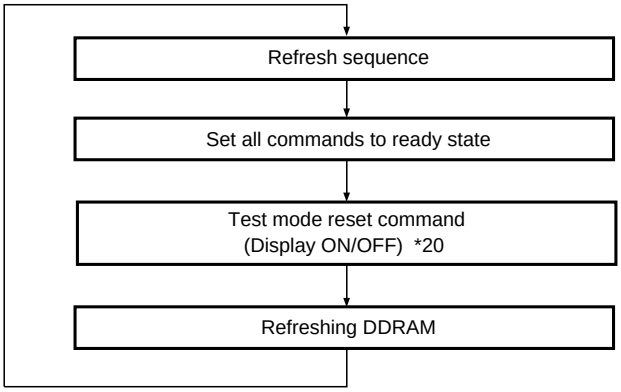
Figure 23

V_{OUT} is not shorted to V_{DD2} by reset command, so t_H is longer than the case of $\overline{RES}$ pin=LOW.
As t_{H0}=175(µs/V), Δt_H=0.23(µs/V/nF) by measurement, t_H is calculated as follows, when V_0=7V and CL=100pF.

$t_H = t_{H0} \times V_0 + \Delta t_H \times CL \times V_0 = 175 \times 7 + 0.23 \times 100 \times 7 = 1386 \mu s$

(3) Refresh

It is recommended to turn on the refresh sequence regularly at specified interval.



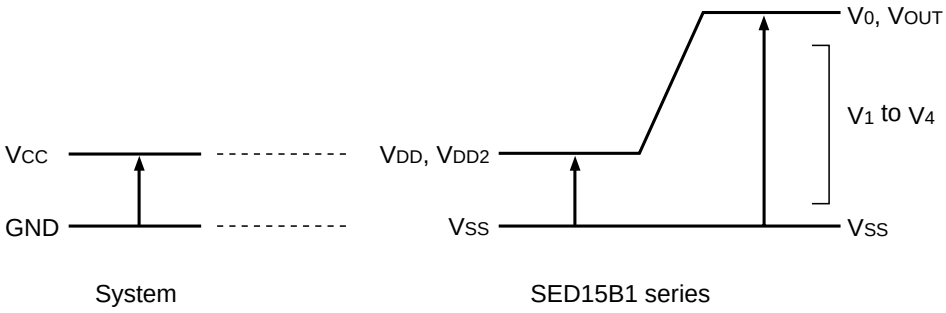
Notes: Reference items
*20: Command description; Display ON/OFF

9. ABSOLUTE MAXIMUM RATING

Unless otherwise noted, V_{SS} = 0V.

Table 15

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DD}	–0.3 to 7.0	V
Power supply voltage (2)		V_{DD2}	–0.3 to 7.0	V
	Double boosting		–0.3 to 7.0	
	Triple boosting		–0.3 to 6.0	
	Quadruple boosting		–0.3 to 4.5	
	Quintuple boosting		–0.3 to 3.6	
Power supply voltage (3)		V_0, V_{OUT}	–0.3 to 18.0	V
Power supply voltage (4)		V_1, V_2, V_3, V_4	–0.3 to V_0	V
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature		T_{OPR}	–40 to 85	°C
Storage temperature	TCP	T_{STR}	–55 to 100	°C
	Bare chip		–55 to 125	



Notes and Conditions

1. Voltage $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ must always be satisfied.
2. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

10. ELECTRICAL CHARACTERISTICS

DC Characteristics

Table 16 V_{SS}=0V, V_{DD}=3V±10%, Ta=–40 to 85°C unless otherwise noted.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage(1)	Recommended operation	V_{DD}	(Relative to V_{SS})	1.8	–	3.6	V	V_{DD} *1
	Operational			1.7	–	5.5	V	
Power voltage(2)	Recommended operation	V_{DD2}	(Relative to V_{SS})	1.8	–	3.6	V	V_{DD2} *1
	Operational			1.7	–	5.5		
	Booster circuit operatinal voltage		Double boosting	3.0	–	5.5		
			Triple boosting	2.0	–	5.0		
			Quadruple boosting	1.7	–	4.0		
			Quintuple boosting	1.7	–	3.0		
Voltage regulator operational voltage		V_{OUT}	(Relative to V_{SS})	6.0	–	16.0	V	V_{OUT}
Voltage follower operational voltage		V_0		4.5	–	16.0	V	V_0 *2
		V_1, V_2		0.6×V_0	–	V_0		V_1,V_2
		V_3, V_4		V_{SS}	–	0.4×V_0		V_3,V_4
Reference voltage		V_{REG}	Ta=25°C	1.26	1.30	1.34	V	*3
High-level input voltage		V_{IH}		0.8×V_{DD}	–	V_{DD}	V	*4
Low-level input voltage		V_{IL}		V_{SS}	–	0.2×V_{DD}	V	
High-level output voltage		V_{OH}	I_{OH}=-0.5mA	0.8×V_{DD}	–	V_{DD}	V	*5
Low-level output voltage		V_{OL}	I_{OL}=0.5mA	V_{SS}	–	0.2×V_{DD}	V	
Input leakage current		I_{LI}		–1.0	–	–1.0	µA	*6
Output leakage current		I_{LO}		–3.0	–	–3.0	µA	*7
LCD driver ON resistance		R_{ON}	V_0=8V Ta=25°C		2.0	5.0	KΩ	SEGn, COMn *8
Static current consumption		I_{DDQ}	Ta=25°C	–	0.01	5	µA	V_{DD}, V_{DD2}
		I_{0Q}	V_0=16V Ta=25°C	–	0.01	15	µA	V_5
Input terminal capacitance		C_{IN}	f =1MHz Ta=25°C		20	35	pF	
Oscillation frequency		f_{OSC}	Ta=25°C	4.55	5.2	5.85	kHz	*9

Relationship between oscillation frequency f_{osc} and frame rate frequency f_{FR} : $f_{FR} = f_{osc}/ 65$
Relationship between external clock (CL) frequency f_{CL} and frame rate frequency f_{FR} : $f_{FR} = f_{CL}/ 8/ 65$

Current consumption

Dynamic current consumption (1) : During display, when the internal power supply circuit is OFF (external power supply is used).

Table 17 Display Pattern OFF Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
SED15B1***	I_0(1)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V	–	20	33	µA	*10
		V_{DD}=V_{DD2}=2.7V, V_0=11.0V	–	29	48		

Table 18 Display Pattern Checker Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
SED15B1***	I_0(1)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V	–	24	40	µA	*10
		V_{DD}=V_{DD2}=2.7V, V_0=11.0V	–	33	55		

Dynamic current consumption (2) : During display, when the internal power supply circuit is ON.

Table 19 Display Pattern OFF Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
SED15B1***	I_{DD}+I_{DD2} (2)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V Triple boosting	–	75	125	µA	*9
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	96	160		
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	119	198		

Table 20 Display Pattern Checker Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
SED15B1***	I_{DD}+I_{DD2} (2)	V_{DD}=V_{DD2}=2.7V, V_0=8.0V Triple boosting	–	86	143	µA	*9
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	110	183		
		V_{DD}=V_{DD2}=2.7V, V_0=8.0V Quadruple boosting	–	136	227		

Table 21 Power saver Ta=25˚C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
SED15B1***	I_{DD}(2)	V_{DD}=V_{DD2}=1.7V to 3.6V	–	0.01	5	µA	*9

Reference data

Dynamic current consumption (1) : During display, when the internal power supply circuit is OFF (external power supply is used).

Conditions : Internal power supply OFF. External supply in use.
V_0=8.0V, Display pattern : OFF, Ta=25˚C

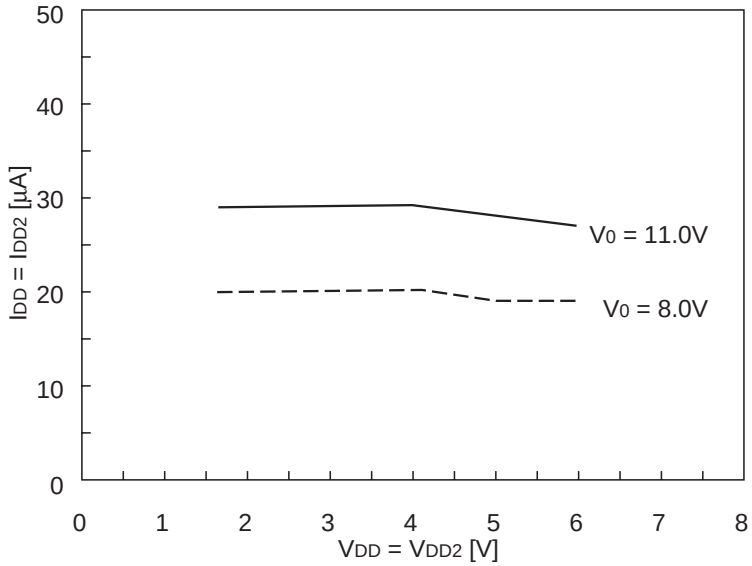


Figure 24

Conditions : Internal power supply OFF. External supply in use.
V_0=8.0V, Display pattern : Checker, Ta=25˚C

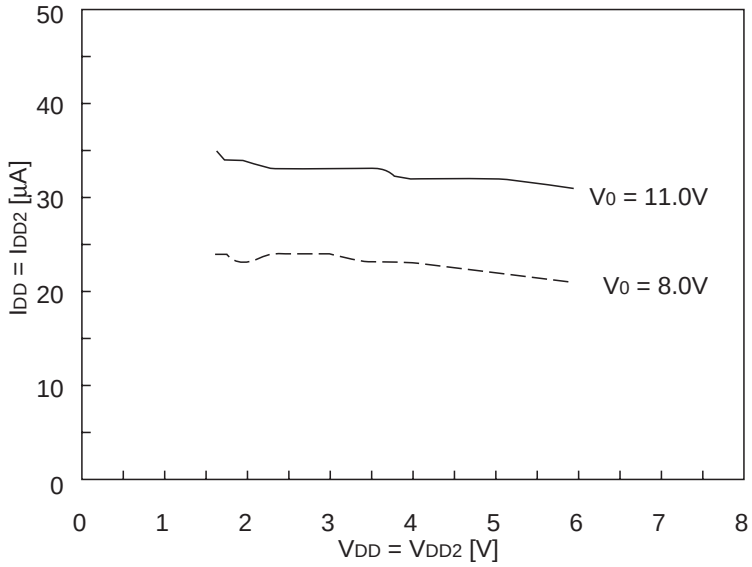


Figure 25

Dynamic current consumption (2) : During display, when the internal power supply circuit is ON.

Conditions : Internal power supply ON.
V_0=8.0V, Display pattern : OFF, Ta=25˚C

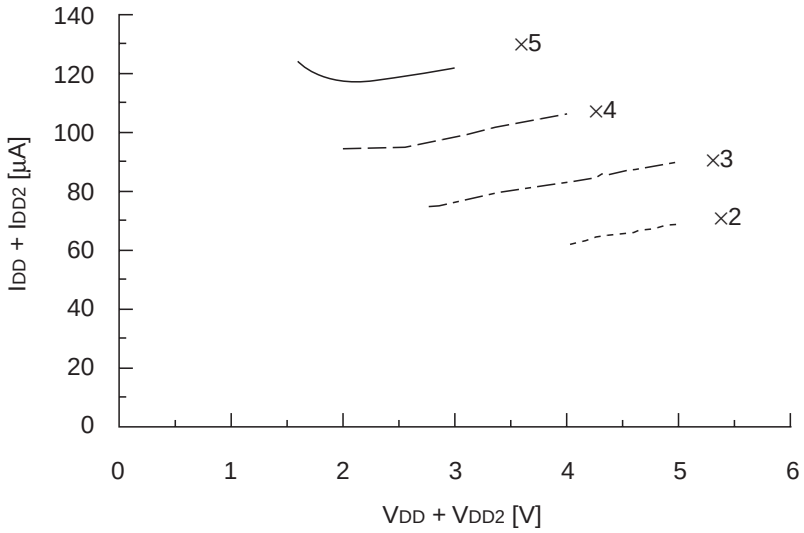


Figure 26

Conditions : Internal power supply ON.
V_0=8.0V, Display pattern : Checker, Ta=25˚C

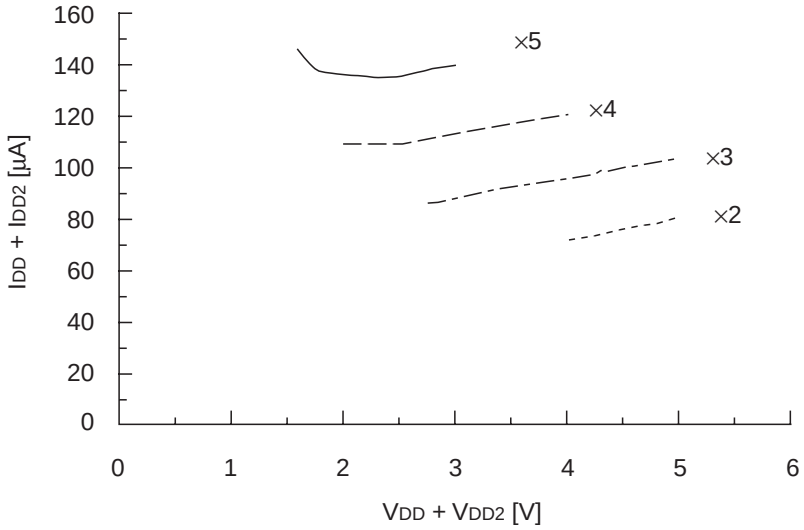


Figure 27

Dynamic current consumption (3) : During access and display (Checker pattern is constantly written at f_{CYC} and displayed), when the on-chip power supply circuit is ON.

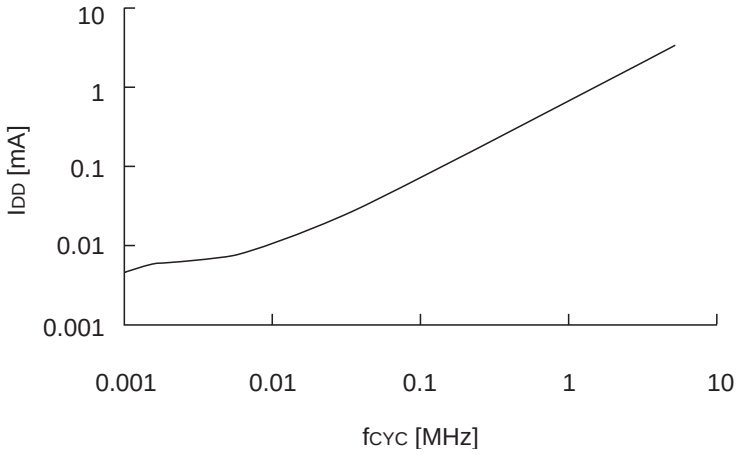


Figure 28

V_{DD}, V_{DD2} and V_0 (V_{OUT}) operation voltage range

(1) SED15B1D0B

① V_{DD}=V_{DD2}

In the range of V_{DD}=V_{DD2}<3.2V, the maximum V_0 voltage is determined by V_{OUT} voltage of the quintuple boosting. It is necessary to keep V_{OUT} > V_0 for preventing irregular display. The voltage of $|V_{OUT} - V_0|$ is determined by LCD panel, so it is recommended to check the actual LCD module and set them.

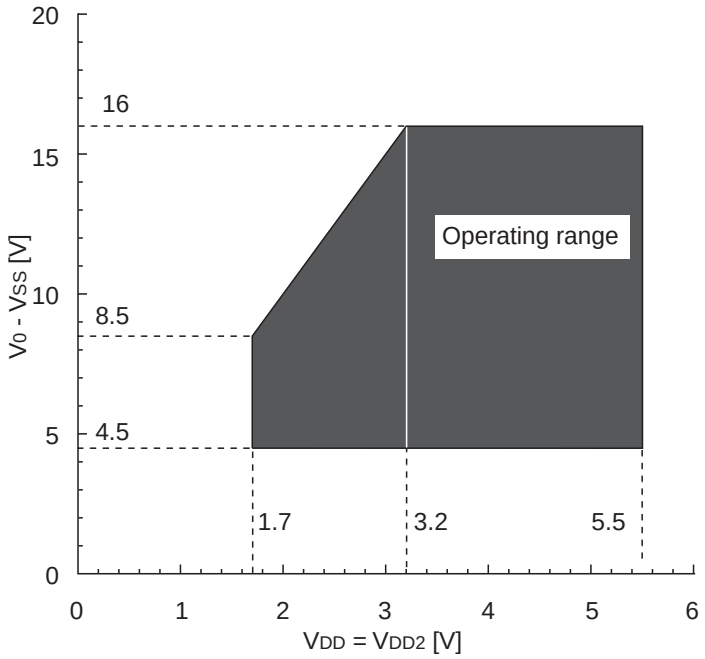


Figure 29

② V_{DD}<V_{DD2}

In the case, it is necessary to keep 1.7V≤V_{DD}≤V_{DD2}≤3.6V. And the V_{DD2} should be set to keep V_{OUT}>V_0.

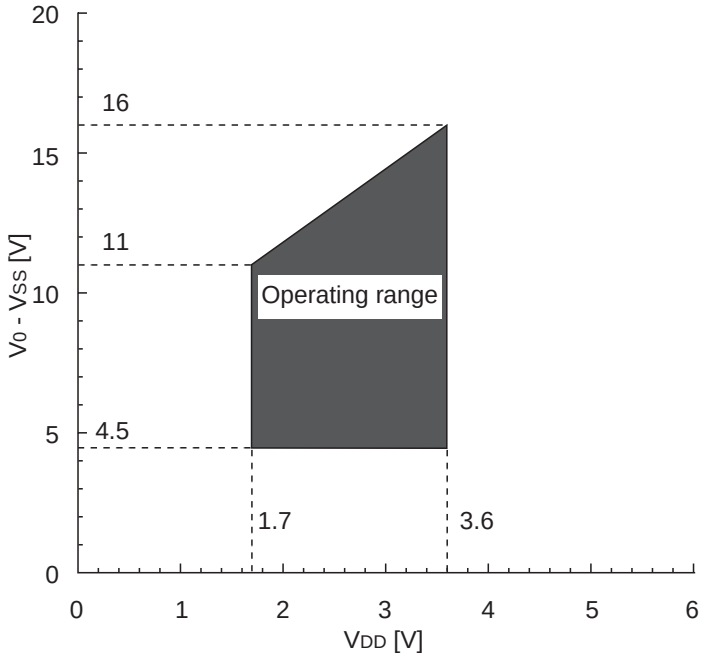


Figure 30

(2) SED15B1D1B
If $V_{DD}=V_{DD2}$, the operating range of V_{DD}/V_{DD2} is $1.7V \le V_{DD}=V_{DD2} \le 4.5V$. And if $V_{DD}<V_{DD2}$, the operating range of V_{DD}/V_{DD2} is $1.7V \le V_{DD}<V_{DD2} \le 3.6V$
① Eternal voltage : V_{OUT}
In this case, the relationship between V_{OUT} and V_{DD}/V_{DD2} is required as shown in Figure 31.

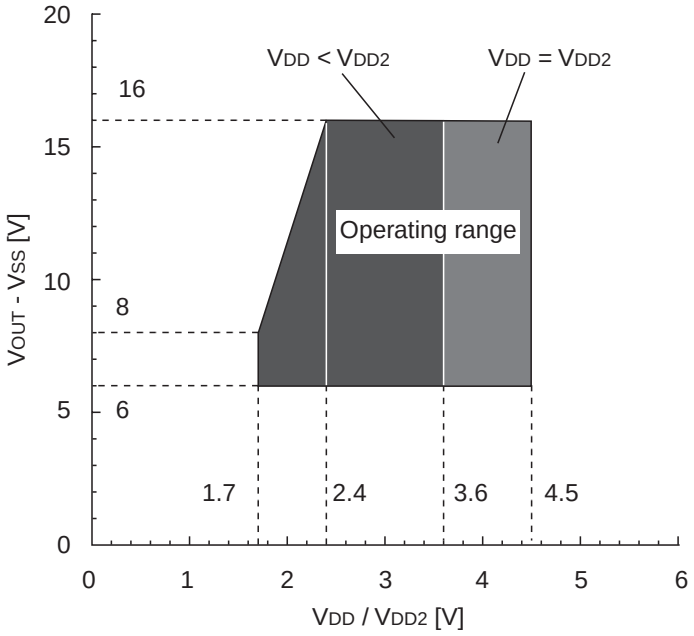


Figure 31

② Eternal voltage : V_0
In this case, the relationship between V_0 and V_{DD}/V_{DD2} is required as shown in Figure 32.

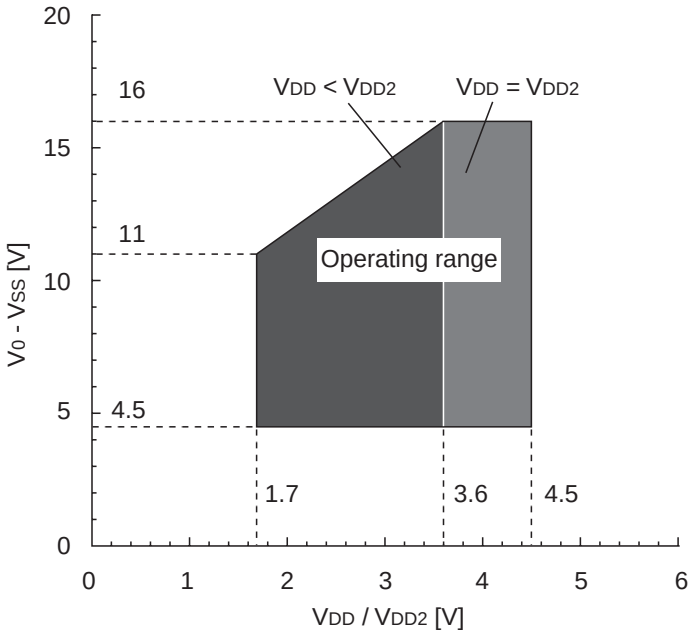


Figure 32

(3) SED15B1D2B
Eternal voltage: V_0, V_1 to V_4
In this case, V_0 operating range is same as Figure 32, and $V_0 \ge V_1 \ge V_2 \ge V_3 \ge V_4 \ge V_{SS}$ is required.

*1. Though the wide range of operating voltage is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage during being accessed from MPU.
This V_{DD}, V_{DD2} operational voltage range (1.7V to 5.5V) is in case of $V_{DD}=V_{DD2}$. If $V_{DD}\neq V_{DD2}$, it becomes to be $1.7V\leq V_{DD}<V_{DD2}\leq 3.6V$.
*2. V_{DD}, V_{DD2} and V_0 operating voltage range is shown in Figure.
*3. V_{REG} is internal constant voltage source for V_0 voltage regulator circuit.
*4. D7 (SI), D6 (SCL), D5 to D0, A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$),C86, P/S and CL pins
*5. D7 to D0 pins
*6. A0, $\overline{CS}$, $\overline{RES}$, $\overline{RD}$ (E), $\overline{WE}$ (R/$\overline{W}$), C86, P/S and CL pins
*7. D7 (SI), D6 (SCL) and D5 to D0 pins
*8. Resistance value when 0.1V is applied between the output pin SEGn or COMn and each power supply pin (V_0, V_1, V_2, V_3, V_4, V_{SS}). This is specified in the “Voltage follower operating voltage” range. $R_{ON} = 0.1V/\Delta I$ (ΔI : Current flowing when 0.1V is applied between that output pin and those power supply pin).
*9. Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc.

Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080-series MPU)

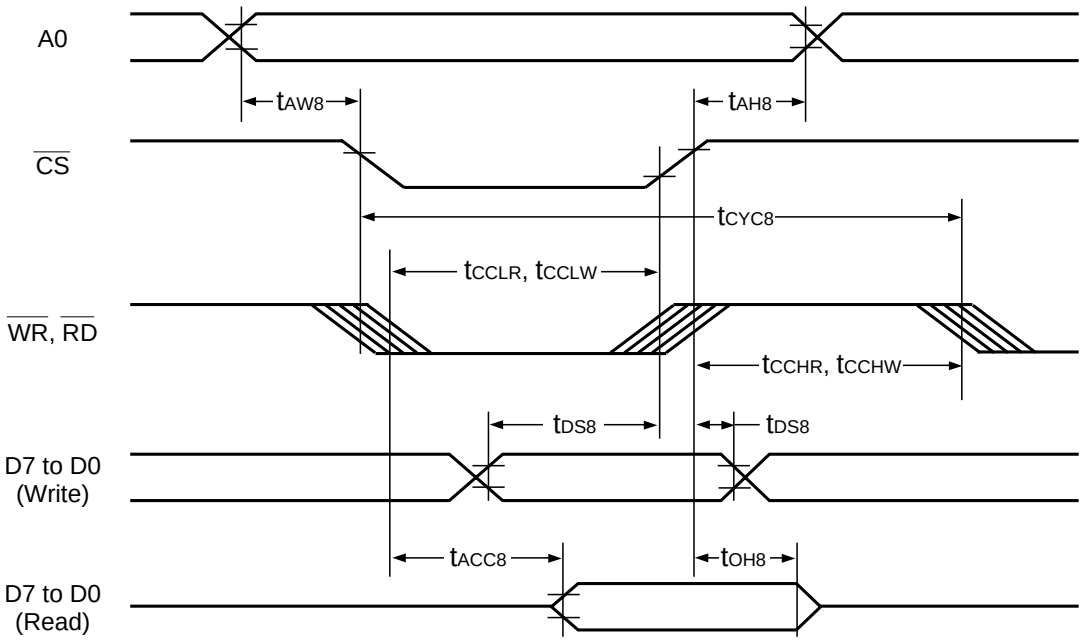


Figure 33

Table 22 [V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		160	–	
Control LOW pulse width(WR)	$\overline{WR}$	t_{CCLW}		30	–	
Control LOW pulse width(RD)	$\overline{RD}$	t_{CCLR}		70	–	
Control HIGH pulse width(WR)	$\overline{WR}$	t_{CCHW}		30	–	
Control HIGH pulse width(RD)	$\overline{RD}$	t_{CCHR}		30	–	
Data setup time	D7 to D0	t_{DS8}		20	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	70	
Output disable time		t_{OH8}		5	50	

Table 23 [V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		260	–	
Control LOW pulse width(WR)	$\overline{WR}$	t_{CCLW}		60	–	
Control LOW pulse width(RD)	$\overline{RD}$	t_{CCLR}		120	–	
Control HIGH pulse width(WR)	$\overline{WR}$	t_{CCHW}		60	–	
Control HIGH pulse width(RD)	$\overline{RD}$	t_{CCHR}		60	–	
Data setup time	D7 to D0	t_{DS8}		35	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	120	
Output disable time		t_{OH8}		10	100	

Table 24 [V_{DD}=1.7V to 2.7V, Ta=–40 to 85°C]

Item	Signal	Symbol	Condition	Min.	Max.	Units
Address hold time	A0	t_{AH8}		0	–	ns
Address setup time		t_{AW8}		0	–	
System cycle time		t_{CYC8}		700	–	
Control LOW pulse width(WR)	$\overline{WR}$	t_{CCLW}		120	–	
Control LOW pulse width(RD)	$\overline{RD}$	t_{CCLR}		240	–	
Control HIGH pulse width(WR)	$\overline{WR}$	t_{CCHW}		120	–	
Control HIGH pulse width(RD)	$\overline{RD}$	t_{CCHR}		120	–	
Data setup time	D7 to D0	t_{DS8}		90	–	
Data hold time		t_{DH8}		0	–	
Access time		t_{ACC8}	CL=100pF	–	240	
Output disable time		t_{OH8}		10	200	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) ≤ (t_{CYC8}-t_{CCLW}-t_{CCHW}) or (t_r, t_f) ≤ (t_{CYC8}-t_{CCLR}-t_{CCHR}).
*2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
*3. t_{CCLW} and t_{CCLR} are specified by the overlap period in which $\overline{CS}$ is “0” and $\overline{WR}$, $\overline{RD}$ are “0”.

System Bus Read/Write Characteristics 2 (For the 6800-series MPU)

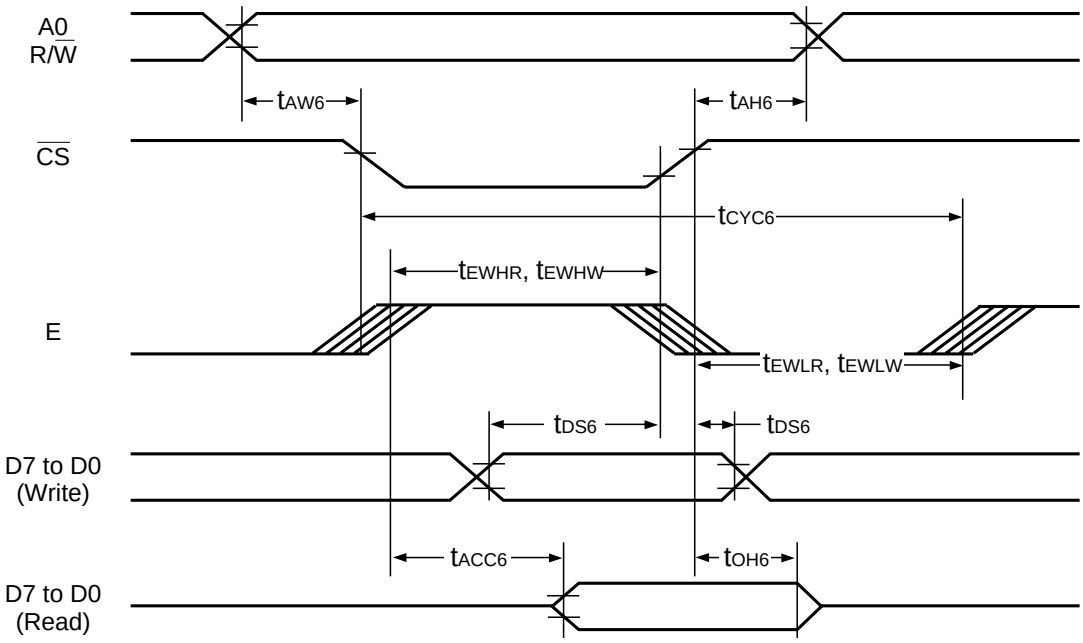


Figure 34

Table 25 [V_{DD}=4.5V to 5.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0, $\overline{WR}$	t_{AH6}		0	–	ns
Address setup time			t_{AW6}		0	–	
System cycle time			t_{CYC6}		160	–	
Enable HIGH pulse width	Width	E	t_{EWHW}		30	–	
	Read		t_{EWHR}		70	–	
Enable LOW pulse width	Width	E	t_{EWLW}		30	–	
	Read		t_{EWLR}		30	–	
Data setup time		D7 to D0	t_{DS6}		20	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	70	
Output disable time			t_{OH6}		5	50	

Table 26 [V_{DD}=2.7V to 4.5V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		260	–	
Enable	Width	E	t_{EWHW}		60	–	
HIGH pulse width	Read		t_{EWHR}		120	–	
Enable	Width		t_{EWLW}		60	–	
LOW pulse width	Read		t_{EWLR}		60	–	
Data setup time		D7 to D0	t_{DS6}		35	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	120	
Output disable time			t_{OH6}		10	100	

Table 27 [V_{DD}=1.7V to 2.7V, Ta=–40 to 85°C]

Item		Signal	Symbol	Condition	Min.	Max.	Units
Address hold time		A0,	t_{AH6}		0	–	ns
Address setup time		$\overline{WR}$	t_{AW6}		0	–	
System cycle time			t_{CYC6}		700	–	
Enable	Width	E	t_{EWHW}		120	–	
HIGH pulse width	Read		t_{EWHR}		240	–	
Enable	Width		t_{EWLW}		120	–	
LOW pulse width	Read		t_{EWLR}		120	–	
Data setup time		D7 to D0	t_{DS6}		90	–	
Data hold time			t_{DH6}		0	–	
Access time			t_{ACC6}	CL=100pF	–	240	
Output disable time			t_{OH6}		10	200	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 10ns or less. When the system cycle time is extremely fast, it is specified by (t_r, t_f) ≤ (t_{CYC6}-t_{EWHW}-t_{EWLW}) or (t_r, t_f) ≤ (t_{CYC6}-t_{EWHR}-t_{EWLR}).
*2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
*3. t_{EWHW} and t_{EWHR} are specified by the overlap period in which $\overline{CS}$ is “0” and E is “1”.

Serial interface

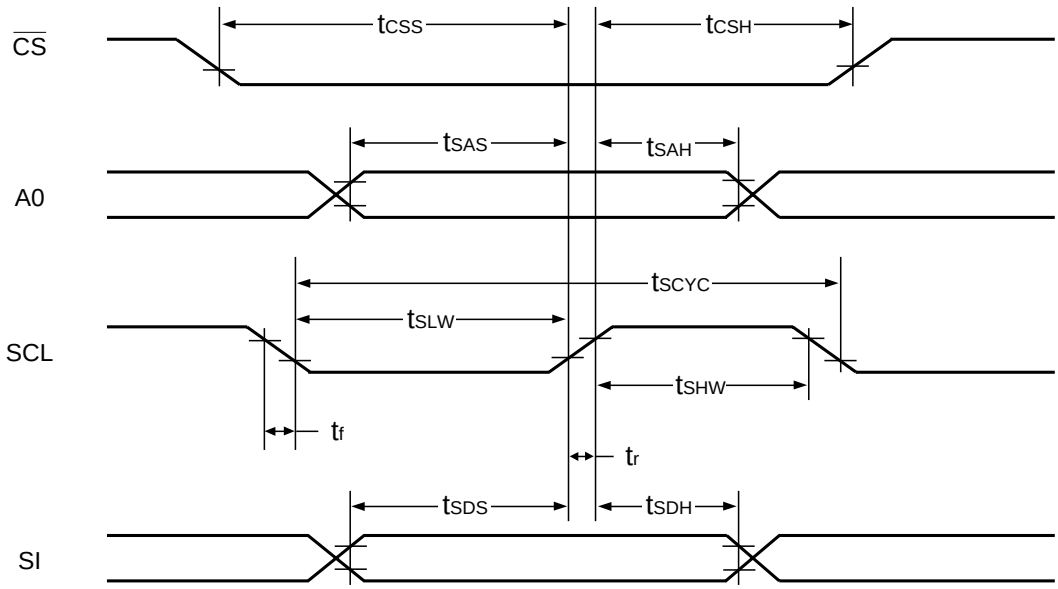


Figure 35

Table 28 V_{DD}=4.5 to 5.5V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		40	–	ns
Serial clock HIGH pulse width		t_{SHW}		15	–	
Serial clock LOW pulse width		t_{SLW}		15	–	
Address setup time	A0	t_{SAS}		10	–	
Address hold time		t_{SAH}		20	–	
Data setup time	SI	t_{SDS}		3	–	
Data hold time		t_{SDH}		3	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		10	–	
		t_{CSH}		25	–	

Table 29 V_{DD}=2.7 to 4.5V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		70	–	ns
Serial clock HIGH pulse width		t_{SHW}		25	–	
Serial clock LOW pulse width		t_{SLW}		25	–	
Address setup time	A0	t_{SAS}		20	–	
Address hold time		t_{SAH}		40	–	
Data setup time	SI	t_{SDS}		5	–	
Data hold time		t_{SDH}		5	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		15	–	
		t_{CSH}		50	–	

Table 30 V_{DD}=1.7 to 2.7V, Ta=–40 to 85°C

Item	Signal	Symbol	Condition	Min.	Max.	Units
Serial clock cycle	SCL	t_{SCYC}		150	–	ns
Serial clock HIGH pulse width		t_{SHW}		50	–	
Serial clock LOW pulse width		t_{SLW}		50	–	
Address setup time	A0	t_{SAS}		45	–	
Address hold time		t_{SAH}		90	–	
Data setup time	SI	t_{SDS}		10	–	
Data hold time		t_{SDH}		10	–	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		50	–	
		t_{CSH}		100	–	

Note : 1. The input Signal rise and fall times must be with in 10ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Reset timing

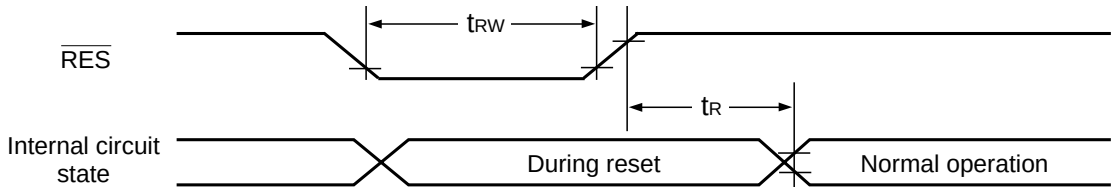


Figure 36

Table 31 V_{DD}=4.5 to 5.5V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	250	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		250	–	

Table 32 V_{DD}=2.7 to 4.5V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	500	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		500	–	

Table 33 V_{DD}=1.7 to 2.7V, Ta=–40 to 85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Units
Reset time		t_R		–	1000	ns
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	–	

Note : 1. The input Signal rise and fall times must be with in 10ns.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

Notes for Power on Sequence

It is preferable to turn on power supply V_{DD} and V_{DD2} at the same time, but if V_{DD} turn on after V_{DD2}, then it is necessary that the below 3 conditions are satisfied.

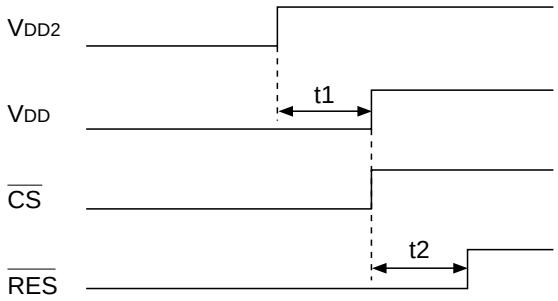


Figure 37

A. t1 < 1ms, during this timing, all input pins are fixed to V_{SS}.
B. $\overline{CS}$ becomes HIGH simultaneously with V_{DD}.
C. t2 > 100ns (Reset is canceled after V_{DD2} and rise up).

11. THE MPU INTERFACE (REFERENCE EXAMPLES)

The SED15B1 series can directly be connected to the 80 system MPU and 68 series MPU. It can also be operated with a fewer signal lines by using the serial interface.
After the initialization using the RES pin, the respective input pins of the SED15B1 series need to controlled normally.

(1) 80 series MPU

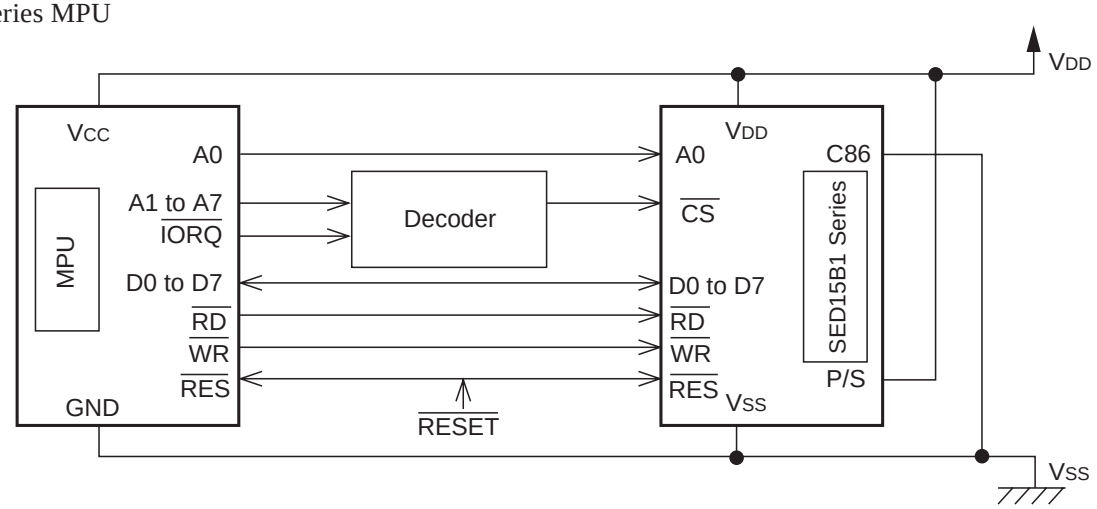


Figure 38

(2) 6800 series MPU

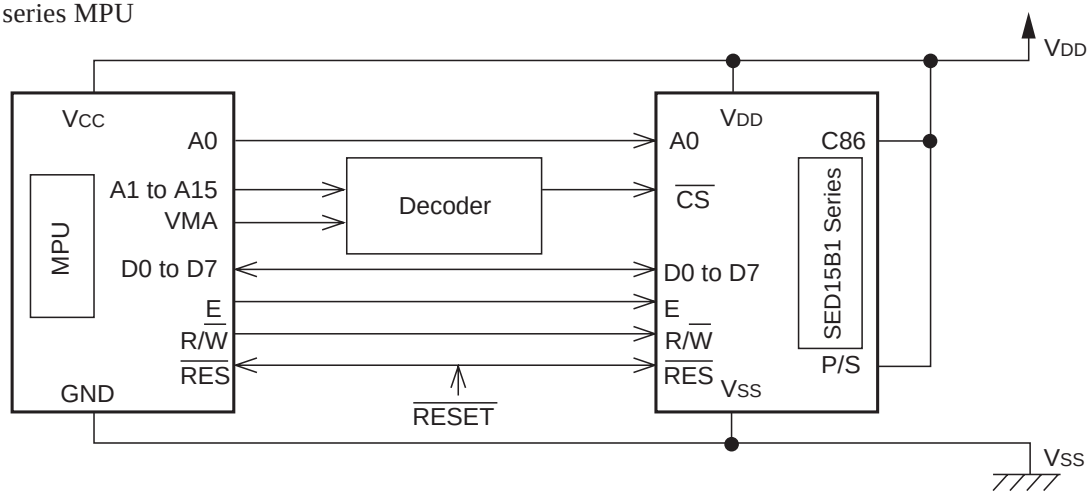


Figure 39

(3) Using serial interface

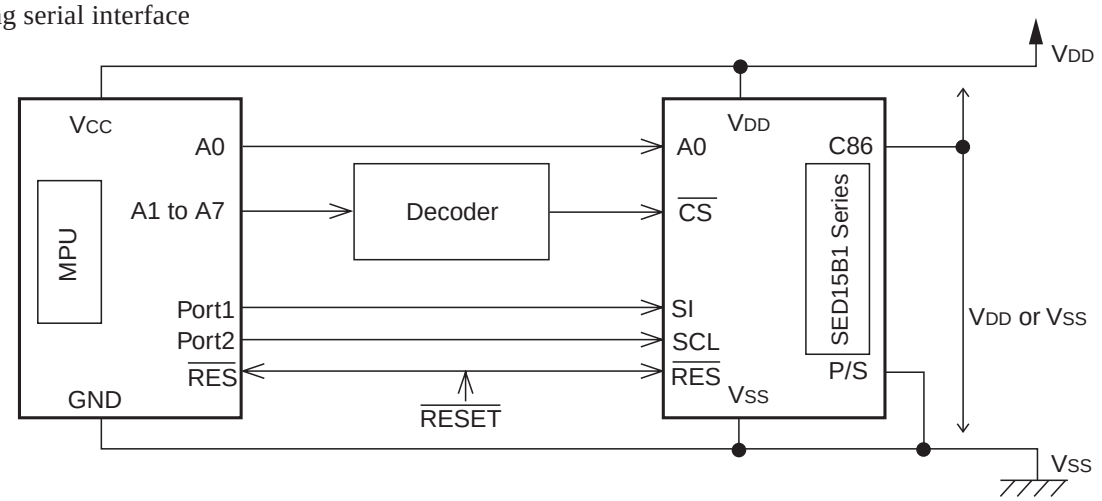


Figure 40

12. NOTES

Please be advised on the following points in the use of this development specification.

1. This development specification is subject to change without previous notice.
2. This development specification does not guarantee or furnish the industrial property right not its execution.
   Application examples in this development specification are intended to ensure your better understanding of the product. Thus the manufacturer shall not be liable for any trouble arising in your circuits from using such application example.
   Numerical values provided in the property table of this manual are represented with their magnitude on the numerical line.
3. No part of this development specification may not be reproduced, copied or used for commercialpurpose without a written permission from the manufacturer.

In handling of semiconductor devices, your attention is required to following points.

[Precaution on light]

Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs mounted on the boards or products, make sure that:

(1) Your design and mounting layout done are so that the IC is not exposed to light in actual use.

(2) The IC is protected from light in the inspection process.

(3) The IC is protected from light in its front, rear and side faces.

[Precautions when installing the COG]

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.

Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

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