8. SED1651
Dot Matrix LCD Common Driver

CONTENTS

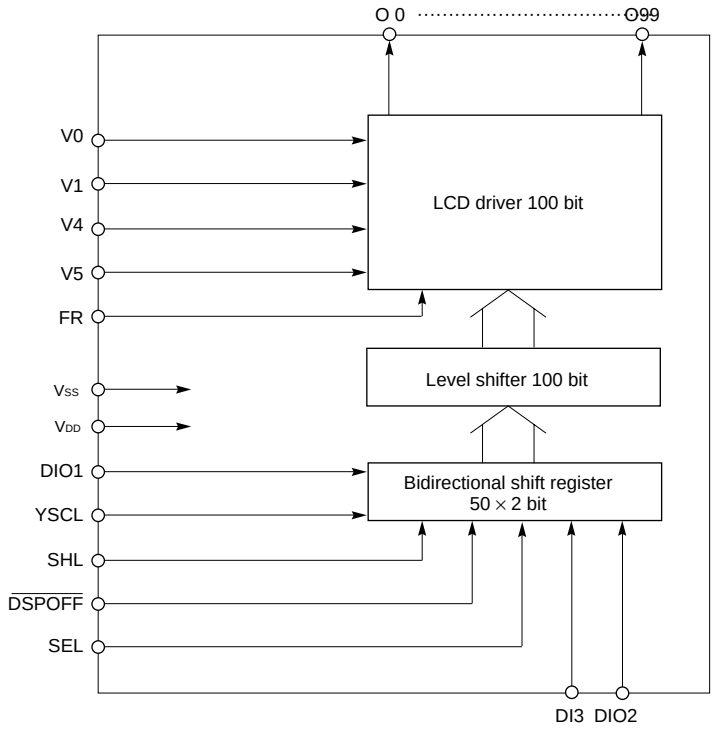
OVERVIEW

The SED1651 is a 100 output low-power resistance common)row) driver which is suitable for driving a very high capacity dotmatrix LCD panels. It is intended to be used in conjunction with the SED1648 as a pair.
Since the SED1651 is so designed to drive LCD's over a wide range of voltages, and also the maximum potential V_0 of its LCD driving bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.

FEATURES

- Number of LCD drive output segments: 100
- Super slim chip configuration
- Common output ON resistance: 750Ω (Typ.)
- Display capacity ... Possible to display 640 × 480 dots.
- Selectable pin output shift direction
- No bias display OFF function
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –8 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging SED1651D$_{0A}$ (AL-pad die form)
- No radial rays countermeasure taken in designing

BLOCK DIAGRAM

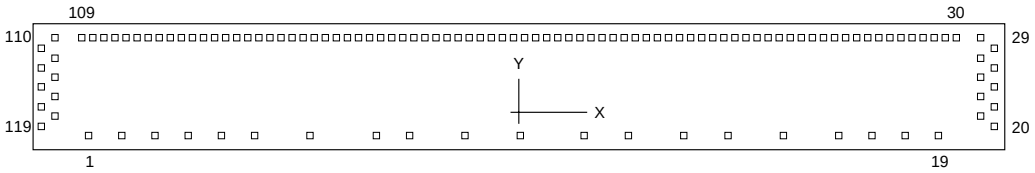


PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>O0 to O99</td><td>O</td><td>LCD drive common (row) output
The output changes at the YSCL falling edge.</td><td>80</td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>50 × 2 bits bidirectional shift register serial data input/output
To be set to input or output according to the SHL input
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>This is the input pin of scanning pulse in the 50 × 2 bits configuration.
When SEL = L, the DI3 pin to V_{SS} or GND.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Selection input of bidirectional shift register operating mode
H ... 50 × 2 (DI3 input) L ... 100</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input
The scanning data is shifted at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control input
<table>
<tr><th>SHL</th><th>O output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 49 50 → 99</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>99 → 50 49 → 0</td><td>Ourput</td><td>Input</td></tr>
</table>
When SEL = “H”, the DI3 input is set to O50 (SHL = “L”) or O49 (SHL = “H”).
When SEL = “L”, the D13 input is ignored and the DIO inputs are shifted continuously.</td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOFF}}$</td><td>I</td><td>LCD display blanking control input
When “L” is input, the content of shift register is cleared and all common outputs become the V_0 level instantaneously.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output converted signal input</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V (GND) V_{SS}: –2.7 V to –5.5 V</td><td>3</td></tr>
<tr><td>V0, V1,
V4, V5</td><td>Power supply</td><td>LCD drive power supply V_5: –8 V to –28 V
$V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$</td><td>8</td></tr>
</table>

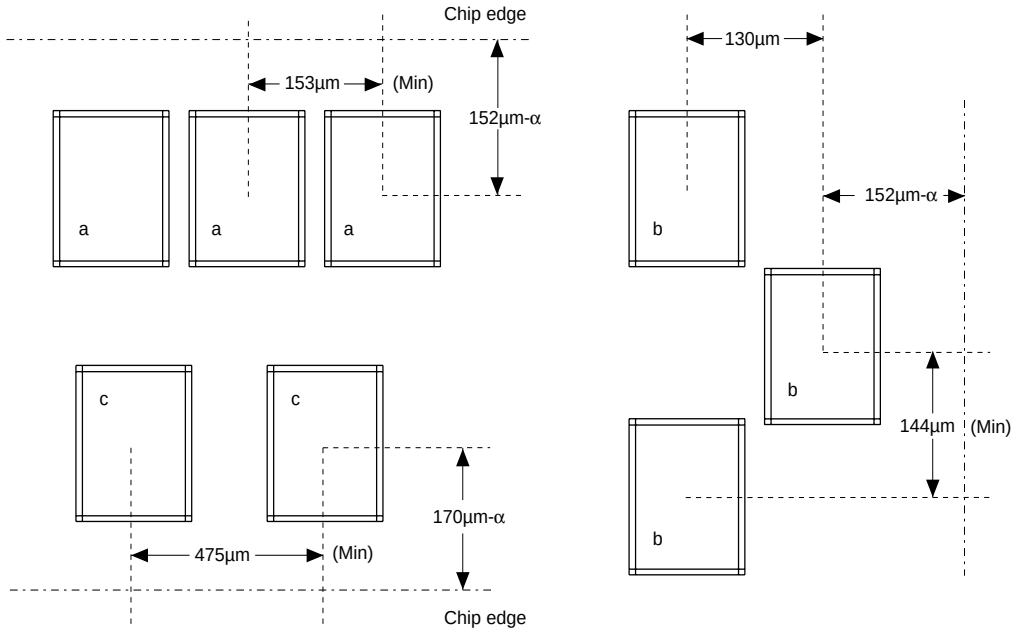
Respectively
Total: 119

PAD LAYOUT AND COORDINATES



Chip size: ..... 13.43 mm × 1.76 mm
Chip thickness: ..... 400 µm (Typ.)

1) AL pad specifications (SED1651D0A)



Pad	a	Opening (X, Y)	110 × 110µm	PAD No 30 to 109
Pad	b	Opening (X, Y)	110 × 110µm	PAD No 20 to 29, 110 to 119
Pad	c	Opening (X, Y)	110 × 110µm	PAD No 1 to 19

Unit (μm)

PAD		Actual dimensions	
NO.	NAME	X	Y
1	DIO2	–5985	–709
2	V0	–5510	
3	V1	–5035	
4	V4	–4560	
5	V5	–4038	
6	V_{SS}	–3164	
7	SEL	–2280	
8	SHL	–1767	
9	DI3	–1064	
10	YSCL	–181	
11	V_{DD}	770	
12	$\overline{\text{DSPOFF}}$	1283	
13	FR	2176	
14	V_{SS}	2879	
15	V5	3753	
16	V4	4560	
17	V1	5035	
18	V0	5510	
19	DIO1	5985	
20	O0	6560	–610
21	O1	6430	–466
22	O2	6560	–321
23	O3	6430	–177
24	O4	6560	–32
25	O5	6430	112
26	O6	6560	257
27	O7	6430	401
28	O8	6560	545
29	O9	6430	690
30	O10	6079	727
31	O11	5925	
32	O12	5771	
33	O13	5617	
34	O14	5463	
35	O15	5310	
36	O16	5156	
37	O17	5002	
38	O18	4848	
39	O19	4694	
40	O20	4540	
41	O21	4386	
42	O22	4232	

PAD		Actual dimensions	
NO.	NAME	X	Y
43	O23	4078	727
44	O24	3924	
45	O25	3771	
46	O26	3617	
47	O27	3463	
48	O28	3309	
49	O29	3155	
50	O30	3001	
51	O31	2847	
52	O32	2693	
53	O33	2539	
54	O34	2385	
55	O35	2232	
56	O36	2078	
57	O37	1924	
58	O38	1770	
59	O39	1616	
60	O40	1462	
61	O41	1308	
62	O42	1154	
63	O43	1000	
64	O44	846	
65	O45	693	
66	O46	539	
67	O47	385	
68	O48	231	
69	O49	77	
70	O50	–77	
71	O51	–231	
72	O52	–385	
73	O53	–539	
74	O54	–693	
75	O55	–846	
76	O55	–1000	
77	O57	–1154	
78	O58	–1308	
79	O59	–1462	
80	O60	–1616	
81	O61	–1770	
82	O62	–1924	
83	O63	–2078	
84	O64	–2232	

PAD		Actual dimensions	
NO.	NAME	X	Y
85	O65	–2385	727
86	O66	–2539	
87	O67	–2693	
88	O68	–2847	
89	O69	–3001	
90	O70	–3155	
91	O71	–3309	
92	O72	–3463	
93	O73	–3617	
94	O74	–3771	
95	O78	–3924	
96	O76	–4078	
97	O77	–4232	
98	O78	–4386	
99	O79	–4540	
100	O80	–4694	
101	O81	–4848	
102	O82	–5002	
103	O83	–5156	
104	O84	–5310	
105	O85	–5463	
106	O86	–5617	
107	O87	–5771	
108	O88	–5925	
109	O89	–6079	
110	O90	–6430	690
111	O91	–6560	545
112	O92	–6430	401
113	O93	–6560	257
114	O94	–6430	112
115	O95	–6560	–32
116	O96	–6430	–177
117	O97	–6560	–321
118	O98	–6430	–466
119	O99	–6560	–610

FUNCTIONAL DESCRIPTION

Shift register

This is a bidirectional shift register to transfer common data.
Being a 50 × 2 bits configuration, this register can select 50 × 2 bits or 100 bits according to the status of SEL.
When the 50 × 2 bits configuration is selected, the input of the 50-bit shift register becomes D13.

Level shifter

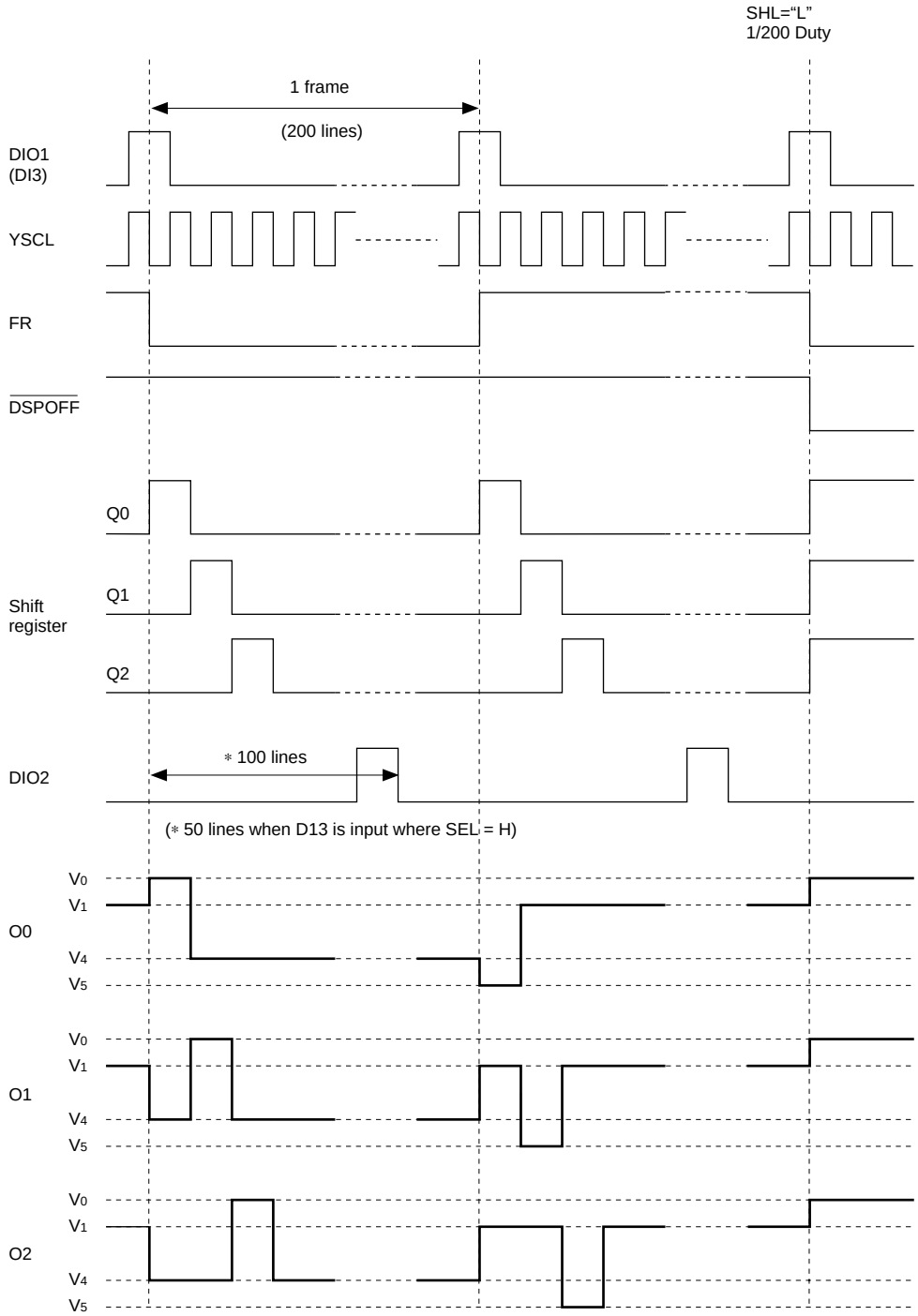
This is a level interface circuit used to convert the signal voltage level from the logic system level to LCD drive level.

LCD driver

This driver outputs the LCD drive voltage.
The relationship among the display blanking signal $\overline{\text{DSPOFF}}$, contents of shift register, AC converted signal FR and On output voltage is as shown in the table below:

$\overline{\text{DSPOFF}}$	Content of shift register	FR	O output voltage	
H	H	H	V_5	(Select level)
		L	V_0	
	L	H	V_1	(Non-select level)
		L	V_4	
L	–	–	V_0	–

TIMING CHART



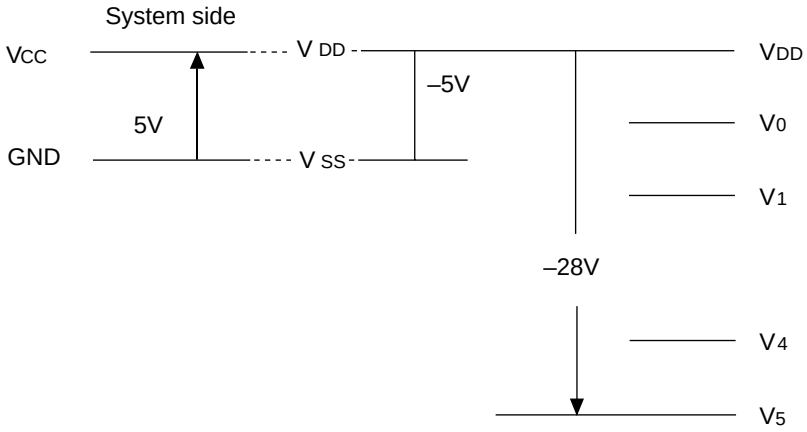
ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltage	V_I	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg 1	–65 to +150	°C

Notes*

1. The voltage of V_0, V_1, V_4 and V_5 must always satisfy the condition of $V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$.



2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or less can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
   Care should be taken to the power supply sequence especially in the system power ON or OFF.

ELECTRICAL CHARACTERISTICS

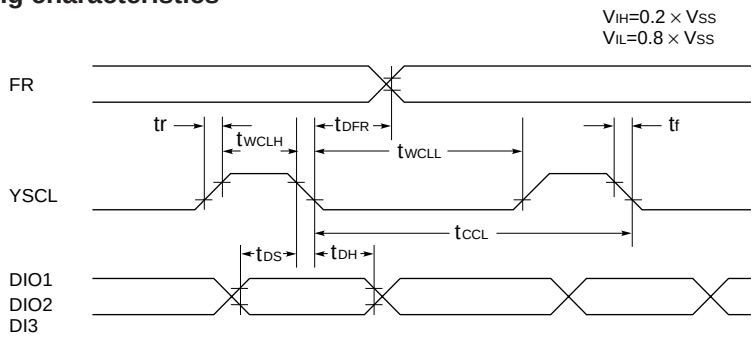
DC characteristics

Unless otherwise specified, $V_{DD} = V_0 = 0V$, $V_{SS} = -5.5V$–$2.7V$, Ta = –40 to 85°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–12.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–8.0	V	V_5
Supply voltage (2)	V_0	–	2.5	–	0	V	V_0
Supply voltage (3)	V_1	–	$2/9 \cdot V_5$	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	–	V_5	–	$7/9 \cdot V_5$	V	V_4
"H" input voltage	V_{IH}	–	$0.2 \cdot V_{SS}$	–	–	V	DIO1, DIO2, FR, YSCL, SHL, DI3 $\overline{DSPOFF}$, SEL
"L" input voltage	V_{IL}	–	–	–	$0.8 \cdot V_{SS}$	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA	V_{DD}–0.4	–	–	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=0.3mA	–	–	V_{SS}+0.4	V	
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	–	–	2.0	µA	YSCL, SHL, DI3 $\overline{DSPOFF}$, FR, SEL
Input/output leakage current	$I_{LI/O}$	$V_{SS} \le V_{IN} \le 0V$	–	–	5.0	µA	DIO1, DIO2
Static current	I_{DDS}	V_5=–12.0 ~ –28.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔV_{ON}=0.5V $V_0=V_{DD}$, V_1=–1.5V V_4=–18.5V V_5=–20.0V	–	0.75	1.0	KΩ	O0~O99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$, f_{YSCL}=12KHz Frame frequency=60Hz Input data: 1/200 Ta=25°C ?	–	7	15	µA	V_{SS}
		V_{SS}=–3.0V Other conditions are the same as V_{SS} = –5.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0V, V_0=0V, V_1=1.5V, V_4=18.5V, V_{EE}=V5=–20.0V Other conditions are the same as in the item of ISS 1.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{DSPOFF}$, FR, DI3, SEL
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

AC CHARACTERISTICS

Input timing characteristics



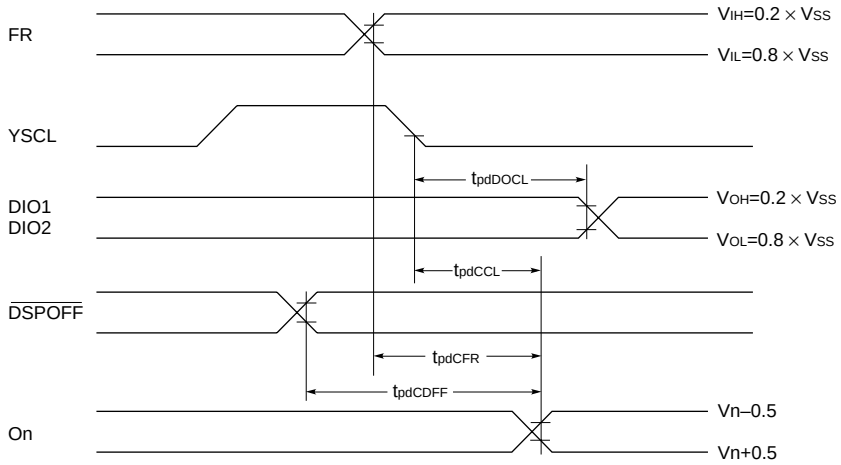
VSS=–5.0V±0.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	500	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	70	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	100	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–300	300	ns

VSS=–5.0V±0.5V, Ta=–40 to 85°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Input signal rise time	t_r	–	–	50	ns
Input signal fall time	t_f	–	–	50	ns
YSCL period	t_{CCL}	–	1000	–	ns
YSCL “H” pulsewidth	t_{WCLH}	–	160	–	ns
YSCL “L” pulsewidth	t_{WCLL}	–	330	–	ns
Data setup time	t_{DS}	–	200	–	ns
Data hold time	t_{DH}	–	10	–	ns
Allowable FR delay time	t_{DFR}	–	–500	500	ns

Output timing characteristics



VSS=–5.0±10%, Ta=–40 to +85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	tpdDOCL	CL=15pF	–	350	ns
(YSCL - fall to On output) delay time	tpdCCL	V5=–12.0 to –28.0V	–	1.0	µs
($\overline{\text{DSPOFF}}$ to On output) delay time	tpdCDOFF				
(FR to On Output) delay time	tpdCFR	CL=100pF	–	1.0	µs

VSS=–4.5–2.7V, Ta=–40 to +85°C

Parament	Symbol	Condition	Min.	Max.	Unit
(YSCL - fall to DIO) delay time	tpdDOCL	CL=15pF	–	400	ns
(YSCL - fall to On output) delay time	tpdCCL	V5=–12.0 to –28.0V	–	2.0	µs
($\overline{\text{DSPOFF}}$ to On output) delay time	tpdCDOFF				
(FR to On Output) delay time	tpdCFR	CL=100pF	–	2.0	µs

LCD DRIVE POWER

Each voltage level forming method

To obtain each voltage level for LCD driving, it is optimum to divide the resistance of potential between V_{DDH} and GND to drive the LCD using the voltage follower with an operational amplifier. In taking into consideration of such a case using the operational amplifier, the maximum potential level V_0 for LCD driving has been made a separate pin from V_{DD}.
When no operational amplifier is used in V_0, set $V_0 = V_{DD}$.
When a resistive divider is used, set it to a resistance value as low as possible in the system power capacity.
When a series resistance exists in the power supply line of V_{DD}, a voltage drop of V_{DD} occurs at the LSI power supply pin, the relationship with the LCD's intermediate potential ($V_{DD} \geq V_0 \geq V_1 \geq V_4 \geq V_5$) cannot be met, this causing the LSI to be broken down in some cases. When a protection resistor is inserted, it is necessary to stabilize the voltage by capacitance.

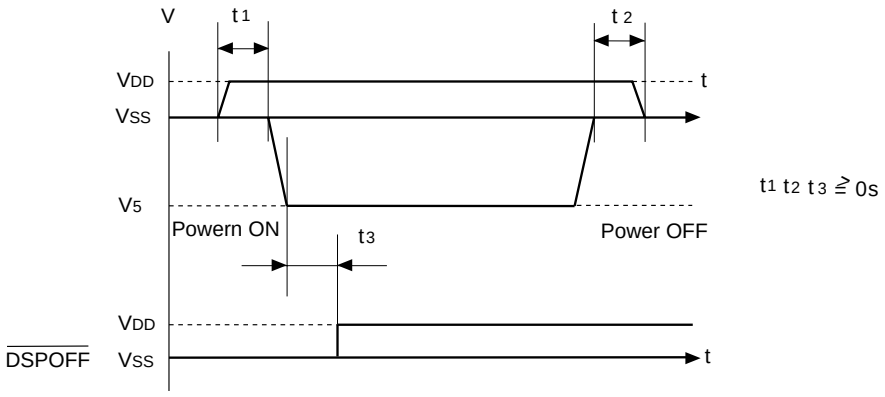
Note in power ON/OFF

Since this LSI is high in the voltage of LCD driving system, when a high voltage is applied to the LCD driving system with the logic system power supply kept floating or above V_{SS} = –2.5 V, an overcurrent flows and LSI breaks down in some cases.
To avoid this, it is recommended to suppress the potential of LCD drive output to V_0 level using the display off function ($\overline{DSPOFF}$) until the LCD driving system voltage is stabilized.

Be sure to follow the power ON/OFF sequence as shown below:

At power ON ... Logic system ON → LCD driving system ON or simultaneous ON of the both
At power OFF ... LCD driving system OFF → Logic system OFF or simultaneous OFF of the both

For a countermeasure to such overcurrent, it is effective to put a high-speed melting fuse or protection resistor in series with the LCD power unit.
It is then required to select the optimum value in the protection resistance according to the capacitance of LC cell.



TYPICAL CIRCUIT DIAGRAM

Configuration Drawing of Large Screen LCD