7. SED1753
LCD Driver

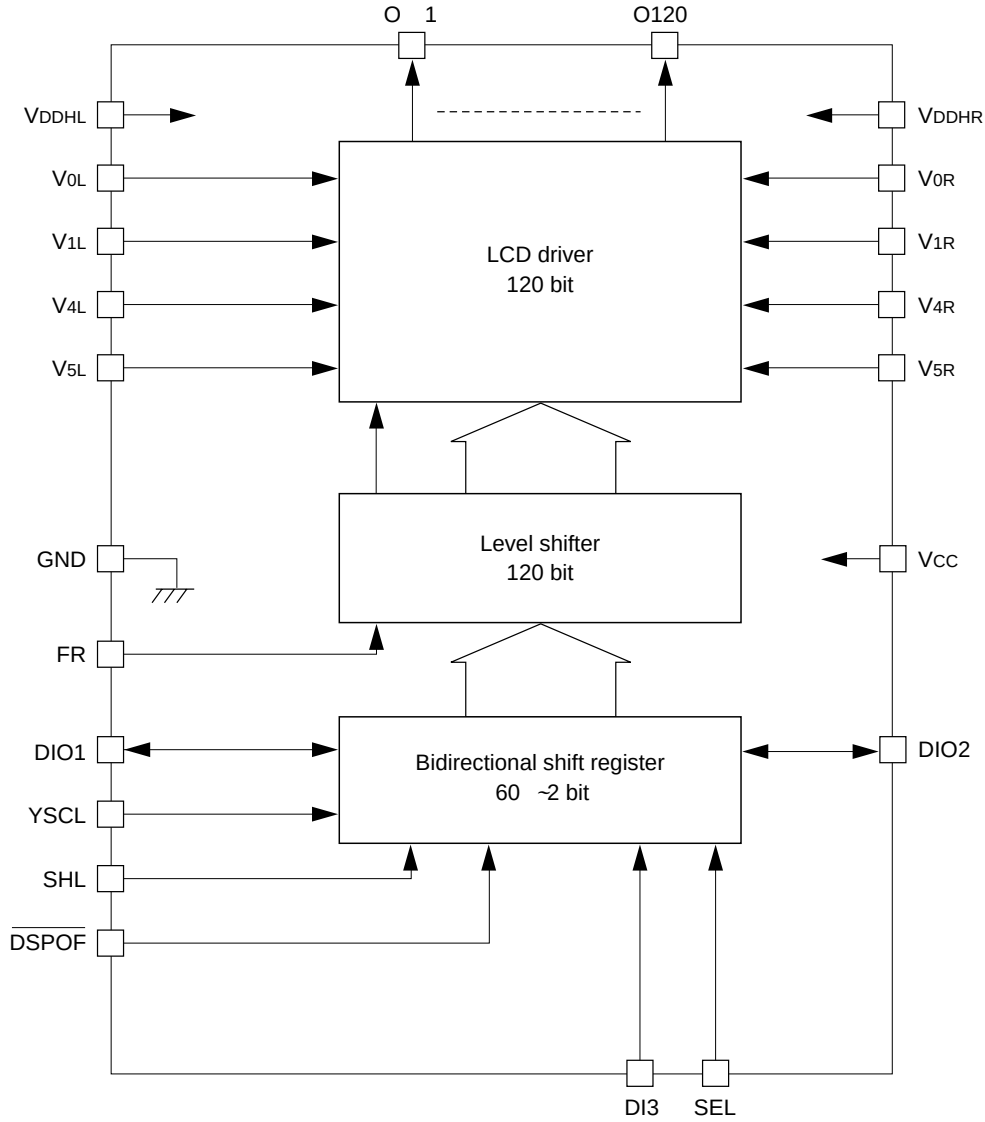
Contents

The SED1753 is a 120-output low output resistance-common (low) driver most suited to drive the extra large-capacity dot matrix liquid crystal panel. It is used paired with the SED1752 and DES1758. It ensures high-resolution thanks to the wide LCD drive voltage range.
This driver can be employed in a wide range of applications for the long type chip layout suited for smaller LCD panels. It promises the highest driver efficiency for panels with 1/240, 1/300 and 1/480 duty thanks to bidirectional driver output sequences, higher tension resistance than current models and 60 × 2 pairs of low output impedance LCD output.

FEATURES

- 120 LCD drive outputs (60 × 2 structure)
- Common output ON resistance: 0.3KΩ (Typ.)
- Applicable for high duty : 1/480 (Reference)
- Pin selectable output shift direction
- Non-bias display off function
- Long-sideways chip
- LCD power offset bias adjustable corresponding to V_{DDH} and GND levels
- Wide LCD drive voltage range: 8V to 42V
- Logic system power supply: 2.7 to 5.5V
- Package: TCP
- This IC is not designed for radiation protection

BLOCK DIAGRAM



BLOCK FUNCTIONS

Shift register

Bidirectional shift register for common data transfer. It has 60 × 2 bit structure, and allows selection between 60 × 2 bit and 120 bit depending on state of SEL.
When 60 × 2 bit structure is selected, input to the succeeding 60 bit shift register is DI3.

Level shifter

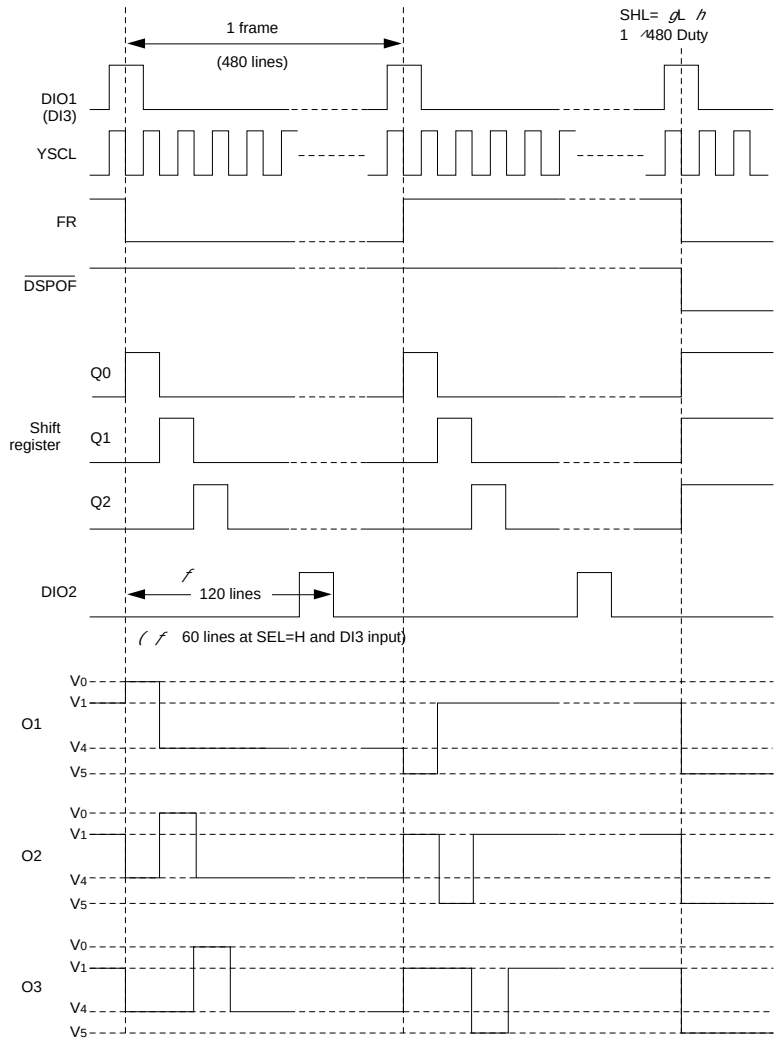
Voltage level interface circuit for converting voltage level of a signal from logic system level to LCD drive level.

LCD driver

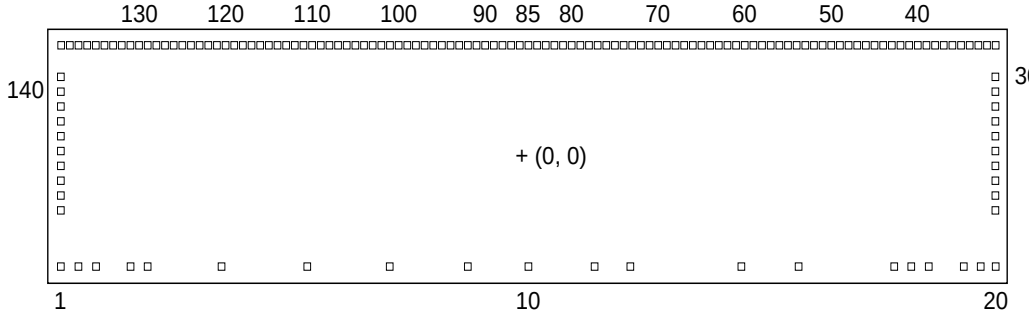
Outputs LCD drive voltage. The following table shows the relation between display blanking signal $\overline{DSPOF}$, shift register contents, frame signal FR and common output voltage.

$\overline{DSPOF}$	Shift register contents	FR	On output voltage	
H	H	H	V_5	On level
		L	V_0	
	L	H	V_1	Off level
		L	V_4	
L	—	—	V_5	—

Timing diagram



BUMP LAYOUT



Chip size	9.41 mm × 2.23 mm
Pad pitch	83.6 µm
Chip thickness	625 µm × 25 µm

1) Au bump specification (SED1753D0B) (For reference)
Au vertical bump

	Scribe horizonal	×	Scribe vertical	±	tolerance	
Bump size A	75.1 µm	×	79.8 µm	±	4 µm	(Pad No. 1 to 22, 147, 148)
Bump size B	74.1 µm	×	74.1 µm	±	4 µm	(Pad No. 23 to 30, 139 to 146)
Bump size C	65.6 µm	×	80.8 µm	±	4 µm	(Pad No. 31 to 35, 134 to 138)
Bump size D	54.2 µm	×	80.8 µm	±	4 µm	(Pad No. 36 to 84, 86 to 133)
Bump size E	98.8 µm	×	80.8 µm	±	4 µm	(Pad No. 85)
Bump thickness	17 to 28 µm					

BUMP CENTER COORDINATE

PAD No.	PIN Name	X	Y
1	Dummy	-4536	-940
2	V1L	-4393	-940
3	V4L	-4236	-909
4	V5L	-3899	-940
5	Dummy	-3748	-940
6	GND	-2992	-957
7	DI01	-2144	-952
8	FR	-1349	-952
9	$\overline{\text{DSP0F}}$	-573	-952
10	SHL	-13	-952
11	SEL	652	-952
12	DI3	1010	-952
13	YSCL	2077	-952
14	DI02	2636	-952
15	VCC	3560	-952
16	Dummy	3729	-952
17	V5R	3899	-952
18	V4R	4236	-909
19	V1R	4392	-940
20	*1	4535	-940
21	V0R	4524	-477
22	VDDHR	4524	-324
23	Dummy	4542	-175
24	O120	4542	-52
25	O119	4542	72
26	O118	4542	195
27	O117	4542	319
28	O116	4542	442
29	O115	4542	566
30	O114	4542	689
31	*2	4546	959
32	O113	4451	959
33	O112	4356	959
34	O111	4261	959
35	O110	4166	959
36	O109	4077	959
37	O108	3993	959
38	O107	3910	959
39	O106	3826	959
40	O105	3743	959
41	O104	3659	959
42	O103	3575	959
43	O102	3492	959
44	O101	3408	959
45	O100	3325	959
46	O99	3241	959
47	O98	3157	959
48	O97	3074	959
49	O96	2990	959
50	O95	2907	959
51	O94	2823	959
52	O93	2739	959
53	O92	2656	959
54	O91	2572	959
55	O90	2489	959
56	O89	2405	959
57	O88	2321	959
58	O87	2238	959
59	O86	2154	959
60	O85	2071	959
61	O84	1987	959
62	O83	1903	959

PAD No.	PIN Name	X	Y
63	O82	1820	959
64	O81	1736	959
65	O80	1653	959
66	O79	1569	959
67	O78	1485	959
68	O77	1402	959
69	O76	1318	959
70	O75	1235	959
71	O74	1151	959
72	O73	1067	959
73	O72	984	959
74	O71	900	959
75	O70	817	959
76	O69	733	959
77	O68	649	959
78	O67	566	959
79	O66	482	959
80	O65	399	959
81	O64	315	959
82	O63	231	959
83	O62	148	959
84	O61	64	959
85	O60	–42	959
86	O59	–148	959
87	O58	–231	959
88	O57	–315	959
89	O56	–399	959
90	O55	–482	959
91	O54	–566	959
92	O53	–649	959
93	O52	–733	959
94	O51	–817	959
95	O50	–900	959
96	O49	–984	959
97	O48	–1067	959
98	O47	–1151	959
99	O46	–1235	959
100	O45	–1318	959
101	O44	–1402	959
102	O43	–1485	959
103	O42	–1569	959
104	O41	–1653	959
105	O40	–1736	959
106	O39	–1820	959
107	O38	–1903	959
108	O37	–1987	959
109	O36	–2071	959
110	O35	–2154	959
111	O34	–2238	959
112	O33	–2321	959
113	O32	–2405	959
114	O31	–2489	959
115	O30	–2572	959
116	O29	–2656	959
117	O28	–2739	959
118	O27	–2823	959
119	O26	–2907	959
120	O25	–2990	959
121	O24	–3074	959
122	O23	–3157	959
123	O22	–3241	959
124	O21	–3325	959

PAD No.	PIN Name	X	Y
125	O20	–3408	959
126	O19	–3492	959
127	O18	–3575	959
128	O17	–3659	959
129	O16	–3743	959
130	O15	–3826	959
131	O14	–3910	959
132	O13	–3993	959
133	O12	–4077	959
134	O11	–4166	959
135	O10	–4261	959
136	O9	–4356	959
137	O8	–4451	959
138	*2	–4546	959
139	O7	–4542	689
140	O6	–4542	566
141	O5	–4542	442
142	O4	–4542	319
143	O3	–4542	195
144	O2	–4542	72
145	O1	–4542	–52
146	Dummy	–4542	–175
147	VDDHL	–4545	–324
148	V0L	–4545	–477

*1: Do not connect with other terminals as the setting is GND level.
*2: Do not connect with other terminals as the setting is VDDH level.

PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Numbers of pins</th></tr>
<tr><td>O1 to O120</td><td>O</td><td>LCD drive common (low) output.
The output changes at the YSCL falling edge.</td><td>120</td></tr>
<tr><td>DIO1, DIO2</td><td>I/O</td><td>60 × 2 bit bidirectional shift register scan pulse.
The pin is set to input or output depending on the SHL input.
The output changes at the YSCL falling edge.</td><td>2</td></tr>
<tr><td>DI3</td><td>I</td><td>Scan pulse input pin for 60 × 2 bit structure.
DI3 is connected to GND when SEL is at low-level.</td><td>1</td></tr>
<tr><td>SEL</td><td>I</td><td>Selective input of the bidirectional shift register operation modes.
H: 60 × 2 (DI3 input). L: 120.</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input.
It shifts scan data at the falling edge.</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and DIO pin I/O control signal input.
<table>
<tr><th>SHL</th><th>O output shift direction</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td>H</td><td>1 ⟶ 60 61 ⟶ 120</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>120 ⟶ 61 60 ⟶ 1</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{\text{DSPOF}}$</td><td>I</td><td>Liquid crystal display blanking control signal input.
Entering “L” causes all common outputs to go V_5 level.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD drive output frame signal input.</td><td>1</td></tr>
<tr><td>GND, V_{CC}</td><td>Power</td><td>Logic operation power.
GND: 0V V_{CC}: +2.7V to 5.5V</td><td>2</td></tr>
<tr><td>V_{0L}, V_{1L}, V_{4L}
V_{5L}, V_{DDH}
V_{0R}, V_{1R}, V_{4R}
V_{5R}, V_{DDHR}</td><td>Power</td><td>LCD drive power.*1
GND: 0V V_{DDH}: 8V to 42V
$V_{DDH} \geq V_0 \geq V_1 \geq 8/9V_{DDH}$
$1/9V_{DDH} \geq V_4 \geq V_5 \geq$ GND</td><td>10</td></tr>
<tr><td></td><td></td><td>Total</td><td>140</td></tr>
</table>

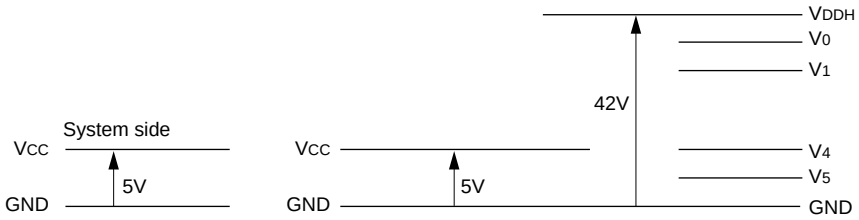
*1: Each pair of V_{DDH} and V_0 to V_5 must be connected to the LCD drive power supply. The above LCD drive power voltage range indicates the recommended value.

ABSOLUTE MAXIMUM RATING

Items	Codes	Ratings	Units
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage (2)	V_{DDH}	–0.3 to +45.0	V
Supply voltage (3)	V_0, V_1, V_4, V_5	GND – 0.3 to V_{DDH} + 0.3	V
Input voltage	V_I	GND – 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	GND – 0.3 to V_{CC} + 0.3	V
DIO output current	I_0	20	mA
Operating temperature	Topr	–40 to +85	°C
Chip storage temperature	Tstg1	–65 to +150	°C
TCP product storage temperature	Tstg2	–55 to +125	°C

Note 1: ALL stated voltages assume GND = 0V.

Note 2: V_0, V_1, V_4 and V_5 voltages shall always satisfy the condition of $V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq GND$.



Note 3: Do not allow the logic power goes floating state or drop below V_{CC} = 2.6V while applying the LCD drive power. Otherwise, the LSI could be permanently damaged. Special care is needed for the system power on or off sequences.

ELECTRIC CHARACTERISTICS

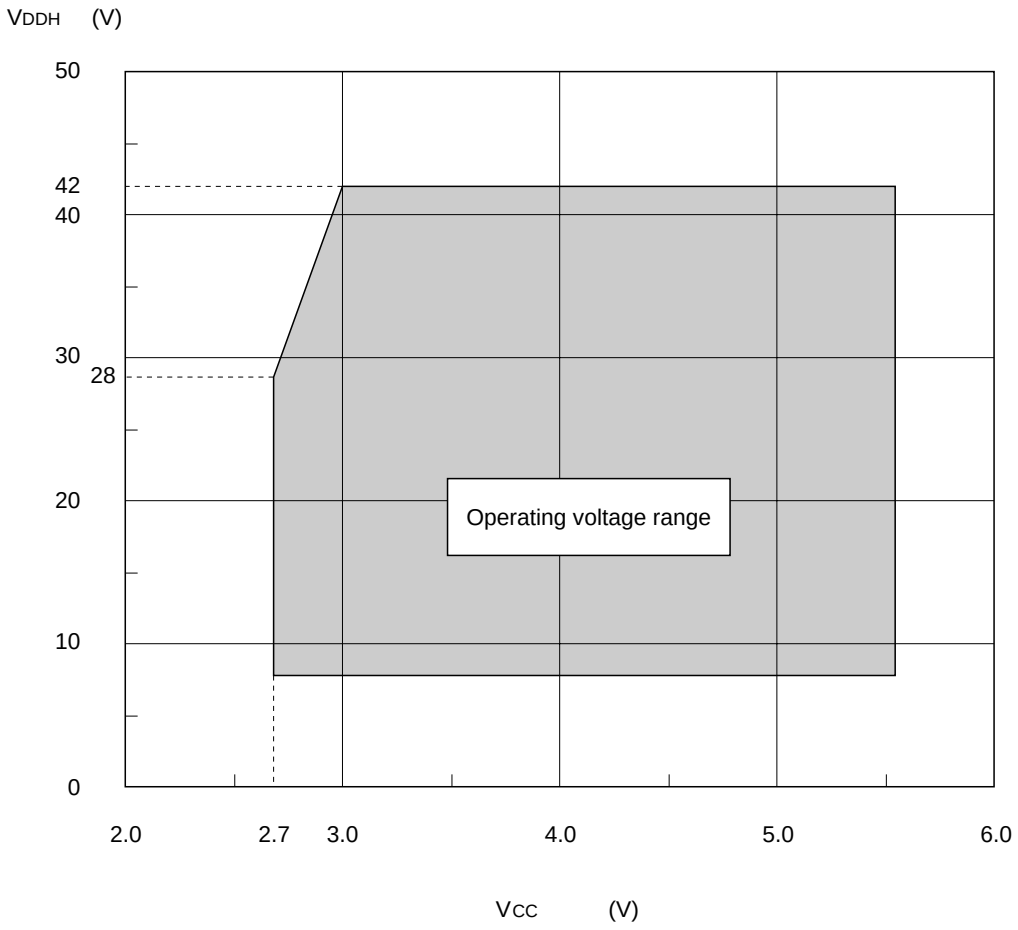
DC Characteristics

Except where otherwise specified,
GND = V_5 = 0V, V_{CC} = 5.0V±10%, Ta = –40 to 85°C are assumed.

Items	Codes	Conditions		Applicable pins	Min.	Typ.	Max.	Units
Supply voltage (1)	V_{CC}	—		V_{CC}	2.7	5.0	5.5	V
Recommended operating voltage	V_{DDH}	V_{CC} = 2.7 to 5.5V		V_{DDHL}, V_{DDHL} V_{0L}, V_{0R}	14.0	—	40.0	V
Operatable voltage	V_{DDH}	Function			8.0	—	42.0	V
Supply voltage (2)	V_1	Recommended value		V_{1L}, V_{1R}	8/9•V_{DDH}	—	V_{DDH}	V
Supply voltage (3)	V_4	Recommended value		V_{4L}, V_{4R}	GND	—	1/9•V_{DDH}	V
High-level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5V		DIO1, DIO2, FR, YSCL,	0.8•V_{CC}	—	—	V
Low-level input voltage	V_{IL}			SHL, DI3 $\overline{\text{DSPOF}}$, SEL	—	—	0.2•V_{CC}	V
High-level output voltage	V_{OH}	V_{CC} = 2.7 to 5.5V	I_{OH} = –0.3mA	DIO1, DIO2	V_{CC} – 0.4	—	—	V
Low-level output voltage	V_{OL}		I_{OL} = 0.3mA		—	—	GND + 0.4	V
Input leak current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		YSCL, SHL, DI3, $\overline{\text{DSPOF}}$, FR, SEL	—	—	2.0	µA
I/O current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2	—	—	5.0	µA
Rest current	I_{GND}	V_{DDH} = 14.0 to 42.0V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V Ta = 25°C	V_{DDH} = +36.0V, 1/24	O1 to O120	—	0.29	0.48	KΩ
			V_{DDH} = +26.0V, 1/20		—	0.3	0.5	
In-chip deviation	ΔR_{COM}	V_{DDH} = +36.0V, 1/24 bias			—	—	50	Ω
Mean operating current (1)	I_{CC}	V_{CC} = +5.0V, V_{IH} = V_{CC} V_{IL} = GND, f_{YSCL} = 33.6KHz f_{FR} = 70Hz, input data: 1/480 Ta = 25°C, no load		V_{CC}	—	13	26	µA
		V_{CC} = 3.0V Other conditions are the same as when V_{CC} = 5.0V.			—	8	18	
Mean operating current (2)	I_{DDH}	V_{DDH} = V_0 = 30.0V, V_1 = 28.0V V_4 = 2.0V, V_5 = 0.0V, V_{CC} = 5.0V Other conditions are the same as those in the Icc column.		V_{DDHL} V_{DDHR}	—	8	20	µA
Input terminal capacity	C_I	Freq. = 1MHz Ta = 25°C Independent chips		YSCL, SHL, $\overline{\text{DSPOF}}$, FR, DI3, SEL	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			DIO1, DIO2	—	—	15	pF

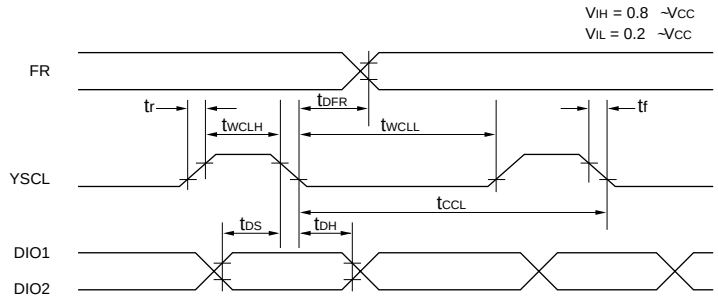
Operating voltage range V_{CC}–V_{DDH}

The V_{DDH} voltage must be selected within the following V_{CC} and V_{DDH} operating voltage range.



AC Characteristics

Input timing characteristics



(VCC = +5.0V ±10%, Ta = –40 to +85°C)

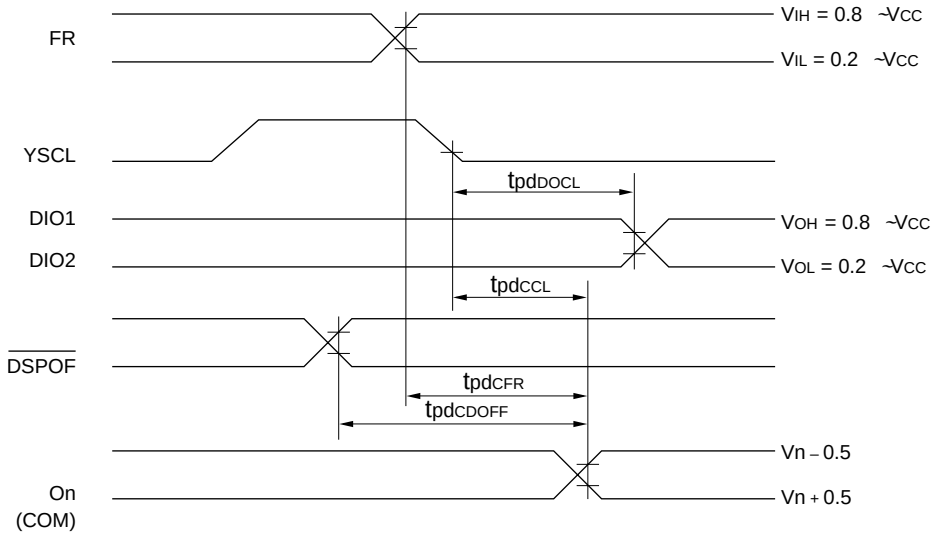
Items	Codes	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	400	—	ns
YSCL high-level pulse width	t_{WCLH}	—	60	—	ns
YSCL low-level pulse width	t_{WCLL}	—	330	—	ns
Data setup time	t_{DS}	—	50	—	ns
Data hold time	t_{DH}	—	40	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

(VCC = 2.7V to 4.5V, Ta = –40 to +85°C)

Items	Codes	Conditions	Min.	Max.	Units
YSCL cycle	t_{CCL}	—	800	—	ns
YSCL high-level pulse width	t_{WCLH}	—	80	—	ns
YSCL low-level pulse width	t_{WCLL}	—	660	—	ns
Data setup time	t_{DS}	—	90	—	ns
Data hold time	t_{DH}	—	70	—	ns
Input signal rise time	t_r	—	—	50	ns
Input signal fall time	t_f	—	—	50	ns

*1: t_{DFR}: FR signal transition point and LP signal falling timing must be basically selected within the range in which normal On output waveform is produced at 0ns.

Output timing characteristics



(VCC = 5.0V ±10%, VDDH = 14.0 to 42.0V, Ta = –40 to +85°C)

Items	Symbols	Conditions	Min.	Max.	Units
YSCL falling edge → DIO delay time	t_{pdDOCL}	CL = 15pF	—	100	ns
YSCL falling edge → On output delay time	t_{pdCCL}	CL = 100pF	—	200	ns
$\overline{DSPOF}$ → On output delay time	$t_{pdCDOFF}$				
FR → On output delay time	t_{pdCFR}		—	300	ns

(VCC = 2.7V to 4.5V, VDDH = 14.0 to 28.0V, Ta = –40 to +85°C)

Items	Symbols	Conditions	Min.	Max.	Units
YSCL falling edge → DIO delay time	t_{pdDOCL}	CL = 15pF	—	200	ns
YSCL falling edge → On output delay time	t_{pdCCL}	CL = 100pF	—	400	ns
$\overline{DSPOF}$ → On output delay time	$t_{pdCDOFF}$				
FR → On output delay time	t_{pdCFR}		—	600	ns

LCD DRIVE POWER SUPPLY

Setting up respective voltage levels

When setting up respective voltage levels for LCD drive, it is the best way to resistively divide the potential between V_{DDH}–GND to drive the LCD by means of voltage follower using an operation amplifier.

In consideration of the case of using an operation amplifier, the LCD driving minimum potential V_0 and V_{DDH} are separated and independent terminals are used. Likewise, the LCD driving minimum potential V_5 and GND are separated and independent terminals are used.

Normally, V_0–V_{DDH} and V_5–GND are connected respectively, and V_1 and V_4 are driven by means of voltage follower. When driving V_0 by means of voltage follower, the potential difference between V_{DDH}–V_0 must be kept at 0V to 2.5V since efficacy of the LCD driving output driver deteriorates if V_0 potential goes beyond V_{DDH}.

When resistance exists in series in the power supply lines of GND and V_{DDH}, I_{DDH} at signal change causes voltage drop at GND and V_{DDH} of the supply terminals of the LSI disabling them to maintain current relations with the LCD intermediate potentials of ($V_{DDH} \geq V_0 \geq V_1 \geq V_4 \geq V_5 \geq$ GND), thus leading to breakdown or destruction of the LSI.

When using a protective resistor, do not fail to stabilize the voltage using appropriate capacitance.

On stabilizing the voltage

For preventing an adverse effect due to noise introduced by the supply signal lines on the mounting board, it is recommended to insert bias capacitors, as needed, between power supplies (GND–V_{CC} and GND–V_{DDH}) to stabilize voltage.

Precautions for turning power on or off

Since the LCD drive voltage of these LSIs is high, it can be permanently damaged by excess current if high voltage is applied to the LCD drive circuit with the logic operation power being made floating or the Vccs lowered to 2.6V or less, or when LCD drive signals are output before applied voltage to the LCD drive circuit is stabilized. It is, therefore, suggested to maintain potential of the LCD drive output to V_5 level until the LCD drive circuit voltage is stabilized, using the display off function ($\overline{DSPOF}$).

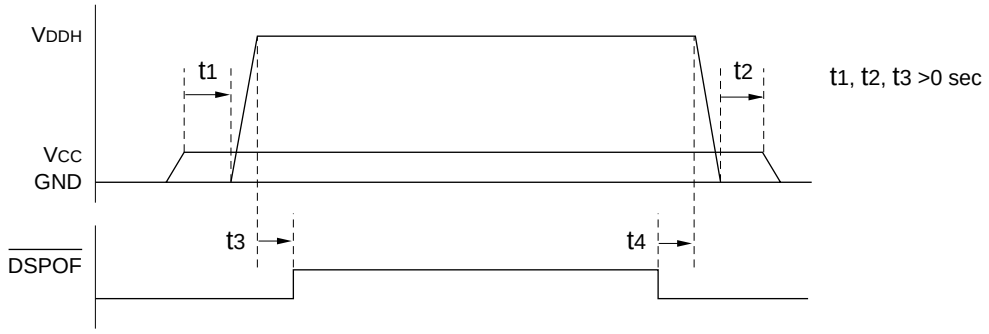
Maintain the following sequences when turning power on or off.

When turning power on:

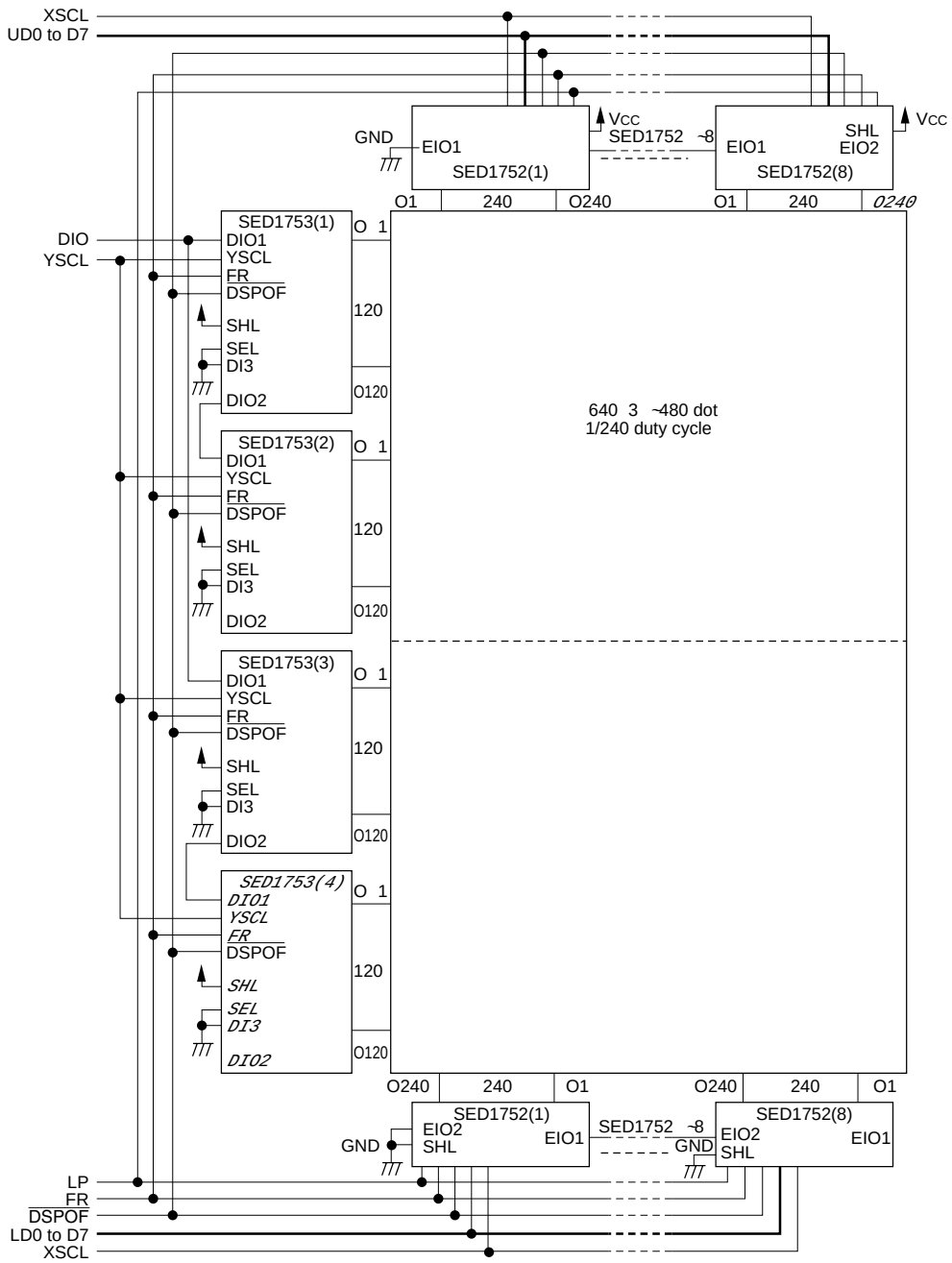
Turn on the logic operation power →
turn on the LCD drive power or turn them on simultaneously.

When turning power off:

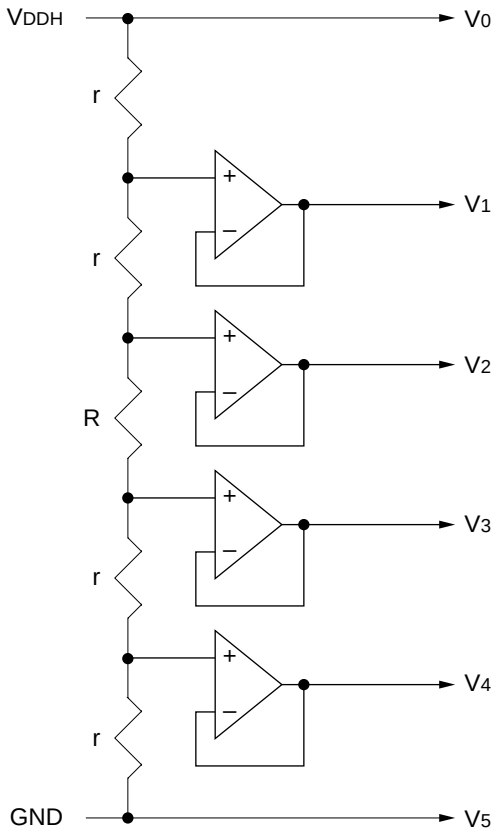
Turn off the LCD drive power →
turn off the logic operation power or turn them off simultaneously.



SAMPLE CIRCUIT



Sample LCD Power Supply Circuit

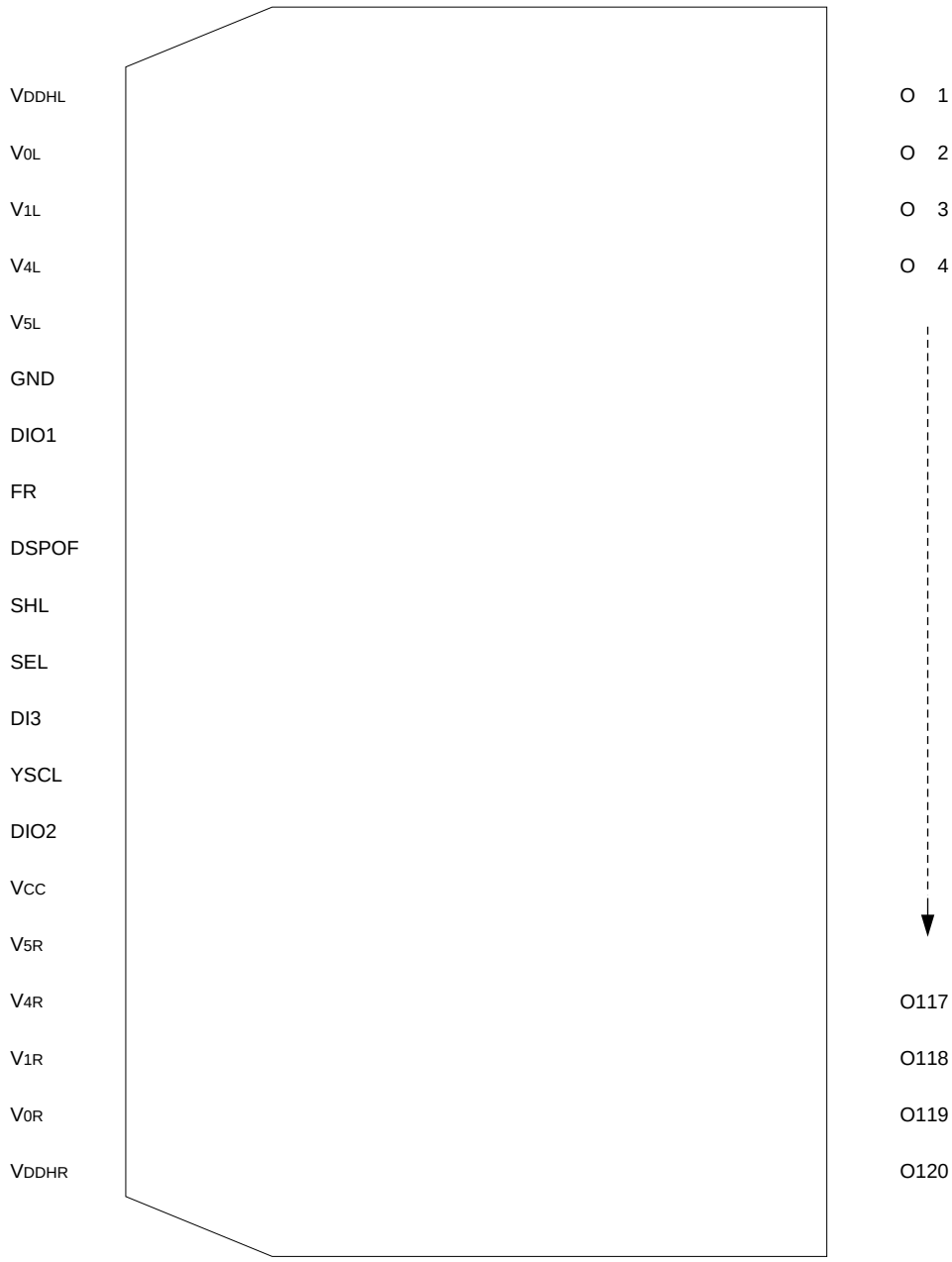


- Smoothing capacitance must be added to the LCD drive power supplies (V_0–V_5) at an appropriate location on the LCD module.
- V_0, V_1, V_4 and V_5 supply power to the SED1753 V_0, V_2, V_3 and V_5 supply power to the SED1752.
- Supplies logic operation voltage to respective ICs.
- For suppressing noise, bias capacitor must be added to an appropriate location between GND–V_{CC} and GND–V_{DDH} to stabilize the supply voltage.
  The high tension resistant supply (GNDR and GNDL) line must be be separated from the logic operation supply (GND) line.

TCP

A Sample SED1753T**TCP Pin Layout

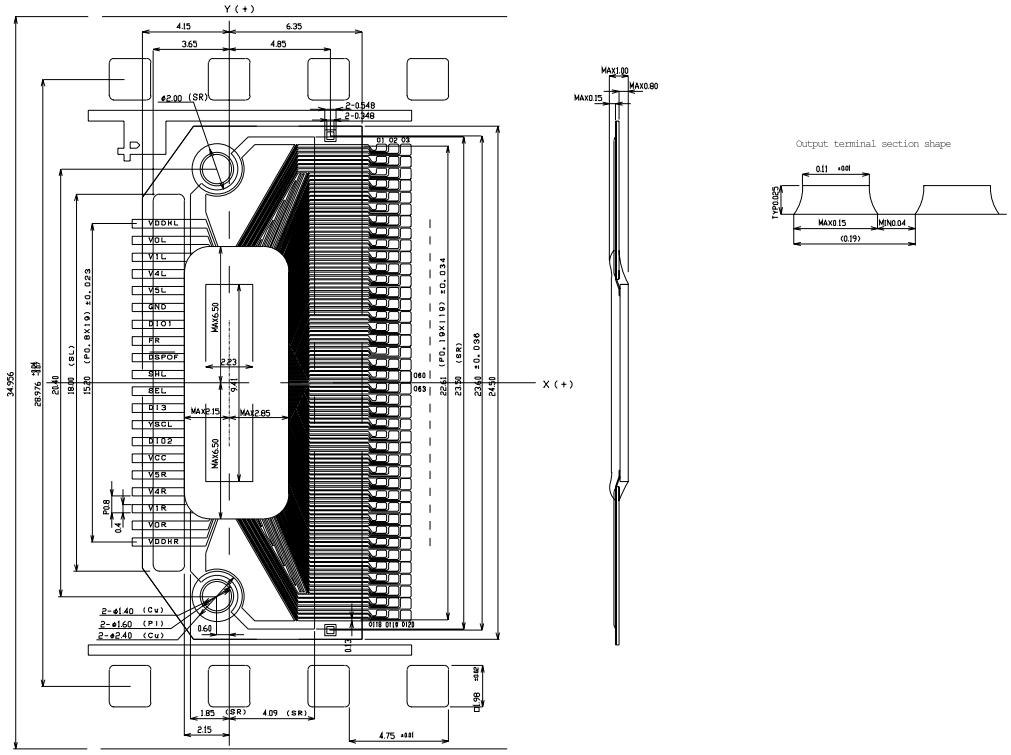
Note: This drawing is not meant to determine contour of the TCP.



DIMENSIONAL OUTLINE DRAWING

SED1753T0A

For reference



Unit: mm