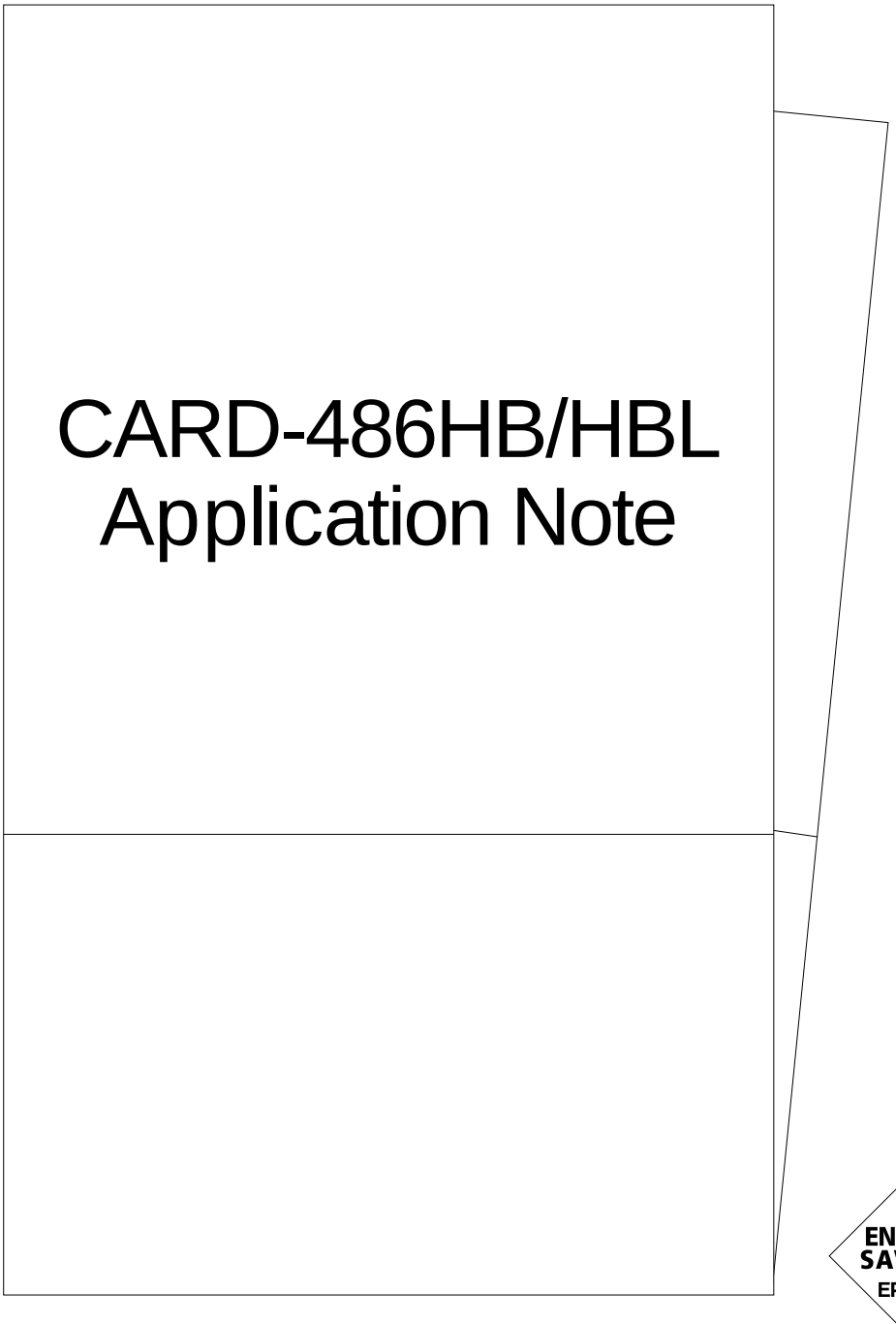
MF1065-01

EPSON

CARD-486HB/HBL Application Note



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NOTICE

1. EASI Specifications

The credit-card size, PC boards having the 236-pin connectors are called “card size PCs.” The Embedded All-in-one System Interface (EASI) standard defines the pin assignment and pin names of the interface connector (236 pins) of card size PCs for their compatibility between the supporting companies (called the EASI group companies). The Epson’s SCE86436 Series card size PCs (called the “CARD-486HB”) satisfy the EASI standard.

The EASI standard groups define 236pins into functional several blocks. Therefore, the customer can easily redesign their products even when replacing several types of card size PCs. If some functions are incompatible between card size PCs due to the chip sets used for those PCs, their blocks are defined by the EASI standard. The customer needs to study the specifications of each card size PC when using a combination of the CARD-486HB and another card size PC. For the terminal block specifications, the customer needs to design a flexible wiring to allow easy change of wirings between connector pins and devices.

Table 1-1 defines the relationship between EASI pin block categories and pin numbers.

Table 1-1 EASI Pin Blocks

Pin block	No. of pins	Pin No.	
Power supply	28	#1, #2 #27 to 30 #59, #60 #82 to 85 #117, #118	#119, #120 #145 to 148 #177, #178 #200 to 203 #235, #236
LCD interface	28	#3 to 14 #19, #20	#121 to 132 #137, #138
CRT interface	8	#15 to 18	#133 to 136
Mouse interface	2	#21	#139
Keyboard interface	2	#22	#140
FDD interface	18	#23 to 26 #31 to 35	#141 to 144 #149 to 153
Serial interface	18	#36 to 44	#154 to 162
Parallel interface	18	#45 to 53	#163 to 171
IDE interface	6	#54 to 56	#172 to 174
Poewr management	12	#57, #58 #61, #62 #115, #116	#175, #176 #179, #180 #233, #234
Speaker interface	2	#63	#181
ROM update interface	6	#64 to 66	#182 to 184
ISA bus	88	#67 to 81 #86 to 114	#185 to 199 #204 to 232

*1 The sync and data signals may vary depending on a combination of LCD panel and card size PC.
*2 Pin #152 (FDMSEL) is not supported.
*3 The assignment of pins 153 (DARX), pin 44 (IRRX) and 162 (IRTX) may differ.
*4 The assignment of pin 171 (LPTDIR) may differ.
*5 The assignment of pins other than pin 57 (SUSSTAT#), pin 58 (BATLOW#), pin 62 (POWERGOOD), pin 175 (VBR) and pin 176 (EXTSMI#) may differ.
*6 The assignment of pin 181 (WDTIM) may differ.
*7 The pin assignment may differ for some card size PCs. The interface is compatible between Seiko Epson's card size PCs (called the "CARD-PC" in this manual).

2. Video Interface

The CARD-486HB contains an IBM PC/AT-compatible video controller, Seiko Epson's SPC8110 which can drive the CRT or LCD display device or both of them simultaneously. These drive modes are called the "CRT display," "LCD display" and "simultaneous display." The video signal outputs are switched by the CARD-486HB BIOS. The basic difference between CRT and LCD interfaces are their outputs; the CRT interface outputs is analog signals but the LCD interface outputs is digital (TTL) signals.

As the different video controller is used for each CARD-PC, an additional circuit may be required if the system card is replaced for applications. For the detailed information, refer to the related CARD-PC hardware manuals.

Note : This interface is not supported by the CARD-486HBL.

2.1 CRT Interface

The CARD-486HB can be attached to the CRT interface port by simple connection of eight signal lines as shown.

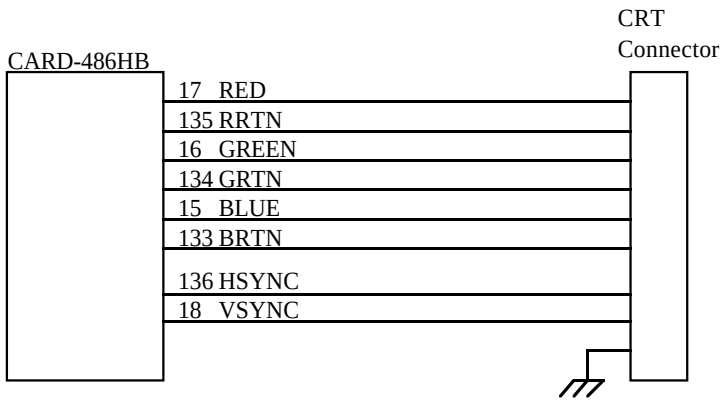


Figure 2-1 CRT Interface

The CARD-486HB contains a CRT display detector circuit which can automatically determine the connection or disconnection of a CRT display and the connection of monochrome or color CRT display.

2.2 LCD Interface

Any of the following LCD panels can be attached to the CARD-486HB's LCD interface:

- QVGA-compatible (320x240) single-panel, STN monochrome LCD panel (having 4x1 bus configuration)
- VGA-compatible (640x480) single-panel, STN monochrome LCD panel (having 8x1 bus configuration)
- VGA-compatible (640x480) dual-panel, STN monochrome LCD panel (having 4x2 bus configuration)
- VGA-compatible (640x480) dual-panel, STN color LCD panel (having 8x2 bus configuration)
- SVGA-compatible (800x600) single-panel, STN monochrome LCD panel (having 4x1 bus configuration)
- SVGA-compatible (800x600) dual-panel, STN monochrome LCD panel (having 4x2 bus configuration)
- SVGA-compatible (800x600) dual-panel, STN color LCD panel (having 8x2 bus configuration)
- VGA-compatible (640x480), TFT color LCD panel (having 3x3, 4x3 and 6x3-bit color configuration)
- SVGA-compatible (800x600), TFT color LCD panel (having 6x3-bit color configuration)

Also, the CARD-486HB can control the LCD power supply when it is operating. The LCD power supply can be turned on and off by the signals from the CARD-486HB only if an external power on/off circuit is attached to the LCD display. Figure 2-2 shows the LCD panel power sequence, and Figure 2-3 gives a system connection example.

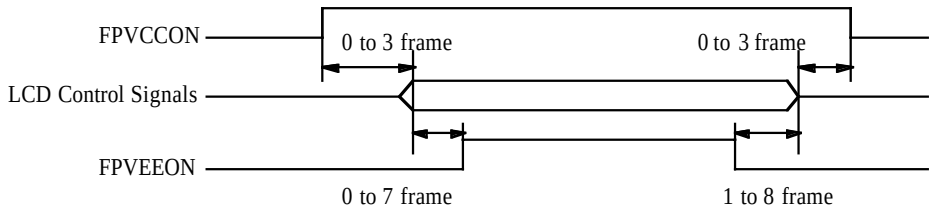


Figure 2-2 LCD Panel Power Sequence

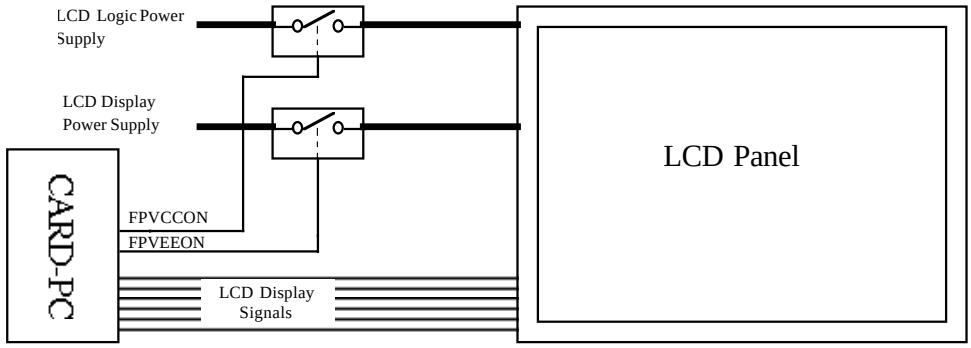


Figure 2-3 System Connection Example

The power sequence timing can be adjusted using a ROM adaptation kit (called the "RAK" in this manual). The following LCD panels are supported by the built-in controller of CARD-486HB. The color STN, single-scan LCD panel is not supported yet.

- Monochrome STN, single-scan LCD panel
  The 320x240-dot and 640x480-dot resolutions are supported. Both 4-bit and 8-bit data transmission rates are supported. LD0 to LD7 LCD data signals are used. Up to 64 tones can be displayed.

- Monochrome STN, dual-scan LCD panel
  The 640x480-dot and 800x600-dot resolutions are supported. Four-bit data transmission is supported. LD0 to LD7 LCD data signals are used. Up to 64 tones can be displayed.

- Color STN, dual-scan LCD panel
  The 640x480-dot and 800x600-dot resolutions are supported. Eight-bit data transmission is supported. LD0 to LD15 LCD data signals are used. Up to 256 colors can be displayed.

- Color TFT (3x3, 4x3 and 6x3-bit) LCD panel
  The 640x480-dot and 800x600-dot resolutions are supported. The 3x3-bit (512-color), 4x3-bit (4096-color) and 6x3-bit (262144-color) resolutions are supported. LD0 to LD17 LCD data signals are used. The TFT panel that uses DE signals for horizontal sync control is also supported. For horizontal sync control, the FPHTIM signal line is connected to the Hsync pin, and the FPBLANK signal line is connected to the DE pin. The TFT panel which controls the display start timing based on the horizontal sync signals and specific FPDOTCLK counts is not supported.

The video interface is set by the BIOS. For some panels, the BIOS needs to be modified by the RAK. For the typical LCD interfacing information, refer to the separate "CARD-PC Technical Information" bulletin. As it is updated periodically, consult to us for the latest issue. The control methods for different LCD types are described in Appendix 2 "Controls for Different LCD Types" of this manual.

The CARD-486HB has been set at the factory to the 640x480-dot, monochrome STN single-scan LCD having the Epson's EG9013 default data.

2.3 Simultaneous CRT and LCD Display

The LCD panel having the following specifications can drive both the LCR and CRT displays simultaneously. Otherwise, the simultaneous LCD and CRT display is not supported.

Table 2-1 LCD Display Frequencies

	Color VGA TFT	Mono STN Dual Scan	Mono STN Single Scan	Color STN dual
Clock frequency (MHz)	25.175	6.294	3.147	12.587
Frame frequency (Hz)	60	120	60	120

2.4 Setup of LCD Panel Parameters

The BIOS panel parameters can be set from the RAK. As the required parameters are provided by the BPM file(s), set them by the RAK. For each LCD connection information, refer to the separate "CARD-PC Technical Information" bulletin. As it is updated periodically, refer to our Home Page for the Internet or contact our sales person in charge for the latest issue.

3. Keyboard and Mouse Interface

As example of keyboard and mouse connection to the CARD-486HB is given in Figure 3-1. An external pull-up resistor is required for the CARD-486HB as the KBCLK, KBDATA, MSCLK and MSDATA are bi-directional signals with open drain outputs.

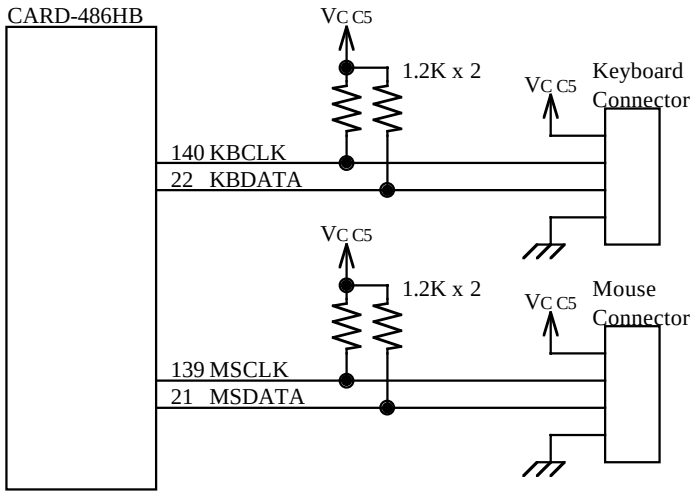
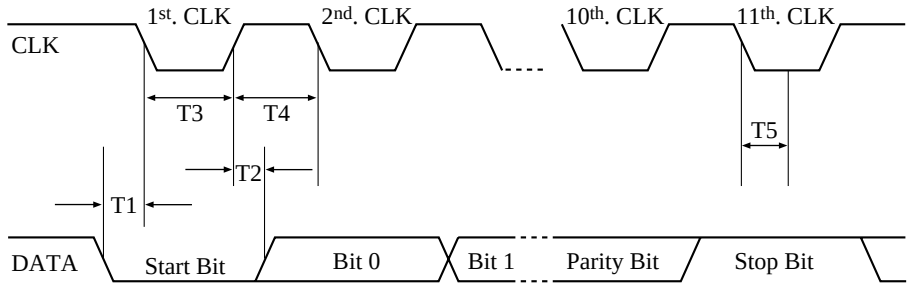


Figure 3-1 Keyboard and Mouse Interface

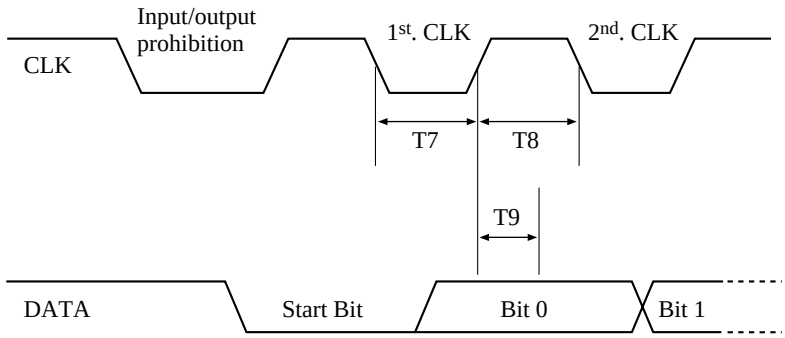
When any of your hardware is connected to the keyboard or the mouse interface of the CARD-486HB, it is necessary that the hardware satisfies the specification of the PS/2 Interface. For reference, the approximate specification of the PS/2 Interface is shown below. For the detailed AC timing of the CARD-486HB, refer to the CARD-486HB Hardware Manual.



Symbol	Parameter	Min.	Max.
T1	DATA-LOW setup time for CLK fall	5	25
T2	Time from CLK rise to DATA settlement	5	T4-5
T3	CLK low pulse width	30	50
T4	CLK high pulse width	30	50
T5	Delay time for 11th CLK fall when transmission is prohibited.	0	50

(Unit : µS)

Figure 3-2 AC Timing of PS/2 Interface for Reference (When signals are received)



Symbol	Parameter	Min.	Max.
T7	CLK low pulse width	30	50
T8	CLK high pulse width	30	50
T9	Device's data fetching time range for CLK rise	5	25

(Unit : µS)

Figure 3-3 AC Timing of PS/2 Interface for Reference (When signals are transmitted)

4. FDD Interface

The following floppy disk drives are supported by the CARD-486HB. Up to two drives (FDDs) can be attached to it.

Table 4-1 Supported FDDs

FDD	Transfer Rate	Rotation Speed	FD	Unformat	Format
5inch FDD	250Kbps	300rpm	2DS	500Kbyte	360Kbyte
5inch FDD	300Kbps	360rpm	2DS	500Kbyte	360Kbyte
	500Kbps	360rpm	2HD	1.6Mbyte	1.2Mbyte
3.5inch FDD	250Kbps	300rpm	2DD	1Mbyte	720Kbyte
	500Kbps	300rpm	2HD	2Mbyte	1.44Mbyte

Figure 4-1 gives an example of a dual-mode FDD connection to the CARD-486HB. An external pull-up resistor is required for the CARD-486HB as the FDWP#, FDRD#, FDINDEX#, FDDCHG# and FDTRK0# signals are output by the open collector of FDD. Although the other signals are also output by the open collector of CARD-486HB, special signal processing is not required as a pull-up resistor is usually contained in the FDD.

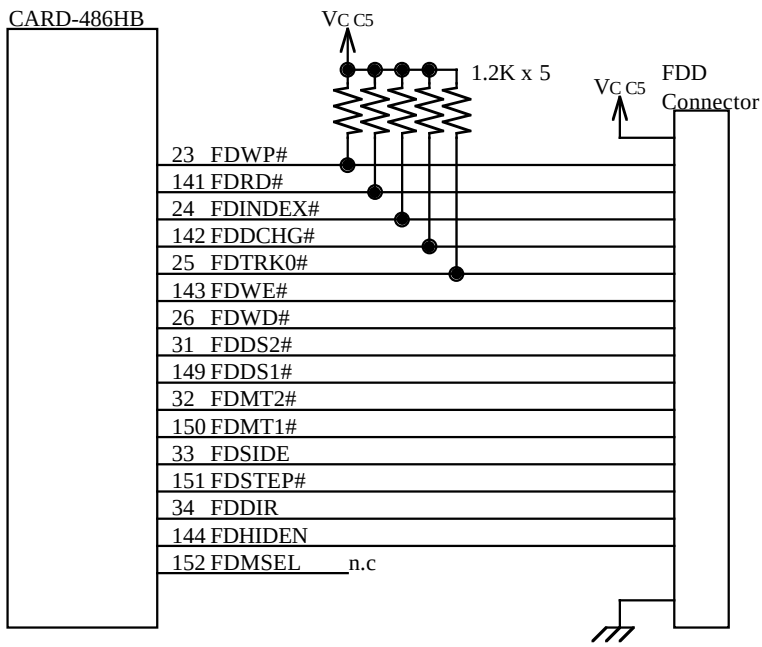


Figure 4-1 Dual-Mode FDD Interface

The functions of the 3-Mode FDD are not supported on the CARD-PC.
To support the 3-Mode FDD, it is necessary to connect a separate FDD controller to the ISA bus. Consult with us about the detail.
Note : This interface is not supported by the CARD-486HBL.

5. Serial Port Interface

5.1 RS-232C Interface

The serial controller of the CARD-486HB contains parts compatible with 16550, and 1.8432MHz has been input to the clock. So, the interface support transmissions from 50bps to 56,000bps (or transmissions up to 57,600bps are applicable with the error of 2.86%).
The CARD-486HB serial port interface can directly drive a TTL device. However, it requires a standard driver and receiver ICs for a long-distance transmission such as RS-232C interface communication. Figure 5-1 gives a circuit example where the NEC's μPD4724 RS-232C driver/receiver microprocessor chip is used. This IC converts the CARD-486HB's TTL level signals into RS-232C standard signals and vice versa. Also, if the CARD-486HB's SMOUTH0 or SMOUTH1 pin is connected to the μPD4724's STBY# pin, this IC can be standed by when the CARD-486HB's serial port is set to the Standby or Suspend mode. When the IC is desired to return from the standby mode by interrupting the serial port or to resume by the RI# signal, it is necessary that the Driver/Receiver IC is set to ON (STBY# = HIGH) at all times.

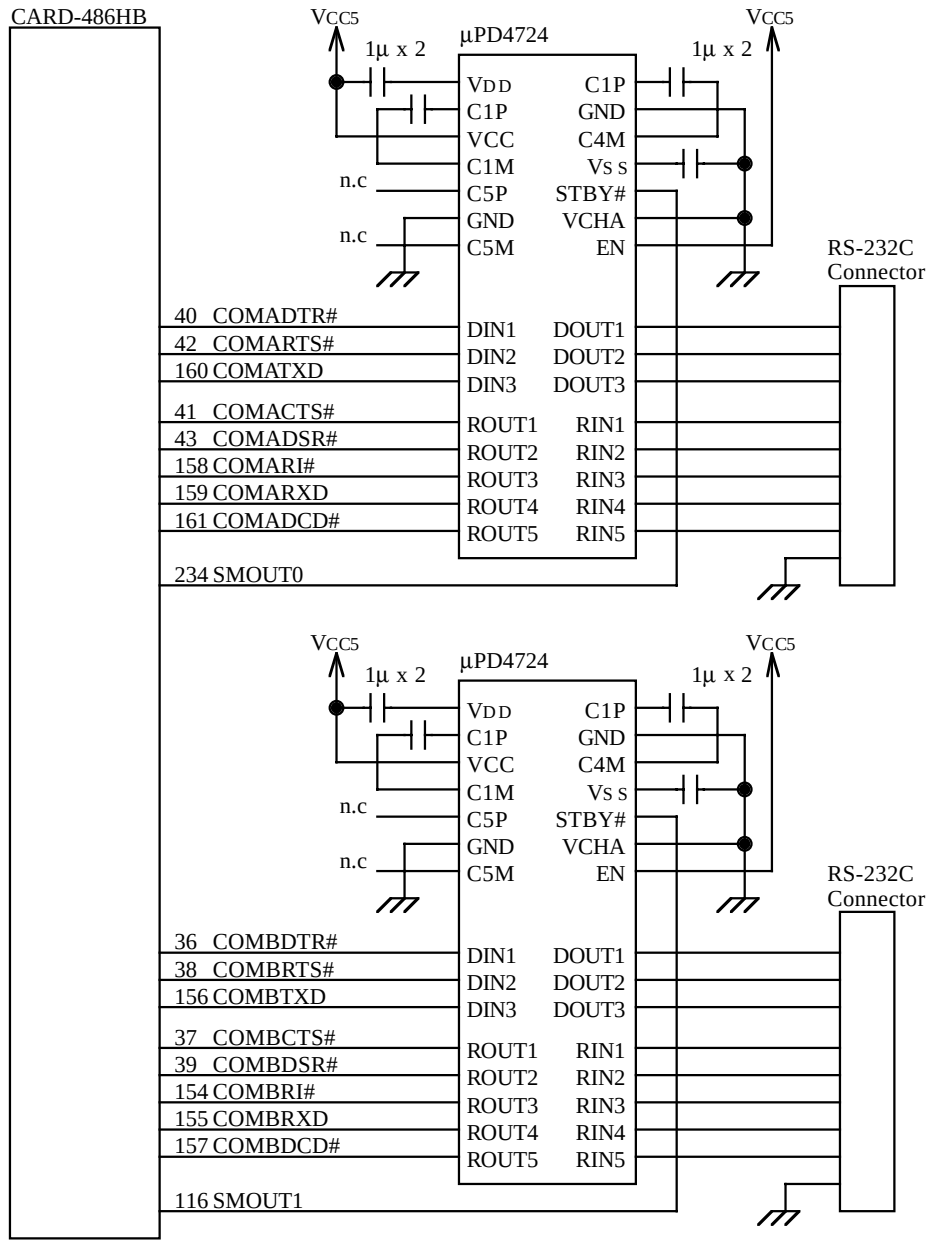


Figure 5-1 RS-232C Interface

5.2 Infrared Transmission

The CARD-486HB supports two types of infrared transmission: the IrDA 1.0 transmission and the ASK transmission. As the CARD-486HB's built-in serial controller is used for infrared transmission, the COMB's serial port cannot be used when the infrared transmission is selected. The IrDA, ASK, or COMB system is selected through CARD-486HB setup or by the RAK. An example of infrared transmission circuit that uses the TEMIC's TFDS3000 is given in Figure 5-2. The TFDS3000 optical module contains the light emission and reception elements for infrared transmission.

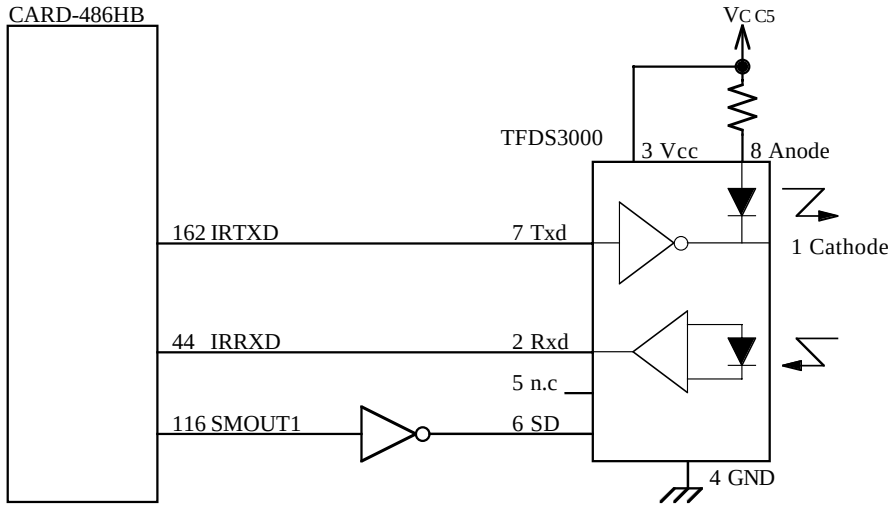


Figure 5-2 IrDA Interface

If the LED is connected to the IrDA optical module, the LED may be destroyed. Therefore, it must be protected by inserting a differentiating circuit or others in the optical module input. The CARD-486HB has the following IRTXD signal polarity.

1. Default (Reset)
   The IRTXD enters a three-state OFF status.

2. During transmission
   The IRTXD sends data when active high. The system must be designed to light the LED when the IRTXD is high.

The IRTXD can be designed to send data when active low. However, this requires the BIOS modification.

6. Parallel Port Interface

A circuit example of bidirectional parallel port is given in Figure 6-1. Although the data signals are buffered in this example, the CARD-486HB can be connected directly to the parallel port connector without the buffer.

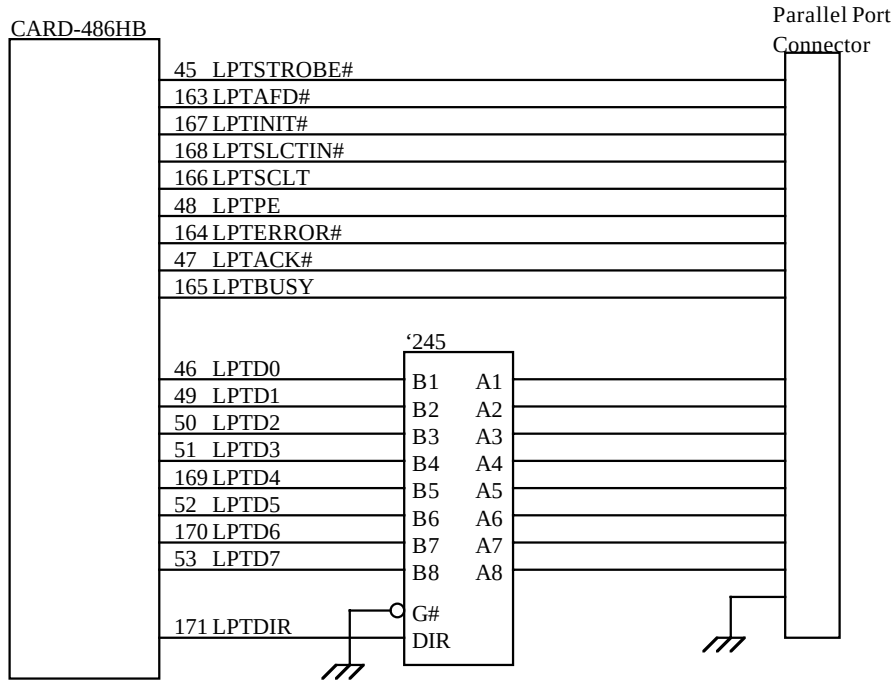


Figure 6-1 Parallel Port Interface

When adding a pull-up and pull-down resistors to the signals for static electricity protection or others, set the resistors in the same direction as the CARD-486HB's internal ones. (Use a pull-up resistor for the pulled up signals, and use the pull-down resistor for the pulled down signals.)

Table 6-1 Pull-up/Pull-down Resistors of Parallel Port

Signal name	Resistor
LPTSTROBE#	Pull-up resistor
LPTAFD#	Pull-up resistor
LPTINIT#	Pull-up resistor
LPTSLCTIN#	Pull-up resistor
LPTSLCT	Pull-down resistor
LPTPE	Pull-down resistor
LPTERROR	Pull-up resistor
LPTACK#	Pull-up resistor
LPTBUSY	Pull-up resistor
LPTD0..7	Pull-down resistor

As the parallel port input and output consist of CMOS devices, an input current problem may occur if no buffer is used.

Table 6-2 Input Current into Parallel Port

Problem	CARD-486HB's power supply	Device power supply
1. There is no problem.	ON	ON
2. Current may enter in the CARD-486HB's parallel port.	OFF	ON
3. Current may flow from the CARD-486HB to the device.	ON	OFF
4. There is no problem.	OFF	OFF

As defined on Table 6-2, a current flow occurs if either of CARD-486HB and device power supplies is turned OFF and if the other power supply is turned ON. This can cause a large current to flow in forward direction through the input protection diode or parasitic diode during input or output into/from CMOS devices. The CMOS devices may be latched up and, in the worst case, they may be destroyed. For example, if the power supply of a device (such as a printer) is turned ON and if the CARD-486HB is turned OFF and connected to it, the current enough to the device latch-up may flow immediately after the CARD-486HB's power supply is turned ON. Avoid to use the parallel port if problem 2 or 3 (defined on Table 6-2) can occur.

7. HDD Interface

7.1 HDD Interface of CARD-486HB

The CARD-486HB BIOS supports up to four large capacity HDDs (2 primary port and 2 secondary port). However, the hardware of the CARD-486HB supports the primary port only. When 3 or more HDD interfaces are necessary, a secondary port has to be installed outside. The standard specifications of the secondary port are as follows:

Table 7-1 Standard Specification of Secondary HDD Port

I/O Port

Address	Register Name
170h	Data Register
171h	Error Register
172h	Sector Count
173h	Sector Number
174h	Cylinder High
175h	Cylinder Low
176h	SDH Register
177h	Status Register
376h	SDH Register
377h	Status Register

Hardware Interrupt : IRQ15

Contact us directly for concrete circuit examples, etc.

7.2 Buffered HDD Interface

Data buses of the HDD interface (such as SA0 to SA2, IOW#, IOR# and IOCS16#) are also used for a device of another ISA bus. Therefore, the load of these signals may increase and the IDE HDD, other devices, and the CARD-486HB itself may operate abnormally. Also, when the CARD-486HB is connected to an IDE HDD using a signal cable, the signals may be affected by noise. Usually, a buffer must be entered between the CARD-486HB and the IDE HDD as shown in Figure 7-1.

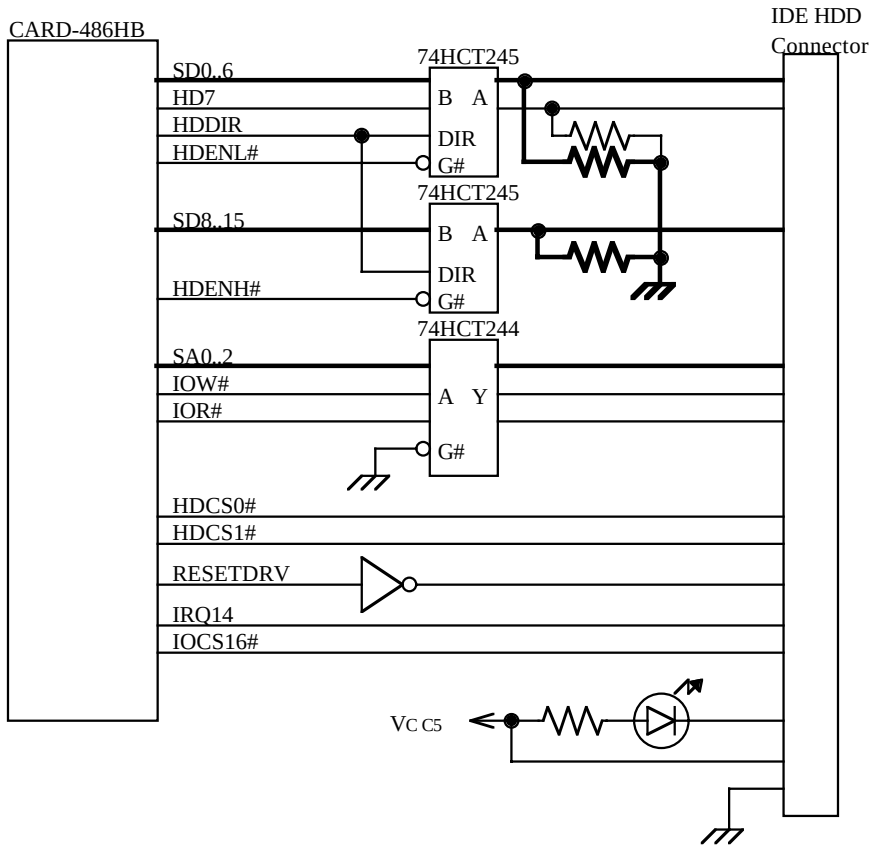


Figure 7-1 Buffered IDE HDD Interface

7.3 Direct HDD Interface

If the signal lines are not shared by another device and the cable noise affection is small, the CARD-486HB can be connected to the IDE HDD directly as the Chip Select and other signals required for the IDE HDD are generated by the CARD-486HB.

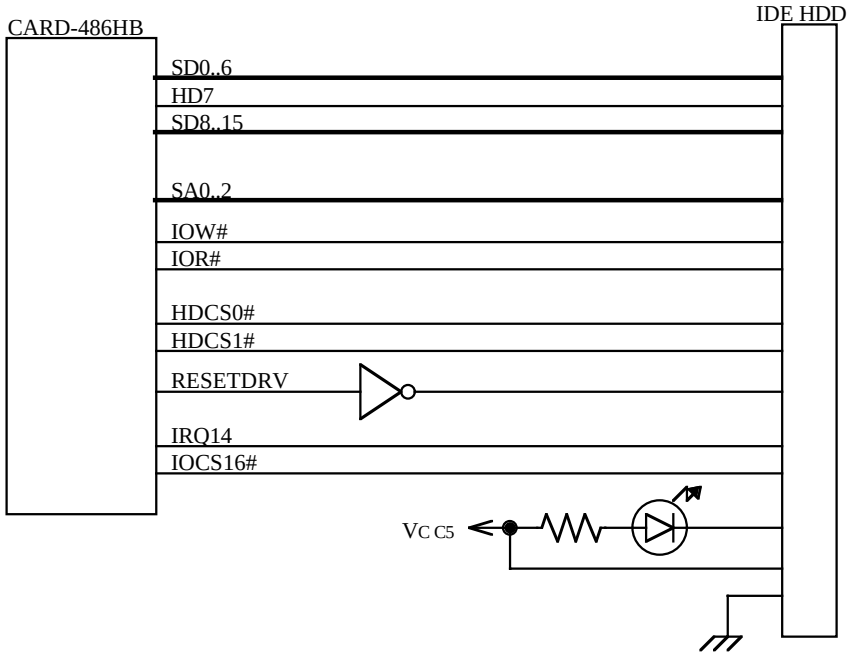


Figure 7-2 Direct IDE HDD Interface

7.4 HDD Power Down

The hard disk drive (HDD) is not always used. It is accessed only when a file is read or written, and it is almost idle. However, the power is consumed during idle status. Although some HDDs have the Power Save mode under software control, their power consumption cannot be reduced to zero during idle. While the CARD-486HB can completely cut off the HDD power if an external circuit as shown in Figure 7-2 is attached to the CARD-486HB.

The CARD-486HB's external circuit uses the SMOUT2 signal to turn the HDD power on or off. For the standard BIOS setup, the SMOUT2 is set to low when the HDD idle status is detected. The SMOUT2 is set to high when the HDD is accessed.

When the HDD's power supply is turned off, the HDD must be electrically disconnected from all other devices including the CARD-486HB completely. If not disconnected, the other devices may not operate normally. Therefore, the HDD must be buffered and the buffer must be controlled appropriately. The HDCS0# and HDCS1# chip select signals and the HDENH# and HDENL# data buffer control signals are controlled by the CARD-486HB. However, the other signals need to be controlled by the CARD-486HB's external control circuit. Also, when the HDD's power supply is turned on, the HDD must be reset (power-on reset). If not reset, the HDD does not operate normally. Therefore, a reset signal generation circuit is also required.

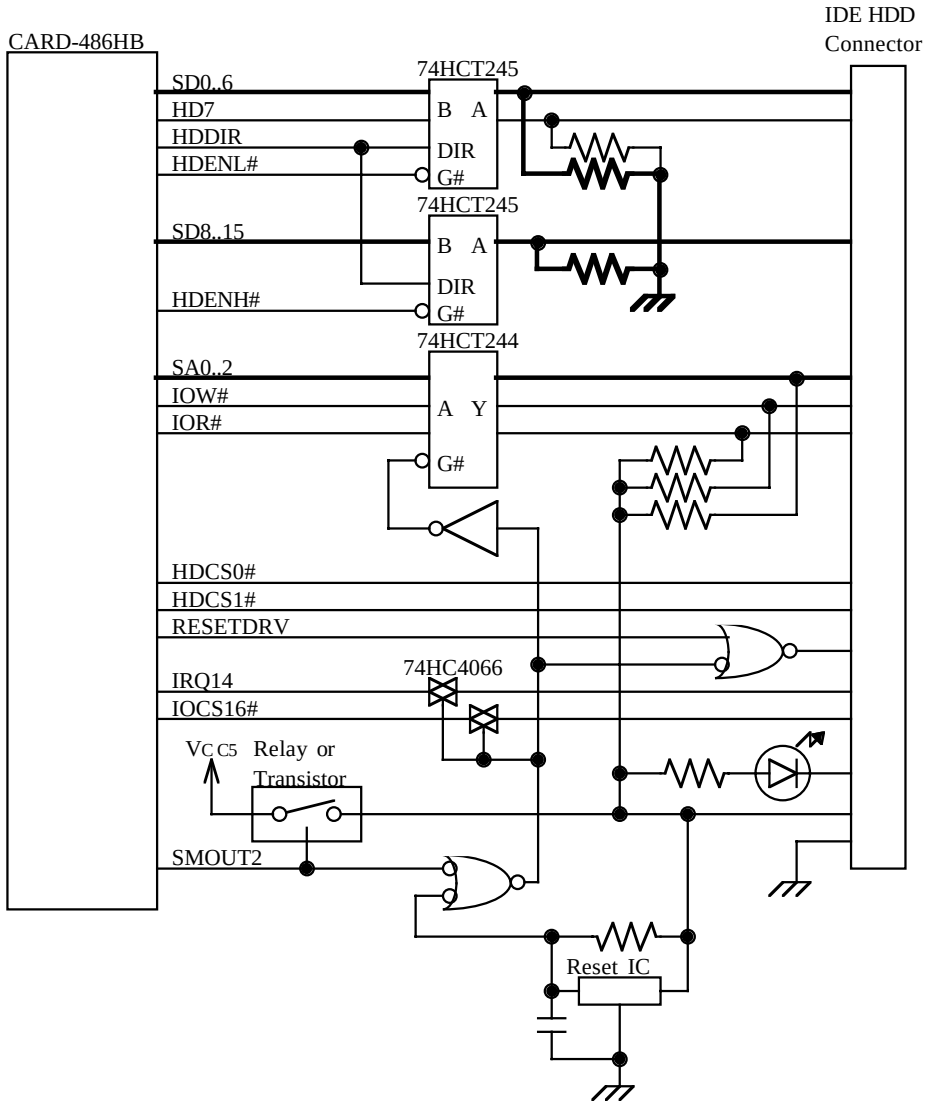


Figure 7-3 IDE HDD Interface with Power-Down Control

8. ISA Bus Interface

8.1 Expansion of I/O Device

8.1.1 I/O Address

The I/O space of the CARD-486HB is 1Kbytes (000h - 3FFh) like IBM PC/-AT. Also, the internal I/O device of the CARD-486HB decodes only 10bits of Addresses SA0 - SA9. The spaces from 000h to 0FFh are internally used by the CARD-486HB and cannot be used on the ISA bus. Also, some addresses between 100h and 3FFh are internally used by the CARD-486HB. When functions are expanded on to the ISA bus, these I/O addresses internally used by the CARD-486HB should not be used.
I/O addresses internally used by the CARD-486HB and those used on the ISA bus are as follows:

Table 8-1 I/O Addresses

Address	Availability	
000h to 0FFh	Since being internally used by the CARD-486HB, these addresses cannot be used on the ISA bus.	
100h to 16Fh	Can be used on the ISA bus.	
170h to 178h	Are used by the secondary HDD.	(Note 1)
179h to 1EFh	Can be used on the ISA bus.	
1F0h to 1F8h	Are used by the HDD.	(Note 2)
1F9h to 277h	Can be used on the ISA bus.	
278h to 27Fh	Are used by the Parallel Ports.	(Note 3)
280h to 2E7h	Can be used on the ISA bus.	
2E8h to 2EFh	Are used by the Serial Ports.	(Note 4)
2F0h to 2F7h	Can be used on the ISA bus.	
2F8h to 2FFh	Are used by the Serial Ports.	(Note 4)
300h to 377h	Can be used on the ISA bus.	
378h to 37Fh	Are used by the Parallel Ports.	(Note 3)
380h to 3AFh	Can be used on the ISA bus.	
3B0h to 3DFh	Are used by the VGA.	(Note 2)
3E0h to 3E7h	Can be used on the ISA bus.	
3E8h to 3EFh	Are used by the Serial Ports.	(Note 4)
3F0h to 3F7h	Are used by the FDC.	(Note 2)
3F8h to 3FFh	Are used by the Serial Ports.	(Note 4)

(Note 1) If the ISA bus does not have the secondary HDD I/F, these I/O addresses can be used on the ISA bus.
(Note 2) If these functions are not used, the I/O addresses can be used on the ISA bus.
(Note 3) As the CARD-486HB has a single parallel port controller, one of two areas can be used on the ISA bus. If the parallel port is not used, both of two areas can be used on the ISA bus.
(Note 4) As the CARD-486HB has two serial port controllers, at least two of four areas can be used on the ISA bus. If the serial ports are not used, all four areas can be used on the ISA bus.

8.1.2 Decoding of I/O Address

Internal I/O addresses of the CARD-486HB are decoded in 10bits from SA0 to SA9 like IBM PC/-AT. So, it should be noted that I/O addresses of 400h or over are duplicated to those from 00h to 3FFh. For example, when an I/O device (for full decoding of SA0 - SA15) with 0400h - 040Fh is designed and accesses to 400h - 40Fh, the device will collide against the DMA register (000h - 00Fh) inside the CARD-486HB and the CARD-486HB will not operate normally. When an I/O device fully decoded is mapped in the I/O spaces of 400h or over, an I/O address must be selected so that addresses of lower 10bits do not overlap the internal I/O device of the CARD-486HB.
When the CARD-486HB starts a DMA transfer from a memory to an I/O, the memory address is output to the address buses (SA0-19, LA16-23) and both IOW# and MEMR# become active at the same time. During a DMA transfer from an I/O to a memory, the memory address is output to the address buses and both IOR# and MEMW# become active at the same time. This means that, during a DMA transfer, IOR# or IOW# becomes active despite of memory address. Therefore, the I/O device must be set not to operate even when addresses for the DMA transfer agree with the ones being used by yourself. The AEN is used to realize this. The AEN turns into “HIGH” during the DMA transfer. In general, the I/O device must be designed so as to prohibit address decoding when the AEN is “HIGH.”

A simple example is given below. This I/O device is assumed to use the I/O address of 100h.

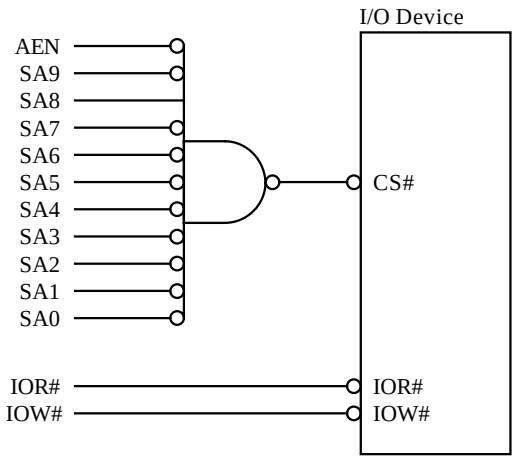


Figure 8-1 I/O Device Connection Example

8.2 Memory Device Expansion

The 16M-byte memory space is provided for ISA buses. SMEMR# and SMEMW# are memory control signals for the XT buses (having a 1M-byte memory space), and they are set to active only when zero to 1M-byte memory is accessed. MEMR# and MEMW# are memory control signals for AT buses (having a 16M-byte memory space), and they are valid in all memory areas of ISA bus space. Similar to the I/O addresses, the memory addresses used by the CARD-486HB's built-in DRAM or flash ROM cannot be used on the ISA buses. When the CARD-486HB's built-in DRAM is accessed, the SMEMR#, SMEMW#, MEMR#, and MEMW# are kept inactive on the ISA buses. The CARD-486HB's memory map for the standard BIOS is shown on Table 8-2.

Table 8-2 CARD-486HB Memory Map

Address	Device mapped	
000000h to 09FFFFh	DRAM	
0A0000h to 0BFFFFh	VGA	(note5)
0C0000h to 0C7FFFh	DRAM(VGA BIOS)	(note5)
0C8000h to 0CFFFFh	ISA	(note6)
0D0000h to 0D7FFFh	ISA	(note6)
0D8000h to 0DFFFFh	ISA	(note6)
0E0000h to 0E7FFFh	ISA	(note6)
0E8000h to 0EFFFFh	ISA	(note6)
0F0000h to 0FFFFFh	DRAM(BIOS)	
100000h to 3FFFFFh	DRAM	
400000h to 7FFFFFh	DRAM or ISA	(note7)
800000h to BFFFFFh	DRAM or ISA	(note7)
C00000h to FBFFFFh	DRAM or ISA	(note7)
FC0000h to FEFFFFh	FLASH ROM	
FF0000h to FFFFFFh	FLASH ROM	

(Note 5) Can be used for the ISA bus if the CARD-486HB's built-in VGA is not used.
(Note 6) See Chapter 10 "User Programs."
(Note 7) Depends on the CARD-486HB's built-in DRAM capacity.

If the memory is expanded on ISA buses, the following problems may occur:

If the memory is expanded on ISA buses, the memory is accessed in the basic cycle of ISA buses (that is, 6.77 to 10MHz system clocks). If a program is located in a memory area that has been expanded for ISA buses and if its codes are executed, its access time may be longer than the time of internal memory access. This performance difference may cause an FDD access problem in some applications.

8.3 8/16-bit Devices

The I/O and memory data can be transferred in 8-bit or 16-bit mode on ISA buses. If the target in a cycle is an 8-bit device, the CARD-486HB sends data using SD0 to SD7 only. If it is a 16-bit device, the CARD-486HB sends data using SD0 to SD15.
Therefore, if the target is a 16-bit device, MEMCS16# or IOCS16# must be driven actively by the device so that the 16-bit target device is posted to the CARD-486HB. As MEMCS16# and IOCS16# can be used for "Wired OR," they must be driven with the open collector. As they are internally pulled up by the CARD-486HB, they are usually inactive (they are not driven when low). Therefore, for the 8-bit devices, MEMCS16# and IOCS16# need not be driven inactively.

8.3.1 16-bit Memory Device

A memory device having 16-bit data must make MEMCS16# active by the end of "Ts" as shown in Figure 8-2. As the CARD-486HB latches the MEMCS16# at the end of "Ts," its active setup in any other period is meaningless.

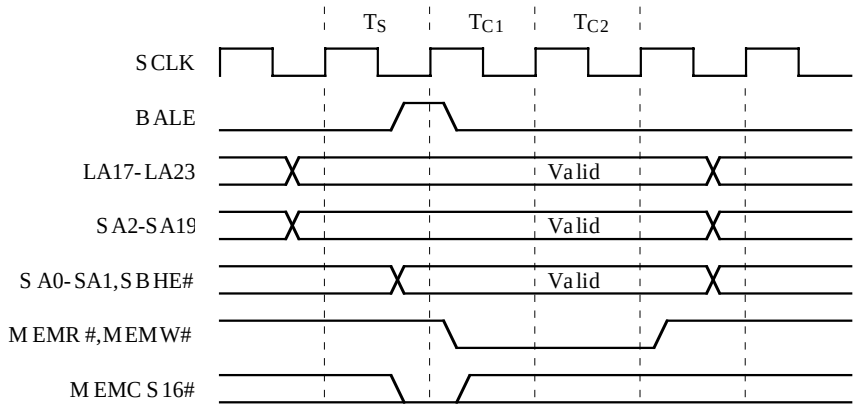


Figure 8-2 MEMCS16# Timing Chart

An example of MEMCS16# generator circuit is given in Figure 8-3. This is an example memory device which uses memory addresses A00000h to BFFFFFh. The addresses are decoded and the MEMCS16# is driven by the open collector.

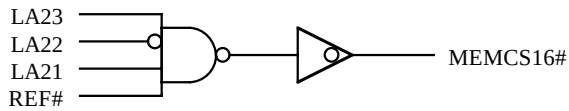


Figure 8-3 MEMCS16# Example (1)

The MEMCS16# is also used to determine the use of 8-bit or 16-bit memory during DMA transfer. The circuit shown in Figure 8-3 has no problem.

Figure 8-4 gives another example where memory addresses 0D0000h to 0DFFFFh are used by the memory device.

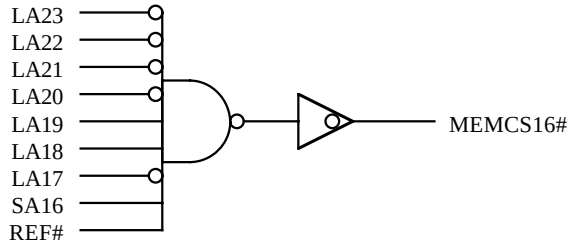


Figure 8-4 MEMCS16# Example (2)

The device of this example also decodes addresses and makes MEMCS16# active by the open collector. The SA16 is used for address decoding. If the CARD-486HB is used, SA2 to SA19 and LA17 to LA23 are output as the valid data in the same timing. This timing have an enough time for address decoding and for MEMCS16# driving (that is, the enough time to the end of "Ts" after address enabling). If IBM PC/-AT (or the CARD-386/486 fitted with SL chip set of Intel Corp.) is used, SA2 to SA19 become enabled in the same timing as SA0, SA1 and SBHE# shown in Figure 8-2. Therefore, the time period from address enabling (SA16 in this example) to the end of TS (address decoding time) is reduced. So, the system may not latch correct values of the MEMCS16# and may malfunction. Most of the latest PCs do not malfunction because they output SA and LA in the same timing as shown in the specification of the CARD-486HB. Our future CARD-PCs will succeed the specification, and no latching with the BALE is necessary for generation of the MEMCS16# and for memory address decoding (generation of memory chip select signal.

8.3.2 16-bit I/O Devices

An IOCS16# timing chart is shown in Figure 8-5. As the IOCS16# is not latched by the CARD-486HB, it must be kept active from the end of "Tc1" to the cycle end.

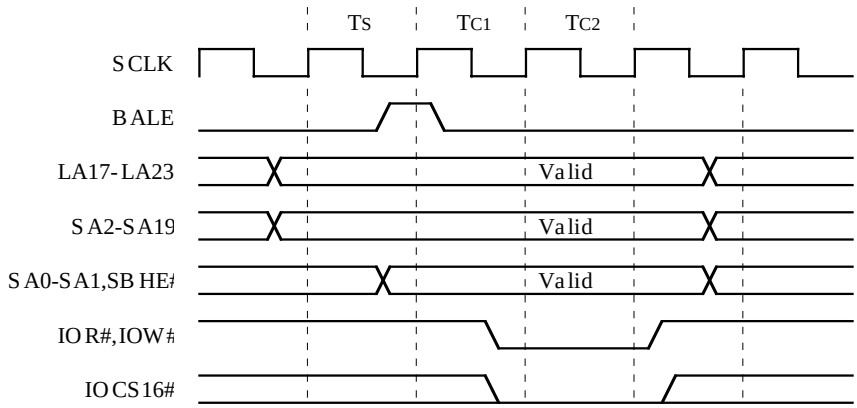


Figure 8-5 IOCS16# Timing Chart

For IOCS16# generation, the addresses are decoded and the IOCS16# is driven by the open collector.

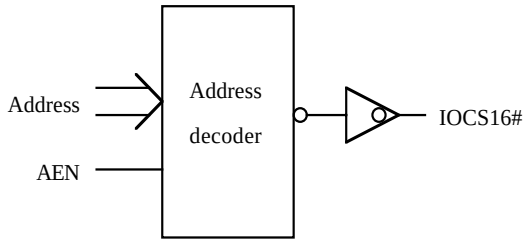


Figure 8-6 IOCS16# Example

8.3.3 16-bit Device Data Buses

When the CPU reads data from a device on the ISA bus, the device drives data (which is valid to the data bus) when the read command (IOR#, MEMR# or SMEMR#) is active. However, the 16-bit device must drive the data buses by considering not only the commands but also the SA0 and SBHE# as defined on Table 8-3.

Table 8-3 Data Buffer Control

Read command	SA0	SBHE#	SD0 to SD7	SD8 to 15
Inactive	x	x	Must not be driven	Must not be driven
Active	0	1	Must be driven	Must not be driven
Active	1	0	Most not be driven	Must be driven
Active	0	0	Must be driven	Must be driven

This data buffer control is required to prevent a conflicted data bus.

An example of conflict of a 16-bit device is given in Figure 8-7, Data Bus Conflict. Though the device has the 16-bit buses, the CPU may not always access 16-bit data (SA0=Low and SBHE#=Low) and sometimes accesses the low-order bytes (SA0=Low and SBHE#=High) only or the high-order bytes (SAO=High and SBHE#=Low) only. When the CPU reads the high-order bytes only, the device outputs data to SD8 to SD15. At the time, the CARD-486HB outputs the same data as those to SD8 to SD15 to SD0 to SD7. (This is the specification of the controller SPC8210 which is fitted in the CARD-486HB.) If the device is designed to drive SD0 to SD7 even when the CPU reads high-order bytes only, the CARD-486HB will also drive SD0 to SD7 and data bus conflicts will occur.

Such conflict may also occur during DMA transfer. The data buses must be driven by following the definition of Table 8-3.

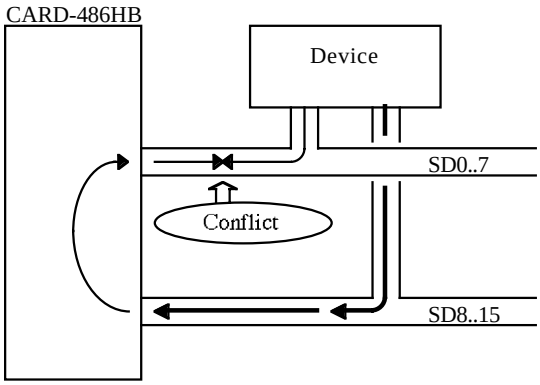


Figure 8-7 Data Bus Conflict

In this example, the CPU reads SD8 to SD15 only (but ignores SD0 to SD7). This conflict does not affect on the read data. Therefore, if a conflict occurs, the CARD-486HB and devices are seemed to operate normally. Such conflict can be detected only when SD0 to SD7 are read on an oscilloscope or others. However, such circuit design must be avoided because the signal conflict can affect on the current consumption and device service life.

An example of 16-bit memory device circuit is given in Figure 8-8. The above discussed points have been well considered in this circuit design. This example uses memory addresses 0D0000h to 0DFFFFh.

8.3.4 8-bit Device Data Buses

In the read cycle of the 8-bit device shown in Figure 8-7 (when MEMCS16# and IOCS16# are not asserted), data are always accessed through SD0 to SD7 of the data base. So, the buffer has to drive SD0 to SD7 only all the times. If it drives SD8 to SD15 as well, conflicts will occur. An example of 8-bit device conflict is given in Figure 8-8. Since the device is of a 8-bit type, the CPU always accesses 8-bit data (SD0 to SD7) irrespective of even address or odd address. When the CPU reads odd addresses (SA0=High and SBHE#=High), the CARD-486HB outputs the same data as those to SD0 to SD7 to SD8 to SD15. The CPU reads data of SD8 to SD15. (This is the specification of the controller SPC8210 which is fitted in the CARD-486HB.) If the device is designed to drive SD8 to SD15 at the time, the CARD-486HB will also drive SD8 to SD15 and data bus conflicts will occur. In this case, the CPU cannot read correct data and the system may malfunction.

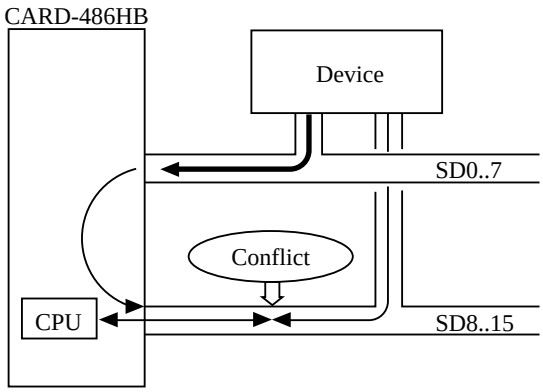


Figure 8-8 Data Bus Conflict

Figure 8-9, Memory Circuit Example, gives an example of the circuit of a 16-bit memory device. In this example, the memory device uses memory addresses 0D0000h to 0DFFFFh.

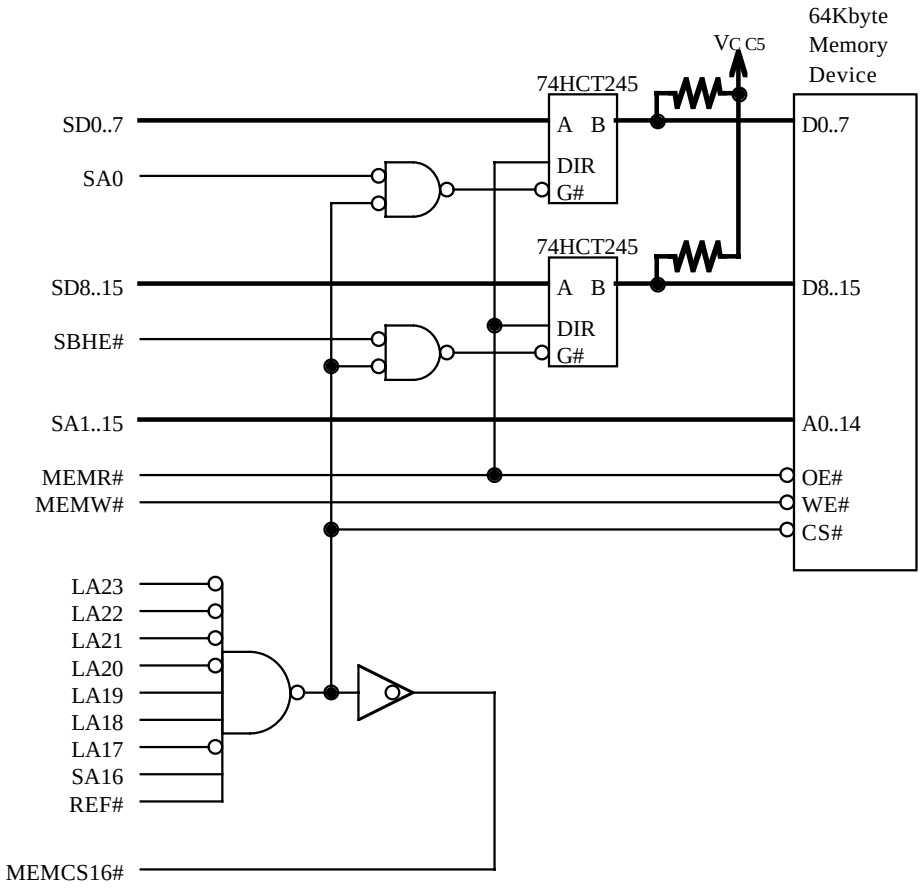


Figure 8-9 Memory Circuit Example

8.4 IRQ and DRQ

When using the IRQ and DRQ provided by the CARD-486HB, consider the following notes.

The IRQ6 and DRQ2 signals are used by the CARD-486HB's built-in FDD interface. As shown in Figure 8-10, the IRQ/DRQ from the built-in FDD controller and the IRQ/DRQ from the ISA bus are "wired ORed." Therefore, if the built-in FDD interface is used, the IRQ6 and DRQ2 on the ISA buses must be disconnected or set to high impedance.

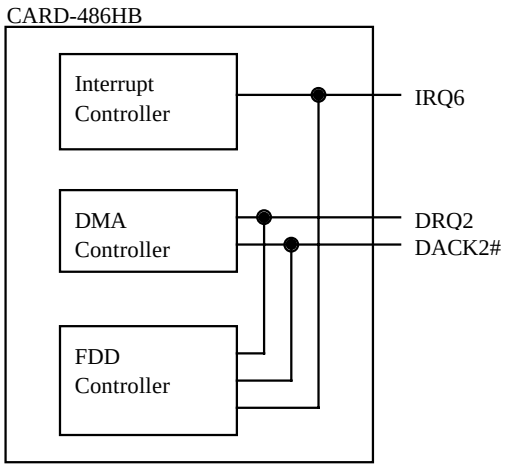


Figure 8-10 IRQ6/DRQ2 Block Diagram

Similarly, some of IRQ3, IRQ4, IRQ10 and IRQ11 are used for the serial interface, and either IRQ5 or IRQ7 is used for the parallel interface.
The actual IRQ signal usage for the interface is determined by CARD-486HB setup or set by the ROM Adaptation Kit (RAK).
Though the signal IRQ12 is used for the mouse interface, the RAK can disable the signal from the mouse on the CARD-486HB. So, the signal can be used as an interrupt from the ISA bus. Since being contained in the specifications of the CARD-486HB, etc., however, the function may not be supported on our future CARD-PCs, and your thorough examination of the influence is required.

8.5 ISA Data Buses

Some applications write data in I/O ports and read them immediately after it to determine the presence of optional boards. In such case, the application programs are expecting to have the data change on the data bus if no I/O port exists. If an I/O port exists, there is no problem. However, if no I/O port exists and if the written data is kept on the data bus until the next bus cycle, the application may incorrectly determine that a board exists although no actual board does exist. To avoid such problem, the data buses must be pulled up.

8.6 Bus Clock (SCLK)

The ISA-bus works based on the bus clock (SCLK). Since the CARD-486HB divides the CPUCLK to generate the SCLK, however, the clock frequency varies with the model (the frequency of the applicable CPU). When the CARD-486HB frequency is 16MHz, for example, the SCLK frequency is calculated to 8MHz by dividing 16MHz by 2. When the CARD-486HB frequency is 33MHz, the SCLK frequency comes to 8.33MHz as 33MHz is divided by 4. Since the CPUCLK is itself generated by the PLL, some error is included in it. So, the SCLK frequency may occur include some error. For this reason, the SCLK cannot be used for accurate clocks. For clocks which are required to be accurate, use the OSC (14.31818MHz) which is asynchronous with the SCLK or provide oscillators partially. Also, timing of the ISA-bus depends on the SCLK, and the total system has to be designed so flexibly that it can work even though the SCLK frequency fluctuates between 6.78MHz and 10MHz.

9. Power Management

9.1 System Management OUT (SMOUT)

The CARD-486HB's standard BIOS can control the power of the following devices by using SMOUT0 to SMOUT2.

SMOUT0: Controls the COMA. When the COMA is standed by or when the CARD-486HB is in Suspend mode, SMOUT0 is set to low. Therefore, the driver/receiver IC of RS-232C interface can be standed by.

SMOUT1: Controls the COMB. When the COMB is standed by or when the CARD-486HB is in Suspend mode, SMOUT1 is set to low. Therefore, the driver/receiver IC of RS-232C interface can be standed by.

SMOUT2: Controls the HDD. When the HDD is standed by or when the CARD-486HB is in Suspend mode, SMOUT2 is set to low. Therefore, the HDD's power supply can be turned off by this SMOUT2. The HDD uses a lot of signals which are shared by ISA buses. If the shared signals are not isolated when the HDD is turned off, a malfunction may result.

SMOUT3 is used to switch the voltage of PGM flash-ROM update power supply.

9.2 Battery Monitor Signals

The CARD-486HB provides the BATWARN# and BATLOW# pins to alarm the battery power to the battery drive system. When these signals are set to active, the CARD-486HB's standard BIOS executes the following processing (these processing can be disabled by CARD-486HB setup).

- BATWARN#
  This input signal is used to alarm the battery low level. When this signal is set to active, the low battery alarm beep sounds at the speaker interface.

- BATLOW#
  The above described BATWARN# can sound the beep to alarm low battery power. However, if the battery is further discharged and if the system cannot operate with the current battery, this signal is set to active. The active BATLOW# can set the CARD-486HB to the Suspend mode.

9.3 EXTSMI#

When the EXTSMI# is set to active, the CPU can be interrupted and any desired program can be executed regardless of the current application and operating systems. However, this program is unique to the system, it is not supported by the CARD-486HB's standard BIOS. A new program must be created to use the EXTSMI#.

9.4 Suspend Mode

The CARD-486HB supports the Suspend mode to stand by the CPU and other devices and to hold the memory and register data with the minimum current consumption. When the CARD-486HB's standard BIOS detects a falling edge of SRBTN# signal (if the Suspend mode has been enabled during setup), it enters the Suspend mode. When the BIOS exists the Suspend mode (called the "resume"), the CARD-486HB returns to the status before it has entered the Suspend mode. The system can be resumed in the following three ways:

1. When a falling edge of SRBTN# is detected
2. When a falling edge of COMARI# or COMBRI# is detected
3. When the clock time specified during setup has come

Tables 13-2 to 13-10 define the CARD-486HB pin state in Suspend mode of BIOS standard setup. The CARD-486HB's current consumption may increase in certain pin state and external pin termination of the CARD-486HB. To avoid the increased current consumption, the following points must be considered:

(1) If a pull-up resistor is added to a pin which is driven during low by the CARD-486HB, the current flows through the resistor and the current consumption increases.
The table of Section 13 "Pin Assignment" shows the pin which is driven during low regardless of whether the CARD-486HB has its pull-up resistors or not. However, these pull-up resistors are disconnected when the low signal is driven by the CARD-486HB. Therefore, no current flows through the pull-up resistors.

(2) If a pull-down resistor is added to a pin which is driven during high by the CARD-486HB, the current flows through the resistor and the current consumption increases.
The table of Section 13 "Pin Assignment" shows the pin which is driven during high regardless of whether the CARD-486HB has its pull-up resistors or not. However, these pull-up resistors are disconnected when the high signal is driven by the CARD-486HB. Therefore, no current flows through the pull-up resistors.

(3) When a pin having a pull-up resistor is set to low, the current flows through the pull-up resistor and the current consumption increases.

(4) When a pin having a pull-down resistor is set to high, the current flows through the pull-down resistor and the current consumption increases.

(5) If an input pin has no pull-up or pull-down resistor, its signal level must be set to prevent an input floating.

(6) If the CARD-486HB having the three-state off output is kept on and if it is connected to the CMOS device, the device input must be set previously by the pull-up or pull-down resistor.

(7) If a device is connected to a pin having the following status, its power supply can be turned off during Suspend mode:

- The output pin having the three-state off signals
- The pin driven with low
- The input pin having a pull-down resistor
- The I/O pin which is used for input and which has a pull-down resistor

The pins in other state can cause the current to flow through their pull-up or pull-down resistors or the input floating. Therefore, the device power supply cannot be turned off. A buffer is required between the CARD-486HB and the device to turn the device power supply off (see Section 7.4 for details).

10. User Programs

The CARD-486HB contains a 256K-byte flash ROM to store the BIOS/SETUP and other data. However, half of its memory are is empty and the user can store programs and data in this empty area. These programs and data can be copied to addresses 0A0000h to 0EFFFFh of DRAM and executed. As the destination memory area of programs is changed to the DRAM for mapping, the area on the ISA buses cannot be used.

For program storage in the flash ROM, refer to the CARD-PC Adaptation Kit Manual.

11. Others

11.1 Generic Timer Output (Watchdog Timer)

The CARD-486HB has a generic timer that can be used as a watchdog timer. The timer uses channel 1 of the 8254 extension timer having the 8kHz reference clock. The timer's OUT1 signal is directly output to the WDTIM# pin of CARD-486HB.

To use the CARD-486HB's watchdog timer:

(1) Set the timer.

(2) Reset the timer by the application software before timeout, and restart the timer.

(3) The WDTIM# is set to active if the timer is not reset but timed out due to a software overrun or others.

The CARD-486HB provides the following BIOS functions to use its watchdog timer:

- Watchdog timer status collect function
- Protect mode interface routine address collect function
- Timer setup, start and reset functions

(For details, refer to the BIOS Reference Manual.)

The WDTIM# is usually kept high. When a timeout occurs, the WDTIM# is set to low. The timeout recovery processing depends on the CARD-486HB's external circuit setup. The following circuit is usually used.

(1) The WDTIM# is connected to an IRQ pin, and the CPU is interrupted during timeout.

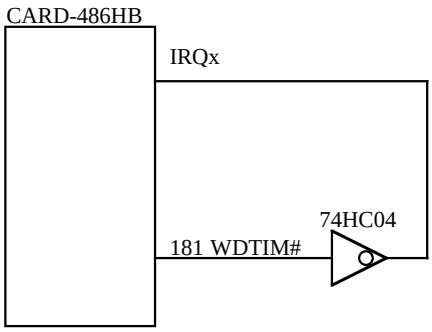


Figure 11-1 CPU Interrupt by WDTIM#

(2) The WDTIM# is connected to the IOCHCK# pin, and the CPU is interrupted with NMI during timeout.

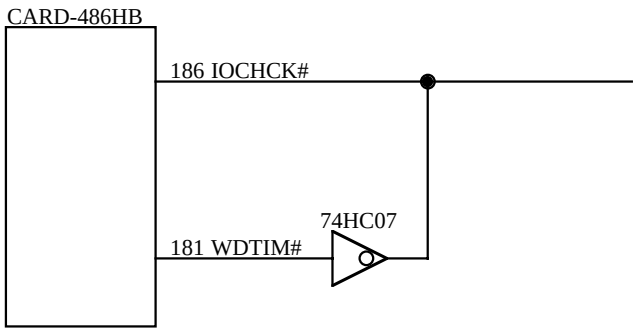


Figure 11-2 NMI by WDTIM#

(3) The WDTIM# is connected to the EXTSMI# pin, and the CPU is interrupted with SMI during timeout.

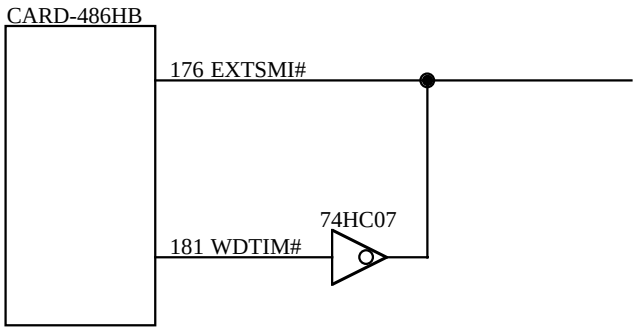


Figure 11-3 SMI by WDTIM#

(4) The WDTIM# is connected to the POWERGOOD pin, and the CARD-486HB is reset during timeout.

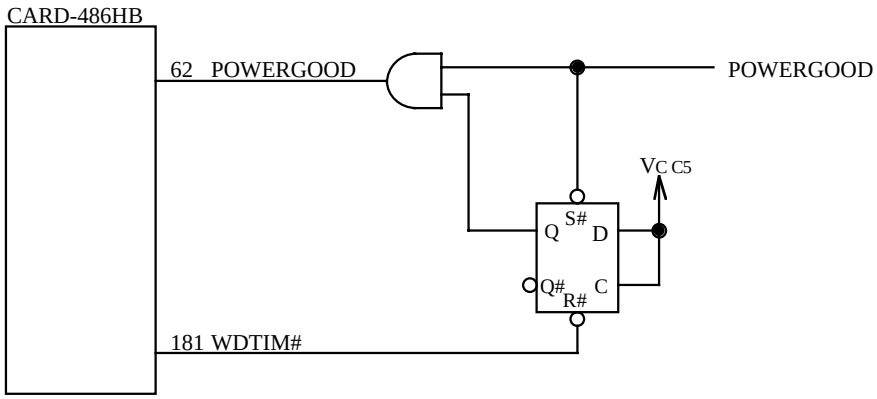


Figure 11-4 CARD-486HB Reset by WDTIM#

This figure gives just an idea of resetting the CARD-486HB by the WDTIM#. When the CMOS-RAM in the CARD-486HB is backed up by battery, glitches may occur at the POWERGOOD terminal and the contents of the CMOS-RAM may be destroyed. For the detail, see 11.2, 11.2.1, 11.3 and 11.4.
The separate processing routines are required for CPU interrupt, NMI, and SMI processing.

11.2 Updating of Flash ROM

The CARD-486HB contains the 256K-byte flash ROM to store BIOS programs. It can be updated in the following two ways:

(1) Update the flash ROM without removing the CARD-486HB from the system device.

(2) Update the flash ROM by using the CARD-PC ROM writer.

11.2.1 Flash ROM Update Circuit

To update the flash ROM without removing the CARD-486HB from the system device, supply the +12V power to the PGM pin. Use 0 to 5 Vdc during normal operation.
To write the updated data in the flash ROM, use the Epson's "WFLASH.EXE" flash ROM update program. The circuit shown in Figure 11-5 is required to use the "WFLASH.EXE" program.

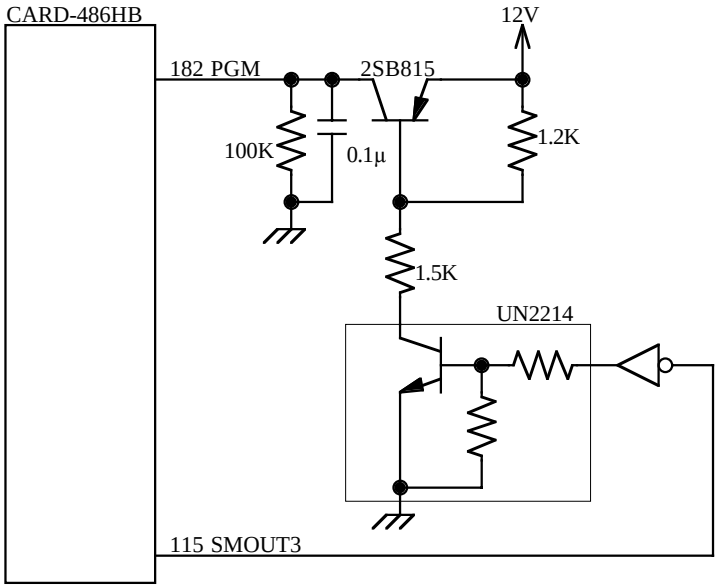


Figure 11-5 Flash ROM Update Circuit

11.2.2 ROM Writer for CARD-PC

For the information about the CARD-PC ROM writer, refer to the CARD-PC ROM Writer Manual.
The FLOAT# and ROMCE0# pins are used only to connect the CARD-PC ROM writer. Disconnect these pins during normal operations.

11.3 Backup of RTC and CMOS RAM

Even while the power to the system is off, data in the RTC and the CMOS RAM of the CARD-486HB are maintained if an external backup power is supplied to the system.

11.3.1 Backup of RTC and COM RAM

The V_{BK} power pin is used to backup the Real-Time Clock (RTC) and CMOS RAM. When the CARD-486HB is powered (when on) (by V_{CC5} or V_{CC3}), the same power as the V_{CC5} pin is supplied to the V_{BK} pin. When the CARD-486HB is not powered (when off), the power is supplied from the backup battery (such as lithium battery). A sample circuit for power switching is shown in Figure 11-6.

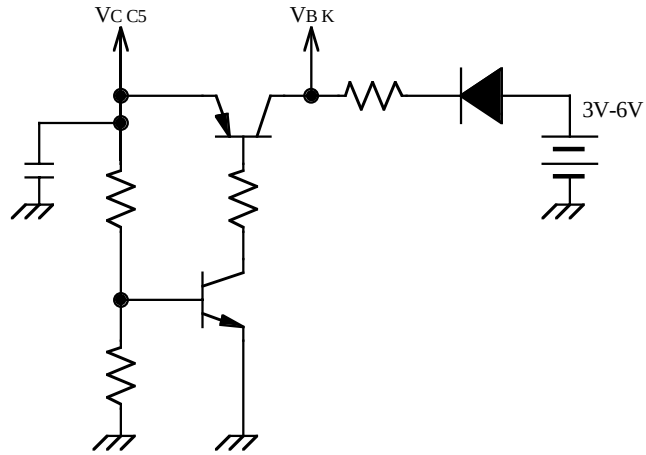


Figure 11-6 Power Switching Sample Circuit (1)

If the RTC and CMON RAM need not be backed up, the same power as the CARD-486HB's V_{CC5} pin must be supplied to the V_{BK} pin. As the standard BIOS setup of the CARD-486HB assumes the completed backup of RTC and CMOS RAM, the BIOS must be modified by the RAK if they are not backed up.

11.3.2 Precautions on System backing-up RTC/CMOS RAM

If the back-up power is not supplied, for some reason, to the system which is expected to receive the power to back up the RTC and the CMOS RAM, the BIOS of the CARD-486HB will take some actions to prevent trouble. In this case (selection by the RAK), pay attention to the following:
When backing up the RTC and the CMOS of the CARD-PC, the CARD-PC requires that the voltage of the back-up battery is 2.5V or more. Maintain this voltage during the back-up period. If the voltage goes below 2.5V, data in the RTC (time, etc.) and the one in the CMOS RAM (setup information, etc.) will be destroyed.
The RTC controller of the CARD-PC has bits to indicate "The back-up power was not supplied during a power-off period." (CMOS RAM index ODh. For the detail, refer to the BIOS Reference Manual.). This state results from any of the following:

- The CARD-PC has come off the system.
- The back-up battery has been completely discharged (to 0V).
- The back-up battery was removed or was installed again after removal.

The BIOS of the CARD-486HB has the function to correct data in the RTC and the CMOS RAM by checking the bit information in the RTC controller or data in the RTC and the CMOS RAM. (Check sum inspection. But date and time information cannot be detected until they come to abnormal values.) This selection and setting to the BIOS are made by the RAK. When "No supply of back-up power" is detected, or when the data in the RTC or the CMOS RAM are destructive (when check sum errors or abnormal date and time information are detected), the preset default CMOS values will be set.

When the default CMOS values are loaded, the SETUP information may change and the system action may be affected. So, the bits to indicate the load of default CMOS values are available on the BIOS of the CARD-486HB.

[CMOS RAM Index OEh]
bit 11 : Default CMOS values are loaded.
0 : Default CMOS values are not loaded.

These bits are not cleared (=0) until the SETUP of the CARD-486HB is started. So, troubles after change of the SETUP information can be prevented by installing the program, which takes proper actions at the starting referring to these bits, in the beginning part of the start system.

11.4 Power (V_{CC5}/V_{CC3}) and POWERGOOD

Figure 11-7 shows the V_{CC5}, V_{CC3} and POWERGOOD power sequence when the power supply is turned on and off. The V_{CC5} must always be greater than or equal to the V_{CC3} in any timing other than the one shown in the figure.
If the CARD-486HB is not reset during power-on, it cannot start the normal operations. Therefore, the POWERGOOD must be inserted in the timing shown in the figure.
The POWERGOOD signal is also used to isolate the CARD-486HB's built-in RTC and CMOS RAM. Therefore, if the POWERGOOD is set to high before the V_{BK} is switched from the lithium battery to V_{CC5}, the RTC or COM RAM contents may be destroyed. When the V_{BK} is powered by the lithium battery, the POWERGOOD must not exceed 0.8 V.

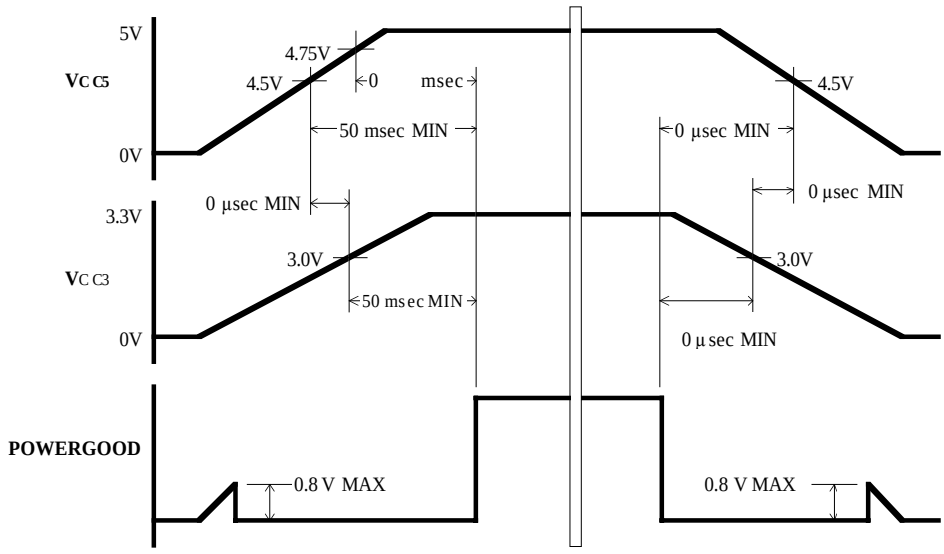


Figure 11-7 Power-Up/Down Sequence

Reference information:

Battery and VCC switching, and POWERGOOD generator circuit

The MAXIM's MAX703 allows to readily construct the battery and VCC switching circuit and the POWERGOOD signal generator circuit. Figure 11-8 shows a reference circuit.

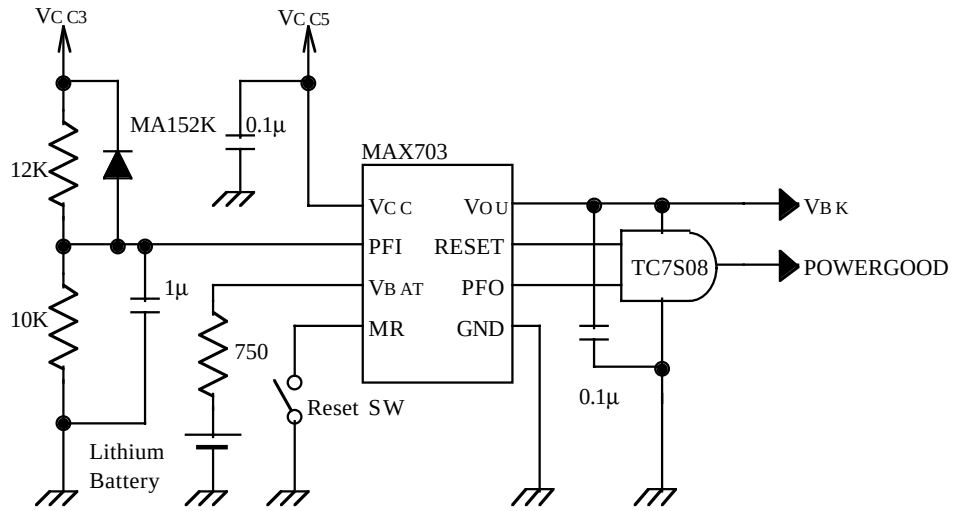


Figure 11-8 Power Switching Sample Circuit (2)

When using the watchdog timer in the above circuit configuration, don't connect the WDTIM# signal directly to the MR pin. The MR pin is (artificially) pulled up to the VOU inside the MAX703. If the WDTIM# is directly connected, some current will leak from the VBK to the WDTIM# signal when the power supply is turned off (VCC5=VCC3=0V), and the life of the lithium battery will be shortened extremely. So, when the power supply is turned off, it is necessary to separate the MR from the WDTIM# signal completely. (See Figure 11-9, Sample Circuit Separating MR from WDTIM#.)

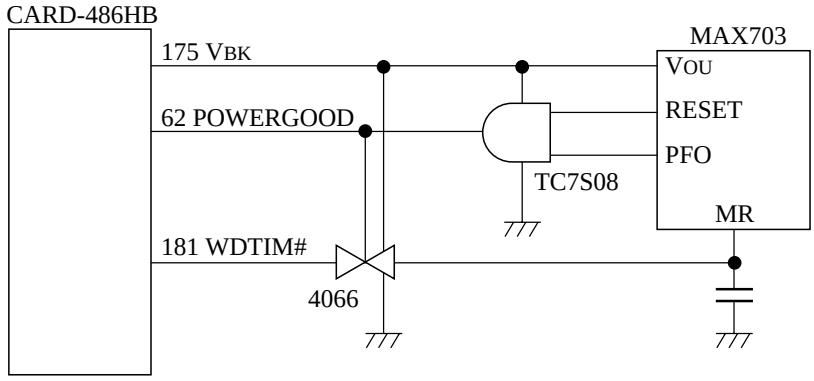


Figure 11-9 Sample Circuit Separating MR from WDTIM#

12. Matters to be Noted in Use of Card PC

12.1 Power Supply and Grounding

12.1.1 Power Supply Connection

As the CARD-486HB contains the high-speed CPU and peripheral circuits, its current consumption greatly varies when operating. To keep the stable operation and high display quality of the CARD-486HB under such conditions, connect the CARD-486HB's power pins (V_{CC5} and V_{CC3}) and ground pins to the power circuit having the lowest possible impedance. Use the power circuit having the current capacity appropriate to the customer's applications, and assure the instantaneous current supply capacity. Also, take appropriate actions against the noise to suppress both the high- and low-frequency noise.

12.1.2 Cabling of Power Supply

The CARD-486HB's external power and ground leads must be connected to their planes to minimize the wiring inductance. If the plane wiring is unavailable, use the thick leads as much as possible to minimize the noise.

12.1.3 Capacitor Insertion

To assure the stable CARD-486HB operations, insert a capacitor between its power supply and the ground.

Between V_{CC3} and GND pins:
47 to 470μF (Two 47μF capacitors in parallel connection are recommended to use.)
Insert the capacitor(s) close to the V_{CC3} (pin No. 82, 83, 200 or 201).
Also, we recommend to insert a capacitor into a position close to the V_{CC3} (pin No. 29, 30, 147 or 148).

Between V_{CC5} and GND pins:
10 to 100μF (The 47μF capacitor is recommended to use.)

As the appropriate capacitance varies depending on the system and applications, check the requirements and select the most appropriate capacitors. Use organic-semiconductor, aluminum solid electrolytic capacitors or others which have the low impedance and better temperature characteristics. We recommend to mount the 0.01 to 0.47μF capacitor (together with the above described capacitor in parallel layout) close to the connectors.

Always use these capacitors especially when using the CARD-486HB/33MHz.

12.2 Matters to be Noted in Designing of Printed Circuit Board

(1) Since many wires are used for the address and data buses of the CARD-PC, signal energy will increase if they change at the same time. And dragging wires may influence other signals. So, it is necessary in general to arrange waveforms by inserting damping resistors in the address and data buses or to separate them from other signals.
(2) For reset, clock and other control lines, noises may be superimposed in the buses due to cross talk. In that case, the following measures will be taken for example:
- Use guard patterns to reduce influences of other signal on signals which cause troubles to the system as a result of clock delay or separate them from other signals.
- Remove noises from signals like reset signal having timing margin by using integrators.

(3) In general, the output impedance of the CMOS output buffer is some ohms to tens of ohms. In case of wiring of printed circuit boards, however, characteristic impedances are more than 100ohms, and the impedance of the output buffer does not match the wiring ones. Therefore, waveforms may be confused due to influence of reflection in some patterns of printed circuit boards. Check each waveform, and insert damping resistors or terminating resistors in the printed circuit if necessary.
(4) When BIOS data are transferred from the flash memory in the CARD-PC to the shadow area of the RAM in the CARD-PC, the bus changes more severely than usual. BIOS data are transferred to the shadow area immediately after the power card is turned on or when the setup is terminated. Check influence of bus noise when data are transferred from the flash memory to the RAM as well.

12.3 Connection of CARD-PC Frame

The CARD-PC frame and the signal ground are connected at a point near the EASI connector in the CARD-PC. The system configuration determines which is better, one-point connection of the frame and the signal ground near the EASI connector or connection of the frame and the mother board ground with the shortest distance between them. So, printed circuit boards must be designed so as to suit for the both connections. The connecting method is decided after the system configuration is checked.

12.4 Accuracy of RTC

The RTC of the CARD-PC is as accurate as +/-100PPM (+/-8.65 sec./day). If the system requires more accurate time keeping function, connect an external RTC.
The accuracy of the RTC depends on oscillating frequency of the crystal oscillator for the RTC. Even at the ordinary temperature, the crystal oscillator generates frequency with some error, and the oscillating frequency fluctuates depending on temperature. The frequency error at the ordinary temperature is +/-50PPM. The relations between temperature and frequency are expressed by secondary curves. The frequency is highest at 25°C or so and lowers as the temperature changes. When the internal temperature of the CARD-PC is 70°C which is the highest working temperature of the CARD-PC, the frequency is 70PPM lower than that at the ordinary temperature. The frequency is 20PPM lower at 0°C than that at the ordinary temperature. So, the overall RTC accuracy is +/-100PPM or so.
Since the internal temperature rises as the CARD-PC is heated, the RTC is considered in general to delay. When the CARD-PC is left at the ordinary temperature after the power is turned off, the frequency error is smaller than that during operation.

13. Pin Termination

This section defines the pin characteristics and the processing of pins when not used.

Table 13-1 Explanation of Table Names and Symbols

Pin No.	Indicates the pin number.
Signal Name	Indicates the pin (or signal) name.
Type	Indicate the signal I/O type of each pin when operating. I : Input O : Output IO : Input and output IO OD : Input and the open-drain output OD : Open-drain output
Term	Indicates the pin termination with a pull-up or pull-down resistor or bus hold circuit in the CARD-486HB. xxPU : The pin is terminated with an xx-ohm, pull-up resistor. xxPD : The pin is terminated with an xx-ohm, pull-down resistor. HOLD : The pin is terminated with the bus hold circuit. The resistor has the average resistance. The CARD-386 and CARD-486 have the pull-up or pull-down resistors so that they are disconnected in the Suspend mode. However, the CARD-486HB is not disconnected.
Drive	Indicates the pin drive capacity. I_{OL} : The input current which can hold the low level. I_{OH} : The output current which can hold the high level.
Suspend	Indicates the pin status when the CARD-486HB is in the Suspend mode. Input : The input must be defined although it does not affect on the CARD-486HB's operations. If the CARD-486HB has built-in, pull-up or pull-down resistor or bus hold circuit pins, the input is determined by these values. Active : Used as the input pin. These pins affect on the CARD-486HB's operations. Drive : Drives the high or low signal line. Drive(H) : Drives the high signal line. Drive(L) : Drives the low signal line. 3-State : The three-state logic is turned off. 0V : 0V level (analog signal) These state are set when the CARD-486HB's standard BIOS is used.
Termination of unused pins	Defines the termination of pins if their functions are not used. If a pin requires its input level to be set, the pin must be terminated outside of the CARD-486HB. n.c : Terminate the pin with no connection. Pull-up : Add a pull-up resistor to the pin.

Table 13-2 VGA Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
3	EXDOTCLK	O	---	24, 8	Drive(L)	n.c
4	LD6	O	---	24, 8	Drive(L)	n.c
5	LD4	O	---	24, 8	Drive(L)	n.c
6	LD2	O	---	24, 8	Drive(L)	n.c
7	LD0	O	---	24, 8	Drive(L)	n.c
8	FPVTIM	O	---	24, 8	Drive(L)	n.c
9	FPAC	O	---	24, 8	Drive(L)	n.c
10	FPVCCON	O	---	6, 2	Drive(L)	n.c
11	LD9	O	---	24, 8	Drive(L)	n.c
12	LD11	O	---	24, 8	Drive(L)	n.c
13	LD13	O	---	24, 8	Drive(L)	n.c
14	LD15	O	---	24, 8	Drive(L)	n.c
15	BLUE	O	150PD	-	0V	n.c
16	GREEN	O	150PD	-	0V	n.c
17	RED	O	150PD	-	0V	n.c
18	VSYNC	O	---	12, 4	Drive(L)	n.c
19	LD17	O	---	24, 8	Drive(L)	n.c
121	FPDOTCLK	O	---	24, 8	Drive(L)	n.c
122	LD7	O	---	24, 8	Drive(L)	n.c
123	LD5	O	---	24, 8	Drive(L)	n.c
124	LD3	O	---	24, 8	Drive(L)	n.c
125	LD1	O	---	24, 8	Drive(L)	n.c
126	FPHTIM	O	---	24, 8	Drive(L)	n.c
127	LD8	O	---	24, 8	Drive(L)	n.c
128	FPVEEON	O	---	6, 2	Drive(L)	n.c
129	FPBLANK#	O	---	24, 8	Drive(L)	n.c
130	LD10	O	---	24, 8	Drive(L)	n.c
131	LD12	O	---	24, 8	Drive(L)	n.c
132	LD14	O	---	24, 8	Drive(L)	n.c
133	BRTN	--	---	-	-	n.c
134	GRTN	--	---	-	-	n.c
135	RRTN	--	---	-	-	n.c
136	HSYNC	O	---	12, 4	Drive(L)	n.c
137	LD16	O	---	12, 8	Drive(L)	n.c

The VGA interface is not connected inside the CARD-486HBL. Even so, do not connect signals of the signal colliding direction to the VGA interface to outside when any card other than CARD-486HBL is inserted.

Table 13-3 Keyboard and Mouse Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
21	MSDATA	IO OD	---	24,-	Input	Pull-up
139	MSCLK	IO OD	---	24,-	Input	Pull-up
22	KBDATA	IO OD	---	24,-	Input	Pull-up
140	KBCLK	IO OD	---	24,-	Input	Pull-up

Table 13-4 Floppy Disk (FD) Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
23	FDWP#	I	---	-	Input	Pull-up
24	FDINDEX#	I	---	-	Input	Pull-up
25	FDTRK0#	I	---	-	Input	Pull-up
26	FDWD#	OD	---	38,-	Drive	n.c
31	FDDS2#	OD	---	38,-	Drive	n.c
32	FDMT2#	OD	---	38,-	Drive	n.c
33	FDSIDE	OD	---	38,-	Drive	n.c
34	FDDIR	OD	---	38,-	Drive	n.c
141	FDRD#	I	---	-	Input	Pull-up
142	FDDCHG#	I	---	-	Input	Pull-up
143	FDWE#	OD	---	38,-	Drive	n.c
144	HDHIDEN	OD	---	38,-	Drive	n.c
149	FDDS1#	OD	---	38,-	Drive	n.c
150	FDMT1#	OD	---	38,-	Drive	n.c
151	FDSTEP#	OD	---	38,-	Drive	n.c

The FDD interface is not connected inside the CARD-486HBL. Even so, do not connect signals of the signal colliding direction to the FDD interface to prevent signals from colliding when any card other than CARD-486HBL is inserted.

Table 13-5 Serial Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
36	COMBDTR#	O	---	8, 8	3-State	n.c
37	COMBCTS#	I	50KPU	-	Input	n.c
38	COMBRTS#	O	---	8, 8	3-State	n.c
39	COMBDSR#	I	50KPU	-	Input	n.c
154	COMBRI#	I	50KPU	-	Input/Active	n.c
155	COMBRXD	I	50KPD	-	Input	n.c
156	COMBTXD	O	---	8, 8	3-State	n.c
157	COMBDCD#	I	50KPU	-	Input	n.c
40	COMADTR#	O	---	8, 8	3-State	n.c
41	COMACTS#	I	50KPU	-	Input	n.c
42	COMARTS#	O	---	8, 8	3-State	n.c
43	COMADSR#	I	50KPU	-	Input	n.c
158	COMARI#	I	50KPU	-	Input/Active	n.c
159	COMARXD	I	50KPD	-	Input	n.c
160	COMATXD	O	---	8, 8	3-State	n.c
161	COMADCD#	I	50KPU	-	Input	n.c
162	IRTXD	O	---	24, 12	3-State	n.c
44	IRRXD	I	50KPU	-	Input	n.c
153	DARXD	I	50KPU	-	Input	n.c

(Note) If the resume with the modem ring is enabled, the CARD-486HB is resumed when the COMARI# or COMBRI# is made active.

Table 13-6 Parallel Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
45	LPTSTROBE#	IO OD	4.7KPU	12,-	Input	n.c
46	LPTD0	IO	50KPD	8, 8	Input/Drive	n.c
47	LPTACK#	I	60KPU	-	Input	n.c
48	LPTPE	I	20KPD	-	Input	n.c
49	LPTD1	IO	50KPD	8, 8	Input/Drive	n.c
50	LPTD2	IO	50KPD	8, 8	Input/Drive	n.c
51	LPTD3	IO	50KPD	8, 8	Input/Drive	n.c
52	LPTD5	IO	50KPD	8, 8	Input/Drive	n.c
53	LPTD7	IO	50KPD	8, 8	Input/Drive	n.c
163	LPTAFD#	IO OD	4.7KPU	12,-	Input	n.c
164	LPTERROR#	I	60KPU	-	Input	n.c
165	LPTBUSY	I	20KPU	-	Input	n.c
166	LPTSLCT	I	20KPD	-	Input	n.c
167	LPTINIT#	IO OD	4.7KPU	12,-	Input	n.c
168	LPTSLCTIN#	IO OD	4.7KPU	12,-	Input	n.c
169	LPTD4	IO	50KPD	8, 8	Input/Drive	n.c
170	LPTD6	IO	50KPD	8, 8	Input/Drive	n.c
171	LPTDIR	O	---	8, 8	Drive	n.c

Table 13-7 HDD Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
54	HDDIR	O	---	8, 8	Drive(L)	n.c
55	HDENL#	O	---	8, 8	Drive(H)	n.c
56	HDCS0#	O	---	12, 12	High-Z	n.c
172	HD7	IO	50KPU	12, 12	Input	n.c
173	HDENH#	O	---	8, 8	Drive(H)	n.c
174	HDCS1#	O	---	12, 12	High-Z	n.c

Table 13-8 ISA Bus Interface

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
67	SD7	IO	50KPU	12, 12	Input	n.c
68	SD6	IO	50KPU	12, 12	Input	n.c
69	SD5	IO	50KPU	12, 12	Input	n.c
70	SD4	IO	50KPU	12, 12	Input	n.c
71	SD3	IO	50KPU	12, 12	Input	n.c
72	SD2	IO	50KPU	12, 12	Input	n.c
73	SD1	IO	50KPU	12, 12	Input	n.c
74	SD0	IO	50KPU	12, 12	Input	n.c
75	IOCHRDY	IO OD	1KPU	12,-	Input	n.c
76	AEN	O	---	12, 12	Drive(L)	n.c
77	SA19	O	HOLD	12, 12	Drive	n.c
78	SA18	O	HOLD	12, 12	Drive	n.c
79	SA17	O	HOLD	12, 12	Drive	n.c
80	SA16	IO	HOLD	12, 12	Drive	n.c
81	SA15	IO	HOLD	12, 12	Drive	n.c
86	SA14	IO	HOLD	12, 12	Drive	n.c
87	SA13	IO	HOLD	12, 12	Drive	n.c
88	SA12	IO	HOLD	12, 12	Drive	n.c
89	SA11	IO	HOLD	12, 12	Drive	n.c
90	SA10	IO	HOLD	12, 12	Drive	n.c
91	SA9	IO	HOLD	12, 12	Drive	n.c
92	SA8	IO	HOLD	12, 12	Drive	n.c
93	SA7	IO	HOLD	12, 12	Drive	n.c
94	SA6	IO	HOLD	12, 12	Drive	n.c
95	SA5	IO	HOLD	12, 12	Drive	n.c
96	SA4	IO	HOLD	12, 12	Drive	n.c
97	SA3	IO	HOLD	12, 12	Drive	n.c

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
98	SA2	IO	HOLD	12, 12	Drive	n.c
99	SA1	IO	HOLD	12, 12	Drive	n.c
100	SA0	IO	HOLD	12, 12	Drive	n.c
101	SBHE#	IO	HOLD	12, 12	Drive	n.c
102	LA23	IO	HOLD	12, 12	Drive	n.c
103	LA22	IO	HOLD	12, 12	Drive	n.c
104	LA21	IO	HOLD	12, 12	Drive	n.c
105	LA20	IO	HOLD	12, 12	Drive	n.c
106	LA19	IO	HOLD	12, 12	Drive	n.c
107	LA18	IO	HOLD	12, 12	Drive	n.c
108	LA17	IO	HOLD	12, 12	Drive	n.c
109	MEMR#	IO	50KPU	12, 12	Drive(H)	n.c
110	MEMW#	IO	50KPU	12, 12	Drive(H)	n.c
111	SD8	IO	50KPU	12, 12	Input	n.c
112	SD9	IO	50KPU	12, 12	Input	n.c
113	SD10	IO	50KPU	12, 12	Input	n.c
114	SD11	IO	50KPU	12, 12	Input	n.c
185	RESETDRV	O	---	12, 12	Drive(L)	n.c
186	IOCHCK#	I	4.7KPU	-	Input	n.c
187	IRQ9	I	50KPU	-	Input	n.c
188	DRQ2	IO	50KPD	12, 2	Input/Drive	n.c
189	WS0#	I	1KPU	-	Input	n.c
190	SMEMW#	O	---	12, 12	Drive(H)	n.c
191	SMEMR#	O	---	12, 12	Drive(H)	n.c
192	IOW#	IO	50KPU	12, 12	Drive(H)	n.c
193	IOR#	IO	50KPU	12, 12	Drive(H)	n.c
194	DACK3#	O	---	8, 8	Drive(H)	n.c
195	DRQ3	I	50KPD	-	Input	n.c
196	DACK1#	O	---	8, 8	Drive(H)	n.c
197	DRQ1	I	50KPD	-	Input	n.c
198	REF#	IO OD	1.2KPU	12,-	3-State	n.c
199	SCLK	O	---	12, 12	Drive(L)	n.c
204	IRQ7	IO	50KPU	8, 8	Input/Drive	n.c
205	IRQ6	IO	50KPU	12, 2	Input/Drive	n.c
206	IRQ5	IO	50KPU	8, 8	Input/Drive	n.c
207	IRQ4	IO	50KPU	8, 8	Input/Drive	n.c
208	IRQ3	IO	50KPU	8, 8	Input/Drive	n.c
209	DACK2#	O	---	8, 8	Drive(H)	n.c
210	TC	O	---	12, 12	Drive(L)	n.c
211	BALE	O	---	12, 12	Drive(L)	n.c

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
212	OSC	O	---	8, 8	Drive	n.c
213	MEMCS16#	I	1KPU	-	Input	n.c
214	IOCS16#	I	1KPU	-	Input	n.c
215	IRQ10	IO	50KPU	8, 8	Input/Drive	n.c
216	IRQ11	IO	50KPU	8, 8	Input/Drive	n.c
217	IRQ12	IO	50KPU	8, 8	Input/Drive	n.c
218	IRQ15	I	50KPU	-	Input	n.c
219	IRQ14	I	50KPU	-	Input	n.c
220	DACK0#	O	---	8, 8	Drive(H)	n.c
221	DRQ0	I	50KPD	-	Input	n.c
222	DACK5#	O	---	8, 8	Drive(H)	n.c
223	DRQ5	I	50KPD	-	Input	n.c
224	DACK6#	O	---	8, 8	Drive(H)	n.c
225	DRQ6	I	50KPD	-	Input	n.c
226	DACK7#	O	---	8, 8	Drive(H)	n.c
227	DRQ7	I	50KPD	-	Input	n.c
228	MASTER#	I	1KPU	-	Input	n.c
229	SD12	IO	50KPU	12, 12	Input	n.c
230	SD13	IO	50KPU	12, 12	Input	n.c
231	SD14	IO	50KPU	12, 12	Input	n.c
232	SD15	IO	50KPU	12, 12	Input	n.c

Table 13-9 Power Management

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
57	SUSSTAT#	O	---	8, 8	Drive(L)	n.c
58	BATLOW#	I	50KPU	---	Active	n.c
61	BATWRN#	I	50KPU	---	Input	n.c
176	EXTSMI#	I	50KPU	---	Input	n.c
180	SRBTN#	I	50KPU	---	Active	n.c
115	SMOUT3	O	---	8, 8	Drive(H)	n.c
116	SMOUT1	O	---	8, 8	Drive(L)	n.c
233	SMOUT2	O	---	8, 8	Drive(L)	n.c
234	SMOUT0	O	---	8, 8	Drive(L)	n.c

(Note) The CARD-486HB is not resumed if the BATLOW# is kept active.

Table 13-10 Others

Pin No.	Signal Name	Type	Term	Drive I_{OL},I_{OH} (mA)	Suspend	Termination of unused pins
62	POWERGOOD	I	---	---	Active	Can not be unused
63	SPKOUT	O	---	4, 4	Drive(L)	n.c
181	WDTIM#	O	---	4, 4	Drive	n.c
64	FLOAT#	I	25KPU	-	Active	n.c
65	ROMCE0#	IO	---	4, 4	Drive(H)	n.c

(Note 1) Pins FLOAT# and ROMCE0# are used to update the CARD-486HB's flash ROM using the ROM writer. These pins must be disconnected during normal operations.
(Note 2) The CARD-486HB is reset when the POWERGOOD is made inactive.

Reserved pins (pins 20, 35, 66, 138, 152, 179, 183, and 184)

All of these reserved pins must be disconnected as they will be used by other functions in the future.

14. Mounting and Fixture

14.1 Mounting Procedure

Figure 14-1 shows a dimensional drawing for socket mounting, Figure 14-2 shows a dimensional drawing of board holes, and Figure 14-3 shows the pin number location.

Card socket

- Use a 1.6-mm or less thickness board to mount the card socket.
- Use two M2.5x8 hex nuts to fix the card socket.

Card fixture

If the CARD-486HB is not fixed well, it may be removed from the socket due to the vibration and mechanical shock. We recommend to use the SEK6675P01 card stopper or equivalent which can fix the card to the socket and provide the enough heat radiation capability.
The card stopper can be mounted by using the same nuts as the socket fixture nuts. When using the stopper, use the M2.5x14 setscrews and fix the socket first.

To fix the card, refer to the following figures. Keep the distance (A) between the CARD-486HB and Card holder within 0.5 ±0.2 mm.

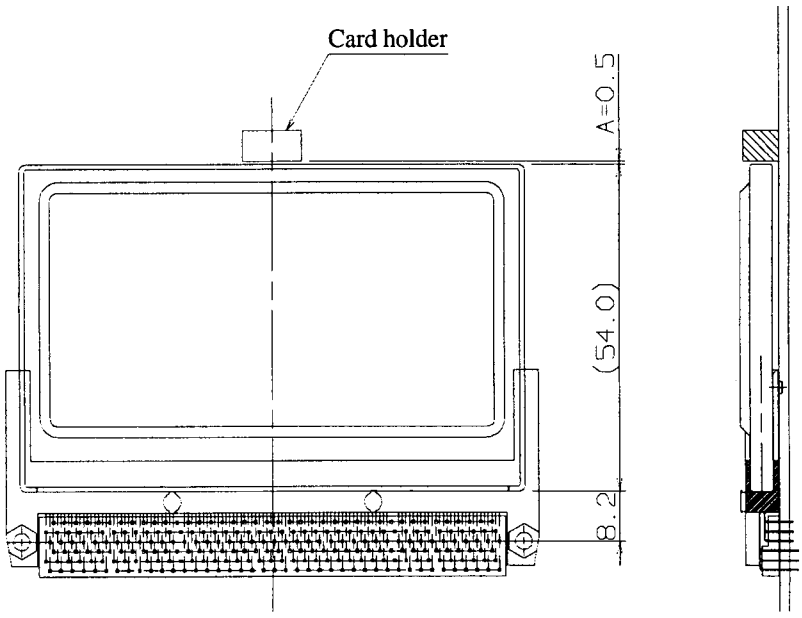


Figure 14-1 Dimensional Drawing for Card holder

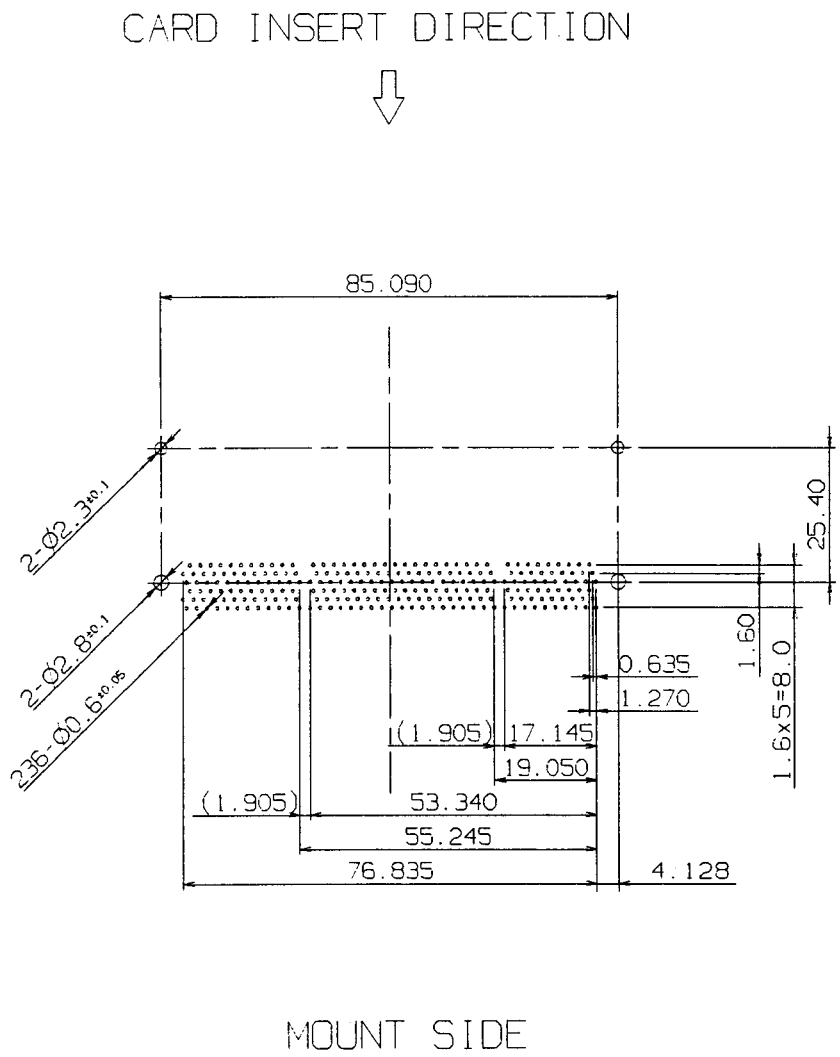


Figure 14-2 Dimensional Drawing of Board Holes

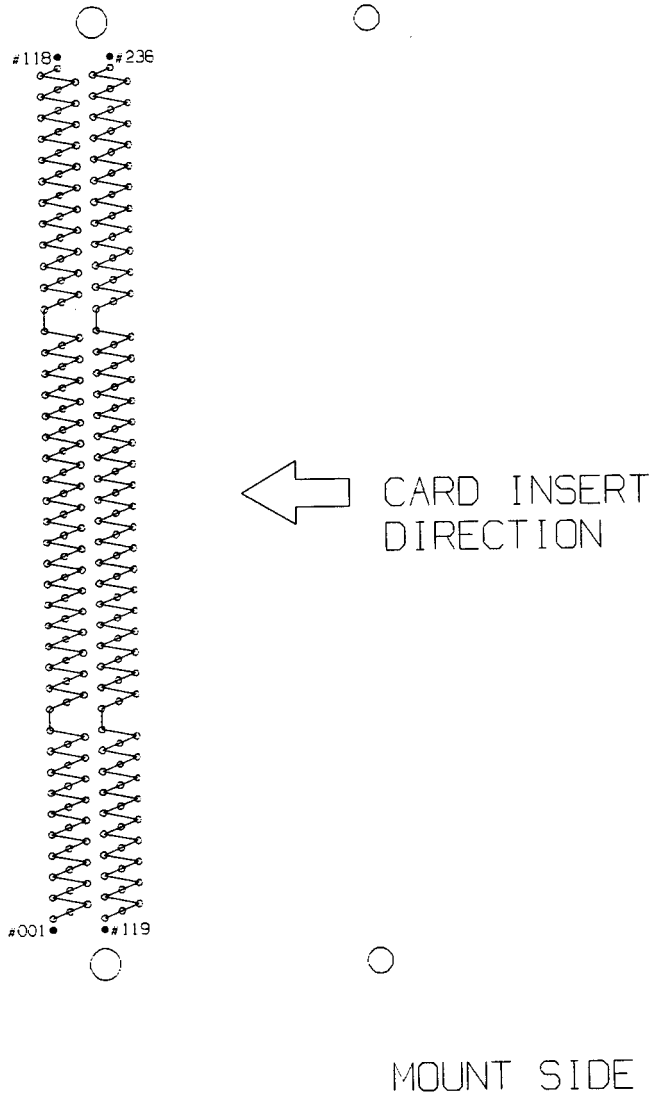


Figure 14-3 Pin Number Mounting Location Chart

14.2 Card Socket and Card Stopper

Two types of card sockets are provided. They are the card socket having an ejector, and the card socket having no ejector (see Table 14-1).

Table 14-1 List of Card Sockets and Stoppers

Model	Specifications
SEK6669P$_{01}$	236-pin socket without card ejector
SEK6669P$_{02}$	236-pin socket with a card ejector
SEK6675P$_{01}$	Card stopper
SEK6676P$_{01}$	Card stopper having the heat radiation capability (Note 1)
SEK6677P$_{01}$ SEK6678P$_{01}$	Stand-off card socket (Note 2)

(Note 1) SEK6676P01 is of higher radiation performance than SEK6675PO1.

(Note 2) The stand-off socket consists of two socket parts: the SEK6676P$_{01}$ part which connects to the board, and the SEK6678P$_{01}$ part to fix the CARD-PC. The heat radiation stopper which can be used together with the stand-off card socket is not provided yet. Consult to Seiko Epson if such stopper is required.

These sockets can be inserted and pulled off 1,000 times. Though the socket on the CARD-PC side is supposed to be hardly inserted and pulled off 1,000 times, the one on the receiving side may be inserted and pulled out more than 1,000 times when the BIOS is modified by the ROM writer or when acceptance inspections are conducted using the card checker. However, insert and pull out the socket up to 1,000 times to protect the CARD-PC. When the ROM writer is inserted and pulled out more than 1,000 times, replace the socket.

14.3 Cautions on Mounting CARD-486HB

When designing how the system with CARD-486HB is mounted, take influences on and from peripheral devices into account.
The working temperature specification (atmospheric temperature (Ta) range and case temperature (Tc) range) of the CARD-486HB is as shown in the table below. Any one temperature must be satisfied. The Ta applies when the supply voltage is typ.
The case temperature (Tc) measuring point is shown in Figure 14-5.

Table 14.21 Working Temperature Range of CARD-486HB

Model Name	Working Temperature Range
SCE8643600, SCE8643603	Ta=0 to 55°C or Tc=0 to 70°C
SCE8643605	Ta=0 to 50°C or Tc=0 to 70°C
SCE8640600, SCE8640603	Ta=0 to 65°C or Tc=0 to 70°C

(Note 1) Ta is applicable when the supply voltage is typ.
(Note 2) For the working temperature of the CARD-PCs, Ta or Tc should be satisfied. The both temperatures need not be satisfied at the same time.
(Note 3) During suspended time, the working temperature (Ta) range is 0 to 70°C and is common to all models.

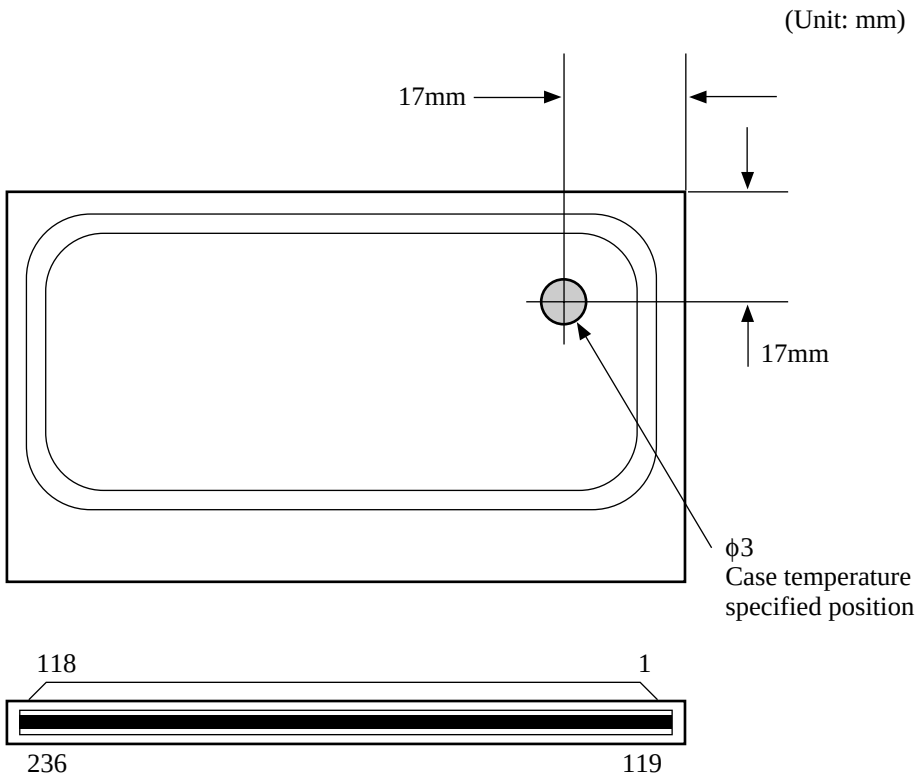


Figure 14-5 Housing Surface Temperature Measuring Point

(Unit: mm)

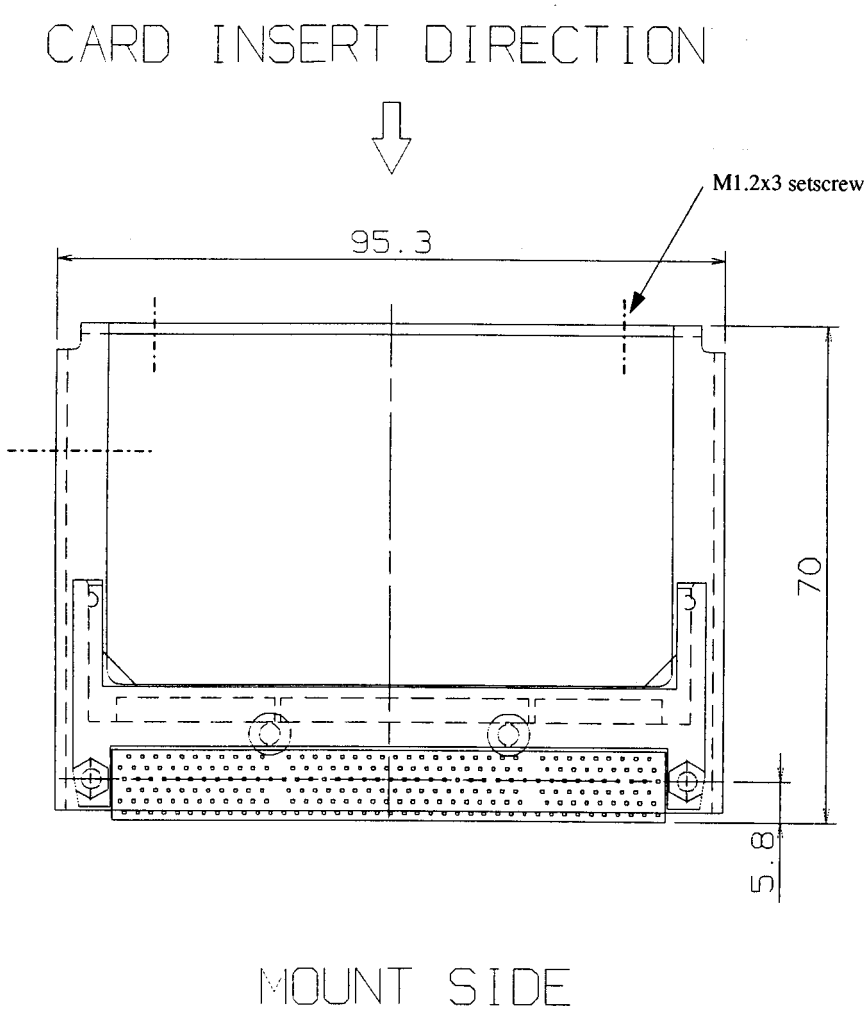


Figure 14-6 Dimensions when Card Stopper (SEK6676P01) is mounted

Appendix 1. Controls for Different LCD Types

This manual classifies the LCDs into groups by their general display systems. This section outlines how to control the LCDs by their types. For the full information about the LCD connection to the CARD-486HB, refer to the separate "CARD-PC Technical Information" bulletin. As it is updated periodically, consult to us for the latest issue.

1.1 STN LCDs

The panels of the improved STN quality are sometimes called the NTN, FTN and DSTN panels. However, all of them have the same interface as the STN panel and this manual calls them as "STN panels."

There are two types of STN LCDs: the monochrome STN LCDs and color STN LCDs. In most cases, the color LCD consists of multiple RGB color filters attached to the monochrome STN LCD. the color STN LCD for VGA display has the pixels three times larger than the monochrome STN LCD.

As an eight-bit monochrome STN LCD sends the pixels of data width in a single clock, the data of LCD's eight pixels is sent in a single clock. While an eight-bit color STN LCD can send only "8/3" pixels (total of 8 bits for RGBRGB data) in a single clock. As the data layout is not compatible between the monochrome and color STN LCDs, the color STN signal output cannot be displayed correctly on the monochrome STN LCD. Also, the monochrome STN signal output cannot be displayed correctly on the color
STN LCD.

In the operating principle, the STN LCDs require the positive or negative driving power. Some LCDs which have a small number of pixels (for calculator display and others) can be driven by the 5V or 12V power. However, the STN LCDs for the PCs generally require +20 to +40V or -15 to -35V driving power. Also, many LCDs require the power on/off sequence between the drive power supply and the logic signal circuits. Therefore, a separate power on/off control circuit may be required.

In addition, the STN LCDs can be classified into several groups by the data width which can be transmitted at a single time. The number of bits of this data transmission width differs from the number of bits used for color TFT LCDs.

1.1.1 STN Single-Scan LCDs

This type of LCDs are driven so that the screen display data is transmitted for the data bus width of each line from left to right. The data width can be 4 bits, 8 bits and others. Generally, the left section screen data is used as the data bus MSB (see Table A1-1).

Table A1-1 Relationship between 8-bit Single Scan STN data and screen for VGA Display

→	← 8-bit data for each width (Data bus width)						
1.1	1.2	1.3	1.4	1.5	- - - - - - - - - - - -	1.79	1.80
2.1	2.2	2.3	2.4	2.5	- - - - - - - - - - - -	2.79	2.80
3.1	3.2	3.3	3.4	3.5	- - - - - - - - - - - -	3.79	3.80
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
479.1	479.2	479.3	479.4	479.5	- - - - - - - - - - - -	479.79	479.80
480.1	480.2	480.3	480.4	480.5	- - - - - - - - - - - -	480.79	480.80

Data transmission sequence: 1.1/1.2/1.3/.../1.79/1.80/2.1/1.2/.../480.79/480.80

The external clocks must be entered for data transmission (called the “dot clocks”). The FPDOTCLK of the CARD-486HB is the dot clock. The sync signal (FPVTIM) is required to indicate the top end of the screen, and the sync signal (FPHTIM) is required to indicate the left end of the screen. Therefore, three lines of signal inputs are required except in addition to the data.

1.1.2 STN Dual-Scan Monochrome LCDs

This type of LCDs has two upper and lower areas of the screen, and the screen display data is transmitted for each line separately. The data bus width can be 4 bits by 2, 8 bits by 2, and others. Similar to the STN single scan data, the data configuration is generally the MSB for the left and the LSB for the right (see Table A1-2).

Table A1-2 Relationship between 4bitsx2 Dual Scan STN data and screen for VGA Display

→	← 4-bit data for each width (Data bus width)					
U1.1	U1.2	U1.3	U1.4	- - - - - - -	U1.159	U1.160
U2.1	U2.2	U2.3	U2.4	- - - - - - -	U2.159	U2.160
⋮	⋮	⋮	⋮	⋮	⋮	⋮
U239.1	U239.2	U239.3	U239.4	- - - - - - -	U239.159	U239.160
U240.1	U240.2	U240.3	U240.4	- - - - - - -	U240.159	U240.160
L1.1	L1.2	L1.3	L1.4	- - - - - - -	L1.159	L1.160
L2.1	L2.2	L2.3	L2.4	- - - - - - -	L2.159	L2.160
⋮	⋮	⋮	⋮	⋮	⋮	⋮
L239.1	L239.2	L239.3	L239.4	- - - - - - -	L239.159	L239.160
L240.1	L240.2	L240.3	L240.4	- - - - - - -	L240.159	L240.160

The following data sets are transmitted simultaneously:

Upper screen data: U1.1/U1.2/ . . . /U1.159/U1.160/U2.1/U2.2/ . . . /U240.159/U240.160
Lower screen data: L1.1/L1.2/ . . . /L1.159/L1.160/L2.1/L2.2/ . . . /L240.159/L240.160

Some LCDs require a lower-screen display position start signal input or the clocks having different timing for upper and lower screen sections. Except for these special products, most of the dual-scan STN LCDs are the same as the single-scan STN LCDs.
Therefore, three signal lines are required in addition to the data signals. These three are the dot clock (FPDOTCLK), sync signal (FPVTIM) indicating the screen top end, and the sync signal (FPHTIM) indicating the screen left end.

1.2 TFT LCDs

1.2.1 TFT having a timing of screen display data by counting FPDOTCLKs

The CARD-486HB does not support this type of TFT LCDs.

Two types of such TFT LCDs are commonly used. The TFT LCD which displays the screen data in the timing of 144 FPDOTCLKs after the fall of FPHTIM (this type is called the “C144 type” in this manual), and the TFT LCD which displays the screen data in the timing of 104 FPDOTCLKs after the rise of FPHTIM (this type is called the “C104 type” in this manual).

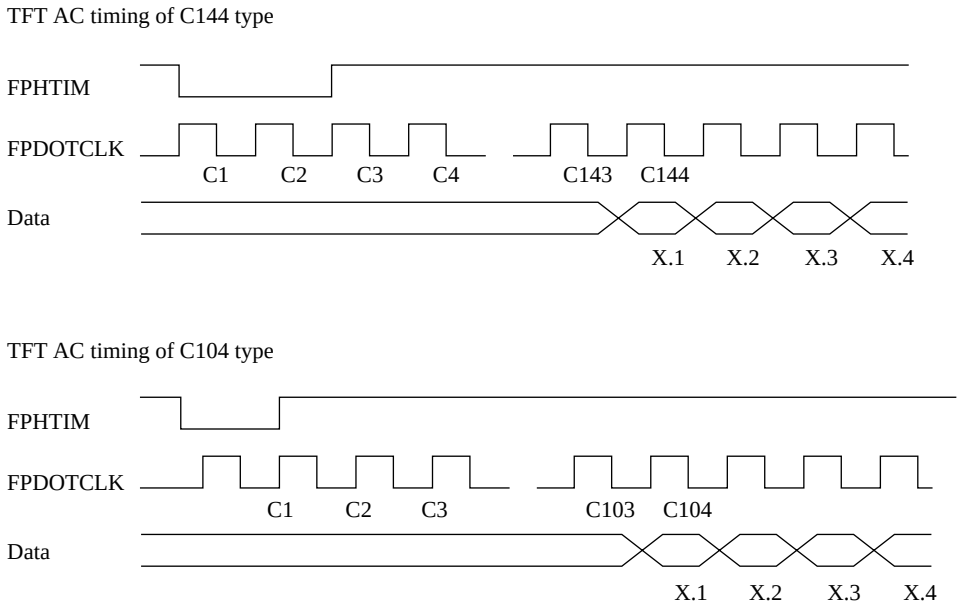


Figure A1-1 TFT AC Timing Chart

1.2.2 TFT using sync signals in the timing of screen display data

The timing of screen display data is determined by the externally input sync signals (DE) for this type of TFT LCDs (it is called the “DE type” in this manual). Some models use the same sync signal to determine the screen top and bottom display positions. The CARD-486HB may display the data if its parameters are modified. For details, refer to the “CARD-PC Technical Reference.”

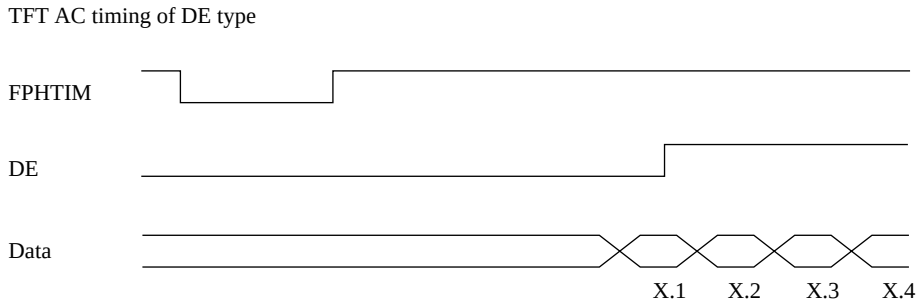


Figure 1-2 DE Type TFT AC Timing Chart

1.2.3 TFT supporting the selection of the above two functions

This type of TFT LCDs can switch the display position setup terminal to use either the internal fixed values or external sync signals. This type of TFT LCDs are most commonly used on the market. The CARD-486HB uses the external sync signals for its control.

The maximum number of display colors of a TFT LCD is classified into 512 colors (3 bits for each color), 4096 colors (4 bits for each color), 260,000 colors (6 bits for each color) and others. The CARD-486HB can be connected to all of these color TFT LCDs.

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First issue February,1998
Printed in Japan Ⓗ A