EPSON

CARDPRESSO

HARDWARE MANUAL

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1.Basic Specification

The CARDPRESSO is an AT add-on half-size CARD using a CARD-PC, equipped with two PCMCIA sockets and a PC/104 expansion bus connector, thus allowing easy function expansion.

1.1.CARD-PC

Can be selected from the CARD-486HB series and CARD-586 series. For detailed specifications, refer to the CARD-PC Hardware Manual. The CARDPRESSO does not work as PC option board. The CARD-PC must be installed on the CARDPRESSO.

Note
CARDPRESSO does not have Power Management features.
It can't be used for the product with the combination of CARDPRESSO and CARD-686.

1.2.PCMCIA Controller

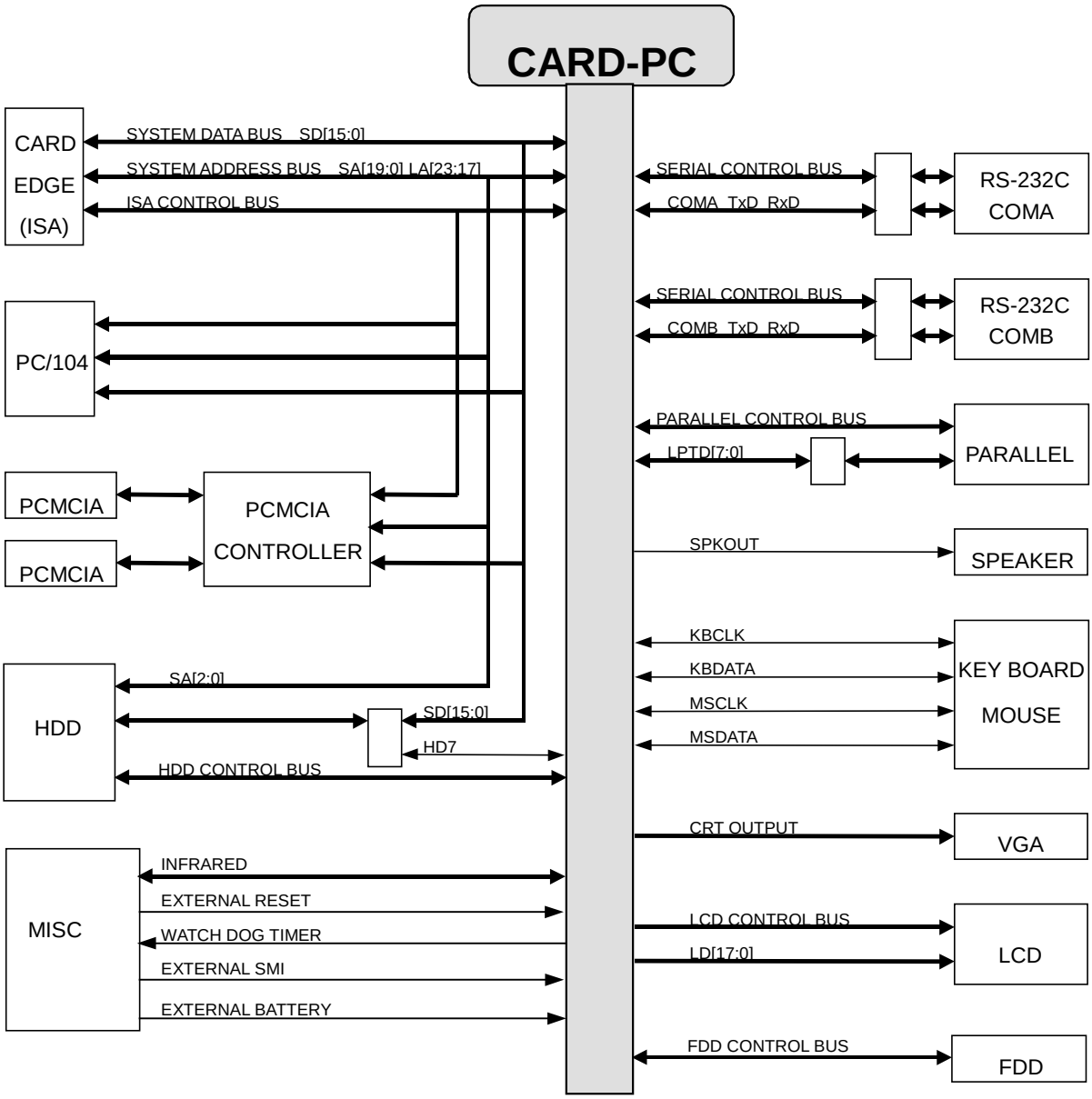
CL_PD6720(CIRRUS LOGIC)

1.3.Interfaces

Interface	Connector	Description
PCMCIA I/F	JEIDA 4.2,PCMCIA 2.1	2slot(TypeⅣ、TypeⅡ)
SERIAL I/F	9pin D-Sub 10pin header(2.54mmpitch)	2ports RS-232C
PARALLEL I/F	26pin header(2.54mmpitch)	Centronics compliant 8-bit parallel PS/2-style bi-directional parallel support EPP
CRT I/F	15pinD-Sub	Analog RGB VGA(*)
LCD I/F	50pin header(1.27mmpitch)	FTN MONO(*) TFT COLOR(*) STN MONO/COLOR(*)
KEYBOARD/ MOUSE I/F	Mini-Din type 6pin header(2.54mmpitch)	PS/2 keyboard (to connect a PS/2 mouse, use a keyboard/mouse branching connector)
PC/104 I/F	104pin stackthrough connector	16-bit bus
IDE I/F	40pin header(2.54mmpitch)	3.5“HDD IDE HDD(up to 8.4GB) support
FDD I/F	34pin header(2.54mmpitch)	3.5" 1.44 MB, 5.25" 1.2 MB FDD(*)
MISC I/F	16pin header(2.54mmpitch)	External Reset Watchdog Timer Infrared Communication External Backup Power Input
POWER SUPPLY I/F	5pin header Backup Battery	±5V、±12V、GND 3V Lithium Battery

(*) Not Support CARD-486HBL

1.4.Block Diagram



2.Interface Connector Terminal Assignments and Functions

This chapter describes the interface connector terminal assignments and functions for the CARDPRESSO. The terminals are classified as follows:

I:	Input terminal
O:	Output terminal
O OD:	Output terminal open drain output
I/O:	Input/output terminal
I/O OD:	Input/output terminal open drain input/output
AO:	Analog output terminal
Power:	Power and ground terminals

2.1.CARD-PC Interface

There is a 236-pin connector for the CARD-PC.

CN1 : CARD-PC Connector			
Pin	Signal Name	Type	Function
1	GND	Power	
2	GND	Power	
3	RESERVE		
4	LD6	I	LCD data input
5	LD4	I	LCD data input
6	LD2	I	LCD data input
7	LD0	I	LCD data input
8	FPVTIM	I	Flat Panel Vertical Timing signal
9	FPAC	I	Flat Panel AC signal
10	FPVCCON	I	Flat Panel Vcc Control signal
11	LD9	I	LCD data input
12	LD11	I	LCD data input
13	LD13	I	LCD data input
14	LD15	I	LCD data input
15	BLUE	AI	VGA CRT blue analog input
16	GREEN	AI	VGA CRT green analog input
17	RED	AI	VGA CRT red analog input
18	VSYNC	I	VGA CRT Vertical Synchronization signal
19	LD17	I	LCD data input
20	RESERVE		
21	MSDATA	I/O OD	PS/2 style mouse data line
22	KBDATA	I/O OD	PS/2 style keyboard data line
23	FDWP#	O	FDD Write Protect signal
24	FDINDEX#	I	FDD Index pulse input
25	FDTRK0#	O	FDD Track0 signal
26	FDWD#	I	FDD Write Data input
27	P5V	Power	+5VDC
28	P5V	Power	+5VDC
29	P3V	Power	+3.3VDC
30	P3V	Power	+3.3VDC
31	FDDS2#	I	FDD Drive Select 2 input
32	FDMT2#	I	FDD Motor select 2 input
33	FDSIDE	I	FDD head select input
34	FDDIR	I	FDD head actuator direction input
35	RESERVE		
36	COMBDTR#	I	COM B Data Terminal Ready
37	COMBCTS#	O	COM B Clear To Send
38	COMBRTS#	I	COM B Request To Send
39	COMBDSR#	O	COM B Data Set Ready
40	COMADTR#	I	COM A Data Terminal Ready
41	COMACTS#	O	COM A Clear To Send
42	COMARTS#	I	COM A Request To Send
43	COMADSR#	O	COM A Data Set Ready
44	IRRXD	O	IrDA-SIR Receive Data
45	LPTSTROBE#	I	Line Printer Strobe signal
46	LPTD0	I/O	Line Printer bi-directional data signal
47	LPTACK#	O	Line Printer Acknowledge signal
48	LPTPE	O	Line Printer Paper Empty signal
49	LPTD1	I/O	Line Printer bi-directional data signal
50	LPTD2	I/O	Line Printer bi-directional data signal

51	LPTD3	I/O	Line Printer bi-directional data signal
52	LPTD5	I/O	Line Printer bi-directional data signal
53	LPTD7	I/O	Line Printer bi-directional data signal
54	HDDIR	I	HDD external buffer direction control signal
55	HDENL#	I	HDD external buffer (low-byte) enable signal
56	HDCS0#	I	HDD controller select 0 signal (1F0H~1F7H)
57	RESERVE		
58	RESERVE		
59	GND	Power	
60	GND	Power	
61	RESERVE		
62	POWERGOOD	O	Power Good status input signal
63	SPKOUT	I	Digital signal output to drive an external speaker
64	RESERVE		
65	RESERVE		
66	RESERVE		
67	SD7	I/O	System Data bus
68	SD6	I/O	System Data bus
69	SD5	I/O	System Data bus
70	SD4	I/O	System Data bus
71	SD3	I/O	System Data bus
72	SD2	I/O	System Data bus
73	SD1	I/O	System Data bus
74	SD0	I/O	System Data bus
75	IOCHRDY	I/O OD	I/O Channel Ready signal for bus cycle termination
76	AEN	I	Address Enable signal, indicate DMA cycle or refresh cycle
77	SA19	I/O	System Address bus
78	SA18	I/O	System Address bus
79	SA17	I/O	System Address bus
80	SA16	I/O	System Address bus
81	SA15	I/O	System Address bus
82	P3V	Power	+3.3VDC
83	P3V	Power	+3.3VDC
84	P5V	Power	+5VDC
85	P5V	Power	+5VDC
86	SA14	I/O	System Address bus
87	SA13	I/O	System Address bus
88	SA12	I/O	System Address bus
89	SA11	I/O	System Address bus
90	SA10	I/O	System Address bus
91	SA9	I/O	System Address bus
92	SA8	I/O	System Address bus
93	SA7	I/O	System Address bus
94	SA6	I/O	System Address bus
95	SA5	I/O	System Address bus
96	SA4	I/O	System Address bus
97	SA3	I/O	System Address bus
98	SA2	I/O	System Address bus
99	SA1	I/O	System Address bus
100	SA0	I/O	System Address bus
101	SBHE#	I/O	System Byte High Enable signal
102	LA23	I/O	Latchable Address bus
103	LA22	I/O	Latchable Address bus
104	LA21	I/O	Latchable Address bus
105	LA20	I/O	Latchable Address bus
106	LA19	I/O	Latchable Address bus
107	LA18	I/O	Latchable Address bus
108	LA17	I/O	Latchable Address bus
109	MEMR#	I/O	Memory Read signal
110	MEMW#	I/O	Memory Write signal
111	SD8	I/O	System Data bus
112	SD9	I/O	System Data bus
113	SD10	I/O	System Data bus
114	SD11	I/O	System Data bus
115	SMOUT3	I	System power Management Output signal
116	SMOUT1	I	System power Management Output signal
117	GND	Power	
118	GND	Power	
119	GND	Power	
120	GND	Power	

121	FPDOTCLK	I	Flat Panel Dot Clock signal
122	LD7	I	LCD data input
123	LD5	I	LCD data input
124	LD3	I	LCD data input
125	LD1	I	LCD data input
126	FPHTIM	I	Flat Panel Horizontal Timing signal
127	LD8	I	LCD data input
128	FPVEEON	I	Flat Panel Vee control signal
129	BLANK#	I	Flat Panel Blank signal
130	LD10	I	LCD data input
131	LD12	I	LCD data input
132	LD14	I	LCD data input
133	BRTN	O	Blue return signal
134	GRTN	O	Green return signal
135	RRTN	O	Red return signal
136	HSYNC	I	VGA CRT Horizontal Synchronization signal
137	LD16	I	LCD data input
138	RESERVE		
139	MSCLK	I/O OD	PS/2 style mouse clock line
140	KBCLK	I/O OD	PS/2 style keyboard clock line
141	FDRD#	O	FDD Read Data signal
142	FDDCHG#	O	FDD Disk Change signal
143	FDWE#	I	FDD Write Enable input
144	FDHIDEN	I	FDD High Density control input
145	P5V	Power	+5VDC
146	P5V	Power	+5VDC
147	P3V	Power	+3.3VDC
148	P3V	Power	+3.3VDC
149	FDDS1#	I	FDD Drive Select 1 input
150	FDMT1#	I	FDD Motor Select 1 input
151	FDSTEP#	I	FDD Stepping motor drive signal input
152	RESERVE		
153	DARXD	O	Digital ASK Receive Data
154	COMBRI#	O	COM B Ring Indicator signal
155	COMBRXD	O	COM B Receive Data
156	COMBTXD	I	COM B Transmit Data
157	COMBDCD#	O	COM B Data Carrier Detect
158	COMARI#	O	COM A Ring Indicator signal
159	COMARXD	O	COM A Receive Data
160	COMATXD	I	COM A Transmit Data
161	COMADCD#	O	COM A Data Carrier Detect
162	IRTXD	I	Ir Transmit Data
163	LPTAFD#	I	Line Printer Auto Feed signal
164	LPTERROR#	O	Line Printer Error signal
165	LPTBUSY#	O	Line Printer Busy signal
166	LPTSLCT	O	Line Printer Selected signal
167	LPTINIT#	I	Line Printer Initialize input
168	LPTSLTCIN#	I	Line Printer Select In signal
169	LPTD4	I/O	Line Printer data bus
170	LPTD6	I/O	Line Printer data bus
171	LPTDIR	I	Line Printer external data buffer direction control signal
172	HD7	I/O	HDD data bit 7
173	HDENH#	I	HDD external buffer (high-byte) enable signal
174	HDCS1#	I	HDD controller select 1 signal (3F6H~3F7H)
175	VBAK	Power	Real-Time-Clock back up power
176	EXTSMI#	O	External System Management Interrupt output, generate SMI#
177	GND	Power	
178	GND	Power	
179	RESERVE		
180	RESERVE		
181	WDOUT#	I	Watch Dog Timer Out signal
182	PGM	O	ROM write power supply
183	RESERVE		
184	RESERVE		
185	RESETDRV	I	Reset Drive signal
186	IOCHCK#	O	I/O Channel Check, indicate parity error on ISA bus
187	IRQ9	O	Interrupt Request signal
188	DRQ2	O	DMA Request signal
189	WS0#	I/O OD	Zero wait-state request signal
190	SMEMW#	I	System Memory Write signal (0~FFFFFH)

191	SMEMR#	I	System Memory Read signal (0~FFFFFH)
192	IOW#	I/O	I/O Write signal
193	IOR#	I/O	I/O Read signal
194	DACK3#	I	DMA Acknowledge signal
195	DRQ3	O	DMA Request signal
196	DACK1#	I	DMA Acknowledge signal
197	DRQ1	O	DMA Request signal
198	REF#	I/O OD	Refresh cycle signal
199	SCLK	I	System clock input (8MHz, 50% duty cycle)
200	P3V	Power	+3.3VDC
201	P3V	Power	+3.3VDC
202	P5V	Power	+5VDC
203	P5V	Power	+5VDC
204	IRQ7	O	Interrupt Request signal
205	IRQ6	O	Interrupt Request signal
206	IRQ5	O	Interrupt Request signal
207	IRQ4	O	Interrupt Request signal
208	IRQ3	O	Interrupt Request signal
209	DACK2#	I	DMA Acknowledge signal
210	TC	I	DMA Terminal Count signal
211	BALE	I	Buffered Address Latch Enable signal
212	OSC	I	14.31818MHz clock output (50% duty cycle)
213	MEMCS16#	I/O OD	Memory Chip Select 16, indicate 16-bit capability
214	IOCS16#	I/O OD	I/O Chip Select 16, indicate 16-bit capability
215	IRQ10	O	Interrupt Request signal
216	IRQ11	O	Interrupt Request signal
217	IRQ12	O	Interrupt Request signal
218	IRQ15	O	Interrupt Request signal
219	IRQ14	O	Interrupt Request signal
220	DACK0#	I	DMA Acknowledge signal
221	DRQ0	O	DMA Request signal
222	DACK5#	I	DMA Acknowledge signal
223	DRQ5	O	DMA Request signal
224	DACK6#	I	DMA Acknowledge signal
225	DRQ6	O	DMA Request signal
226	DACK7#	I	DMA Acknowledge signal
227	DRQ7	O	DMA Request signal
228	MASTER#	O	External bus-master request signal
229	SD12	I/O	System Data bus
230	SD13	I/O	System Data bus
231	SD14	I/O	System Data bus
232	SD15	I/O	System Data bus
233	SMOUT2	I	System power Management Output signal
234	SMOUT0	I	System power Management Output signal
235	GND	Power	
236	GND	Power	

For details refer to the CARD-PC Hardware Manual.

2.2.PCMCIA Interface

The CARDPRESSO is equipped with two sockets (Socket 0, Socket 1) complying with the PCMCIA 2.1 standard. When both sockets are used simultaneously, Socket 1 can be used up to Type II.

CN2 : Memory CARD Interface				CN2 : I/O & Memory CARD Interface			
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	GND	Power		1	GND	Power	
2	D3	I/O	Data bit	2	D3	I/O	Data bit
3	D4	I/O	Data bit	3	D4	I/O	Data bit
4	D5	I/O	Data bit	4	D5	I/O	Data bit
5	D6	I/O	Data bit	5	D6	I/O	Data bit
6	D7	I/O	Data bit	6	D7	I/O	Data bit
7	CE1#	O	CARD Enable	7	CE1#	O	CARD Enable
8	A10	O	Address bit	8	A10	O	Address bit
9	OE#	O	Output Enable	9	OE#	O	Output Enable
10	A11	O	Address bit	10	A11	O	Address bit
11	A9	O	Address bit	11	A9	O	Address bit
12	A8	O	Address bit	12	A8	O	Address bit
13	A13	O	Address bit	13	A13	O	Address bit
14	A14	O	Address bit	14	A14	O	Address bit
15	WE#	O	Write Enable	15	WE#	O	Write Enable
16	READY	I	Ready	16	IREQ#	I	Interrupt Request
17	VCC	Power	Supply Voltage	17	VCC	Power	Supply Voltage
18	VPP	Power	Program Voltage	18	VPP	Power	Program Voltage
19	A16	O	Address bit	19	A16	O	Address bit
20	A15	O	Address bit	20	A15	O	Address bit
21	A12	O	Address bit	21	A12	O	Address bit
22	A7	O	Address bit	22	A7	O	Address bit
23	A6	O	Address bit	23	A6	O	Address bit
24	A5	O	Address bit	24	A5	O	Address bit
25	A4	O	Address bit	25	A4	O	Address bit
26	A3	O	Address bit	26	A3	O	Address bit
27	A2	O	Address bit	27	A2	O	Address bit
28	A1	O	Address bit	28	A1	O	Address bit
29	A0	O	Address bit	29	A0	O	Address bit
30	D0	I/O	Data bit	30	D0	I/O	Data bit
31	D1	I/O	Data bit	31	D1	I/O	Data bit
32	D2	I/O	Data bit	32	D2	I/O	Data bit
33	WP	I	Write Protect	33	IOIS16#	I	I/O port is 16-bit
34	GND	Power		34	GND	Power	
35	GND	Power		35	GND	Power	
36	CD1#	I	CARD Detect	36	CD1#	I	CARD Detect
37	D11	I/O	Data bit	37	D11	I/O	Data bit
38	D12	I/O	Data bit	38	D12	I/O	Data bit
39	D13	I/O	Data bit	39	D13	I/O	Data bit
40	D14	I/O	Data bit	40	D14	I/O	Data bit
41	D15	I/O	Data bit	41	D15	I/O	Data bit
42	CE2#	O	CARD Enable	42	CE2#	O	CARD Enable
43	VS1#	I	Voltage Sense	43	VS1#	I	Voltage Sense
44	RESERVED			44	IORD#	O	I/O Read
45	RESERVED			45	IOWR#	O	I/O Write
46	A17	O	Address bit	46	A17	O	Address bit
47	A18	O	Address bit	47	A18	O	Address bit
48	A19	O	Address bit	48	A19	O	Address bit
49	A20	O	Address bit	49	A20	O	Address bit
50	A21	O	Address bit	50	A21	O	Address bit
51	VCC	Power	Supply Voltage	51	VCC	Power	Supply Voltage
52	VPP	Power	Program Voltage	52	VPP	Power	Program Voltage
53	A22	O	Address bit	53	A22	O	Address bit
54	A23	O	Address bit	54	A23	O	Address bit
55	A24	O	Address bit	55	A24	O	Address bit
56	A25	O	Address bit	56	A25	O	Address bit
57	VS2#	I	Voltage Sense	57	VS2#	I	Voltage Sense
58	RESET	O	CARD Reset	58	RESET	O	CARD Reset
59	WAIT#	I	Extend bus cycle	59	WAIT#	I	Extend bus cycle
60	RESERVED			60	INPACK#	I	Input acknowledge
61	REG#	O	Register select	61	REG#	O	Register select
62	BVD2	I	Battery Voltage	62	SPKR#	I	Digital audio wave form
63	BVD1	I	Battery Voltage	63	STSCHG#	I	CARD status changed
64	D8	I/O	Data bit	64	D8	I/O	Data bit
65	D9	I/O	Data bit	65	D9	I/O	Data bit
66	D10	I/O	Data bit	66	D10	I/O	Data bit
67	CD2#	I	CARD Detect	67	CD2#	I	CARD Detect
68	GND	Power		68	GND	Power	

2.3.PCMCIA Interface (ATA-MODE)

The CARDPRESSO uses a CL_PD6720 (Cirrus Logic) as PCMCIA controller, and ATA interface settings can be made.

CN2 : PCMCIA-ATA mode Interface							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	GND	Power		35	GND	Power	
2	D3	I/O	Data bit	36	CD1#	I	CARD Detect
3	D4	I/O	Data bit	37	D11	I/O	Data bit
4	D5	I/O	Data bit	38	D12	I/O	Data bit
5	D6	I/O	Data bit	39	D13	I/O	Data bit
6	D7	I/O	Data bit	40	D14	I/O	Data bit
7	CE1#	O	CARD Enable	41	D15	I/O	Data bit
8	(A10)	O	optional	42	CE2#	O	CARD Enable
9	OE#	O	Output Enable	43	RESERVED		
10	(A11)	O	optional	44	IORD#	O	I/O Read
11	A9	O	Address bit	45	IOWR#	O	I/O Write
12	A8	O	Address bit	46	(A17)	O	optional
13	(A13)	O	optional	47	(A18)	O	optional
14	(A14)	O	optional	48	(A19)	O	optional
15	WE#	O	Write Enable	49	(A20)	O	optional
16	READY	I	Ready	50	(A21)	O	optional
17	VCC	Power	Supply Voltage	51	VCC	Power	Supply Voltage
18	VPP	Power	Vpp or NC	52	VPP	Power	VPP or NC
19	(A16)	O	optional	53	(A22)	O	optional
20	(A15)	O	optional	54	(A23)	O	optional
21	(A12)	O	optional	55	(A24)	O	optional
22	A7	O	Address bit	56	(A25)	O	optional
23	A6	O	Address bit	57	NC		
24	A5	O	Address bit	58	RESET	O	CARD Reset
25	A4	O	Address bit	59	WAIT#	I	Extend bus cycle
26	A3	O	Address bit	60	INPACK#	I	Input acknowledge
27	A2	O	Address bit	61	REG#	O	Register select
28	A1	O	Address bit	62	"H"	I	
29	A0	O	Address bit	63	"H"	I	
30	D0	I/O	Data bit	64	D8	I/O	Data bit
31	D1	I/O	Data bit	65	D9	I/O	Data bit
32	D2	I/O	Data bit	66	D10	I/O	Data bit
33	IOIS16#	I	I/O is 16-bit	67	CD2#	I	CARD Detect
34	GND	Power		68	GND	Power	

2.4.Serial Interface

The CARDPRESSO is equipped with two serial interfaces complying with the RS-232C standard. CN3 is a 9-pin D-sub connector and CN4 a 10-pin header type connector.

CN3 : Serial(COM A) Connector				CN4 : Serial(COM B) Connector			
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	DCD#_A	I	Data Carrier Detect	1	DCD#_B	I	Data Carrier Detect
2	RXD_A	I	Receive Data	2	DSR#_B	I	Data Set Ready
3	TXD_A	O	Transmit Data	3	RXD_B	I	Receive Data
4	DTR#_A	O	Data Terminal Ready	4	RTS#_B	O	Request To Send
5	GND	Power		5	TXD_B	O	Transmit Data
6	DSR#_A	I	Data Set Ready	6	CTS#_B	I	Clear To Send
7	RTS#_A	O	Request To Send	7	DTR#_B	O	Data Terminal Ready
8	CTS#_A	I	Clear To Send	8	RI#_B	I	Ring Indicator
9	RI#_A	I	Ring Indicator	9	GND	Power	
				10	NC		

For details refer to the CARD-PC Hardware Manual.

2.5.Parallel Interface

The CARDPRESSO is equipped with a Centronics-compliant 8-bit parallel port. CN5 is a 26-pin header, and thus an adapter cable is required for connection to a standard 25-pin D-sub connector.

CN5 : Parallel Connector

Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	STB#	O	Line printer strobe signal	14	GND	Power	
2	AFD#	O	Line printer auto feed	15	PD6	I/O	Line printer data bit
3	PD0	I/O	Line printer data bit	16	GND	Power	
4	ERROR#	I	Line printer error signal	17	PD7	I/O	Line printer data bit
5	PD1	I/O	Line printer data bit	18	GND	Power	
6	INIT#	O	Line printer initialize signal	19	ACK#	I	Line printer acknowledge
7	PD2	I/O	Line printer data bit	20	GND	Power	
8	SLCTIN#	O	Line printer select in signal	21	BUSY#	I	Line printer busy signal
9	PD3	I/O	Line printer data bit	22	GND	Power	
10	GND	Power		23	PE	I	Line printer paper end
11	PD4	I/O	Line printer data bit	24	GND	Power	
12	GND	Power		25	SLCT	I	Line printer selected signal
13	PD5	I/O	Line printer data bit	26	NC		

For details refer to the CARD-PC Hardware Manual.

2.6.IDE Interface

The CARDPRESSO is equipped with an IDE interface. CN9 is a 40-pin header connector.

CN9 : IDE Connector

Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	RESETDRV#	O	Reset from host	21	NC		
2	GND	Power		22	GND	Power	
3	HDATA7	I/O	Disk drive data bit	23	HIOW#	O	I/O Write signal
4	HDATA8	I/O	Disk drive data bit	24	GND	Power	
5	HDATA6	I/O	Disk drive data bit	25	HIOR#	O	I/O Read signal
6	HDATA9	I/O	Disk drive data bit	26	GND	Power	
7	HDATA5	I/O	Disk drive data bit	27	IOCHRDY	I OD	I/O channel ready
8	HDATA10	I/O	Disk drive data bit	28	BALE	O	Buffered address enable
9	HDATA4	I/O	Disk drive data bit	29	NC		
10	HDATA11	I/O	Disk drive data bit	30	GND	Power	
11	HDATA3	I/O	Disk drive data bit	31	IRQ14	I	Interrupt request
12	HDATA12	I/O	Disk drive data bit	32	IOCS16#	I OD	Indicate 16-bit cycle
13	HDATA2	I/O	Disk drive data bit	33	HSA1	O	Address bit
14	HDATA13	I/O	Disk drive data bit	34	PDIAG	I/O	Used for drive diagnostic
15	HDATA1	I/O	Disk drive data bit	35	HSA0	O	Address bit
16	HDATA14	I/O	Disk drive data bit	36	HSA2	O	Address bit
17	HDATA0	I/O	Disk drive data bit	37	HDCS0#	O	Chip select of 1Fx
18	HDATA15	I/O	Disk drive data bit	38	HDCS1#	O	Chip select of 3Fx
19	GND	Power		39	DASP#	I	Used to drive LED
20	KEY			40	GND	Power	

2.7.CRT Interface

The CARDPRESSO is equipped with a CARD interface. CN11 is a 15-pin D-sub connector.

CN11 : CARD Connector

Pin	Signal Name	Type	Function
1	RED	AO	Red analog signal output
2	GREEN	AO	Green analog signal output
3	BLUE	AO	Blue analog signal output
4	NC		
5	GND	Power	
6	RED RETURN	I	Return path
7	GREEN RETURN	I	Return path
8	BLUE RETURN	I	Return path
9	NC		
10	GND	Power	
11	NC		
12	NC		
13	HSYNC	O	Vertical Synchronization signal
14	VSYNC	O	Horizontal Synchronization signal
15	NC		

For details refer to the CARD-PC Hardware Manual.

2.8.PC/104 Expansion Bus

The CARDPRESSO is equipped with a connector supporting the PC/104 expansion bus. The PC/104 expansion bus is an adaptation of the ISA bus to a 64-pin connector and a 40-pin connector. Using the PC/104 expansion bus allows functions to be expanded at low cost and with space saving.

CN6、CN7 :PC/104 Connector

Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
A1	IOCHCK#	I	I/O Channel Check	B1	GND	Power	
A2	SD7	I/O	System Data bit	B2	RESETDRV	O	System Reset signal
A3	SD6	I/O	System Data bit	B3	P5V	Power	+5VDC
A4	SD5	I/O	System Data bit	B4	IRQ9	I	Interrupt request signal
A5	SD4	I/O	System Data bit	B5	M5V	Power	-5VDC
A6	SD3	I/O	System Data bit	B6	DRQ2	I	DMA Request signal
A7	SD2	I/O	System Data bit	B7	M12V	Power	-12VDC
A8	SD1	I/O	System Data bit	B8	ENDXFR#	I/O OD	Zero wait state request
A9	SD0	I/O	System Data bit	B9	P12V	Power	+12VDC
A10	IOCHRDY	I/O OD	I/O Channel Ready	B10	KEY		
A11	AEN	O	Address Enable	B11	SMEMW#	O	Memory read (~1MB)
A12	SA19	O	System Address bit	B12	SMEMR#	O	Memory write (~1MB)
A13	SA18	O	System Address bit	B13	IOW#	I/O	I/O write
A14	SA17	O	System Address bit	B14	IOR#	I/O	I/O read
A15	SA16	I/O	System Address bit	B15	DACK3#	O	DMA acknowledge
A16	SA15	I/O	System Address bit	B16	DRQ3	I	DMA request
A17	SA14	I/O	System Address bit	B17	DACK1#	O	DMA acknowledge
A18	SA13	I/O	System Address bit	B18	DRQ1	I	DMA request
A19	SA12	I/O	System Address bit	B19	REFRESH#	I/O OD	Refresh cycle
A20	SA11	I/O	System Address bit	B20	SCLK	O	8MHz System Clock
A21	SA10	I/O	System Address bit	B21	IRQ7	I	interrupt request
A22	SA9	I/O	System Address bit	B22	IRQ6	I	interrupt request
A23	SA8	I/O	System Address bit	B23	IRQ5	I	interrupt request
A24	SA7	I/O	System Address bit	B24	IRQ4	I	interrupt request
A25	SA6	I/O	System Address bit	B25	IRQ3	I	interrupt request
A26	SA5	I/O	System Address bit	B26	DACK2#	O	DMA acknowledge
A27	SA4	I/O	System Address bit	B27	TC	O	DMA terminal count
A28	SA3	I/O	System Address bit	B28	BALE	O	Buffered address enable
A29	SA2	I/O	System Address bit	B29	P5V	Power	+5VDC
A30	SA1	I/O	System Address bit	B30	OSC	O	14.31818MHz
A31	SA0	I/O	System Address bit	B31	GND	Power	
A32	GND	Power		B32	GND	Power	
C0	GND	Power		D0	GND	Power	
C1	SBHE#	I/O	Byte High Enable	D1	MEMCS16#	I/O OD	Memory chip select 16
C2	LA23	I/O	Latchable address	D2	IOCS16#	I/O OD	I/O chip select 16
C3	LA22	I/O	Latchable address	D3	IRQ10	I	interrupt request
C4	LA21	I/O	Latchable address	D4	IRQ11	I	interrupt request
C5	LA20	I/O	Latchable address	D5	IRQ12	I	interrupt request
C6	LA19	I/O	Latchable address	D6	IRQ15	I	interrupt request
C7	LA18	I/O	Latchable address	D7	IRQ14	I	interrupt request
C8	LA17	I/O	Latchable address	D8	DACK0#	O	DMA acknowledge
C9	MEMR#	I/O	Memory Read	D9	DRQ0	I	DMA request
C10	MEMW#	I/O	Memory Write	D10	DACK5#	O	DMA acknowledge
C11	SD8	I/O	System Data bit	D11	DRQ5	I	DMA request
C12	SD9	I/O	System Data bit	D12	DACK6#	O	DMA acknowledge
C13	SD10	I/O	System Data bit	D13	DRQ6	I	DMA request
C14	SD11	I/O	System Data bit	D14	DACK7#	O	DMA acknowledge
C15	SD12	I/O	System Data bit	D15	DRQ7	I	DMA request
C16	SD13	I/O	System Data bit	D16	P5V	Power	+5VDC
C17	SD14	I/O	System Data bit	D17	MASTER#	I	Bus master request
C18	SD15	I/O	System Data bit	D18	GND	Power	
C19	KEY			D19	GND	Power	

For details of signals, refer to the CARD-PC Hardware Manual.
For the external dimensions of the PC/104 module, see the physical specifications.

2.9.Keyboard/Mouse Interface

The CARDPRESSO can use a PS/2 type keyboard and mouse. CN10 has the signals for a mouse supplied through pins unused in the standard AT keyboard interface.

For keyboard only: use with direct connection.
For mouse only: branching adapter is required.
For keyboard and mouse: branching adapter is required.

The same signals as CN10 are also provided on CN13, which is a 6-pin header. This can conveniently be used for signals to a built-in keyboard/mouse.

CN10 : keyboard / Mouse Connector							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	KBDATA	I/O OD	Keyboard data line	4	P5V	Power	+5VDC
2	MSDATA	I/O OD	Mouse data line	5	KBCLK	I/O OD	Keyboard clock line
3	GND	Power		6	MSCLK	I/O OD	Mouse clock line

CN13 : keyboard / Mouse Connector							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	KBDATA	I/O OD	Keyboard data line	4	GND	Power	
2	KBCLK	I/O OD	Keyboard clock line	5	MSDATA	I/O OD	Mouse data line
3	P5V	Power	+5VDC	6	MSCLK	I/O OD	Mouse clock line

For details refer to the CARD-PC Hardware Manual.

Note
CN10 and CN13 cannot be used simultaneously for a keyboard or mouse.

2.10.LCD Interface

CN12 : LCD Connector							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	P5V	Power	+5VDC	26	FPAC	O	AC signal
2	GND	Power		27	GND	Power	
3	FPVTIM	O	Vertical timing signal	28	P12V	Power	+12VDC
4	GND	Power		29	P12V	Power	+12VDC
5	FPHTIM	O	Horizontal timing signal	30	P12V	Power	+12VDC
6	GND	Power		31	GND	Power	
7	FPDOTCLK	O	Dot clock signal	32	RESERVE		
8	GND	Power		33	LD9	O	LCD data output
9	P5V	Power	+5VDC	34	LD10	O	LCD data output
10	LD8	O	LCD data output	35	LD11	O	LCD data output
11	LD7	O	LCD data output	36	P5V	Power	+5VDC
12	LD6	O	LCD data output	37	GND	Power	
13	LD5	O	LCD data output	38	LD12	O	LCD data output
14	LD4	O	LCD data output	39	LD13	O	LCD data output
15	P5V	Power		40	LD14	O	LCD data output
16	GND	O		41	LD15	O	LCD data output
17	LD3	O	LCD data output	42	P5V	Power	+5VDC
18	LD2	O	LCD data output	43	GND	Power	
19	LD1	O	LCD data output	44	GND	Power	
20	LD0	O	LCD data output	45	GND	Power	
21	P5V	Power	+5VDC	46	NC		
22	GND	Power		47	NC		
23	FPVEEON	O	Vee control signal	48	NC		
24	FPVCCON	O	Vcc control signal	49	LD17	O	LCD data output
25	BLANK#	O	Panel Blank signal	50	LD16	O	LCD data output

Refer to “CARD-PC Technical Information” for LCD connection.

2.11.FDD Interface

The CARDPRESSO is equipped with an FDD interface. CN14 is a 34-pin header connector.

CN14 : FDD Connector							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
1	NC			18	FDDIR	O	Head stepper direction
2	FDHIDEN	O	High density select	19	GND	Power	
3	NC			20	FDSTEP#	O	Drive head stepper
4	NC			21	GND	Power	
5	NC			22	FDWD#	O	Write data output
6	NC			23	GND	Power	
7	GND	Power		24	FDWE#	O	Write enable
8	FDINDEX#	I OD	Index pulse input	25	GND	Power	
9	GND	Power		26	FDTRK0#	I OD	Track 0 signal input
10	FDDMT1#	O	Turn on drive 1 spindle	27	GND	Power	
11	GND	Power		28	FDWP#	I OD	Write-protect signal input
12	FDDS2#	O	Select drive 2	29	GND	Power	
13	GND	Power		30	FDRD#	I OD	Read data input
14	FDDS1#	O	Select drive 1	31	GND	Power	
15	GND	Power		32	FDSIDE	O	Head select
16	FDMT2#	O	Turn on drive 2 spindle	33	GND	Power	
17	GND	Power		34	FDDCHG#	I OD	Disk change status

For details refer to the CARD-PC Hardware Manual.

2.12.MISC Interface

This is a connector for CARDPRESSO function expansion. CN18 is a 16-pin header connector.

CN18 : MISC Connector			
Pin	Signal Name	Type	Function
1	RESERVE		
2	RESERVE		
3	RESERVE		
4	RESERVE		
5	NC		
6	EXTSMI#	I	External System Management Interrupt Input, generate SMI#
7	NC		
8	WDOUT#	O	Watch Dog Timer Out signal
9	GND	Power	
10	EXTRST#	I	External System Reset signal
11	IRRXD	I	IrDA-SIR Receive Data
12	DARXD	I	Digital ASK Receive Data
13	IRTXD	O	Ir Transmit Data
14	EXTBATT	I	RTC External backup battery input
15	P5V	Power	+5VDC
16	GND	Power	

For details see the section "Misc. Interface Functional Details."

2.13.ISA CARD Edge Interface

The CARDPRESSO is equipped with a 16-bit ISA CARD edge interface.

CN17 :ISA CARD Edge							
Pin	Signal Name	Type	Function	Pin	Signal Name	Type	Function
A1	IOCHCK#	I	I/O Channel Check	B1	GND	Power	
A2	SD7	I/O	System Data bit	B2	RESETDRV	O	System Reset signal
A3	SD6	I/O	System Data bit	B3	P5V	Power	+5VDC
A4	SD5	I/O	System Data bit	B4	IRQ9	I	Interrupt request signal
A5	SD4	I/O	System Data bit	B5	M5V	Power	-5VDC
A6	SD3	I/O	System Data bit	B6	DRQ2	I	DMA Request signal
A7	SD2	I/O	System Data bit	B7	M12V	Power	-12VDC
A8	SD1	I/O	System Data bit	B8	WS0#	I/O OD	Zero wait state request
A9	SD0	I/O	System Data bit	B9	P12V	Power	+12VDC
A10	IOCHRDY	I/O OD	I/O Channel Ready	B10	GND	Power	
A11	AEN	O	Address Enable	B11	SMEMW#	O	Memory read (~1MB)
A12	SA19	O	System Address bit	B12	SMEMR#	O	Memory write (~1MB)
A13	SA18	O	System Address bit	B13	IOW#	I/O	I/O write
A14	SA17	O	System Address bit	B14	IOR#	I/O	I/O read
A15	SA16	I/O	System Address bit	B15	DACK3#	O	DMA acknowledge
A16	SA15	I/O	System Address bit	B16	DRQ3	I	DMA request
A17	SA14	I/O	System Address bit	B17	DACK1#	O	DMA acknowledge
A18	SA13	I/O	System Address bit	B18	DRQ1	I	DMA request
A19	SA12	I/O	System Address bit	B19	REFRESH#	I/O OD	Refresh cycle
A20	SA11	I/O	System Address bit	B20	SCLK	O	8MHz system clock
A21	SA10	I/O	System Address bit	B21	IRQ7	I	interrupt request
A22	SA9	I/O	System Address bit	B22	IRQ6	I	interrupt request
A23	SA8	I/O	System Address bit	B23	IRQ5	I	interrupt request
A24	SA7	I/O	System Address bit	B24	IRQ4	I	interrupt request
A25	SA6	I/O	System Address bit	B25	IRQ3	I	interrupt request
A26	SA5	I/O	System Address bit	B26	DACK2#	O	DMA acknowledge
A27	SA4	I/O	System Address bit	B27	TC	O	DMA terminal count
A28	SA3	I/O	System Address bit	B28	BALE	O	buffered address enable
A29	SA2	I/O	System Address bit	B29	P5V	Power	+5VDC
A30	SA1	I/O	System Address bit	B30	OSC	O	14.31818MHz
A31	SA0	I/O	System Address bit	B31	GND	Power	
C1	SBHE#	I/O	Byte Hi Enable	D1	MEMCS16#	I/O OD	Memory chip select 16
C2	LA23	I/O	Latchable address	D2	IOCS16#	I/O OD	I/O chip select 16
C3	LA22	I/O	Latchable address	D3	IRQ10	I	interrupt request
C4	LA21	I/O	Latchable address	D4	IRQ11	I	interrupt request
C5	LA20	I/O	Latchable address	D5	IRQ12	I	interrupt request
C6	LA19	I/O	Latchable address	D6	IRQ15	I	interrupt request
C7	LA18	I/O	Latchable address	D7	IRQ14	I	interrupt request
C8	LA17	I/O	Latchable address	D8	DACK0#	O	DMA acknowledge
C9	MEMR#	I/O	Memory Read	D9	DRQ0	I	DMA request
C10	MEMW#	I/O	Memory Write	D10	DACK5#	O	DMA acknowledge
C11	SD8	I/O	System Data bit	D11	DRQ5	I	DMA request
C12	SD9	I/O	System Data bit	D12	DACK6#	O	DMA acknowledge
C13	SD10	I/O	System Data bit	D13	DRQ6	I	DMA request
C14	SD11	I/O	System Data bit	D14	DACK7#	O	DMA acknowledge
C15	SD12	I/O	System Data bit	D15	DRQ7	I	DMA request
C16	SD13	I/O	System Data bit	D16	P5V	Power	+5VDC
C17	SD14	I/O	System Data bit	D17	MASTER#	I	Bus master request
C18	SD15	I/O	System Data bit	D18	GND	Power	

For details refer to the CARD-PC Hardware Manual.

2.14.Power Supply Interface

The CARDPRESSO generates its own on-board +3.3 V supply, and thus can operate when supplied with +5 V and +12 V.

CN15 : Power Supply Connector			
Pin	Signal Name	Type	Function
1	P5V	Power	+5VDC
2	P12V	Power	+12VDC
3	M5V	Power	-5VDC
4	M12V	Power	-12VDC
5	GND	Power	

The CARDPRESSO is normally supplied with power through CN15, but it is also possible to supply power through CN17, the ISA CARD edge connector. If supplying power through the ISA CARD edge connector, do not connect power to CN15.

2.15.Backup Battery Interface

The CARDPRESSO uses a coin-sized lithium battery as backup power supply for the built-in real time clock and CMOS RAM. The backup lasts for approximately two years.

Recommended battery: CR2032 manganese dioxide / lithium battery 3 V 220 mAh (Sanyo)

CN16 : Backup Battery Holder			
Pin	Signal Name	Type	Function
1	BATT	Power	+3.0VDC
2	GND	Power	

2.16.CARDPRESSO Power Consumption

The measurements were taken without add-on CARD and PC/104 module. Also because the device type were limited when the measurements were performed, note that the consumption current values will change when devices different that those shown in this table are used.

CARD-PC		Socket 0	Socket 1	FDD	HDD	K/B	CRT	P5V	P12V
CARD-486HB 16MHz	FDD ,HDD R/W	×	×	○	○	○	○	650mA	1mA
CARD-486HB 16MHz	Socket 0 R/W	PC Card 1	PC Card 2	×	×	○	○	920mA	1mA
CARD-486HB 16MHz	Socket 0 R/W	PC Card 3	PC Card 2	×	×	○	○	700mA	1mA
CARD-486HB 33MHz	FDD ,HDD R/W	×	×	○	○	○	○	720mA	1mA
CARD-486HB 33MHz	Socket 0 R/W	PC Card 1	PC Card 2	×	×	○	○	1010mA	1mA
CARD-486HB 33MHz	Socket 0 R/W	PC Card 3	PC Card 2	×	×	○	○	760mA	1mA
CARD-586 66MHz	FDD ,HDD R/W	×	×	○	○	○	○	mA	1mA
CARD-586 66MHz	Socket 0 R/W	PC Card 1	PC Card 2	×	×	○	○	mA	1mA
CARD-586 66MHz	Socket 0 R/W	PC Card 3	PC Card 2	×	×	○	○	mA	1mA
CARD-586 133MHz	FDD ,HDD R/W	×	×	○	○	○	○	720mA	1mA
CARD-586 133MHz	Socket 0 R/W	PC Card 1	PC Card 2	×	×	○	○	1010mA	1mA
CARD-586 133MHz	Socket 0 R/W	PC Card 3	PC Card 2	×	×	○	○	760mA	1mA

○ Device Configuration

- CARDPRESSO SEK0630B0G
- PC CARD 1 Viper8170PA(Integral)
- PC CARD 2 2MB SRAM(EPSON)
- PC CARD 3 FLASH-PACKER 5MB(EPSON)
- FDD FD-235HG(TEAC)
- HDD DALA-3540(IBM)
- Keyboard MODEL E1160A(EPSON)
- CRT VGA XJ9870(APRICOT)

3.Functional Details

3.1.PCMCIA Functional Details

3.1.1.Overview

The CARDPRESSO uses a CL_PD6720 (Cirrus Logic) as PCMCIA controller (PCIC), to comply with PCMCIA Rel. 2.1 / JEIDA Ver. 4.2 standards.

- Support for PCMCIA Rel. 2.1 / JEIDA Ver. 4.2
- Registers upwards compatible with i82365SL
- Five memory windows and two I/O windows
- Support for 8- and 16-bit PCMCIA interface
- Support for ATA interface
- PC CARD live line insertion possible

For details of the PCIC, refer to the CL_PD6710/PD672X Data Sheet from Cirrus Logic. Moreover, by setting the BIOS of the CARD-PC, it is possible to use Socket 0 as a 1.8-inch IDE type ATA. For details of the BIOS set, refer to the document " CARD-PC Setup Utility Set Manual".

3.1.2.PC CARD Socket Signals

3.1.2.1.PCMCIA socket address outputs (AA[25:0], BA[25:0])

AA[25:0] provide the Socket 0 signals and BA[25:0] the Socket 1 signals. These outputs address a maximum 64 MB address space for memory and I/O on the PC CARD bus. For word access AA0 and BA0 are invalid. AA25 and BA25 are the most significant bits and AA0 and BA0 the least significant.

3.1.2.2.PCMCIA socket data I/O signals (AD[15:0], BD[15:0])

AD[15:0] provide the Socket 0 signals and BD[15:0] the Socket 1 signals. This 16-bit data bus is used for memory and I/O devices on the PC CARD bus and for data transfer to and from the CL_PD6720. AD15 and BD15 are the most significant bits and AD0 and BD0 the least significant.

3.1.2.3.Register Access (AREG#, BREG#)

AREG# is an output control signal for reading the attribute memory of a PC CARD for Socket 0; BREG# is the corresponding signal for Socket 1. When accessing the common memory on a PC CARD these are inactive. When these signals are low, attribute memory can be read through AOE#, BOE#, AWE#, and BWE#, and the I/O space can be accessed through AIORD#, BIORD#, AIOWR#, and BIOWR#. Attribute memory is accessed only by even addresses, and therefore for word access AD[7:0] and BD[7:0] data signals are valid, and AD[15:8] and BD[15:8] are invalid. For byte access, odd address accesses are invalid.

3.1.2.4.Card Enable (ACE#[2:1], BCE#[2:1])

ACE#[2:1] are the byte access / word access selection signals for Socket 0; BCE#[2:1] are the corresponding signals for Socket 1. ACE1# and BCE1# control even addresses and ACE2# and BCE2# control odd addresses. In combination with AA0 and BA0, it is possible to access both even and odd addresses using only the eight bits of AD[7:0] and BD[7:0]. The card enable signals are used for accessing common memory, attribute memory, and I/O ports.

3.1.2.5.Output Enable (AOE#, BOE#)

AOE# is an output signal for controlling read data for Socket 0; BOE# is the corresponding signal for Socket 1.

3.1.2.6.Write Enable (AWE#, BWE#)

AWE# is an output signal for controlling write data for Socket 0; BWE# is the corresponding signal for Socket 1.

3.1.2.7.

3.1.2.8.I/O Read (AIORD#, BIORD#)

AIORD# is an output signal for controlling reading from an I/O area for Socket 0; BIORD# is the corresponding signal for Socket 1. These are inactive until the I/O card interface is set.

3.1.2.9.I/O Write (AIOWR#, BIOWR#)

AIOWR# is an output signal for controlling writing to an I/O area for Socket 0; BIOWR# is the corresponding signal for Socket 1. These are inactive until the I/O card interface is set.

3.1.2.10.Ready / Interrupt Request (ARDY, BRDY)

ARDY is a ready/busy (RDY/BSY#) signal from a PC card when using the memory card interface for Socket 0; BRDY is the corresponding signal for Socket 1. The high level indicates ready, and the low level busy. When using the I/O card interface, these are interrupt request signals (IREQ#). These are inputs from the PC card, and are active low.

3.1.2.11.Wait (AWAIT#, BWAIT#)

AWAIT# is an input signal for delaying the in progress memory access cycle or I/O access cycle for Socket 0; BWAIT# is the corresponding signal for Socket 1.

3.1.2.12.Input Acknowledge (AINPACK#, BINPACK#)

AINPACK# is an input signal for Socket 0 which goes low when the I/O interface is being used, ACE#[2:1] and AIORD# are low, and the address on the bus agrees with the I/O port within the PC card. BINPACK# is an input signal for Socket 1 which goes low when the I/O interface is being used, BCE#[2:1] and BIORD# are low, and the address on the bus agrees with the I/O port within the PC card.

3.1.2.13.Write Protect / I/O Is 16 Bit (AWP, BWP)

AWP is an input signal for Socket 0 when the memory interface is being used which indicates the state of the write-protect switch; BWP is the corresponding signal for Socket 1. When the signal is high writing is inhibited, and when low writing is permitted. When using the I/O interface, this is IOCS16#. The IOCS16# signal is an input signal which goes low when 16-bit access is possible to the I/O port being accessed on the interface. During 16-bit access, if this signal is not active the system carries out separate 8-bit accesses to the even byte and odd byte of the required 16-bit port.

3.1.2.14.Reset (ARESET, BRESET)

ARESET is an output signal for resetting Socket 0; BRESET is the corresponding signal for Socket 1.

3.1.2.15.Card Detect (ACD#[2:1], BCD#[2:1])

ACD#[2:1] are input signals for detecting the presence of a PC card in Socket 0; BCD#[2:1] are the corresponding signals for Socket 1. These are connected to ground within the PC card, and are low when a card is inserted, and are caused to go high by pull-up resistors within the host circuit when no card is inserted.

3.1.2.16.Battery Detect 1 / Status Change (ABVD1, BBVD1)

ABVD1 is an input signal for Socket 0 when the memory interface is being used which indicates the state of the battery built into the PC card; BBVD1 is the corresponding signal for Socket 1. When using the I/O interface, this is the STSCHG# signal. The STSCHG# signal is an input signal for warning the system of changes in the ready/busy, write-protect, or battery voltage status, and is active low.

3.1.2.17.Battery Detect 2 / Speaker (ABVD2, BBVD2)

ABVD2 is an input signal for Socket 0 when the memory interface is being used which indicates the state of the battery built into the PC card; BBVD2 is the corresponding signal for Socket 1. These signals can be used in combination with ABVD1 and BBVD1 to determine the corresponding states. When using the I/O interface, this is a digital audio input.

BVD1	BVD2	Status
High	High	Battery voltage is normal.
High	Low	Data is preserved, but battery replacement is required.
Low	High	Data preservation is not guaranteed, and battery replacement is required.
Low	Low	Data preservation is not guaranteed, and battery replacement is required.

3.1.2.18.Voltage Sense (AVS[2:1], BVS[2:1])

AVS[2:1] are input signals indicating the drive voltage level for a PC card inserted in the Socket 0; BVS[2:1] is the corresponding signal for Socket 1. For details see the section "Support for Low Voltage Cards."

3.1.2.19.PC card drive power supply (AVCC, BVCC)

AVCC is the drive power supply for Socket 0; BVCC is the drive power supply for Socket 1. Based on AVC[2:1] and BVS[2:1], +5 V or +3.3 V is applied.

3.1.2.20.PC card program power supply (AVPP, BVPP)

AVPP is the program power supply for Socket 0; BVPP is the program power supply for Socket 1. These are used to supply voltages other than the PC card drive power supply, for programmable memory and I/O cards. Based on the contents of the CL_PD6720 Power Control Register, 0 V, +3.3 V, +5 V, or +12 V is applied.

3.1.3.PCMCIA Bus Timing

Complies with PCMCIA Rel. 2.1 / JEIDA Ver. 4.2.

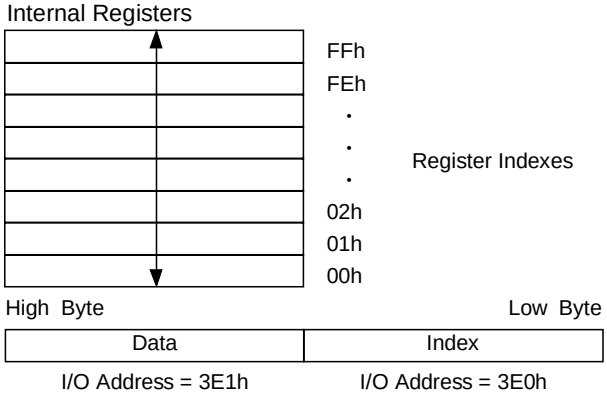
3.1.4.Internal Register Map

The CL_PD6720 uses an indexing method to allow access to its internal registers from the host. In other words, the host first writes an index number to the index register, then reads or writes data in the data register. This allows the host to access the internal registers through only two I/O addresses. The internal registers are compatible with the Intel 82365SL.

The index register and data register are assigned to the following addresses.

Index register = 3E0h
Data register = 3E1h

The following figure shows the configuration of the index register.



The following table lists the internal registers.

Socket 0 INDEX	Socket 1 INDEX	READ/WRITE	RESISTER NAME
00h	40h	R	Chip Revision
01h	41h	R	Interface Status
02h	42h	R/W	Power Control
03h	43h	R/W	Interrupt and General Control
04h	44h	R	Card Status Change
05h	45h	R/W	Management Interrupt Configuration
06h	46h	R/W	Mapping Enable
07h	47h	R/W	I/O Window Control
08h	48h	R/W	I/O Map 0 Start Address Low
09h	49h	R/W	I/O Map 0 Start Address High
0Ah	4Ah	R/W	I/O Map 0 End Address Low
0Bh	4Bh	R/W	I/O Map 0 End Address High
0Ch	4Ch	R/W	I/O Map 1 Start Address Low
0Dh	4Dh	R/W	I/O Map 1 Start Address High
0Eh	4Eh	R/W	I/O Map 1 End Address Low
0Fh	4Fh	R/W	I/O Map 1 End Address High
10h	50h	R/W	Memory Map 0 Start Address Low
11h	51h	R/W	Memory Map 0 Start Address High
12h	52h	R/W	Memory Map 0 End Address Low
13h	53h	R/W	Memory Map 0 End Address High
14h	54h	R/W	Memory Map 0 Address Offset Low
15h	55h	R/W	Memory Map 0 Address Offset High
16h	56h	R/W(bit0=R)	Misc. Control 1
17h	57h	R/W	FIFO Control
18h	58h	R/W	Memory Map 1 Start Address Low
19h	59h	R/W	Memory Map 1 Start Address High
1Ah	5Ah	R/W	Memory Map 1 End Address Low
1Bh	5Bh	R/W	Memory Map 1 End Address High
1Ch	5Ch	R/W	Memory Map 1 Address Offset Low
1Dh	5Dh	R/W	Memory Map 1 Address Offset High
1Eh	5Eh	R/W	Misc. Control 2
1Fh	5Fh	R/W	Chip Information
20h	60h	R/W	Memory Map 2 Start Address Low
21h	61h	R/W	Memory Map 2 Start Address High
22h	62h	R/W	Memory Map 2 End Address Low
23h	63h	R/W	Memory Map 2 End Address High
24h	64h	R/W	Memory Map 2 Address Offset Low
25h	65h	R/W	Memory Map 2 Address Offset High
26h	66h	R/W	ATA Control
27h	67h	-	Reserved
28h	68h	R/W	Memory Map 3 Start Address Low
29h	69h	R/W	Memory Map 3 Start Address High
2Ah	6Ah	R/W	Memory Map 3 End Address Low
2Bh	6Bh	R/W	Memory Map 3 End Address High
2Ch	6Ch	R/W	Memory Map 3 Address Offset Low
2Dh	6Dh	R/W	Memory Map 3 Address Offset High
2Eh	6Eh	-	Reserved
2Fh	6Fh	-	Reserved
30h	70h	R/W	Memory Map 4 Start Address Low
31h	71h	R/W	Memory Map 4 Start Address High
32h	72h	R/W	Memory Map 4 End Address Low
33h	73h	R/W	Memory Map 4 End Address High
34h	74h	R/W	Memory Map 4 Address Offset Low
35h	75h	R/W	Memory Map 4 Address Offset High
36h	76h	R/W	I/O Map 0 Address Offset Low
37h	77h	R/W	I/O Map 0 Address Offset High
38h	78h	R/W	I/O Map 1 Address Offset Low
39h	79h	R/W	I/O Map 1 Address Offset High
3Ah	7Ah	R/W	Setup Timing 0
3Bh	7Bh	R/W	Command Timing 0
3Ch	7Ch	R/W	Recovery Timing 0
3Dh	7Dh	R/W	Setup Timing 1
3Eh	7Eh	R/W	Command Timing 1
3Fh	7Fh	R/W	Recovery Timing 1

3.1.5.Windows Mapping

The CL_PD6720 has five memory windows and two I/O windows. By means of the memory windows, it is possible from the 16 MB address space of the ISA system to address a maximum of 64 MB. Each of the memory windows can be mapped to addresses above 64 KB in 4 KB steps, by setting the following internal registers.

- Mapping Enable Register
- Memory Map [4:0] Start Address Low Register
- Memory Map [4:0] Start Address High Register
- Memory Map [4:0] End Address Low Register
- Memory Map [4:0] End Address High Register
- Memory Map [4:0] Address Offset Low Register
- Memory Map [4:0] Address Offset High Register

The I/O windows provide similar functions to the memory windows, using the following internal registers. For details of the internal registers, refer to the CL_PD6710/PD672X Data Sheet from Cirrus Logic.

- Mapping Enable Register
- I/O Window Control Register
- I/O Map [1:0] Start Address Low Register
- I/O Map [1:0] Start Address High Register
- I/O Map [1:0] End Address Low Register
- I/O Map [1:0] End Address High Register
- I/O Map [1:0] Address Offset Low Register
- I/O Map [1:0] Address Offset High Register

3.1.6.Interrupt

To avoid conflicts with other devices when an interrupt request is received from an I/O PC card, there is a status change such as a PC card being inserted or removed, or for an SRAM card for example there is a change in the battery voltage of the PC card, it is possible to select one of the interrupt lines IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ14, or IRQ15 on the ISA bus, by setting the following internal registers. For details of the internal register values and settings, refer to the CL_PD6710/PD672X Data Sheet from Cirrus Logic.

- Interrupt and General Control Register
- Management Interrupt Configuration Register

3.1.7.Support for Low Voltage Cards

The CARDPRESSO is equipped with a DC power supply and switching circuit for a +3.3 V drive power supply for low voltage PC cards and a +5 V drive power supply for PC cards operating from +5 V, and when the ACD#[2:1] and BCD#[2:1] signals of the PC card socket are low, after considering the AVS[2:1] and BVS[2:1] signals either +3.3 V or +5 V is applied as the PC card drive voltage.

The PC card socket uses a low voltage key pin connector compliant with PCMCIA Rel. 2.1 / JEIDA Ver. 4.2. The following table shows the PC card drive voltage at initial power-on for different types of PC card.

Type of PC Card	Key type	AVS1# BVS1#	AVS2# BVS2#	Voltage level for CIS read-out
CIS : 5V Card	5 V key	High	High	System supplies +5 V to PC card, and reads CIS information.
CIS : 3.3V Card	Low voltage key	Low	High	System supplies +3.3 V to PC card, and reads CIS information.
CIS : 3.3V/5V Card	5 V key	Low	High	System supplies +3.3 V to PC card, and reads CIS information.
CIS : x.xV Card	Low voltage key	High	Low	Not supported. Note: System supplies +3.3 V to the PC card, so if the absolute maximum voltage the card can withstand is less than +3.3 V the card may be damaged. Check with the PC card manual.
CIS : x.xV/3.3V Card	Low voltage key	Low	Low	System supplies +3.3 V to PC card, and reads CIS information.
CIS : X.XV/3.3V/5V Card	5 V key	Low	Low	System supplies +3.3 V to PC card, and reads CIS information.

Note: reset V is a voltage to be defined in future.

For details of the following power control register values and settings, refer to the CL_PD6710/PD672X Data Sheet from Cirrus Logic.

- Interface Status Register
- Power Control Register
- Card Status Change Register
- Management Interrupt Configuration Register

3.1.8.Note with PCMCIA SRAM CARD

When boot-up with the SRAM card which does not meet with the JEIDA/PCMCIA specification, CARDPRESSO does not detect it.

3.1.9.PCMCIA Interface Power Supply

There is a circuit which +5V and +3.3V are changed to power supply of PC card with CARDPRESSO. The maximum current is 600mA of +5V and +3.3V. And the maximum current is 200mA of +12V.

AVCC、BVCC Output Current 600mA Max.
AVPP、BVPP Output Current 200mA Max.

And, a voltage drop occurs when a power supply is supplied to PC card because there is on resistance of switching circuit. For input voltage refer to the bottom figures.

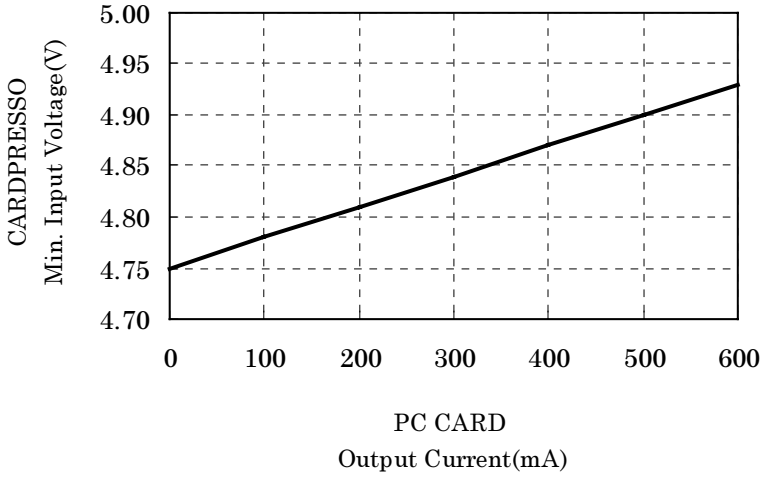


Figure Relations between +5V PC card current and the input voltage of CARDPRESSO

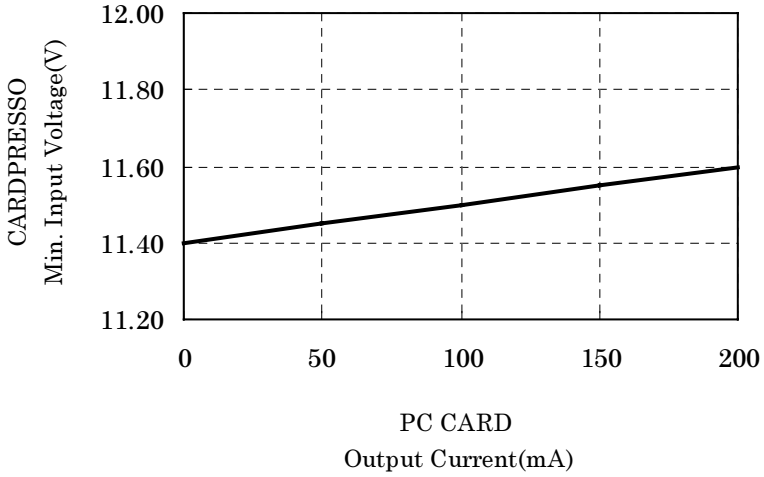


Figure Relations between +12V PC card current and the input voltage of CARDPRESSO

Parameter	Typ	Max	Units
Switch Resistance, Vcc out = 5.0V	210	300	mΩ
Switch Resistance, Vpp out = 12.0V	0.55	1	Ω

3.2.MISC Interface Function Details

The MISC interface (CN18) has a 16-pin header type connector, with the following signals:

- EXTSMI#
- WDOUT#
- IRRXD
- DARXD
- IRTXD
- EXTRST#
- EXTBATT

EXTSMI#, WDOUT#, IRRXD, DARXD and IRTXD are signals for details of the signals, refer to the CARD-PC Hardware Manual.

3.2.1.External Reset Input Signal (EXTRST#)

The external reset input signal is connected to the reset switch (SW1) internal to the CARDPRESSO. For built-in devices, since the reset switch on the board cannot be pressed, a signal can be input from the outside for initialization. When EXTRET# goes low the system is initialized.

Note
The external reset input signal is connected to the VBAK(RTC back up voltage) internal to the CARDPRESSO. Back up current grows up when resetting is made by using the reset terminal with TTL/CMOS and so on.

3.2.2.External Backup Power Input Signal (EXTBATT)

The external backup power input signal is connected to the backup battery connector internal to the CARDPRESSO. For built-in devices, since it is not easy to replace the coin-type battery on the board, a battery can be provided elsewhere for supplying backup power, or a large-capacity battery can be connected to extend the backup time. The backup voltage should be in the range 2.6 V to P5V.

Note
When using an external backup battery, remove the coin-type battery.

4. Switch and Jumper Settings

4.1.Switch Functions

The CARDPRESSO has a reset switch (SW1). The reset switch initializes the system in the same way as at power on.

4.2. Jumper Settings

The CARDPRESSO has jumpers J1, J5 and J6.
Jumper J7 isn't used.

4.2.1.Backup Power Supply On/Off Jumper (J1)

This jumper is provided to switch the backup power supply on and off. For long-term storage, jumper J1 can be set to the OFF position to reduce the drain on the lithium battery.

4.2.2.PCMCIA Controller Select Jumper (J5)

This jumper controls the selection of the PCMCIA controller. Make this setting when using two PCMCIA controllers when a PCMCIA add-on CARD or PC/104 module is connected to the CARDPRESSO.

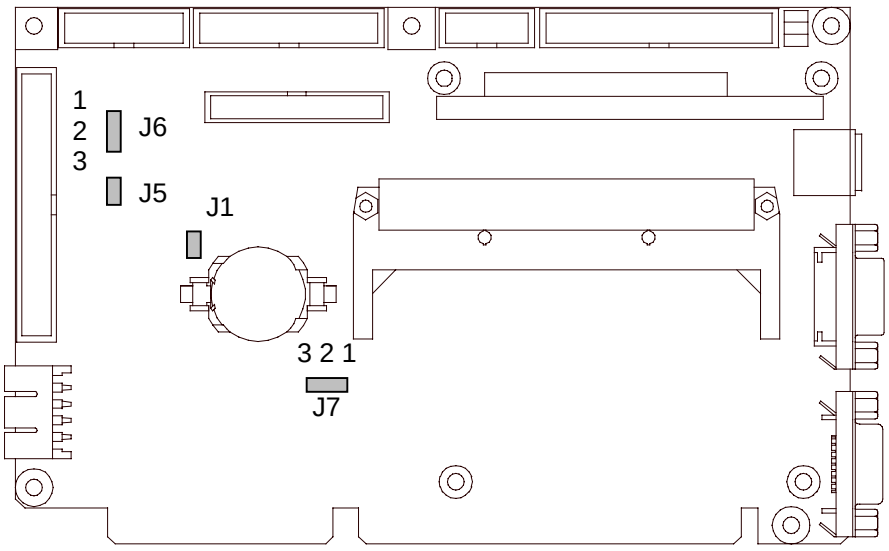
4.2.3.PGM Control Jumper (J6)

This jumper is used to control on/off switching for the VPP (+12 V) supply to the BIOS ROM .

Jumper settings

J1	SHORT(*)	OPEN
	Keep the CARD-PC real time clock and CMOS RAM contents.	Use this setting for long-term storage. The CARD-PC real time clock and CMOS RAM contents will not be preserved.
J5	SHORT	OPEN(*)
	Set the PCMCIA controller to Secondary.	Set the PCMCIA controller to Primary.
J6	1-2(*)	2-3
	VPP is switched on and off by the CARD-PC SMOUT3 signal.	VPP is constantly +12 V.

(*) Factory jumper settings



5. Environmental Characteristics

5.1.Temperature Ranges

Operating 0 to 55 degrees Celsius and
CARD-PC case surface temperature Max. 70 degrees Celsius(CARD-486HB 16MHz)
0 to 50degrees Celsius and
CARD-PC case surface temperature Max. 70 degrees Celsius(CARD-486HB 33MHz)

0 to XX degrees Celsius and
CARD-PC case surface temperature Max. 75 degrees Celsius(CARD-586 66MHz)
0 to 45degrees Celsius and
CARD-PC case surface temperature Max. 70 degrees Celsius(CARD-586 133MHz)

Storage -20 to 60 degrees Celsius

5.2.Humidity Ranges

Operating 0 to 80% (No condensation)
Storage 0 to 80% (No condensation)

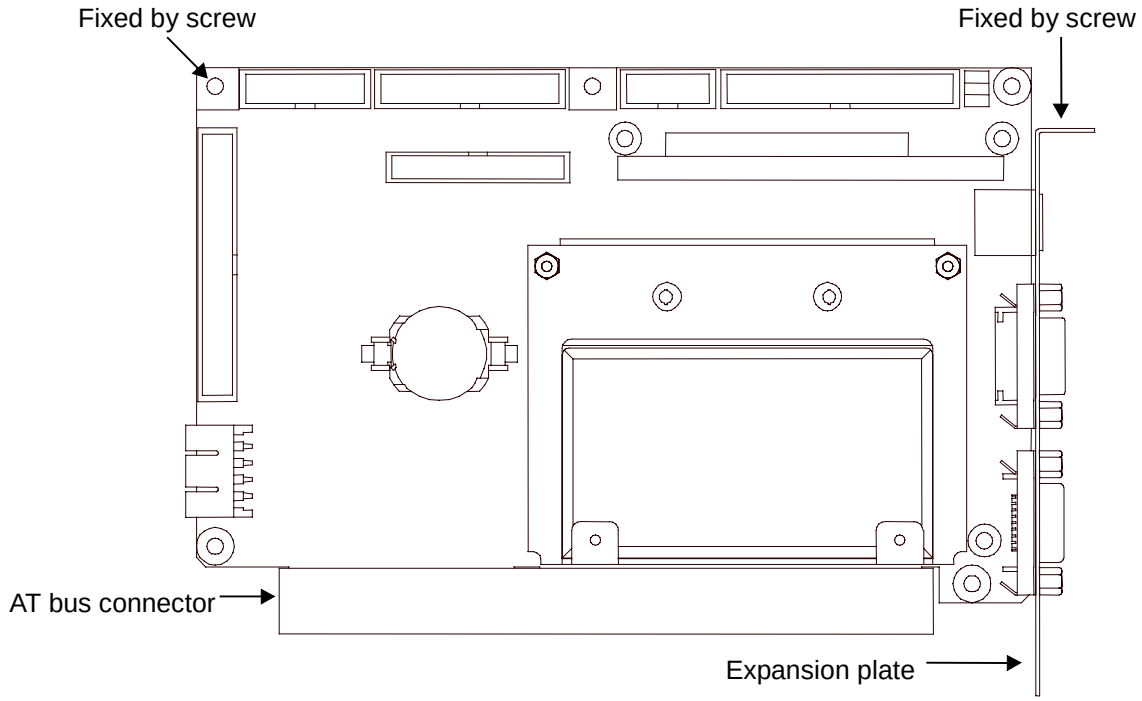
5.3.Vibration Resistance

While operating

Frequency:	10 to 50 Hz
Vibration value:	0.75 mmp_p (no turn-round points)
Vibration waveform:	sine wave
Vibration axes:	X, Y, and Z
Sweep cycle:	1 minute
Test time:	10 minutes in each direction
Fixing Method:	Fix the CARDPRESSO into a test system(The following figure)

While not operating

Frequency:	5 to 50 Hz
Vibration value:	1.00 mmp_p (no turn-round points)
Vibration waveform:	sine wave
Vibration axes:	X, Y, and Z
Sweep cycle:	1 minute
Test time:	2 hours in each direction
Fixing Method:	Fix the CARDPRESSO into a test system(The following figure)



5.4.Resistance to Electrostatic Noise

Contact discharge Minimum ±4.5kV

Note: Above are reference values for when the CARDPRESSO is built into a test system.

6.DC Characteristics

(Recommended and reference values)

6.1.DC Characteristics

6.1.1.Power Supply

Symbol	Parameter	Min	Max	Unit	Note
P5V	Supply Voltage	4.75	5.25	V	
P12V	Supply Voltage	11.4	12.6	V	
M5V	Supply Voltage			V	
M12V	Supply Voltage			V	
BATT EXTBATT	Battery Voltage	2.6	P5V	V	

Note: For details refer to the 3.1.9 PCMCIA Interface Power supply

6.1.2.ISA Bus, PC/104 Interface

Symbol	Parameter	Min	Max	Unit	Note
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.0	P5V+0.3	V	
VOL	Output Low Voltage IOL=12mA		0.4	V	Applies to pins IRQ6、DRQ2
VOL	Output Low Voltage IOL=8mA		0.4	V	Applies to pins IRQ3,4,5,7,10,11,12 Applies to pins DACK0,1,2,3,5,6,7#
VOL	Output High Voltage IOL=12mA		0.4	V	Open Drain Output Applies to pins IOCHRDY、REHRESH#
VOL	Output Low Voltage IOL=12mA		0.4	V	
VOL	Output Low Voltage IOL=2mA		0.26	V	Applies to pin OSC
VOH	Output High Voltage IOH=-2mA	2.4		V	Applies to pins IRQ6、DRQ2
VOH	Output High Voltage IOH=-8mA	2.4		V	Applies to pins IRQ3,4,5,7,10,11,12 Applies to pins DACK0,1,2,3,5,6,7#
VOH	Output High Voltage IOH=-12mA	2.4		V	
VOH	Output High Voltage IOH=-2mA	4.18		V	Applies to pin OSC

6.1.3.Serial Interface

Symbol	Parameter	Min	Max	Unit	Note
VDO	Driver Output Voltage	±7.0		V	
RIN	Receiver Input Voltage	-30	+30	V	

6.1.4.LCD Interface

Symbol	Parameter	Min	Max	Unit	Note
VOL	Output Low Voltage ILO=24mA		0.4	V	
VOL	Output Low Voltage ILO=6mA		0.4	V	Applies to pins FPVCCON,FPVEEON
VOH	Output High Voltage IOH=-8mA	4.0		V	
VOH	Output High Voltage IOH=-2mA	4.0		V	Applies to pins FPVCCON,FPVEEON

6.1.5.Keyboard/Mouse Interface

Symbol	Parameter	Min	Max	Unit	Note
VT+	Input Low Voltage	-0.5	0.6	V	CARD-486HB
VT-	Input Low Voltage	2.4	P5V+0.5	V	CARD-486HB
Vih	Input Hysteresis Voltage	0.1		V	CARD-486HB
VIL	Input Low Voltage	-0.3	0.6	V	CARD-586
VIH	Input High Voltage	2.4	P5V+0.3	V	CARD-586
VOL	Output Low Voltage IOL=24Ma		0.4	V	Open Drain Output

6.1.6.FDD Interface

Symbol	Parameter	Min	Max	Unit	Note
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.0	P5V+0.3	V	
VOL	Output Low Voltage IOL=38mA		0.4	V	Open Drain Output

6.1.7.Parallel Interface

Symbol	Parameter	Min	Max	Unit	Note
VIL	Input Low Voltage	-0.3	0.8	V	
VIL	Input Low Voltage		0.8	V	Applies to pins PD[0:7]
VIH	Input High Voltage	2.0	P5V+0.3	V	
VIH	Input High Voltage	2.0	5.5	V	Applies to pins PD[0:7]
VOL	Output Low Voltage IOL=8mA		0.4	V	Applies to pins STB#,AFD#,INIT#,SLCTIN#
VOL	Output Low Voltage IOL=24mA		0.5	V	Applies to pins PD[0:7]
VOH	Output High Voltage IOL=-8mA	2.4		V	Applies to pins STB#,AFD#,INIT#,SLCTIN#
VOH	Output High Voltage IOL=-15mA	2.0		V	Applies to pins PD[0:7]

6.1.8.PCMCIA Interface

Symbol	Parameter	Min	Max	Unit	Note
VCC5V	Power Supply Voltage	P5V-0.2	P5V	V	Normal operation
VCC3.3V	Power Supply Voltage	3.0	3.6	V	Normal operation
VPP	Program Voltage	P12V-0.2	P12V	V	Normal operation
VIL	Input Low Voltage		0.8	V	
VIH	Input High Voltage	2.0		V	
VILC	Input Low Voltage CMOS		1.0	V	
VIHC	Input High Voltage CMOS	3.5		V	
VOL	Output Low Voltage		0.5	V	Socket_VCC=3.0V IOL=2mA
VOH	Output High Voltage	2.4		V	Socket_VCC=3.0V IOH=2mA
VOHC	Output High Voltage CMOS	Socket_ VCC-0.5		V	Socket_VCC=3.0V IOHC=-1mA
ICC	AVCC,BVCC Output current		600	mA	
IPP	AVPP,BVPP Output current		200	mA	

Note: For details refer to the 3.1.9 PCMCIA Interface Power supply

6.1.9.IDE Interface

Symbol	Parameter	Min	Max	Unit	Note
VIL	Input Low Voltage	-0.3	0.8	V	
VIL	Input Low Voltage	-0.5	0.8	V	Applies to pins HDATA[0:15]
VIH	Input High Voltage	2.0	P5V+0.3	V	
VIH	Input High Voltage	2.0	P5V+0.5	V	Applies to pins HDATA[0:15]
VOL	Output Low Voltage IOL=12mA		0.4	V	
VOL	Output Low Voltage IOL=6mA		0.26	V	Applies to pins HDATA[0:15],HIOR#,HIOW#,HSA[0:2]
VOL	Output Low Voltage IOL=24mA		0.32	V	Applies to pin RESETDRV#
VOH	Output High Voltage IOH=-12mA	2.4		V	
VOH	Output High Voltage IOH=-6mA	4.18		V	Applies to pins HDATA[0:15],HIOR#,HIOW#,HSA[0:2]
VOH	Output High Voltage IOH=-24mA	3.94		V	Applies to pin RESETDRV#

6.1.10.MISC Interface

Symbol	Parameter	Min	Max	Unit	Note
VIL	Input Low Voltage	-0.3	0.8	V	
VIL	Input Low Voltage	-0.3	0.8	V	Applies to pin EXTRST#
VIH	Input High Voltage	2.0	P5V+0.3	V	
VIH	Input High Voltage	2.0	P5V+0.3	V	Applies to pin EXTRST#
VOL	Output Low Voltage IOL=24		0.4	V	Applies to pin IRTXD
VOL	Output Low Voltage IOL=8mA		0.4	V	Applies to pin WDOUT#
VOH	Output High Voltage IOH=-12A	2.4		V	Applies to pin IRTXD
VOH	Output High Voltage IOH=-8mA	2.4		V	Applies to pin WDOUT#

6.2.Power Supply

Symbol	Parameter	Min	Max	Unit	Note
P5V	Supply Current	1.5		A	
P12V	Supply Current	0.1		A	
M5V	Supply Current			A	
M12V	Supply Current			A	

Note 1: When power is supplied from connector CN15, the maximum current which can flow through pin 1 of connector CN15 is 6.0 A, and thus it is not possible to supply a current greater than this.

Note 2: The above current values are only for CARDPRESSO + CARD-PC. These are not included current for peripherals.

Note 3: Both of +5V and + 12V are necessary for CARDPRESSO.

6.3.Terminal Characteristics

This section describes the terminal characteristics of the CARDPRESSO interfaces.

Pin Characteristics	Details
Type	Terminal Type I : Input Terminal O : Output terminal O OD : Output terminal open drain output O TO : Output terminal three-state output I/O : Input/output terminal I/O OD : Input/output terminal open drain AO : Analog output terminal Power : Power and ground terminals
Terminal (termination)	Internal terminating resistor of terminal, and type of resistor HOLD : Bus holder ??PU : ??OHM pull-up resistor ??PD : ??OHM pull-down resistor ??／??PU : CARD-PC／Board ??OHM pull-up resistor
Drive	Drive current (mA) of output terminal or bi-directional terminal Indicated as IOL and IOH

6.3.1.RS232CInterface

CN3

Pin	Signal Name	Type	Terminal	Drive(mA)
1	DCD#_A	I	5.5KPD	---- ----
2	RXD_A	I	5.5KPD	---- ----
3	TXD_A	O	----	---- ----
4	DTR#_A	O	----	---- ----
5	GND	Power	----	---- ----
6	DSR#_A	I	5.5KPD	---- ----
7	RTS#_A	O	----	---- ----
8	CTS#_A	I	5.5KPD	---- ----
9	RI#_A	I	5.5KPD	---- ----

CN4

Pin	Signal Name	Type	Terminal	Drive(mA)
1	DCD#_B	I	5.5KPD	---- ----
2	DSR#_B	I	5.5KPD	---- ----
3	RXD_B	I	----	---- ----
4	RTS#_B	O	----	---- ----
5	TXD_B	O	----	---- ----
6	CTS#_B	I	5.5KPD	---- ----
7	DTR#_B	O	----	---- ----
8	RI#_B	I	5.5KPD	---- ----
9	GND	Power	5.5KPD	---- ----
10	NC	----	----	---- ----

6.3.2.IDE Interface

CN9					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	RESETDRV#	O	----	24	-24
2	GND	Power	----	----	----
3	HDATA7	I/O	100KPD	6	-6
4	HDATA8	I/O	100KPD	6	-6
5	HDATA6	I/O	100KPD	6	-6
6	HDATA9	I/O	100KPD	6	-6
7	HDATA5	I/O	100KPD	6	-6
8	HDATA10	I/O	100KPD	6	-6
9	HDATA4	I/O	100KPD	6	-6
10	HDATA11	I/O	100KPD	6	-6
11	HDATA3	I/O	100KPD	6	-6
12	HDATA12	I/O	100KPD	6	-6
13	HDATA2	I/O	100KPD	6	-6
14	HDATA13	I/O	100KPD	6	-6
15	HDATA1	I/O	100KPD	6	-6
16	HDATA14	I/O	100KPD	6	-6
17	HDATA0	I/O	100KPD	6	-6
18	HDATA15	I/O	100KPD	6	-6
19	GND	Power	----	----	----
20	N/C	----	----	----	----
21	N/C	----	----	----	----
22	GND	Power	----	----	----
23	HIOW#	O	50KPU	6	-6
24	GND	Power	----	----	----
25	HIOR#	O	50KPU	6	-6
26	GND	Power	----	----	----
27	IOCHRDY	I	1KPU	12	
28	BALE	O	----	12	-12
29	N/C	----	----	----	----
30	GND	Power	----	----	----
31	IRQ14	I	50KPU		
32	IOCS16#	I	1KPU		
33	HSA1	O	HOLD	6	-6
34	N/C	----	----	----	----
35	HSA0	O	HOLD	6	-6
36	HSA2	O	HOLD	6	-6
37	HDCS0#	O	----	12	-12
38	HDCS1#	O	----	12	-12
39	DASP#	O	----	----	----
40	GND	Power	----	----	----

6.3.3.LCD Interface

CN12					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	P5V	Power	----	----	----
2	GND	Power	----	----	----
3	FPVTIM	O	----	24	-8
4	GND	Power	----	----	----
5	FPHTIM	O	----	24	-8
6	GND	Power	----	----	----
7	FPDOTCLK	O	----	24	-8
8	GND	Power	----	----	----
9	P5V	Power	----	----	----
10	LD8	O	----	24	-8
11	LD7	O	----	24	-8
12	LD6	O	----	24	-8
13	LD5	O	----	24	-8
14	LD4	O	----	24	-8
15	P5V	Power	----	----	----
16	GND	Power	----	----	----
17	LD3	O	----	24	-8
18	LD2	O	----	24	-8
19	LD1	O	----	24	-8
20	LD0	O	----	24	-8
21	P5V	Power	----	----	----
22	GND	Power	----	----	----
23	FPVEEON	O	----	6	-2
24	FPVCCON	O	----	6	-2
25	BLANK#	O	----	24	-8
26	FPAC	O	----	24	-8
27	GND	Power	----	----	----
28	P12V	Power	----	----	----
29	P12V	Power	----	----	----
30	P12V	Power	----	----	----
31	GND	Power	----	----	----
32	RSV3	----	----	----	----
33	LD9	O	----	24	-8
34	LD10	O	----	24	-8
35	LD11	O	----	24	-8
36	P5V	Power	----	----	----
37	GND	Power	----	----	----
38	LD12	O	----	24	-8
39	LD13	O	----	24	-8
40	LD14	O	----	24	-8
41	LD15	O	----	24	-8
42	P5V	Power	----	----	----
43	GND	Power	----	----	----
44	GND	Power	----	----	----
45	GND	Power	----	----	----
46	NC	----	----	----	----
47	NC	----	----	----	----
48	NC	----	----	----	----
49	LD17	O	----	24	-8
50	LD16	O	----	24	-8

6.3.4.PC/104 Interface

CN6					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
A1	IOCHCK#	I	4.7KPU	----	----
A2	SD7	I/O	50KPU	12	-12
A3	SD6	I/O	50KPU	12	-12
A4	SD5	I/O	50KPU	12	-12
A5	SD4	I/O	50KPU	12	-12
A6	SD3	I/O	50KPU	12	-12
A7	SD2	I/O	50KPU	12	-12
A8	SD1	I/O	50KPU	12	-12
A9	SD0	I/O	50KPU	12	-12
A10	IOCHRDY	I/O OD	1KPU	12	----
A11	AEN	O	----	12	-12
A12	SA19	I/O	HOLD	12	-12
A13	SA18	I/O	HOLD	12	-12
A14	SA17	I/O	HOLD	12	-12
A15	SA16	I/O	HOLD	12	-12
A16	SA15	I/O	HOLD	12	-12
A17	SA14	I/O	HOLD	12	-12
A18	SA13	I/O	HOLD	12	-12
A19	SA12	I/O	HOLD	12	-12
A20	SA11	I/O	HOLD	12	-12
A21	SA10	I/O	HOLD	12	-12
A22	SA9	I/O	HOLD	12	-12
A23	SA8	I/O	HOLD	12	-12
A24	SA7	I/O	HOLD	12	-12
A24	SA6	I/O	HOLD	12	-12
A26	SA5	I/O	HOLD	12	-12
A27	SA4	I/O	HOLD	12	-12
A28	SA3	I/O	HOLD	12	-12
A29	SA2	I/O	HOLD	12	-12
A30	SA1	I/O	HOLD	12	-12
A31	SA0	I/O	HOLD	12	-12
A32	GND	Power	----	----	----
B1	GND	Power	----	----	----
B2	RESETDRV	O	----	12	-12
B3	P5V	Power	----	----	----
B4	IRQ9	I	50KPU	----	----
B5	M5V	Power	----	----	----
B6	DRQ2	IO	50KPD	12	-2
B7	M12V	Power	----	----	----
B8	WS0#	I	1KPU	----	----
B9	P12V	Power	----	----	----
B10	KEY	----	----	----	----
B11	SMEMW#	O	----	12	-12
B12	SMEMR#	O	----	12	-12
B13	IOW#	I/O	50KPU	12	-12
B14	IOR#	I/O	50KPU	12	-12
B15	DACK3#	O	----	8	-8
B16	DRQ3	I	50KPD	----	----
B17	DACK1#	O	----	8	-8
B18	DRQ1	I	50KPD	----	----
B19	REFRESH#	I/O OD	1.2KPU	12	----
B20	SCLK	O	----	12	-12
B21	IRQ7	I/O	50KPU	8	-8
B22	IRQ6	I/O	50KPU	12	-2
B23	IRQ5	I/O	50KPU	8	-8
B24	IRQ4	I/O	50KPU	8	-8
B24	IRQ3	I/O	50KPU	8	-8
B26	DACK2#	O	----	8	-8
B27	TC	O	----	12	-12
B28	BALE	O	----	12	-12
B29	P5V	Power	----	----	----
B30	OSC	O	----	2	-2
B31	GND	Power	----	----	----
B32	GND	Power	----	----	----

CN7					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
C0	GND	Power	----	----	----
C1	SBHE	I/O	HOLD	12	-12
C2	LA23	I/O	HOLD	12	-12
C3	LA22	I/O	HOLD	12	-12
C4	LA21	I/O	HOLD	12	-12
C5	LA20	I/O	HOLD	12	-12
C6	LA19	I/O	HOLD	12	-12
C7	LA18	I/O	HOLD	12	-12
C8	LA17	I/O	HOLD	12	-12
C9	MEMR#	I/O	50KPU	12	-12
C10	MEMW#	I/O	50KPU	12	-12
C11	SD8	I/O	50KPU	12	-12
C12	SD9	I/O	50KPU	12	-12
C13	SD10	I/O	50KPU	12	-12
C14	SD11	I/O	50KPU	12	-12
C15	SD12	I/O	50KPU	12	-12
C16	SD13	I/O	50KPU	12	-12
C17	SD14	I/O	50KPU	12	-12
C18	SD15	I/O	50KPU	12	-12
C19	KEY	----	----	----	----
D0	GND	Power	----	----	----
D1	MEMCS16#	I	1KPU	----	----
D2	IOCS16#	I	1KPU	----	----
D3	IRQ10	I/O	50KPU	8	-8
D4	IRQ11	I/O	50KPU	8	-8
D5	IRQ12	O	50KPU	8	-8
D6	IRQ15	I	50KPU	----	----
D7	IRQ14	I	50KPU	----	----
D8	DACK0#	O	----	8	-8
D9	DRQ0	I	50KPD	----	----
D10	DACK5#	O	----	8	-8
D11	DRQ5	I	50KPD	----	----
D12	DACK6#	O	----	8	-8
D13	DRQ6	I	50KPD	----	----
D14	DACK7#	O	----	8	-8
D15	DRQ7	I	50KPD	----	----
D16	P5V	Power	----	----	----
D17	MASTER#	I	1KPU	----	----
D18	GND	Power	----	----	----
D19	GND	Power	----	----	----

6.3.5.ISA Bus Interface

CN17					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
A1	IOCHCK#	I	4.7KPU	----	----
A2	SD7	I/O	50KPU	12	-12
A3	SD6	I/O	50KPU	12	-12
A4	SD5	I/O	50KPU	12	-12
A5	SD4	I/O	50KPU	12	-12
A6	SD3	I/O	50KPU	12	-12
A7	SD2	I/O	50KPU	12	-12
A8	SD1	I/O	50KPU	12	-12
A9	SD0	I/O	50KPU	12	-12
A10	IOCHRDY	I/O OD	1KPU	12	----
A11	AEN	O	----	12	-12
A12	SA19	I/O	HOLD	12	-12
A13	SA18	I/O	HOLD	12	-12
A14	SA17	I/O	HOLD	12	-12
A15	SA16	I/O	HOLD	12	-12
A16	SA15	I/O	HOLD	12	-12
A17	SA14	I/O	HOLD	12	-12
A18	SA13	I/O	HOLD	12	-12
A19	SA12	I/O	HOLD	12	-12
A20	SA11	I/O	HOLD	12	-12
A21	SA10	I/O	HOLD	12	-12
A22	SA9	I/O	HOLD	12	-12
A23	SA8	I/O	HOLD	12	-12
A24	SA7	I/O	HOLD	12	-12
A24	SA6	I/O	HOLD	12	-12
A26	SA5	I/O	HOLD	12	-12
A27	SA4	I/O	HOLD	12	-12
A28	SA3	I/O	HOLD	12	-12
A29	SA2	I/O	HOLD	12	-12
A30	SA1	I/O	HOLD	12	-12
A31	SA0	I/O	HOLD	12	-12
B1	GND	Power	----	----	----
B2	RESETDRV	O	----	12	-12
B3	P5V	Power	----	----	----
B4	IRQ9	I	50KPU	----	----
B5	M5V	Power	----	----	----
B6	DRQ2	IO	50KPD	12	-2
B7	M12V	Power	----	----	----
B8	WS0#	I	1KPU	----	----
B9	P12V	Power	----	----	----
B10	GND	----	----	----	----
B11	SMEMW#	O	----	12	-12
B12	SMEMR#	O	----	12	-12
B13	IOW#	I/O	50KPU	12	-12
B14	IOR#	I/O	50KPU	12	-12
B15	DACK3#	O	----	8	-8
B16	DRQ3	I	50KPD	----	----
B17	DACK1#	O	----	8	-8
B18	DRQ1	I	50KPD	----	----
B19	REFRESH#	I/O OD	1.2KPU	12	----
B20	SCLK	O	----	12	-12
B21	IRQ7	I/O	50KPU	8	-8
B22	IRQ6	I/O	50KPU	12	-2
B23	IRQ5	I/O	50KPU	8	-8
B24	IRQ4	I/O	50KPU	8	-8
B24	IRQ3	I/O	50KPU	8	-8
B26	DACK2#	O	----	8	-8
B27	TC	O	----	12	-12
B28	BALE	O	----	12	-12
B29	P5V	Power	----	----	----
B30	OSC	O	----	2	-2
B31	GND	Power	----	----	----

CN17					
Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
C1	SBHE	I/O	HOLD	12	-12
C2	LA23	I/O	HOLD	12	-12
C3	LA22	I/O	HOLD	12	-12
C4	LA21	I/O	HOLD	12	-12
C5	LA20	I/O	HOLD	12	-12
C6	LA19	I/O	HOLD	12	-12
C7	LA18	I/O	HOLD	12	-12
C8	LA17	I/O	HOLD	12	-12
C9	MEMR#	I/O	50KPU	12	-12
C10	MEMW#	I/O	50KPU	12	-12
C11	SD8	I/O	50KPU	12	-12
C12	SD9	I/O	50KPU	12	-12
C13	SD10	I/O	50KPU	12	-12
C14	SD11	I/O	50KPU	12	-12
C15	SD12	I/O	50KPU	12	-12
C16	SD13	I/O	50KPU	12	-12
C17	SD14	I/O	50KPU	12	-12
C18	SD15	I/O	50KPU	12	-12
D1	MEMCS16#	I	1KPU	----	----
D2	IOCS16#	I	1KPU	----	----
D3	IRQ10	I/O	50KPU	8	-8
D4	IRQ11	I/O	50KPU	8	-8
D5	IRQ12	O	50KPU	8	-8
D6	IRQ15	I	50KPU	----	----
D7	IRQ14	I	50KPU	----	----
D8	DACK0#	O	----	8	-8
D9	DRQ0	I	50KPD	----	----
D10	DACK5#	O	----	8	-8
D11	DRQ5	I	50KPD	----	----
D12	DACK6#	O	----	8	-8
D13	DRQ6	I	50KPD	----	----
D14	DACK7#	O	----	8	-8
D15	DRQ7	I	50KPD	----	----
D16	P5V	Power	----	----	----
D17	MASTER#	I	1KPU	----	----
D18	GND	Power	----	----	----

6.3.6.Parallel Interface

CN5

Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	STB#	I/O OD	4.7K / 10KPU	12	
2	AFD#	I/O OD	4.7K / 10KPU	12	
3	PD0	I/O	----	24	-15
4	ERROR#	I	60K / 10KPU	----	----
5	PD1	I/O	----	24	-15
6	INIT#	I/O OD	4.7K / 10KPU	12	
7	PD2	I/O	----	24	-15
8	SLCTIN#	I/O OD	4.7K / 10KPU	12	
9	PD3	I/O	----	24	-15
10	GND	Power	----	----	----
11	PD4	I/O	----	24	-15
12	GND	Power	----	----	----
13	PD5	I/O	----	24	-15
14	GND	Power	----	----	----
15	PD6	I/O	----	24	-15
16	GND	Power	----	----	----
17	PD7	I/O	----	24	-15
18	GND	Power	----	----	----
19	ACK#	I	60K / 10KPD	----	----
20	GND	Power	----	----	----
21	BUSY#	I	20K / 10KPD	----	----
22	GND	Power	----	----	----
23	PE	I	20K / 10KPD	----	----
24	GND	Power	----	----	----
25	SLCT	I	20K / 10KPD	----	----
26	NC	----	----	----	----

6.3.7.Keyboard/Mouse Interface

CN10

Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	KBDATA	I/O OD	1.2KPU	24	----
2	MSDATA	I/O OD	1.2KPU	24	----
3	GND	Power	----	----	----
4	P5V	Power	----	----	----
5	KBCLK	I/O OD	1.2KPU	24	----
6	MSCLK	I/O OD	1.2KPU	24	----

6.3.8.MISC Interface

CN11

Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	RESERVED	----	----	----	----
2	RESERVED	----	----	----	----
3	RESERVED	----	----	----	----
4	RESERVED	----	----	----	----
5	NC	----	----	----	----
6	EXTSMI#	I	70K / 100KPU	----	----
7	NC	----	----	----	----
8	WDOUT#	O		4	-4
9	GND	Power	----	----	----
10	EXTRST#	I	250uAPU	----	----
11	IRRXD	I	50KPU	----	----
12	DARXD	I	50KPU	----	----
13	IRTXD	O	----	24	-12
14	EXTBATT	I	----	----	----
15	P5V	Power	----	----	----
16	GND	Power	----	----	----

6.3.9.PCMCIA Interface

CN2

Pin	Signal Name	Pin No	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	GND	69	GND	Power	----	----	----
2	AD3	70	BD3	I/O	----	2	2
3	AD4	71	BD4	I/O	----	2	2
4	AD5	72	BD5	I/O	----	2	2
5	AD6	73	BD6	I/O	----	2	2
6	AD7	74	BD7	I/O	----	2	2
7	ACE1#	75	BCE1#	O TO	----	2	2
8	AA10	76	BA10	O TO	----	2	2
9	AOE#	77	BOE#	O TO	----	2	2
10	AA11	78	BA11	O TO	----	2	2
11	AA9	79	BA9	O TO	----	2	2
12	AA8	80	BA8	O TO	----	2	2
13	AA13	81	BA13	O TO	----	2	2
14	AA14	82	BA14	O TO	----	2	2
15	AWE#	83	BWE#	O TO	----	2	2
16	ARDY	84	BRDY	I	----	----	----
17	AVCC	85	BVCC	Power	----	----	----
18	AVPP1	86	BVPP1	Power	----	----	----
19	AA16	87	BA16	O TO	----	2	2
20	AA15	88	BA15	O TO	----	2	2
21	AA12	89	BA12	O TO	----	2	2
22	AA7	90	BA7	O TO	----	2	2
23	AA6	91	BA6	O TO	----	2	2
24	AA5	92	BA5	O TO	----	2	2
25	AA4	93	BA4	O TO	----	2	2
26	AA3	94	BA3	O TO	----	2	2
27	AA2	95	BA2	O TO	----	2	2
28	AA1	96	BA1	O TO	----	2	2
29	AA0	97	BA0	O TO	----	2	2
30	AD0	98	BD0	I/O	----	2	2
31	AD1	99	BD1	I/O	----	2	2
32	AD2	100	BD2	I/O	----	2	2
33	AWP	101	BWP	I	----	----	----
34	GND	102	GND	Power	----	----	----
35	GND	103	GND	Power	----	----	----
36	ACD1#	104	CD1#	I	----	----	----
37	AD11	105	BD11	I/O	----	2	2
38	AD12	106	BD12	I/O	----	2	2
39	AD13	107	BD13	I/O	----	2	2
40	AD14	108	BD14	I/O	----	2	2
41	AD15	109	BD15	I/O	----	2	2
42	ACE2#	110	BCE2#	O TO	----	2	2
43	AVS1	111	BVS1	I	10KPU	----	----
44	AIORD#	112	BIORD#	O TO	----	2	2
45	AIOWR#	113	BIOWR#	O TO	----	2	2
46	AA17	114	BA17	O TO	----	2	2
47	AA18	115	BA18	O TO	----	2	2
48	AA19	116	BA19	O TO	----	2	2
49	AA20	117	BA20	O TO	----	2	2
50	AA21	118	BA21	O TO	----	2	2
51	AVCC	119	BVCC	Power	----	----	----
52	AVPP2	120	BVPP2	Power	----	----	----
53	AA22	121	BA22	O TO	----	2	2
54	AA23	122	BA23	O TO	----	2	2
55	AA24	123	BA24	O TO	----	2	2
56	AA25	124	BA25	O TO	----	2	2
57	AVS2	125	BVS2	I	10KPU	----	----
58	ARESET	126	BRESET	O TO	----	2	2
59	AWAIT#	127	BWAIT#	I	----	----	----
60	AINPACK#	128	BINPACK#	I	----	----	----
61	AREG#	129	BREG#	O TO	----	2	2
62	ABVD2	130	BBVD2	I	----	----	----
63	ABVD1	131	BBVD1	I	----	----	----
64	AD8	132	BD8	I/O	----	2	2
65	AD9	133	BD9	I/O	----	2	2
66	AD10	134	BD10	I/O	----	2	2
67	ACD2#	135	BCD2#	I	----	----	----
68	GND	136	GND	Power	----	----	----

6.3.10.CRT Interface

CN11

Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	RED	O	150PD	----	----
2	GREEN	O	150PD	----	----
3	BLUE	O	150PD	----	----
4	NC	----	----	----	----
5	GND	Power	----	----	----
6	RRTN	----	----	----	----
7	GRTN	----	----	----	----
8	BRTN	----	----	----	----
9	NC	----	----	----	----
10	GND	Power	----	----	----
11	NC	----	----	----	----
12	NC	----	----	----	----
13	HSYNC	O	----	12	-4
14	VSYNC	O	----	12	-4
15	NC	----	----	----	----

6.3.11.FDD Interface

CN14

Pin	Signal Name	Type	Terminal	Drive (mA) IOL	IOH
1	NC	----	----	----	----
2	FDHIDEN	O OD	----	38	----
3	NC	----	----	----	----
4	NC	----	----	----	----
5	NC	----	----	----	----
6	NC	----	----	----	----
7	GND	Power	----	----	----
8	FDINDEX#	I	1.2KPU	----	----
9	GND	Power	----	----	----
10	FDMT1#	O OD	----	38	----
11	GND	Power	----	----	----
12	FDDS2#	O OD	----	38	----
13	GND	Power	----	----	----
14	FDDS1#	O OD	----	38	----
15	GND	Power	----	----	----
16	FDMT2#	O OD	----	38	----
17	GND	Power	----	----	----
18	FDDIR	O OD	----	38	----
19	GND	Power	----	----	----
20	FDSTEP#	O OD	----	38	----
21	GND	Power	----	----	----
22	FDWD#	O OD	----	38	----
23	GND	Power	----	----	----
24	FDWE#	O OD	----	38	----
25	GND	Power	----	----	----
26	FDTRK0#	I	1.2KPU	----	----
27	GND	Power	----	----	----
28	FDWP#	I	1.2KPU	----	----
29	GND	Power	----	----	----
30	FDRD#	I	1.2KPU	----	----
31	GND	Power	----	----	----
32	FDSIDE	O OD	----	38	----
33	GND	Power	----	----	----
34	FDDCHG#	I	1.2KPU	----	----

7.AC Characteristics

Recommended and reference values of AC characteristics for the CARDPRESSO are shown. For items other than those shown below, refer to the CARD-PC Hardware Manual.

7.1.PC CARD Interface

Calculation of PC CARD bus timing

The minimum timing factors of the PCMCIA cycle are defined as follows:

Setup timing factor: S = (Npres X Nval) + 1
Command timing factor: C = (Npres X Nval) + 1
Recovery timing factor: R = (Npres X Nval) + 1

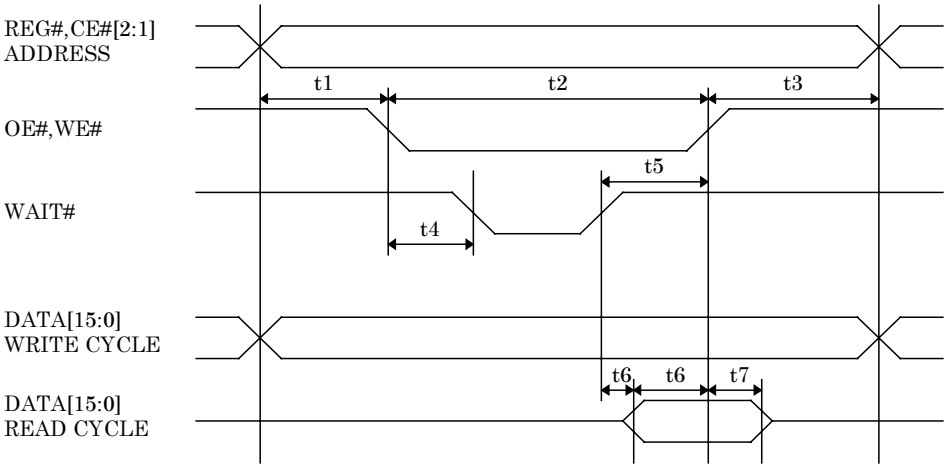
Npres (Setup Prescaler Select) and Nval (Setup Multiplier Value) for each of S, C and R are the values to which the CL_PD6720 internal registers, Setup Timing 0 Register, Command Timing 0 Register, and Recovery Timing 0 Register, are set. By default the values are set as follows. For details, refer to the CL_PD6710/PD672X Data Sheet from Cirrus Logic.

Timing Register Name	Npres	Nval
Setup timing 0	1	1
Command timing 0	1	6
Recovery timing 0	1	0

The calculation is CARD out with the internal clock period Tcp = Tclkp = 69.8 ns (Tclkp: OSC input).

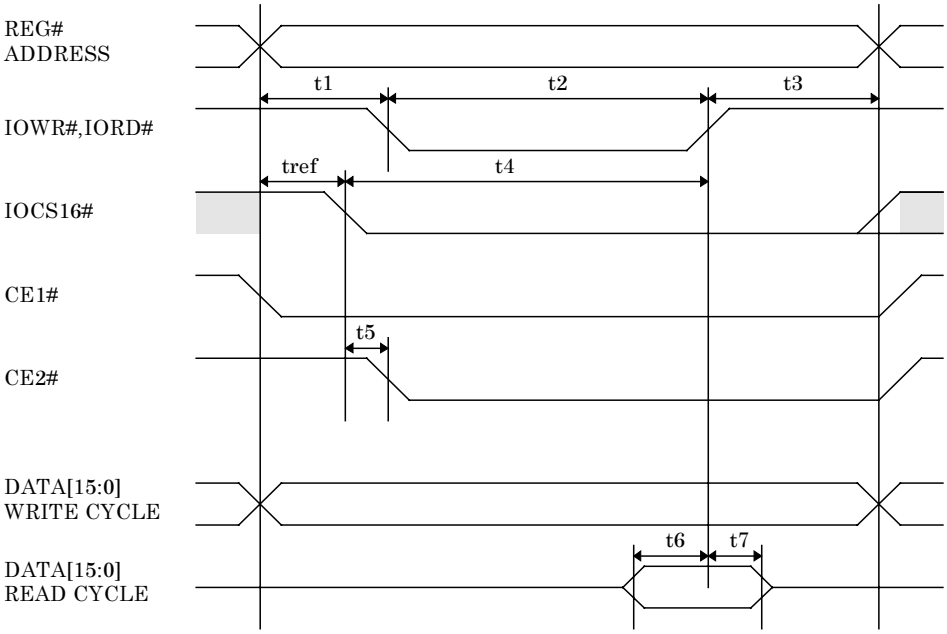
7.1.1.Memory READ / WRITE Timing

Symbol	Parameter	MIN	MAX	Units
t1	CE[2:1]#,REG#, Address, and Write Data setup to Command	(S x Tcp)-10		ns
t2	Command pulse width	(C x Tcp)-10		ns
t3	Address hold and Write Data valid from Command inactive	(R x Tcp)-10		ns
t4	WAIT# active from Command active		(C-2)Tcp-10	ns
t5	Command hold from WAIT# inactive	2Tcp		ns
t6	Data setup before OE# inactive	(2Tcp)+10		ns
t7	Data hold after OE# inactive	0		ns
t8	Data valid from WAIT# inactive	Tcp+10		ns



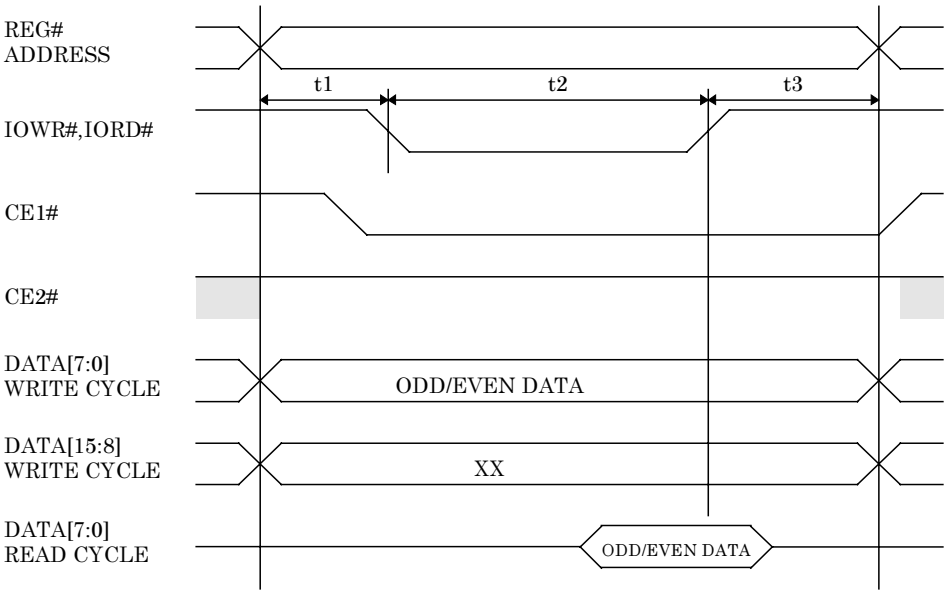
7.1.2.Word I/O READ/WRITE Timing

Symbol	Parameter	MIN	MAX	Units
t1	REG# or Address setup to Command active	(S x Tcp)-10		ns
t2	Command pulse width	(C x Tcp)-10		ns
t3	Address hold and Write Data valid from Command inactive	(R x Tcp)-10		ns
tref	CARD IOIS16# (WP pin) delay from valid Address		35	ns
t4	IOIS16# setup time before Command end	(3Tcp)+10		ns
t5	CE2# delay from IOIS16# active	Tcp-10		ns
t6	Data setup before IORD# inactive	(2Tcp)+10		ns
t7	Data hold after IORD# inactive	0		ns



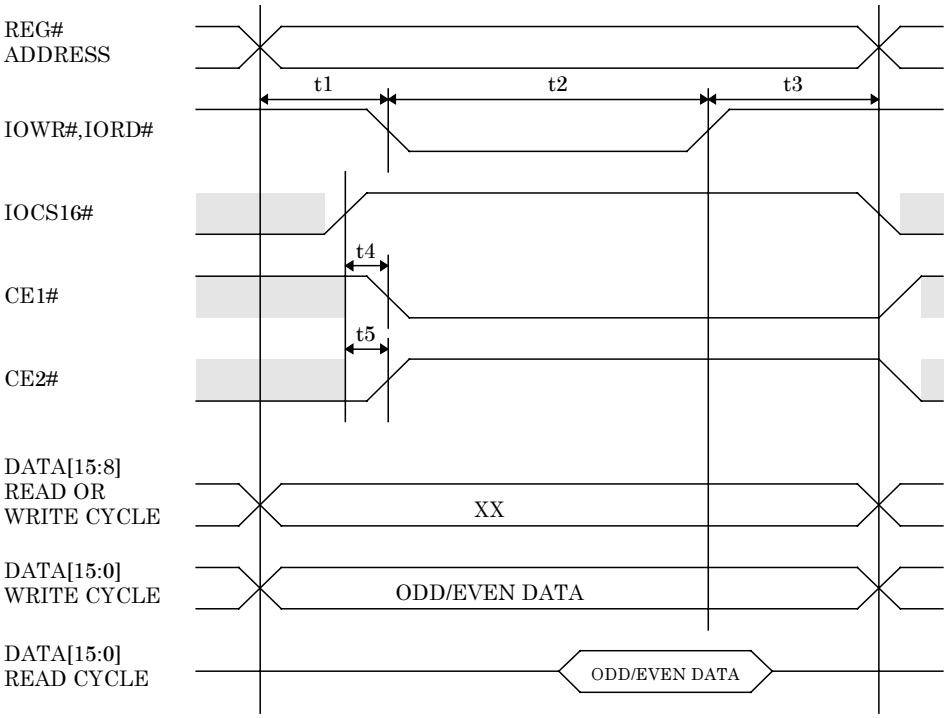
7.1.3.Byte I/O READ/WRITE Timing

Symbol	Parameter	MIN	MAX	Units
t1	Address setup to Command active	(S x Tcp)-10		ns
t2	Command pulse width	(C x Tcp)-10		ns
t3	Address hold from Command inactive	(R x Tcp)-10		ns



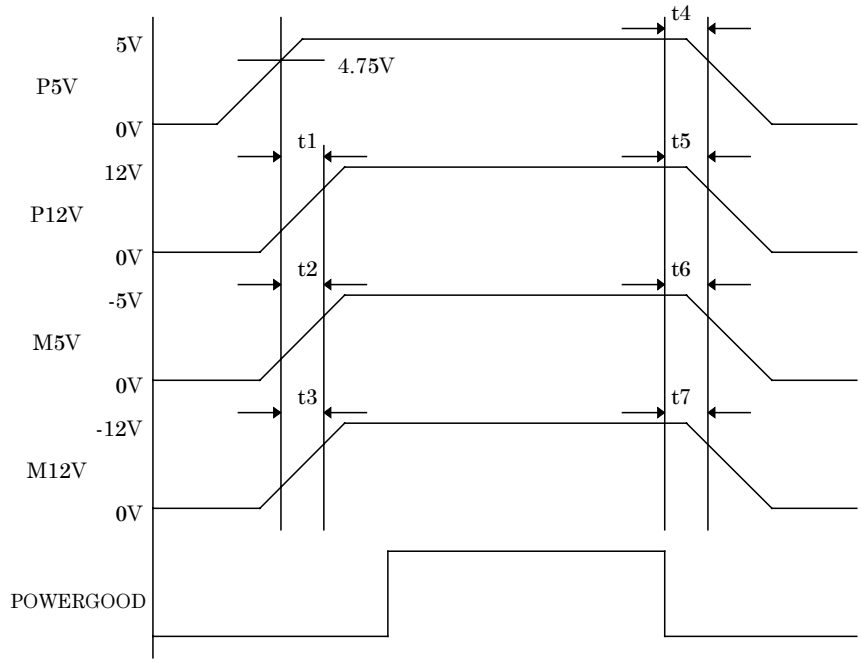
7.1.4.Odd Byte I/O READ/WRITE Timing (Word<-->Byte Conversion)

Symbol	Parameter	MIN	MAX	Units
t1	Address setup to Command active	(S x Tcp)-10		ns
t2	Command pulse width	(C x Tcp)-10		ns
t3	Address hold from Command inactive	(R x Tcp)-10		ns
t4	IOIS16# inactive to CE1# active		20	ns
t5	IOIS16# inactive to CE2# inactive		20	ns



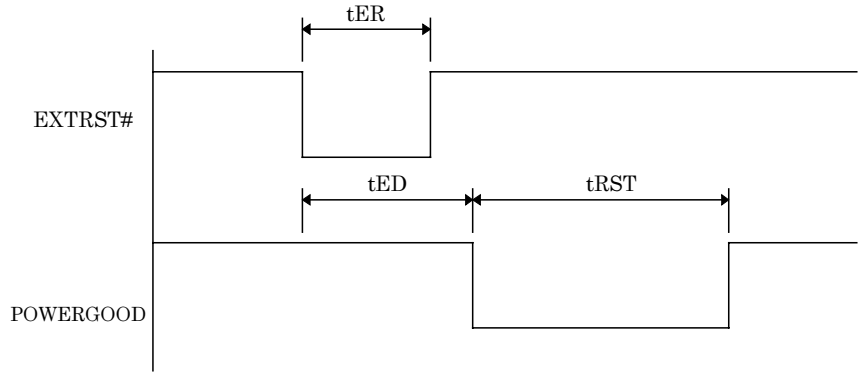
7.2.Power Supply Sequence

Symbol	Parameter	MIN	MAX	Units
t1	P12V ramp to 11.6V from 4.75V of P5V	0	200	ms
t2	M5V ramp to -4.75V from 4.75V of P5V	0	200	ms
t3	M12V ramp to -11.6V from 4.75V of P5V	0	200	ms
t4	POWERGOOD Inactive Setup Time to 4.75V of P5V when P5V are removed	10		ms
t5	POWERGOOD Inactive Setup Time to 11.6V of P12V when P12V are removed	10		ms
t6	POWERGOOD Inactive Setup Time to -4.75V of M5V when M5V are removed	10		ms
t7	POWERGOOD Inactive Setup Time to -11.6V of M12V when M12V are removed	10		ms



7.3.External Reset Input Signal Timing

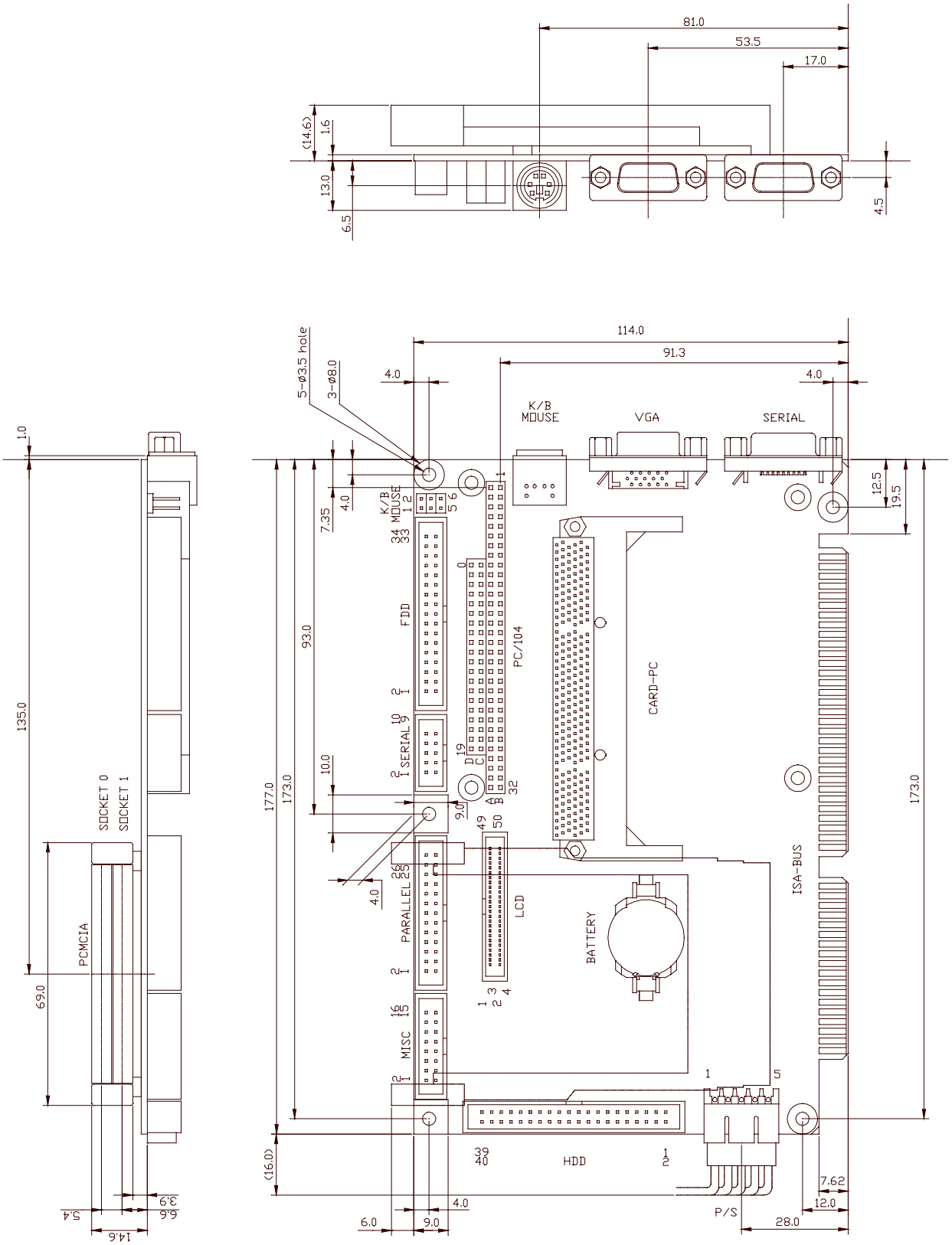
Symbol	Parameter	MIN	MAX	Units
tER	EXTRST# Pulse Width	150		ns
tED	EXTRST# POWERGOOD Delay		250	ns
tRST	Reset Time	140	280	ms



8.Physical Specification

8.1.Board Dimensional Diagram

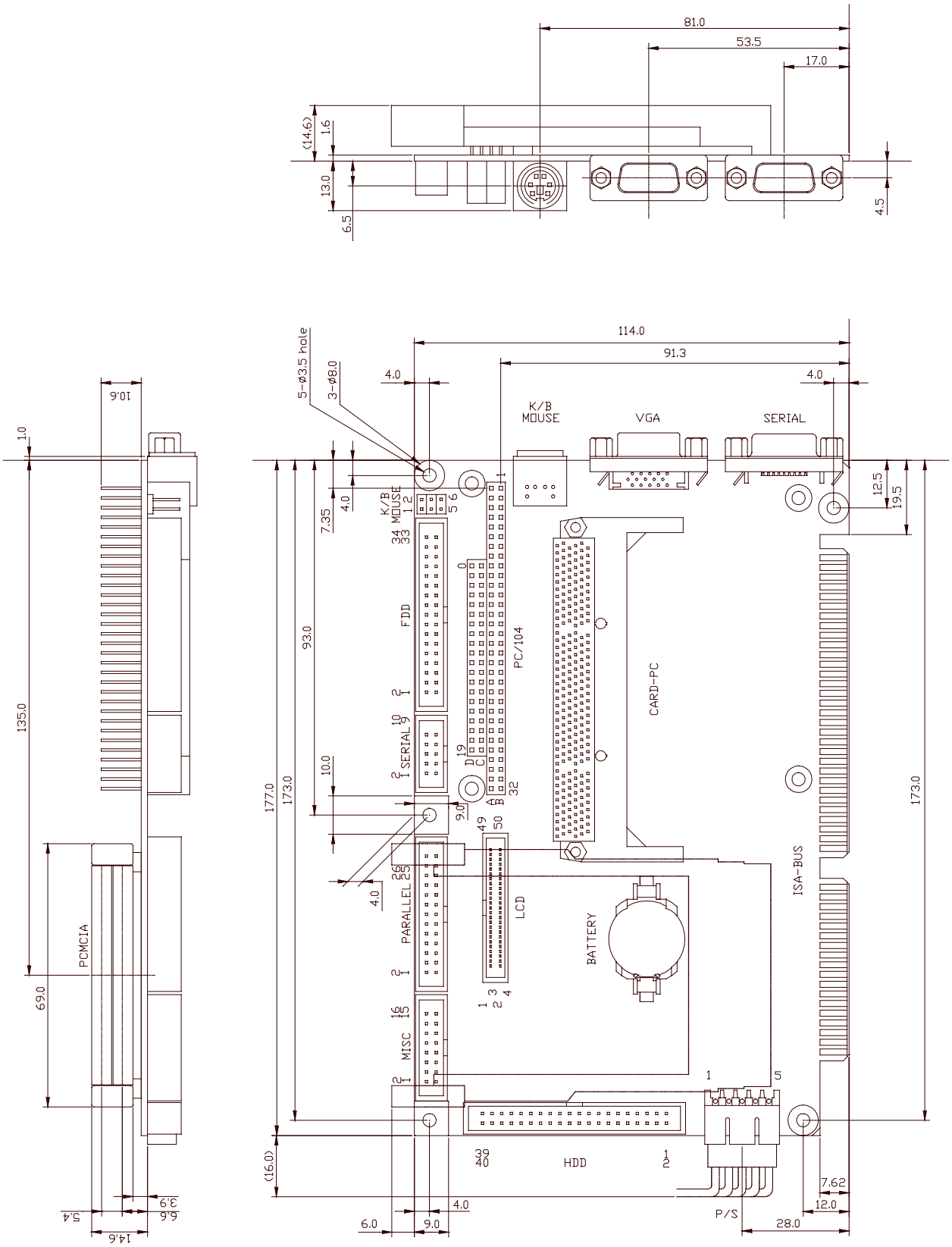
8.1.1.PC/104 Connector Short Lead Type



CARDPRESSO DIMENSIONS

Dimensions are in mm, ±0.8; Drawing is not to scale.

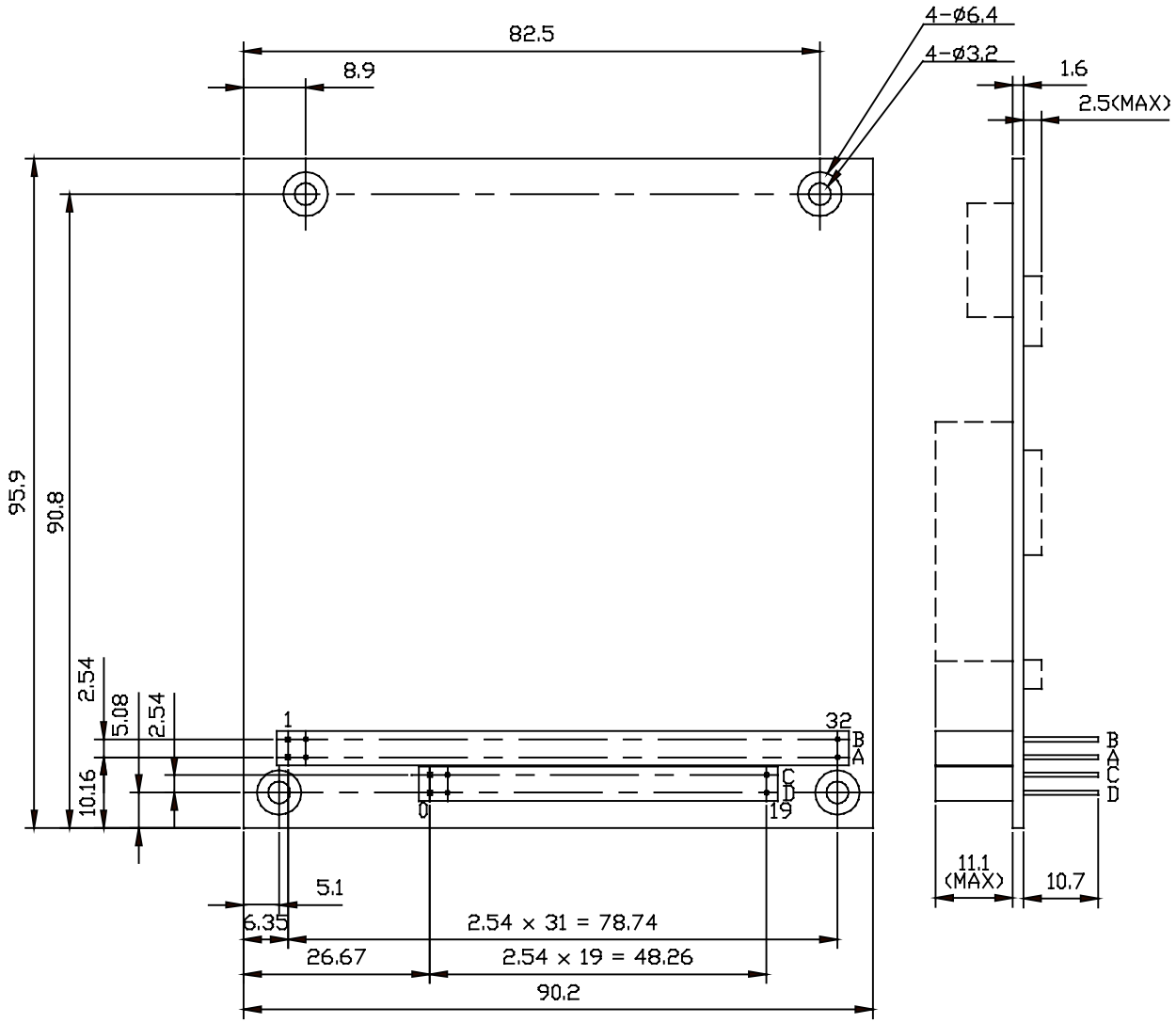
8.1.2.PC/104 Connector Long Lead Type



CARDPRESSO DIMENSIONS

Dimensions are in mm, ±0.8; Drawing is not to scale.

8.2.PC/104 Module Diagram



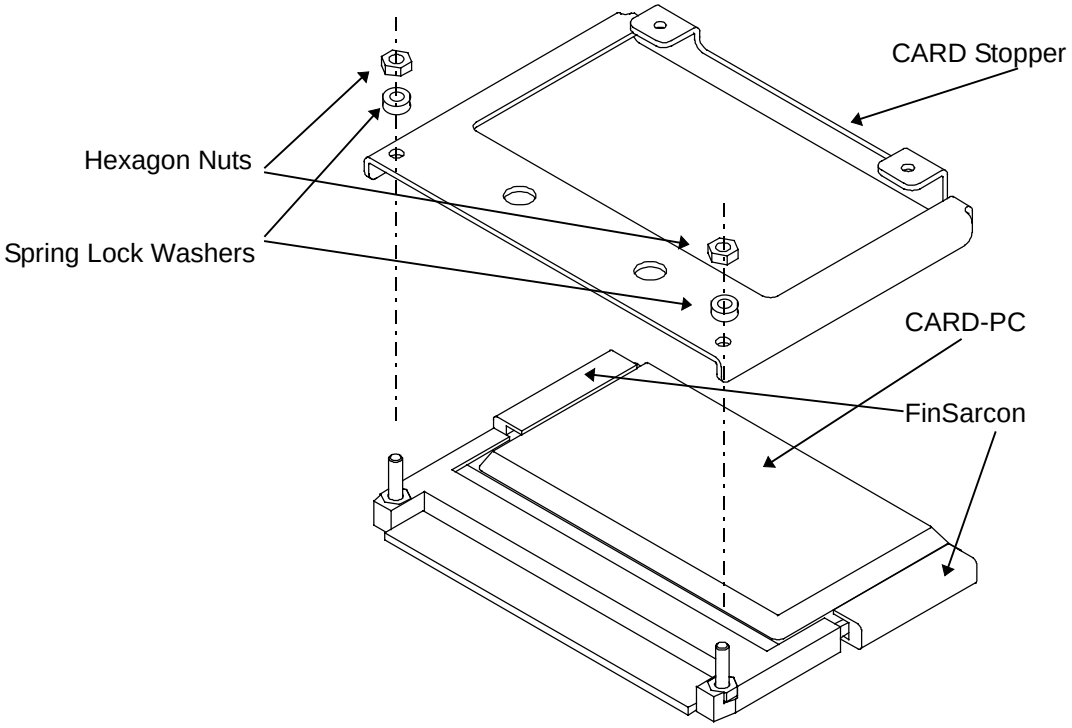
PC/104 16-BIT MODULE DIMENSIONS

Dimensions are in mm, ±0.2; Drawing is not to scale.

9.Handling Instruction

9.1.CARD Stopper Fixing Method

Refer to the following drawing.



Note
The bundled CARD stopper is only for the CARDPRESSO. The standard stoppers (SEK6675P01 and SEK6676P01) are different from it.

9.2.D-Sub Connector fixing method

CN3 (Serial Connector) and CN11 (CARD Connector) are designed assuming a plate between a cable and a connector. When use these connectors , make the plate to fix them.

10.Connector List

CARDPRESSO				Starter Kit Cable Set		
Address		Connector Part Name	Maker	Female Connector Part Name to connect CARDPRESSO	Maker	Cable
CN4	Serial(COM B) I/F	PS-10PE-D4T1-B1	JAE	PS-10SM-D4P1-1D DESP-JB9D	JAE	IW#01A
CN5	Parallel I/F	PS-26PE-D4T1-B1	JAE	PS-26SM-D4P1-1D DESP-JB25S	JAE	IW#02A
CN9	HDD I/F	PS-40PE-D4T1-B1	JAE	PS-40SM-D4P1-1D	JAE	IW#03A
CN10	Keyboard & Mouse I/F	TCS7927-56-401	HOSIDEN	23-94006-102	ASE	Y type connector
CN12	LCD I/F	TX5-50P-D2ST-N1	JAE	TX1-50S-D2P1-1D	JAE	IW#04B
CN13	Keyboard & Mouse I/F	PS-6PF-D4T1-PKL1	JAE	(PS-6SD-D4C2)	(JAE)	**
CN14	FDD I/F	PS-34PE-D4T1-B1	JAE	PS-34SM-D4P1-1D	JAE	IW#05A
CN15	Power Supply	53259-0510	MOLEX	51067-0500 15-48-0212	MOLEX	IW#06A
CN18	MISC I/F	PS-16PE-D4T1-B1	JAE	PS-16SM-D4P1-1D	JAE	IW#07A

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**
The Starter Kit does not include the cable for CN13.

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