MF1339-01

EPSON

CARD-PCI/GX

Application Note

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1. Introduction

This document contains application notes as reference for using CARD-CPI/GX to design systems.

Refer also to the CARD-PCI/GX Hardware Manual, the CARD-PCI/GX Software Manual, the Evaluation Board Hardware Manual, and the CARD-PCI/GX ROM Writer Kit Instruction Manual included in the CARD-PCI/GX ROM Writer Kit (SCE88J8X01).

2. Pin Termination

Table 2.-1, Table 2.-2, and Table 2.-3 indicate the characteristics of the CARD-PCI/GX pins and how to handle these pins when they are not used.

Table 2.-1 Names and description of symbols

Type	Indicates types of pins. I : Input O : Output OD : Open-drain output s/t/s : Sustained tri- state (PCI Ver.2.1 compliant) I/O : Bi-directional I/OD : Bi-directional open-drain output Power : Power
Termination	Indicates internal terminator resistance of pin. xxPU(5V) : Pulled up to 5V at xxΩ resistance xxPU(5VSTB) : Pulled up to V_{CCSTB} at xxΩ resistance xxPU(3.3V) : Pulled up to 3.3V at xxΩ resistance xxPD : Pulled down at xxΩ resistance External[xx] : External pull-up resistance of CARD-PCI/GX is required. Even if pull-up resistance is mounted inside CARD-PCI/GX, because the resistance value is large, some pins require external pull-up. [ ] are examples on how to handle pins.
Drive	Indicates drive current of output pins and bi-directional pins.
Power voltage	Indicates power voltage specifications for each pin. 3.3V : 3.3V tolerant 3.3V/5VT : Output = 3.3V tolerant, Input = 5V tolerant 5VSTB : V_{CCSTB} is supplied to input/output element. 5V : 5V tolerant
RESET, STANDBY	Indicates state of pins in reset or standby state. Input : Is input. HIGH or LOW input is applied from outside the CARD-PCI/GX, and the input level must be definitive. However, such confirmation is not required if the bus holder or pull-up resistance exists inside CARD-PCI/GX. Hi-Z : HIGH impedance. HIGH : Output HIGH. LOW : Output LOW. Drive : Output HIGH or LOW.
Termination of unused pins	Indicates how to handle pins when their functions are not used. For pins which require confirmation of the input level, handling outside CARD-PCI/GX is required. n.c : Left open. Pull-up(5V) : Add a pull-up resistance to between 5V and itself. Pull-up(3.3V) : Add a pull-up resistance to between 3.3V and itself.

Table 2.-2 280pin connector pins

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
1	GND	POWER	---	---	---	---	---	---
2	AD0	I/O	---	5	-2	3.3V	Drive, Drive	n.c
3	AD1	I/O	---	5	-2	3.3V	Drive, Drive	n.c
4	AD2	I/O	---	5	-2	3.3V	Drive, Drive	n.c
5	V_{CC3V}	POWER	---	---	---	---	---	---
6	AD3	I/O	---	5	-2	3.3V	Drive, Drive	n.c
7	AD4	I/O	---	5	-2	3.3V	Drive, Drive	n.c
8	AD5	I/O	---	5	-2	3.3V	Drive, Drive	n.c
9	AD6	I/O	---	5	-2	3.3V	Drive, Drive	n.c
10	AD7	I/O	---	5	-2	3.3V	Drive, Drive	n.c
11	GND	POWER	---	---	---	---	---	---
12	CBE0#	I/O	---	5	-2	3.3V	Drive, Drive	n.c
13	AD8	I/O	---	5	-2	3.3V	Drive, Drive	n.c
14	AD9	I/O	---	5	-2	3.3V	Drive, Drive	n.c
15	AD10	I/O	---	5	-2	3.3V	Drive, Drive	n.c
16	V_{CCSTB}	POWER	---	---	---	---	---	#1) V_{CC5V}
17	AD11	I/O	---	5	-2	3.3V	Drive, Drive	n.c
18	AD12	I/O	---	5	-2	3.3V	Drive, Drive	n.c
19	AD13	I/O	---	5	-2	3.3V	Drive, Drive	n.c
20	AD14	I/O	---	5	-2	3.3V	Drive, Drive	n.c
21	GND	POWER	---	---	---	---	---	---
22	AD15	I/O	---	5	-2	3.3V	Drive, Drive	n.c
23	CBE1#	I/O	---	5	-2	3.3V	Drive, Drive	n.c
24	PAR	I/O	---	5	-2	3.3V	Input, Input	n.c
25	V_{CC5V}	POWER	---	---	---	---	---	---
26	SERR#	I/OD	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	---	3.3V	Input, Input	
27	PERR#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
28	LOCK#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
29	STOP#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
30	DEVSEL#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
31	GND	POWER	---	---	---	---	---	---
32	TRDY#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
33	RESERVED	---	---	---	---	---	---	n.c
34	IRDY#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
35	V_{CC3V}	POWER	---	---	---	---	---	---
36	FRAME#	s/t/s	20kPU(3.3V), EXTERNAL [8.2kPU(3.3V)]	5	-2	3.3V	Input, Input	n.c
37	PME0#	I	4.7kPU(5VSTB)	---	---	#2) 5VSTB	Input, Input	n.c
38	CBE2#	I/O	---	5	-2	3.3V	Drive, Drive	n.c
39	AD16	I/O	---	5	-2	3.3V	Drive, Drive	n.c
40	GND	POWER	---	---	---	---	---	---
41	AD17	I/O	---	5	-2	3.3V	Drive, Drive	n.c
42	AD18	I/O	---	5	-2	3.3V	Drive, Drive	n.c
43	AD19	I/O	---	5	-2	3.3V	Drive, Drive	n.c
44	AD20	I/O	---	5	-2	3.3V	Drive, Drive	n.c
45	V_{CC3V}	POWER	---	---	---	---	---	---
46	AD21	I/O	---	5	-2	3.3V	Drive, Drive	n.c
47	AD22	I/O	---	5	-2	3.3V	Drive, Drive	n.c
48	AD23	I/O	---	5	-2	3.3V	Drive, Drive	n.c
49	CBE3#	I/O	---	5	-2	3.3V	Drive, Drive	n.c
50	GND	POWER	---	---	---	---	---	---
51	AD24	I/O	---	5	-2	3.3V	Drive, Drive	n.c
52	AD25	I/O	---	5	-2	3.3V	Drive, Drive	n.c
53	AD26	I/O	---	5	-2	3.3V	Drive, Drive	n.c
54	AD27	I/O	---	5	-2	3.3V	Drive, Drive	n.c
55	V_{CC3V}	POWER	---	---	---	---	---	---

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
56	AD28	I/O	---	5	-2	3.3V	Drive, Drive	n.c
57	AD29	I/O	---	5	-2	3.3V	Drive, Drive	n.c
58	AD30	I/O	---	5	-2	3.3V	Drive, Drive	n.c
59	AD31	I/O	---	5	-2	3.3V	Drive, Drive	n.c
60	GND	POWER	---	---	---	---	---	---
61	RST#	O	---	16	-16	3.3V	LOW, HIGH	n.c
62	INTD#	I	EXTERNAL [2.7kPU(3.3V)]	---	---	3.3V	Input, Input	Pull-up(3.3V)
63	INTC#	I	EXTERNAL [2.7kPU(3.3V)]	---	---	3.3V	Input, Input	Pull-up(3.3V)
64	INTB#	I	EXTERNAL [2.7kPU(3.3V)]	---	---	3.3V	Input, Input	Pull-up(3.3V)
65	INTA#	I	EXTERNAL [2.7kPU(3.3V)]	---	---	3.3V	Input, Input	Pull-up(3.3V)
66	V_{CC3V}	POWER	---	---	---	---	---	---
67	PCLK2	O	---	8	-8	3.3V	Drive, Drive	---
68	CPUFRQ	I	10kPU(3.3V)	---	---	3.3V	Input, Input	#3) n.c
69	PCLK0	O	---	8	-8	3.3V	Drive, Drive	n.c
70	GND	POWER	---	---	---	---	---	---
71	GND	POWER	---	---	---	---	---	---
72	PCLK1	O	---	8	-8	3.3V	Drive, Drive	n.c
73	ROMDIS	I	10KPD	---	---	5V	Input, Input	#4) n.c
74	GNT0#	O	---	5	-2	3.3V	HIGH, HIGH	n.c
75	V_{CC3V}	POWER	---	---	---	---	---	---
76	REQ0#	I	20kPU(3.3V)	---	---	3.3V	Input, Input	n.c
77	GNT1#	O	---	5	-2	3.3V	HIGH, HIGH	n.c
78	REQ1#	I	20kPU(3.3V)	---	---	3.3V	Input, Input	n.c
79	RESERVED	---	---	---	---	---	---	n.c
80	RESERVED	---	---	---	---	---	---	n.c
81	GND	POWER	---	---	---	---	---	---
82	RESERVED	---	---	---	---	---	---	---
83	KBCLK	I/OD	EXTERNAL [1.2kPU(5V)]	16	---	5V	Input, Input	Pull-up(5V)
84	KBDATA	I/OD	EXTERNAL [1.2kPU(5V)]	16	---	5V	Input, Input	Pull-up(5V)
85	V_{CCBAK}	POWER	---	---	---	---	---	#5) n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
86	MSCLK	I/OD	EXTERNAL [1.2kPU(5V)]	16	---	5V	Input, Input	Pull-up(5V)
87	MSDATA	I/OD	EXTERNAL [1.2kPU(5V)]	16	---	5V	Input, Input	Pull-up(5V)
88	PME1#	I	4.7kPU (5VSTB)	---	---	#2) 5VSTB	Input, Input	n.c
89	PORT4	I/O	EXTERNAL [10kPU(5V)]	2	-2	5V	#7) Input, Input	#6) Pull-up(5V)
90	PORT3	I/O	EXTERNAL [10kPU(5V)]	2	-2	5V	#7) Input, LOW	#6) Pull-up(5V)
91	GND	POWER	---	---	---	---	---	---
92	IRQ5	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
93	LPTBUSY	I	40KPD, EXTERNAL [4.7kPU(5V)]	---	---	5V	Input, Input	n.c
94	LPTSTROBE#	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	Input, Drive	Pull-up(5V)
95	LPTACK#	I	40kPU(5V), EXTERNAL [4.7kPU(5V)]	---	---	5V	Input, Input	n.c
96	V_{CC3V}	POWER	---	---	---	---	---	---
97	LPTSLCT	I	40KPD, EXTERNAL [4.7kPU(5V)]	---	---	5V	Input, Input	n.c
98	LPTPE	I	40kPU(5V) or 40KPD, EXTERNAL [4.7kPU(5V)]	---	---	5V	Input, Input	#8) n.c
99	LPTERROR#	I	40kPU(5V), EXTERNAL [4.7kPU(5V)]	---	---	5V	Input, Input	n.c
100	LPTINIT#	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	Input, Drive	Pull-up(5V)
101	GND	POWER	---	---	---	---	---	---
102	LPTSLCTIN#	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	Input, Drive	Pull-up(5V)

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
103	LPTAFD#	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	Input, Drive	Pull-up(5V)
104	LPTD0	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
105	LPTD1	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
106	V_{CC3V}	POWER	---	---	---	---	---	---
107	LPTD2	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
108	LPTD3	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
109	LPTD4	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
110	GND	POWER	---	---	---	---	---	---
111	LPTD5	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
112	LPTD6	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
113	LPTD7	I/OD	EXTERNAL [4.7kPU(5V)]	14	---	5V	LOW, Hi-Z	n.c
114	PWSW#	I	#9) 1MPU(5VSTB)	---	---	#2) 5VSTB	Input, Input	#9)
115	POFF	OD	#10) EXTERNAL [10kPU(5VSTB)]	14	---	#2) 5VSTB	LOW, LOW	n.c
116	V_{CC5V}	POWER	---	---	---	---	---	---
117	STANDBY#	OD	#11) EXTERNAL [4.7kPU]	16	---	5V	Hi-Z, LOW	n.c
118	USBDP1	I/O	15KPD	---	---	3.3V	Input, Drive	n.c
119	USBDM1	I/O	15KPD	---	---	3.3V	Input, Drive	n.c
120	GND	POWER	---	---	---	---	---	---
121	USBDP0	I/O	15KPD	---	---	3.3V	Input, Drive	n.c
122	USBDM0	I/O	15KPD	---	---	3.3V	Input, Drive	n.c
123	USBCUR#	I	EXTERNAL [10kPU(5V)]	---	---	3.3V/5VT	Input, Input	Pull-up(5V)
124	USBON	O	---	4	-4	3.3V	LOW, Drive	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
125	V_{CC3V}	POWER	---	---	---	---	---	---
126	PCBEEP	O	---	4	-4	3.3V	Drive, Drive	n.c
127	AC97SDOUT	O	---	4	-4	3.3V	Drive, Drive	n.c
128	AC97SDIN0	I	15KPD	---	---	3.3V/5VT	Input, Input	n.c
129	AC97BITCLK	I	15KPD	---	---	3.3V/5VT	Input, Input	n.c
130	GND	POWER	---	---	---	---	---	---
131	AC97SYNC	O	---	4	-4	3.3V	Drive, Drive	n.c
132	AC97RESET#	O	---	16	-16	3.3V	LOW, HIGH	n.c
133	RESERVED	---	---	---	---	---	---	n.c
134	CRTVSYNC	O	---	16	-16	3.3V	LOW, LOW	n.c
135	CRTHSYNC	O	---	16	-16	3.3V	LOW, LOW	n.c
136	V_{CC3V}	POWER	---	---	---	---	---	---
137	CRTB	O	75PD	---	---	---	---	n.c
138	CRTG	O	75PD	---	---	---	---	n.c
139	CRTR	O	75PD	---	---	---	---	n.c
140	GND	POWER	---	---	---	---	---	---
141	GND	POWER	---	---	---	---	---	---
142	FPDOTE	O	---	8	-8	3.3V	LOW, LOW	n.c
143	FPVEEON	O	---	8	-8	3.3V	LOW, LOW	n.c
144	RESERVED	---	---	---	---	---	---	n.c
145	GND	POWER	---	---	---	---	---	---
146	FPVSYNC	O	---	8	-8	3.3V	LOW, LOW	n.c
147	FPDATA0	O	---	8	-8	3.3V	LOW, LOW	n.c
148	FPHSYNC	O	---	8	-8	3.3V	LOW, LOW	n.c
149	FPDATA1	O	---	8	-8	3.3V	LOW, LOW	n.c
150	FPDATA2	O	---	8	-8	3.3V	LOW, LOW	n.c
151	GND	POWER	---	---	---	---	---	---
152	FPDATA3	O	---	8	-8	3.3V	LOW, LOW	n.c
153	FPDISPEN	O	---	8	-8	3.3V	LOW, LOW	n.c
154	FPDATA4	O	---	8	-8	3.3V	LOW, LOW	n.c
155	FPDATA5	O	---	8	-8	3.3V	LOW, LOW	n.c
156	FPDATA6	O	---	8	-8	3.3V	LOW, LOW	n.c
157	FPDATA7	O	---	8	-8	3.3V	LOW, LOW	n.c
158	FPDATA8	O	---	8	-8	3.3V	LOW, LOW	n.c
159	FPDATA9	O	---	8	-8	3.3V	LOW, LOW	n.c
160	FPDATA10	O	---	8	-8	3.3V	LOW, LOW	n.c
161	GND	POWER	---	---	---	---	---	---

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
162	FPDATA11	O	---	8	-8	3.3V	LOW, LOW	n.c
163	FPDATA12	O	---	8	-8	3.3V	LOW, LOW	n.c
164	FPDATA13	O	---	8	-8	3.3V	LOW, LOW	n.c
165	FPDATA14	O	---	8	-8	3.3V	LOW, LOW	n.c
166	FPDATA15	O	---	8	-8	3.3V	LOW, LOW	n.c
167	FPDATA16	O	---	8	-8	3.3V	LOW, LOW	n.c
168	FPDATA17	O	---	8	-8	3.3V	LOW, LOW	n.c
169	RESERVED	---	---	---	---	---	---	n.c
170	RESERVED	---	---	---	---	---	---	n.c
171	GND	POWER	---	---	---	---	---	---
172	RESERVED	---	---	---	---	---	---	n.c
173	RESERVED	---	---	---	---	---	---	n.c
174	RESERVED	---	---	---	---	---	---	n.c
175	V_{CCCORE}	POWER	---	---	---	---	---	---
176	V_{CCCORE}	POWER	---	---	---	---	---	---
177	V_{CCCORE}	POWER	---	---	---	---	---	---
178	V_{CCCORE}	POWER	---	---	---	---	---	---
179	RESERVED	---	---	---	---	---	---	n.c
180	GND	POWER	---	---	---	---	---	---
181	MEMCS16#	I	1kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
182	RESERVED	---	---	---	---	---	---	n.c
183	V_{CCCORE}	POWER	---	---	---	---	---	---
184	V_{CCCORE}	POWER	---	---	---	---	---	---
185	V_{CCCORE}	POWER	---	---	---	---	---	---
186	V_{CCCORE}	POWER	---	---	---	---	---	---
187	RESERVED	---	---	---	---	---	---	n.c
188	ROMCS#	O	---	4	-4	3.3V	HIGH, HIGH	n.c
189	MEMW#	O	4.7kPU(5V)	8	-8	3.3V/5VT	HIGH, HIGH	n.c
190	GND	POWER	---	---	---	---	---	---
191	MEMR#	O	4.7kPU(5V)	8	-8	3.3V/5VT	HIGH, HIGH	n.c
192	SA16	O	20kPU(3.3V)	8	-8	3.3V	LOW, Drive	n.c
193	SA17	O	20kPU(3.3V)	8	-8	3.3V	LOW, Drive	n.c
194	SA18	O	20kPU(3.3V)	8	-8	3.3V	LOW, Drive	n.c
195	SA19	O	20kPU(3.3V)	8	-8	3.3V	LOW, Drive	n.c
196	AEN	O	---	8	-8	3.3V	LOW, LOW	n.c
197	SBHE#	O	20kPU(3.3V)	8	-8	3.3V	LOW, Drive	n.c
198	IRQ10	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
199	IRQ11	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
200	GND	POWER	---	---	---	---	---	---
201	IRQ9	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
202	COM2CTS#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
203	COM2CD#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
204	COM2DSR#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
205	COM2DTR#	O	10kPU(5V)	12	-6	#12) 5V	Hi-Z, Drive	n.c
206	COM2RI#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
207	COM2RTS#	O	---	12	-6	#12) 5V	Drive, Drive	n.c
208	COM2RXD	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
209	COM2TXD	O	---	12	-6	#12) 5V	Drive, Drive	n.c
210	GND	POWER	---	---	---	---	---	---
211	GND	POWER	---	---	---	---	---	---
212	COM1TXD	O	---	12	-6	#12) 5V	Drive, Drive	n.c
213	COM1RXD	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
214	COM1RTS#	O	10kPU(5V)	12	-6	#12) 5V	Hi-Z, Drive	n.c
215	COM1RI#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
216	COM1DTR#	O	10kPU(5V)	12	-6	#12) 5V	Hi-Z, Drive	n.c
217	COM1DSR#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
218	COM1CD#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
219	COM1CTS#	I	---	---	---	#12) 5V	Input, Input	Pull-up(5V)
220	SALATCH	O	---	4	-4	3.3V	LOW, LOW	n.c
221	GND	POWER	---	---	---	---	---	---
222	SD7/SA7	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
223	SD6/SA6	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
224	SD5/SA5	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
225	SD4/SA4	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
226	SD3/SA3	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
227	SD2/SA2	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
228	SD1/SA1	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
229	SD0/SA0	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
230	SD8/SA8	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
231	GND	POWER	---	---	---	---	---	---
232	SD9/SA9	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
233	V_{CCCORE}	POWER	---	---	---	---	---	---
234	SD10/SA10	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
235	SD11/SA11	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
236	SD12/SA12	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
237	SD13/SA13	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
238	SD14/SA14	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c
239	SD15/SA15	I/O	20kPU(3.3V), EXTERNAL [4.7kPU(5V)]	8	-8	3.3V/5VT	Input, Input	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
240	IOR#	O	4.7kPU(5V)	8	-8	3.3V/5VT	HIGH, HIGH	n.c
241	GND	POWER	---	---	---	---	---	---
242	IOW#	O	4.7kPU(5V)	8	-8	3.3V/5VT	HIGH, HIGH	n.c
243	V_{CCCORE}	POWER	---	---	---	---	---	---
244	IOCHRDY	I	1kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
245	IOCS16#	I	1kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
246	POWERGOOD	I	---	---	---	3.3V	Input, Input	#13) Can not be unused
247	IDEINT	#14) I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
248	IDERDY	I	1kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
249	IDEDRQ	I	10KPD	---	---	3.3V/5VT	Input, Input	n.c
250	GND	POWER	---	---	---	---	---	---
251	IDEA0	O	---	8	-8	3.3V	Drive, Drive	n.c
252	IDEA1	O	---	8	-8	3.3V	Drive, Drive	n.c
253	IDEA2	O	---	8	-8	3.3V	Drive, Drive	n.c
254	IDED15	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
255	IDED0	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
256	IDED14	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
257	IDED1	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
258	IDED13	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
259	IDED2	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
260	GND	POWER	---	---	---	---	---	---
261	IDED12	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
262	IDED3	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
263	IDED11	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
264	IDED4	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
265	IDED10	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
266	IDECS3FX#	O	---	8	-8	3.3V	HIGH, HIGH	n.c
267	IDED5	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
268	IDERESET#	O	---	8	-8	3.3V	LOW, HIGH	n.c
269	IDED9	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
270	GND	POWER	---	---	---	---	---	---
271	IDED6	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
272	IDED8	I/O	---	8	-8	3.3V/5VT	Drive, Drive	n.c
273	IDECS1FX#	O	---	8	-8	3.3V	HIGH, HIGH	n.c
274	IDED7	I/O	10kPD	8	-8	3.3V/5VT	Drive, Drive	n.c
275	IDEACK#	O	---	8	-8	3.3V	HIGH, HIGH	n.c

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
276	IDEIOW#	O	---	8	-8	3.3V	HIGH, HIGH	n.c
277	IDEIOR#	O	---	8	-8	3.3V	HIGH, HIGH	n.c
278	FPVDDON	O	---	8	-8	3.3V	LOW, LOW	n.c
279	FPDOTCLK	O	---	8	-8	3.3V	LOW, LOW	n.c
280	GND	POWER	---	---	---	---	---	---

Table 2.-3 FFC connector pins

Pin	Name	Type	Termination	Drive (mA)		Power voltage	RESET, STANDBY	Termination of unused pins
				I_{OL}	I_{OH}			
1	DSKCHG#	I	1kPU(5V)	---	---	5V	Input, Input	n.c
2	WP#	I	1kPU(5V)	---	---	5V	Input, Input	n.c
3	INDEX#	I	1kPU(5V)	---	---	5V	Input, Input	n.c
4	TRK0#	I	1kPU(5V)	--	---	5V	Input, Input	n.c
5	RDATA#	I	1kPU(5V)	---	---	5V	Input, Input	n.c
6	DENSEL	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
7	WGATE#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	HIGH, HIGH	n.c
8	HDSEL	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
9	STEP#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
10	DIR#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
11	WDATA#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
12	DR0#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	Drive, Drive	n.c
13	MTR0#	O	#15) EXTERNAL [4.7kPU(5V)]	40	-4	5V	HIGH, HIGH	n.c
14	GND	POWER	---	---	---	---	---	---
15	IRQ15	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
16	IRQ7	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
17	GND	POWER	---	---	---	---	---	---
18	IRQ14	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c
19	GND	POWER	---	---	---	---	---	---
20	IRQ3	I	10kPU(5V)	---	---	3.3V/5VT	Input, Input	n.c

#1) Connect V_{CC5V} if power management is not available.

#2) It operates at V_{CCSTB} for system power control signal. To maintain compatibility with the CARD-PCI/GX series and for enabling the mother board to be shared, set the input level to LOW or " Hi-Z ". If V_{CCSTB} is not available, it operates at V_{CC5V} via connection of #1).

#3) Settings are different depending on each model of the CARD-PCI/GX series. The CPU clock speed for 200 MHz cards is unconnected (HIGH input from internal pull-up resistance). Refer to the CARD-PCI/GX Hardware Manual for more details.

#4) It starts from the external BIOS ROM at HIGH input, or BIOS ROM of CARD-PCI/GX at LOW input. Because it is pulled down inside CARD-PCI/GX, if connection is not made, it starts from the BIOS ROM of CARD-PCI/GX.

#5) Because a circuitry for switching the system power (V_{CC3V}) is mounted to CARD-PCI/GX, if backup of CMOS RAM is not required, then there will be no problem when connection is not made.

#6) By using software to set the I/O port built into CARD-PCI/GX, the input/output is confirmed. Because the default setting after power is supplied is input, it becomes necessary to mount a pull-up resistance outside CARD-PCI/GX.

#7) This is the default setting of standard BIOS. Setting of Input/Output/Hi-Z can be made using software.

#8) By default, BIOS is set to pull-up.

#9) Input at the timing described in Fig. 3-5 is necessary. Also, even when it is not used, the pin must be handled in the way described in Fig. 3-6

#10) If power is controlled through use of POFF, then connecting the pull-up resistance to V_{CCSTB} is necessary.

#11) Pull up at a power (V_{CC3V}/V_{CC5V}/V_{CCSTB}) suitable for circuit with STANDBY# signal. In the standby mode, V_{CC3V} and V_{CC5V} are not cut off.

#12) Use a COM port driver which operates at 5V or 3.3V, and has 5V tolerant.

#13) Can not be unused. When POWERGOOD becomes inactive, reset occurs at CARD-PCI/GX.

#14) Connected to IRQ14 inside CARD-PCI/GX.

#15) If pull-up resistance is not mounted to the FDD, place a pull-up resistance of about 4.7 K□ between it and V_{CC5V}. If a pull-up resistance is mounted to the FDD, there is no need to place a pull-up resistance to the mother board. Also, this signal is not "OD".

3. Power

This chapter explains the provisions on the POWER ON sequence, and CMOS RAM and RTC backup battery circuitry built into CARD-PCI/GX.

3.1. POWER ON Sequence

This section describes systems where 5V standby power (V_{CCSTB}) is supplied, as well as systems where the power is not supplied

3.1.1. Power sequence of systems with V_{CCSTB} power supplied

Fig. 3-1 shows the power sequence for systems where V_{CCSTB} power (5V standby power) such as ATX power is supplied. In this case, when the power is ON, if CARD-PCI/GX is not reset, the system can not start up normally. As indicated in the figure, after V_{CC5V} / V_{CCCORE} / V_{CC3V} reach the specified power voltage, an input to have the POWERGODD signal become LOW for at least 10 msec is necessary.
When the ATX power supply unit is used, it is possible to use the PWSW# signal to control the ON/OFF of the system. Connect the POWER ON switch to the PWSW# pin (CARD-PCI/GX, 114pin), and connect the POFF signal output (CARD-PCI/GX, 115pin) to the PS-ON pin of the ATX power supply unit. With the fall edge of the PWSW# signal, the POFF signal goes into the LOW level, and V_{CC5V} / V_{CC3V} is supplied.

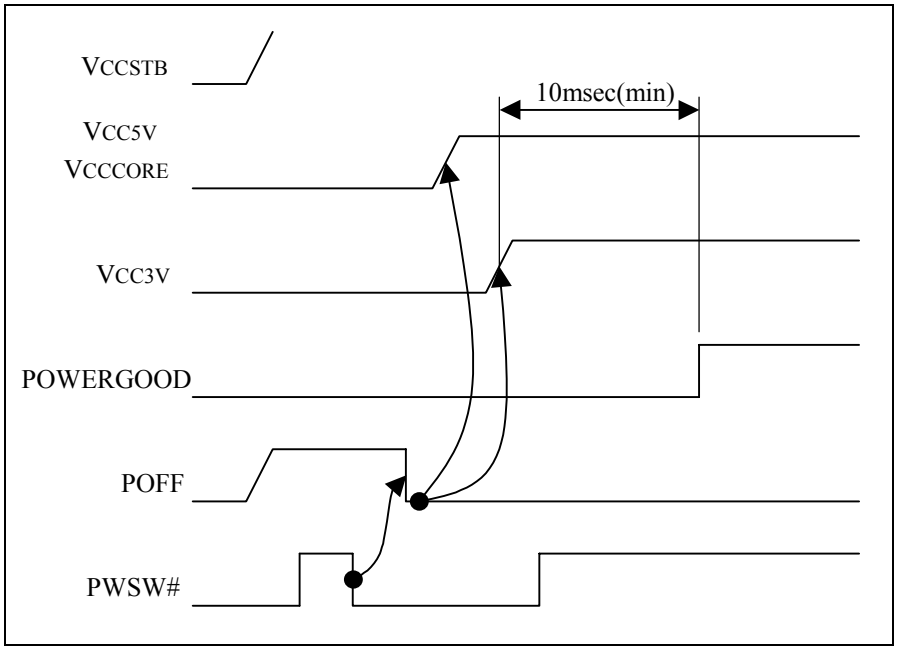


Fig. 3-1 Power ON sequence (in the case where the V_{CCSTB} power is supplied)

To turn the power OFF, the fall edge of the PWSW# signal is also required. With the fall edge of the PWSW# signal, the POFF signal goes into the HIGH level output, and VCC5V / VCC3V becomes OFF. (See Fig. 3-2.)

For this reason, turning the power from ON to OFF while the PWSW# signal at the LOW level can not be done.

Follow Fig. 3-3 and set the PWSW# signal to pulse input.

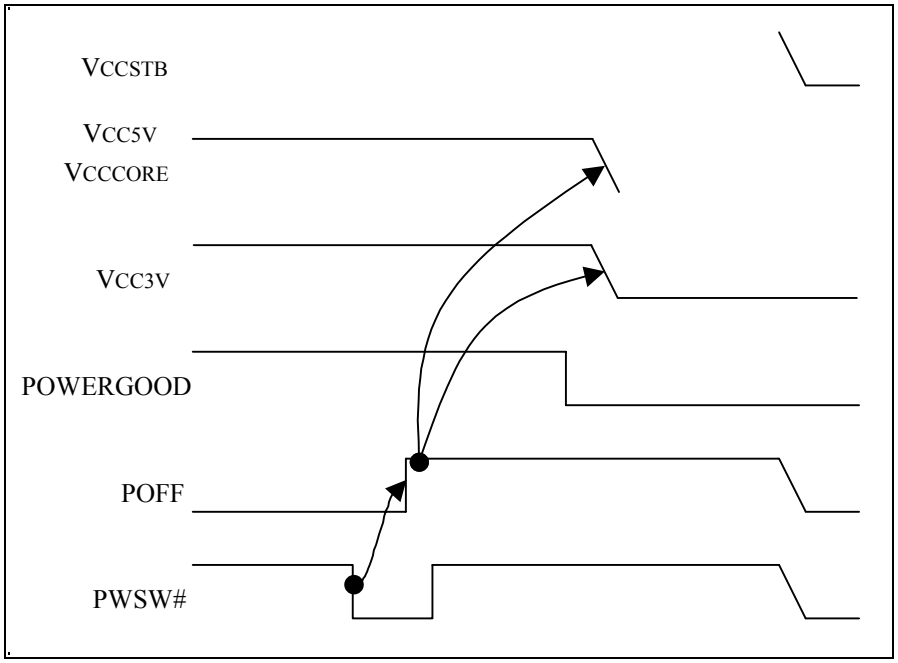


Fig. 3-2 Power OFF sequence (where the VCCSTB power is supplied)

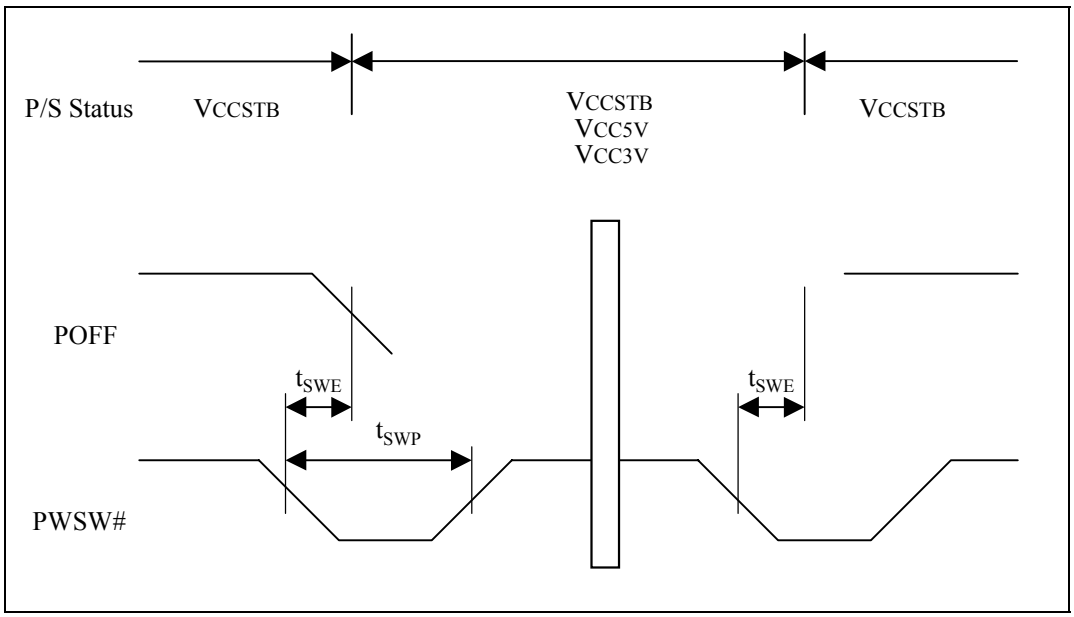


Fig. 3-3 Timing of the PWSW# and POFF signals

Symbol	Parameter	Min.	Max.	Unit
t_{SWE}	Delay from PWSW# Event to POFF	14	16	msec
t_{SWP}	PWSW# Pulse Width	16		msec

3.1.2. Power sequence of systems where the VCCSTB power is not supplied

Fig. 3-4 shows the power sequence of systems where VCCSTB (5V standby power) is not supplied such as the AT power supply unit.

Connect the VCCSTB pin of CARD-PCI/GX to VCC5V. When it is connected, delay the PWSW# signal by more than 20 msec after the rise of VCCSTB, as described in Fig. 3-5. If the delay is less than 20 msec, CARD-PCI/GX may not function normally. Fig. 3-6 shows an example of the PWSW# signal generation circuitry. While it is possible to connect a SUSPEND/RESUME switch to the PWSW# pin, in this example the PWSW# pin is not used. Also, use the POFF signal as unconnected.

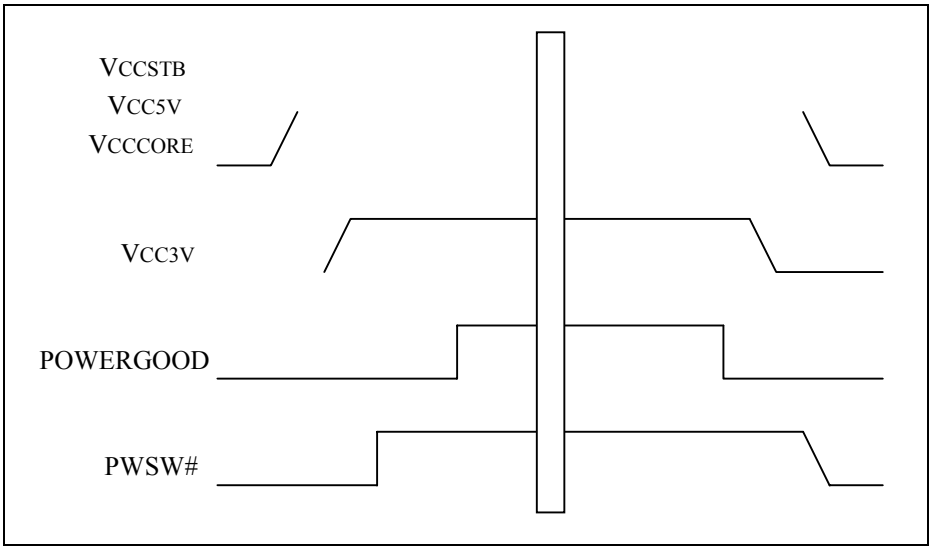


Fig. 3-4 Power sequence (where the VCCSTB power is not supplied and VCCSTB pin =VCC5V)

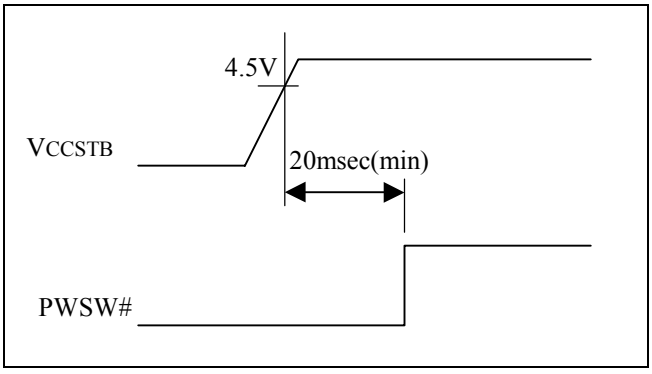


Fig. 3-5 Timing of VCCSTB and PWSW# signals (VCCSTB pin =VCC5V)

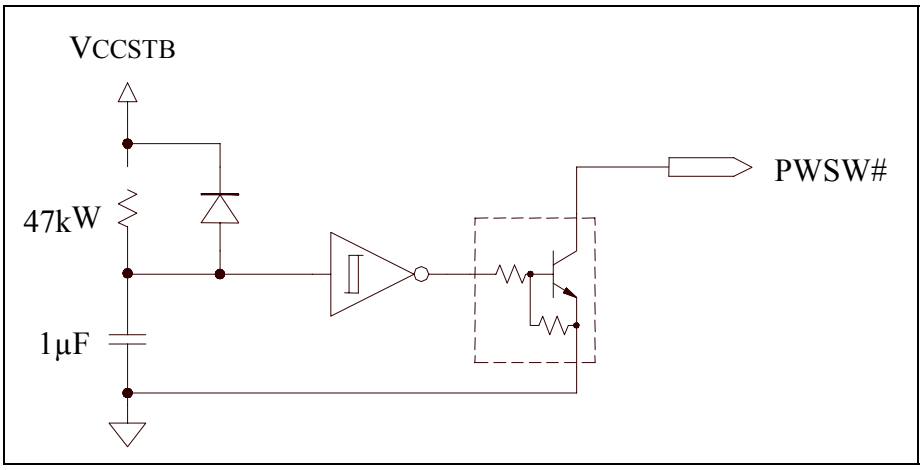


Fig. 3-6 PWSW# pin handling method (VCCSTB pin =VCC5V)

3.1.3. Timing of VCCCORE and VCC3V

Design the power so that when turning the power ON/OFF basically the condition VCCCORE ≥ VCC3V is satisfied, as shown in Fig. 3-7. If for some reason the power can not be designed to satisfy this condition, follow the provisions described in Fig. 3-8.

According to the provisions on CPU's power sequence, when VCCCORE is not supplied, if VCC3V is supplied a peak current of 1.8 A flows to VCC3V. If this situation continues for a long time, the CPU will become damaged in the worse case. Also, if the power capacity has no room, problem may occur so that the system can not start. Therefore, be aware of this problem.

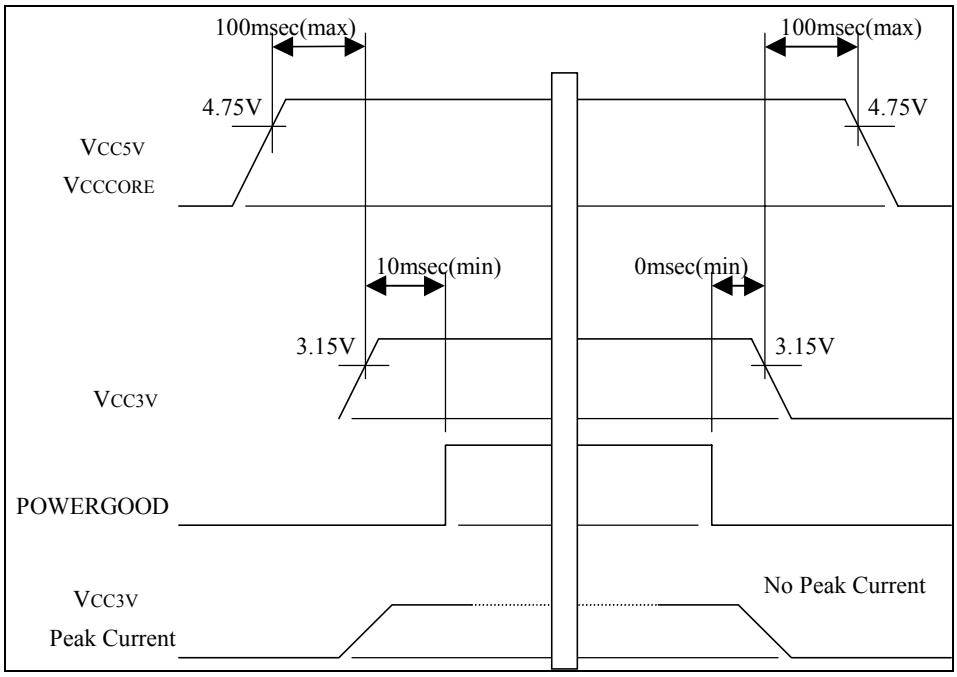


Fig. 3-7 Timing of VCCCORE and VCC3V 1

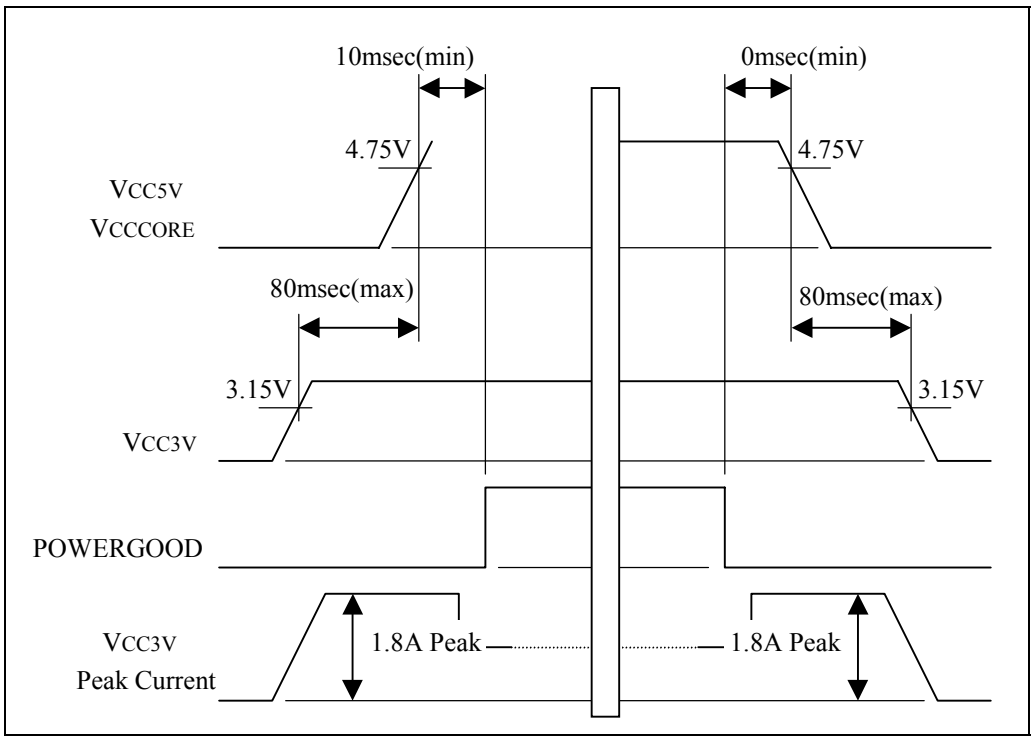


Fig. 3-8 Timing of VCCCORE and VCC3V 2

3.2. RTC Backup Circuitry

The RTC and CMOS RAM built into CARD-PCI/GX have backup power supplied from external sources even when the system's power is OFF, and therefore data can be kept.

3.2.1. Backup power

VCCBAK is a power pin for backup of RTC (Real Time Clock) and CMOS RAM. When CARD-PCI/GX is not supplied with power (power to the VCCSTB pin), in other words when it is OFF, power will be supplied from the backup power source (lithium battery, etc.)

(∗Caution)

To use lithium battery as the backup power, be sure to also design reversed current protection circuitry into the system.

Because a power switch circuitry is built into CARD-PCI/GX to switch between the system power and the backup power, there is no need to design such switch externally. Also, if backup for RTC and CMOS RAM is not required, set the VCCBAK pin as unconnected. In the standard design of CARD-PCI/GX's BIOS, backup of RTC and CMOS RAM is used; therefore, when the backup is not used, use of the modifying tool (ROM ADAPTATION KIT) to modify the BIOS is necessary. Refer to the CARD-PCI/GX Software Manual for details.

3.2.2. Precision of RTC

The precision of CARD-PCI/GX's RTC is approximately within ±100ppm (±8.6 sec/day). If the system requires a more accurate timing function, connect RTC externally, etc. to provide such function.

The precision of the RTC depends on the vibrating frequency of the crystal oscillator of the RTC. For crystal oscillator, at room temperature, the vibration frequency has tolerance, and varies according to change in temperature. The frequency tolerance at room temperature is approximately ±50ppm. The relationship between temperature and frequency is a 2-dimentional curve shown in Fig. 3-9. The frequency is the highest at about 25 °C; when the temperature changes the frequency decreases. When compared with the frequency at room temperature, the frequency at the upper limit of the operating temperature range of CARD-PCI/GX is lower by approximately 70ppm. Also, when compared with the frequency at room temperature, the frequency at around 0 °C is lower by approximately 20ppm. Therefore, the overall precision of the RTC is approximately ±100ppm.

Usually, as the CARD-PC itself generates heat the temperature increases, generally causing the RTC to become late in most cases. When it is placed at room temperature with the power OFF, the error deviation

is smaller than when it is operating.

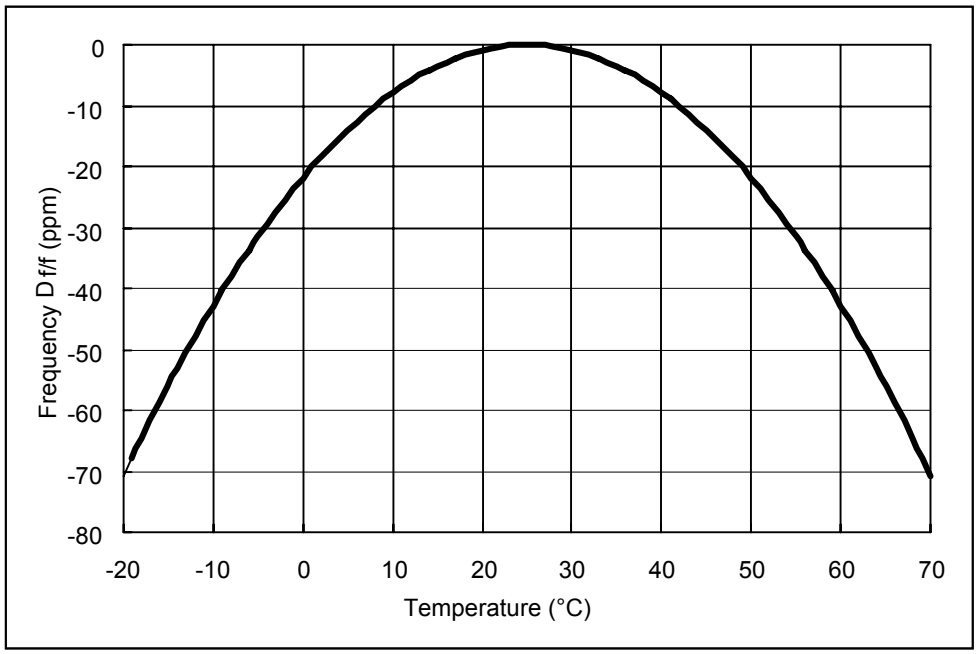


Fig. 3-9 Relationship between temperature and frequency

4. Updating BIOS

This section describes method to use for programming the BIOS image modified using the BIOS modifying tool (ROM ADAPTATION KIT), into the BIOS ROM of CARD-PCI/GX.

There are two methods in such programming, both methods are done with the system which the target CARD-PCI/GX is connected. Table 4-1 shows a comparison of the two methods.

Table 4-1 Comparing re-writing methods

	Rewrite using a utility software	Rewrite using the ROM Writer Kit
Time required for rewrite	Depends on system configuration	About 10 seconds
If rewrite fails, is recovery possible?	No	Yes
Required peripherals	Keyboard, display, FDD or HDD drive where DOS can bootup	None
Restrictions on design	Interfaces required for keyboard, display, FDD or HDD drive where DOS can bootup	Interface for ROM Writer Board connection is required

4.1. Rewrite Using the Utility Software

This method involves booting up DOS with the BIOS inside CARD-PCI/GX to update the BIOS ROM in CARD-PCI/GX itself. This requires the use of AWDFLASH.EXE included in the BIOS modifying tool (ROM ADAPTATION KIT) to perform the rewrite operation. If the rewrite operation fails, then the recovery operation is required, using the method describes in "4.2 Rewriting using the ROM Writer Kit (SCE88J8X01)". Use the following procedure to rewrite the BIOS.

Step1. Connect CARD-PCI/GX to the system.

Step2. Exclude AUTOEXEC.BAT and CONFIG.SYS and bootup DOS.

Step3. Use AWDFLASH.EXE to update the BIOS ROM, as follows:

AWDFLASH FileName /py/Tiny/cp/cd/cc/LD/F

Where FileName = name of BIOS binary for writing to BIOS ROM

When the write operation is finished, reboot the system and the updated BIOS will function. For details, refer to the CARD-PCI/GX Software Manual.

4.2. Rewriting using the ROM Writer Kit (SCE88J8X01)

The ROM Writer Kit (SCE88J8X01) is a kit for updating content of the BIOS ROM of CARD-PCI/GX. This kit contains ROM Writer Board, a cable, and a instruction manual.

ROM Writer Board makes use of a cable set to connect to the system (or mother board) which has the target CARD-PCI/GX connected, and performs updating the BIOS ROM content. For this reason, it is necessary to design an interface connector for connecting ROM Writer Board to your system. ROM Writer Board contains a master BIOS ROM for updating and a ROM for booting ROM Writer. When power is turned ON with ROM Writer Board being connected to the target system, the BIOS ROM of CARD-PCI/GX on the target is automatically updated. Table 4-2 shows the interface connector of ROM Writer Board.

Table 4-2 Interface connector of the ROM Writer Board

Pin	Name	Type	CARD-PCI/GX pin #	Function
1	VCC5V	POWER		+5V
2	SD0/SA0	I/O	229	Data & Address Bit 0
3	SD1/SA1	I/O	228	Data & Address Bit 1
4	SD2/SA2	I/O	227	Data & Address Bit 2
5	VCC5V	POWER		+5V
6	SD3/SA3	I/O	226	Data & Address Bit 3
7	SD4/SA4	I/O	225	Data & Address Bit 4
8	SD5/SA5	I/O	224	Data & Address Bit 5
9	VCC5V	POWER		+5V
10	SD6/SA6	I/O	223	Data & Address Bit 6
11	SD7/SA7	I/O	222	Data & Address Bit 7
12	SD8/SA8	I/O	230	Data & Address Bit 8
13	VCC5V	POWER		+5V
14	SD9/SA9	I/O	232	Data & Address Bit 9
15	SD10/SA10	I/O	234	Data & Address Bit 10
16	SD11/SA11	I/O	235	Data & Address Bit 11
17	GND	POWER		GND
18	SD12/SA12	I/O	236	Data & Address Bit 12
19	SD13/SA13	I/O	237	Data & Address Bit 13

Pin	Name	Type	CARD-PCI/GX pin #	Function
20	SD14/SA14	I/O	238	Data & Address Bit 14
21	GND	POWER		GND
22	SD15/SA15	I/O	239	Data & Address Bit 15
23	SA16	I	192	Address Bit 16
24	SA17	I	193	Address Bit 17
25	GND	POWER		GND
26	SA18	I	194	Address Bit 18
27	SALATCH	I	220	Address Latch
28	PORT3	I	90	Port3
29	GND	POWER		GND
30	ROMDIS	O	73	System ROM Disable
31	ROMCS#	I	188	ROM Chip Select
32	AEN	I	196	Address Enable
33	GND	POWER		GND
34	IOW#	I	242	I/O Write
35	GND	POWER		GND
36	MEMR#	I	191	MEMORY Read
37	GND	POWER		GND
38	MEMW#	I	189	MEMORY Write
39	GND	POWER		GND
40	POWERGOOD	I	246	Power Good Signal

For detailed procedure on updating BIOS ROM using the ROM Writer Kit, refer to the CARD-PCI/GX ROM Writer Kit Instruction Manual being packed to this Kit (SCE88J8X01). A designated software for creating the master BIOS ROM is required. For more information and usage of this software, refer to the following website.

URL http://www.epson.co.jp/CARD-PC/

5. Notes on Usage

5.1. Notes on Printed Board Design

(1) CARD-PCI/GX's PCI bus (AD0 to AD31) and Limited ISA bus (SD0/SA0 to SD15/SA15) have many wiring. For this reason, when they all change at the same time, the energy of the signals becomes large and dragging of the wiring may affect other signals. Therefore, this issue must be tackled by usually adding dumping resistance to the address bus and data bus to smooth off the waveform, or using the GND pattern to increase the distance from other signals.

(2) For the reset signal, clock signal and other control lines, bus noise may heavily overlap due to cross talk, etc. If there is a risk of noise overlapping, use the following solutions to tackle the problem.

- For signals having problem on the system when delay happens, such as the clock signal, use the guard pattern, etc. to reduce impact from other signals, or increase their distance from other signals.
- For signals with margin in timing such as the reset signal, remove noise using an integral circuitry

(3) Generally, the output buffer of CMOS has its output impedance ranging from several ohms to tens of ohms. However, for the wiring of the printed board, its characteristic impedance is over 100 ohms, its output buffer and wiring's impedance matching can not be obtained. As a result, according to the pattern of the board, problems such as reflection may distort the waveform. Therefore, it becomes necessary to check the waveform of each signal and, if necessary, add dumping resistance or the terminal resistance.

(4) When BIOS data is transferred from the BIOS ROM in CARD-PCI/GX to the shadow region of SDRAM in CARD-PCI/GX, change in the bus is more drastic than in the usual case. Transfer to the shadow region of BIOS happens immediately after the power is supplied to the CARD-PCI/GX or when the ROM SETUP is finished. To evaluate whether there is any impact from the bus noise, this should also be done when transferring from BIOS ROM to SDRAM.

5.2. Power and Ground

5.2.1. Connection to power

Because CARD-PCI/GX is a card containing a high-speed CPU and peripheral circuitry, when it operates it causes drastic change in current consumption. To maintain stable operation of CARD-PCI/GX and good display quality in this environment, try as much as possible to connect the power pins (V_{CC5V}, V_{CCCORE}, V_{CC3V}) of CARD-PCI/GX to the power circuitry at a low impedance.
When selecting a power circuitry, use one with power capacity suitable for your application, and be careful to make sure an instant power supply can be secured. Also, precaution should be take to handle noise problem and reduce high frequency noise or low frequency noise.

5.2.2. Power line wiring

For power wiring and ground wiring external to CARD-PCI/GX, try as much as possible to use power plane and ground plane to reduce the wiring impedance. If unfortunately plane connection is not possible, try to use very thick wiring and pay much attention to reducing noise.

5.2.3. Inserting a condenser

To ensue stable CARD-PCI/GX operation, insert a condenser between power and ground. Also, try as much as possible to place the condenser close to the 280pin connector. Table 5-1 shows the recommended value of condenser.

Table 5-1 Recommended capacity of condenser

Power Supply		Recommended value of condenser
V_{CCCORE}	- GND	220µF - 470µF
V_{CC5V}	- GND	220µF - 330µF
V_{CC3V}	- GND	47µF - 100µF
V_{CCSTB}	- GND	10µF - 47µF
V_{CCBAK}	- GND	0.1 - 2.2µF

The best value of condenser changes depending on the system configuration; therefore, check the noise level on your system and select the appropriate value accordingly. When selecting a condenser, pick the type which has a low impedance and good temperature characteristics, such as the organic semiconductor aluminum solid electrolyte condenser. In addition, it is recommended to mount a condenser with good high frequency between 0.01 to 0.47µF running parallel with the condenser described in Table 5-1 to a place close to the connector.

VCCCORE is the input power of the DC-DC converter which generates the core power of the CPU. When the power is turned ON/OFF or when an application software is running, the peak current may flow. While it is possible to share the power with VCC5V, it is recommended that they use separate power lines.

5.2.4. Restrictions on input current of the power pin

Table 5-2 shows the maximum input power provisions of each power pin of VCCCORE and VCC3V of CARD-PCI/GX. If CARD-PCI/GX malfunctions, a current exceeding the current limit shown in Table 5-2 flows in and causes CARD-PCI/GX to heat up excessively. To avoid this problem, design the system so that no current exceeding the current limit will flow in; this can be achieved by inserting, for example, a fuse into the appropriate power line.

In the reference circuitry diagram in chapter 7, a fuse (F501) is added to the VCCCORE pin to achieve this purpose. Refer this diagram together with Table 7-1.

Table 5-2 Maximum current provisions

Symbol	Min.	Max.	Unit	Current Limit
VCCCORE	4.75	5.25	V	2.5A
VCC3V	3.15	3.45	V	3A

5.3. EMC and Static Noise Solution

CARD-PCI/GX is not housed in a case. Also, because the CPU clock runs at high speed, the EMC and static noise issues must be fully studied when designing mother board circuitry, artwork, and the system casing.

Also, CARD-PCI/GX's heat-emitting panel and signal ground are connected inside the card. If the heat-emitting panel is connected to the frame ground of your system, fully check to make sure that there is no unwanted radiation noise emitting and that there is no system malfunctioning caused by static noise. Table 5-3 shows the frequency of the clock used by CARD-PCI/GX.

Table 5-3 Frequency of clock used by CARD-PCI/GX (reference)

Clock Name	Frequency
CPU Clock	199.8MHz
PCICLK0 - 2	33.3MHz
FPDOTCLK	25 - 65MHz
FPDOTE	12.5 - 32.5MHz
CRT Pixel Clock	25.175MHz
PLL Input	14.31818MHz
RTC	32.765kHz

5.4. Other Notes

5.4.1. Notes on designing ISA BUS

When adding a memory device to the ISA BUS at the mother board based on CARD-PCI/GX, pay attention to the following design notes.

(1) Add conditions of ROMCS# (CARD-PCI/GX,188pin) to the decode circuitry of the device's chip select signal and gate signal. This is for closing the device's gate when accessing the BIOS ROM inside CARD-PCI/GX. If ROMCS# is not added to the decode conditions, the data line may come into conflict.

(2) Use SMEMR# / SMEMW#, but not MEMR# / MEMW#. For information on how to generate SMEMR# / SMEMW#, refer to "A-2-6. Generating SMEMR# and SMEMW#" in the CARD-PCI/GX Hardware Manual.

(3) Add ROMCS# to the decode conditions of MEMCS16#, and do not perform drive when accessing the BIOS ROM inside CARD-PCI/GX. For details, refer to "A-2-7. Generating MEMCS16#" in the CARD-PCI/GX Hardware Manual.

5.4.2. About the CPUFREQ signal

The CPUFREQ signal (CARD-PCI/GX, 68pin) is used to set the CPU's clock. In the HIGH performance version of the CARD-PCI/GX series, it is necessary to set the input of the CPUFREQ signal to the LOW level. Provide the jumper to allow for switching of the input level of the CPUFREQ signal or the 0Ω resistance jumper for the future when the HIGH performance version of the CARD-PCI/GX series is used. Table 5-4 shows setting of the CPUFREQ signal.

Table 5-4 Setting the CPUFREQ signal

CARD-PCI/GX Series	CPU Clock	CPUFREQ Signal level
SCE8720C01/02	200MHz	Open
SCE8720C HIGH Performance Version	200MHz or more	LOW

6. Securing and Installing the Interface Connectors

There are two types of CARD-PCI/GX interface connectors, namely the Main connector (280pin) and the FFC connector (20pin). This section describes some notes to pay attention to when designing the board of the connector on the mother board for each of the interface connectors, and how to secure them.

6.1. Main Connector

This section describes the 280pin Main connector.

6.1.1. Shape of CARD-PCI/GX

Fig. 6-1 shows the dimensions of CARD-PCI/GX. Also, note that the position of pin 1 in Fig. 6-1 does not match the actual position of pin 1 marked on the connector.

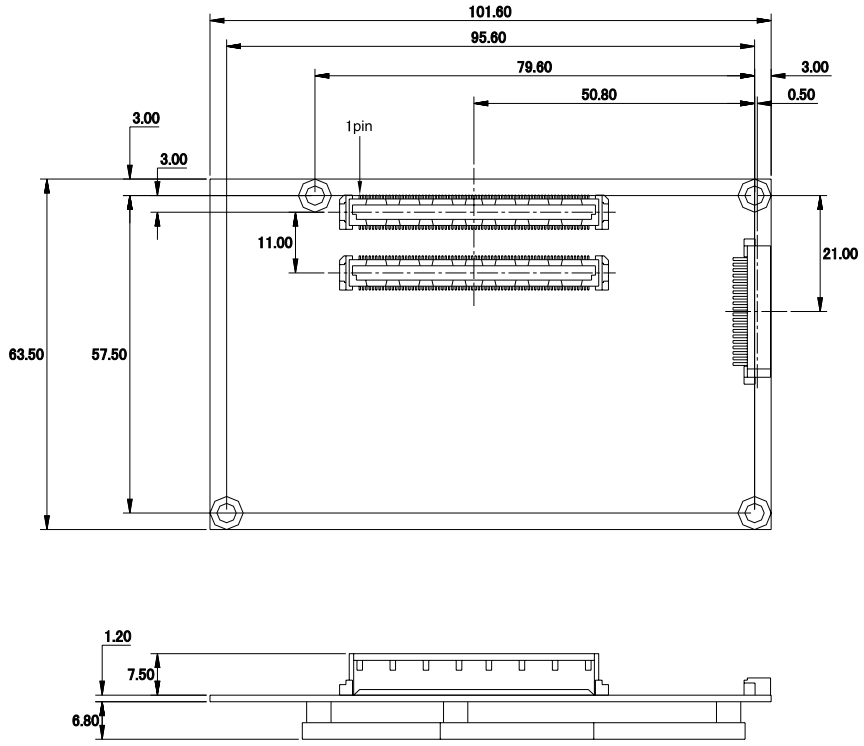


Fig. 6-1 Dimensions of the main connector of CARD-PCI/GX [mm]

6.1.2. Cautions on mother board design

6.1.2.1. Main connector dimensions

Fig. 6-2 indicates the relationship between CARD-PCI/GX's securing hole and the main connector's mounting position, and Fig. 6-3 shows the Main connector's board layout for reference. Use them as reference when designing the mother board of CARD-PCI/GX.

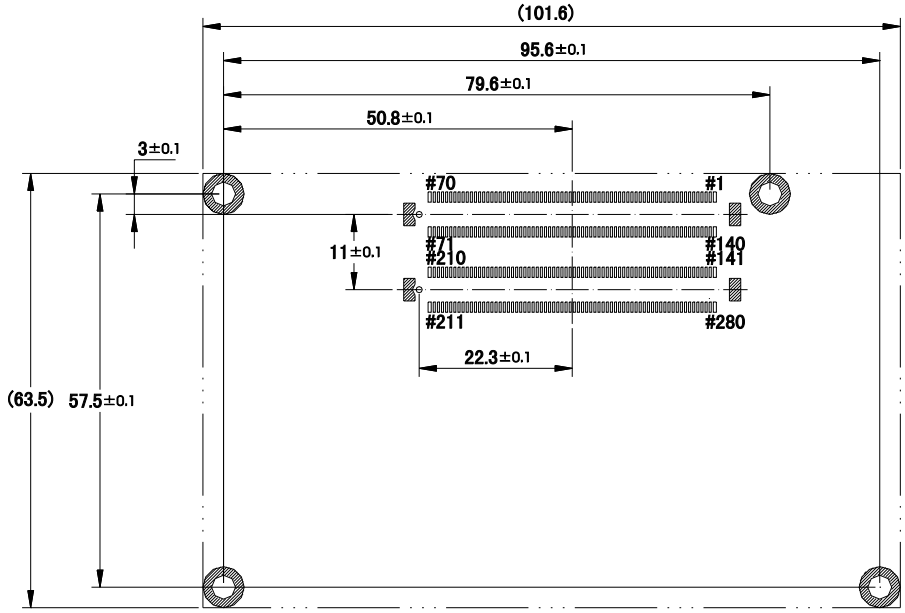


Fig. 6-2 Dimensions of the Main connector's position [mm]

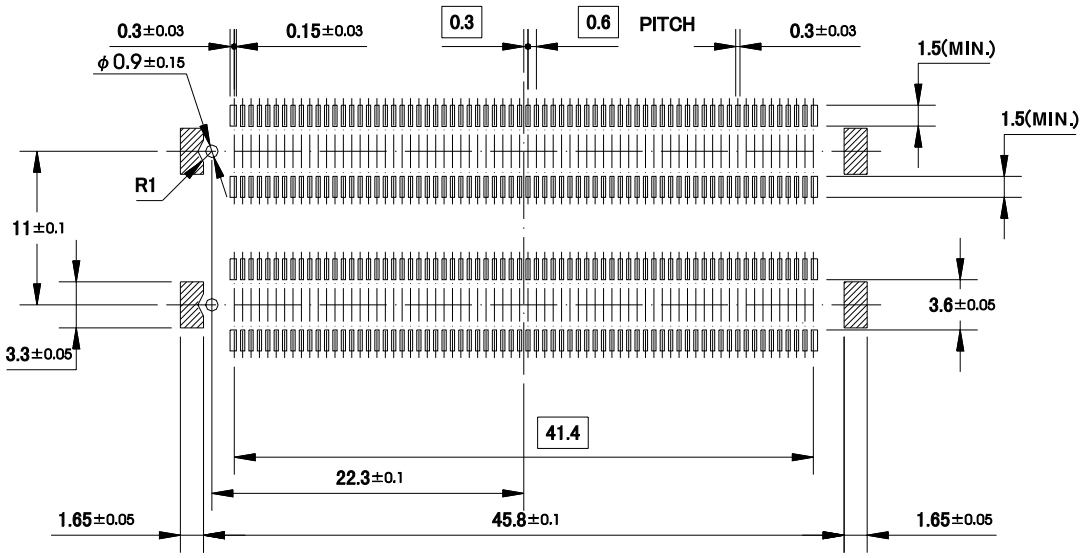


Fig. 6-3 Main connector's reference board layout [mm]

6.1.2.2. Restrictions on height when installing components

Fig. 6-4 shows the height restriction when mounting components to the mother board area beneath CARD-PCI/GX. It is recommended that this area be avoided, because this area can become very hot. If for some reason a component must be mounted in this area, realize you will be liable for any consequences, and you must make sure the component has enough capacity to withstand such high temperature. The restriction figure is based on the receiving connector having a height of 8 mm, as described in Table 6-1

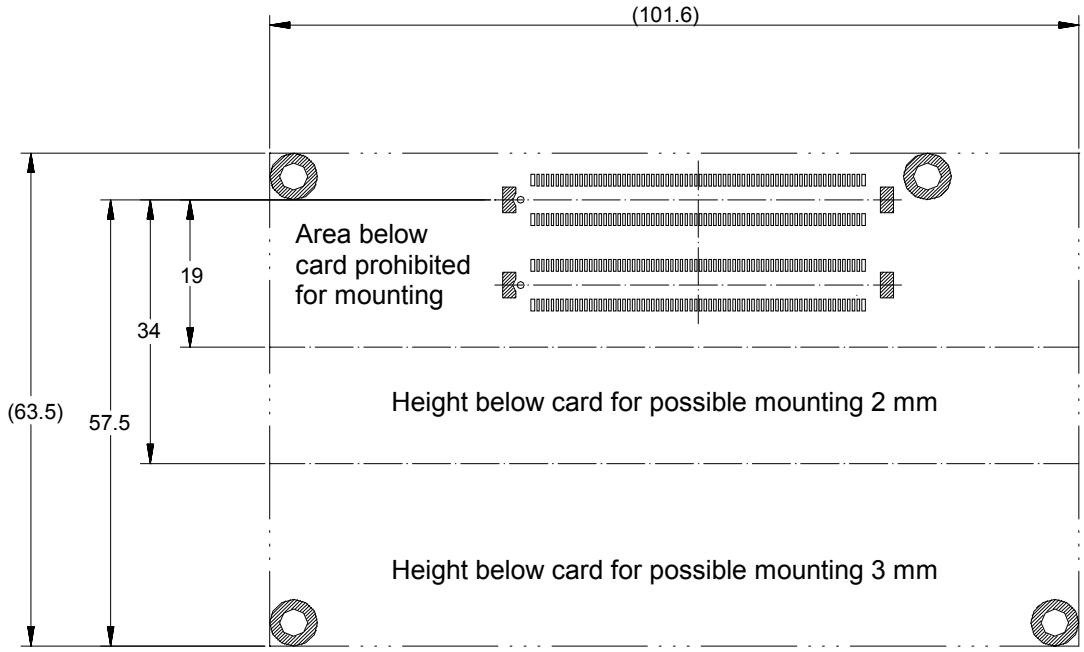


Fig. 6-4 Height restriction on components [mm]

6.1.2.3. Cautions on securing the mother board

As shown in Fig. 6-5, when mounting CARD-PCI/GX, if the securing location for the mother board is away from the connector of CARD-PCI/GX, the mother board becomes bended and CARD-PCI/GX can not be connected firmly. Also, in such situation the mother board may become damaged. Therefore, when designing the mother board, try as much as possible to locate the board securing position close to the Main connector for CARD-PCI/GX.

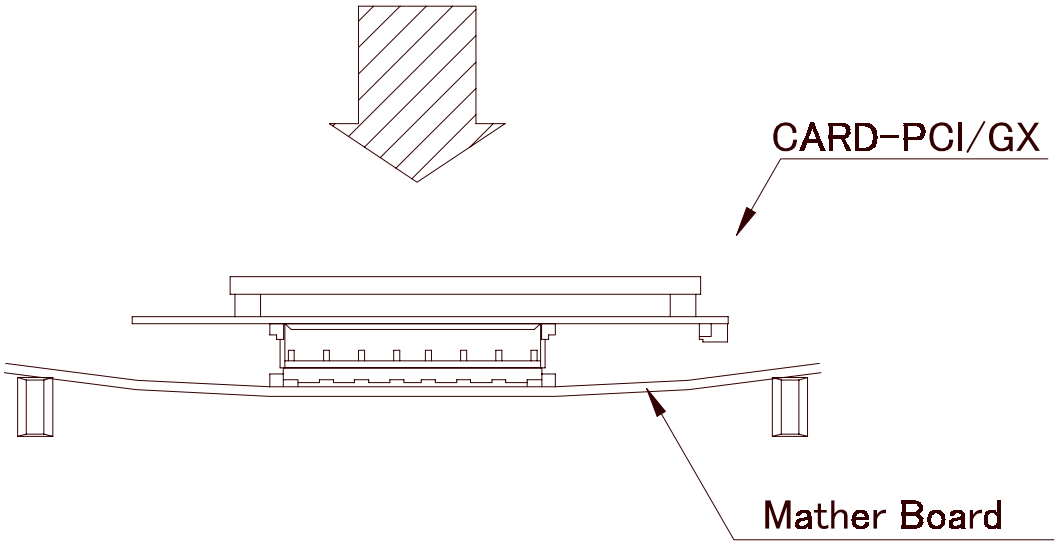


Fig. 6-5 Mother board becoming bended when CARD-PCI/GX is mounted

6.1.3. Installing CARD-PCI/GX

<Items required for securing>

- Spacers (M3) (L=8mm or 16mm) 4pcs
  (Note) Study Table 6-1 and use spacers suitable for the selected receiving connector.
- Screws (M3) (L=5mm) 8pcs

<Installation procedure >

Fig. 6-6 shows the installation diagram.

(1) Locate the four holes on the mother board for securing CARD-PCI/GX, then use the M3 screws to secure the spacers from the under side of the mother board.
(2) Firmly connect CARD-PCI-GX to the 280pin receiving connector. While doing this, be careful the printed board does not become bended, as described in 6.1.2.3.
(3) Use the M3 screws to secure the spacers fixed on the mother board and the four securing holes on CARD-PCI/GX.

<Reference value for controlling torque >

Use 3N·m as a general guideline. However, be aware that this value serves only as a reference. Therefore, be sure to use a torque value suitable for the vibration conditions of the system.

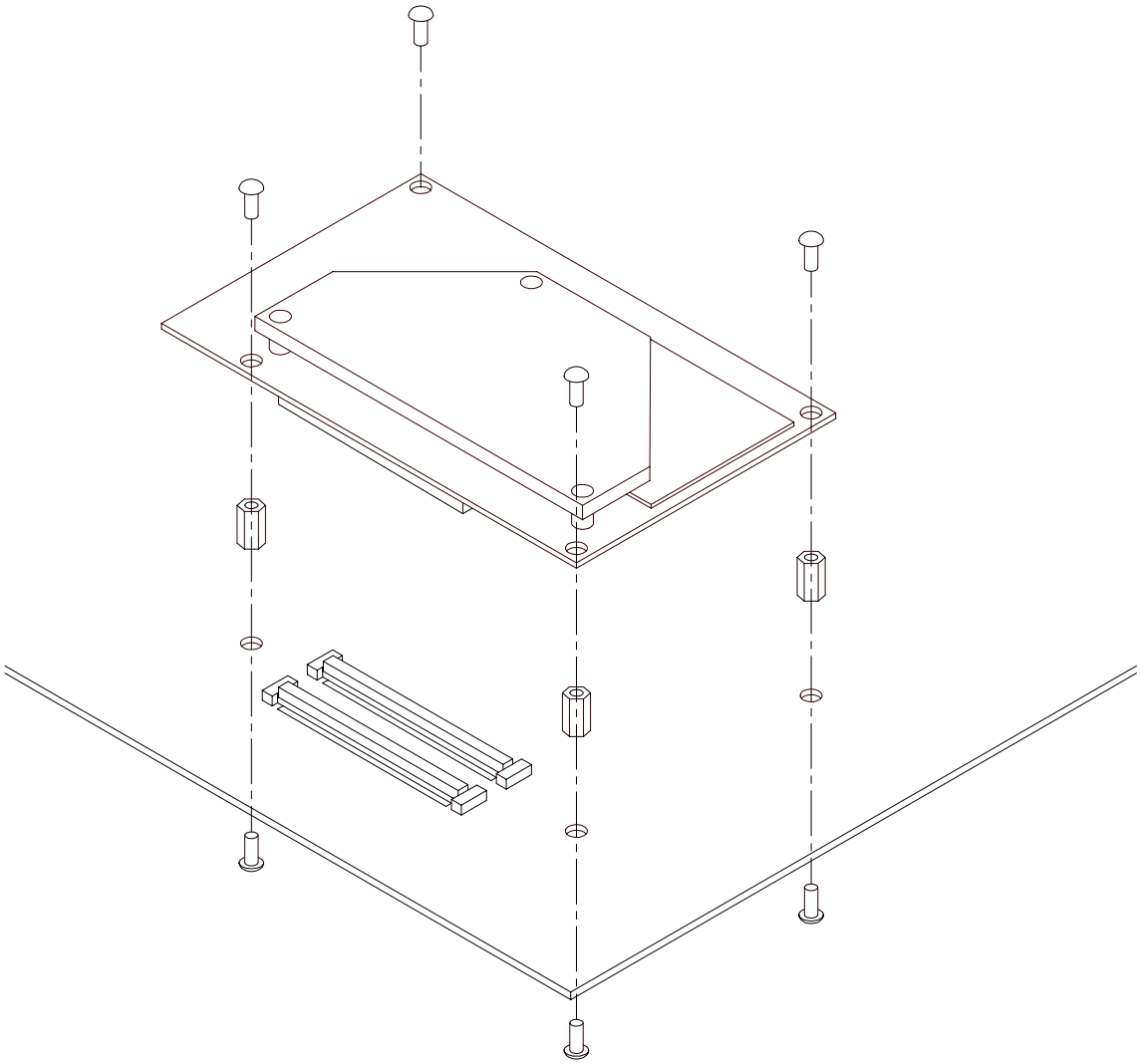


Fig. 6-6 CARD-PCI/GX installation diagram

6.1.4. Connectors

Two types of connectors can be used at the receiving end (mother board) of CARD-PCI/GX, as shown in Table 6-1. Because the height from the mounting surface differs, use a spacer matching the height between the boards.

AMP's 1-353233-0 (8 mm in height) is mounted on CARD-PCI/GX.

Table 6-1 Receiving connector and suitable spacer types

Receiving connector			Suitable spacer	
Maker	Model	Height	Maker	Model
AMP	1-353906-0	8mm	Hirosugi Instrument	ASB-308
AMP	1-353800-0	16mm	Hirosugi Instrument	ASB-316

6.2. FFC Connector

This section describes the 20pin FFC connector. This connector connects to the mother board via the FCC cable. Take note of this when making the FCC cable. Also, a set of FCC cable for evaluation is included in the CARD-PCI/GX Evaluation Kit (SCE88J5X01).

6.2.1. Connectors on CARD-PCI/GX

The 52852-2090 from MOLEX – bottom contact type for FFC/FPC -- is mounted on CARD-PCI/GX. Fig. 6-7 shows the pin arrangement of the FFC connector. Also, note that the position of pin 1 in Fig. 6-7 does not match the actual position of pin 1 marked on the connector.

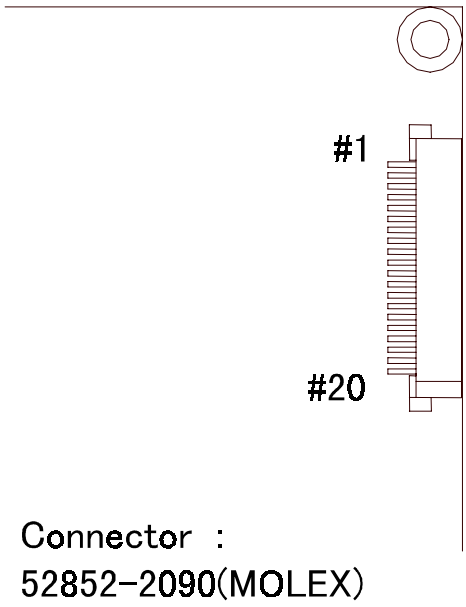


Fig. 6-7 Pin arrangement on the FFC connector

6.2.2. Recommended dimensions of FFC

Use Fig. 6-8 as a reference when making the FFC cable.

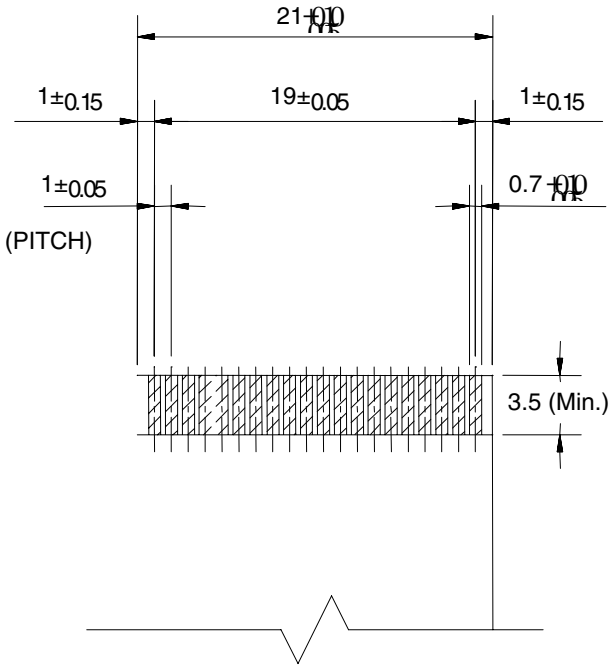


Fig. 6-8 Recommended dimensions suitable for FFC

The FCC cable included in the CARD-PCI/GX Evaluation Kit (SCE88J5X01) use the following steel wire from Hitachi Densen, as follows:

CUJ(1.0) - 20F - 100 - 10S5(B) - M1(20861)

Depending on the connector selected for the mother board, the type of FFC cable to use is different. For the length of the FFC cable, use up to a maximum length of 100 mm.

7. Reference Circuitry

This section describes reference circuitry diagram created based on the Evaluation Board included in the CARD-PCI/GX Evaluation Kit (SCE88J5X01). Note that it is not the Evaluation Board itself.

7.1. Differences with Evaluation Board

Table 7-1 shows its differences with the Evaluation Board. The Evaluation Board comes with the ability to measure the consumption current of CARD-PCI/GX and evaluate CARD-PCI/GX's operation. It differs from the Evaluation Board in that you can delete functions not required on the mother board. Also, components for improving the ease of use are added.

Table 7-1 Differences with the Evaluation Board

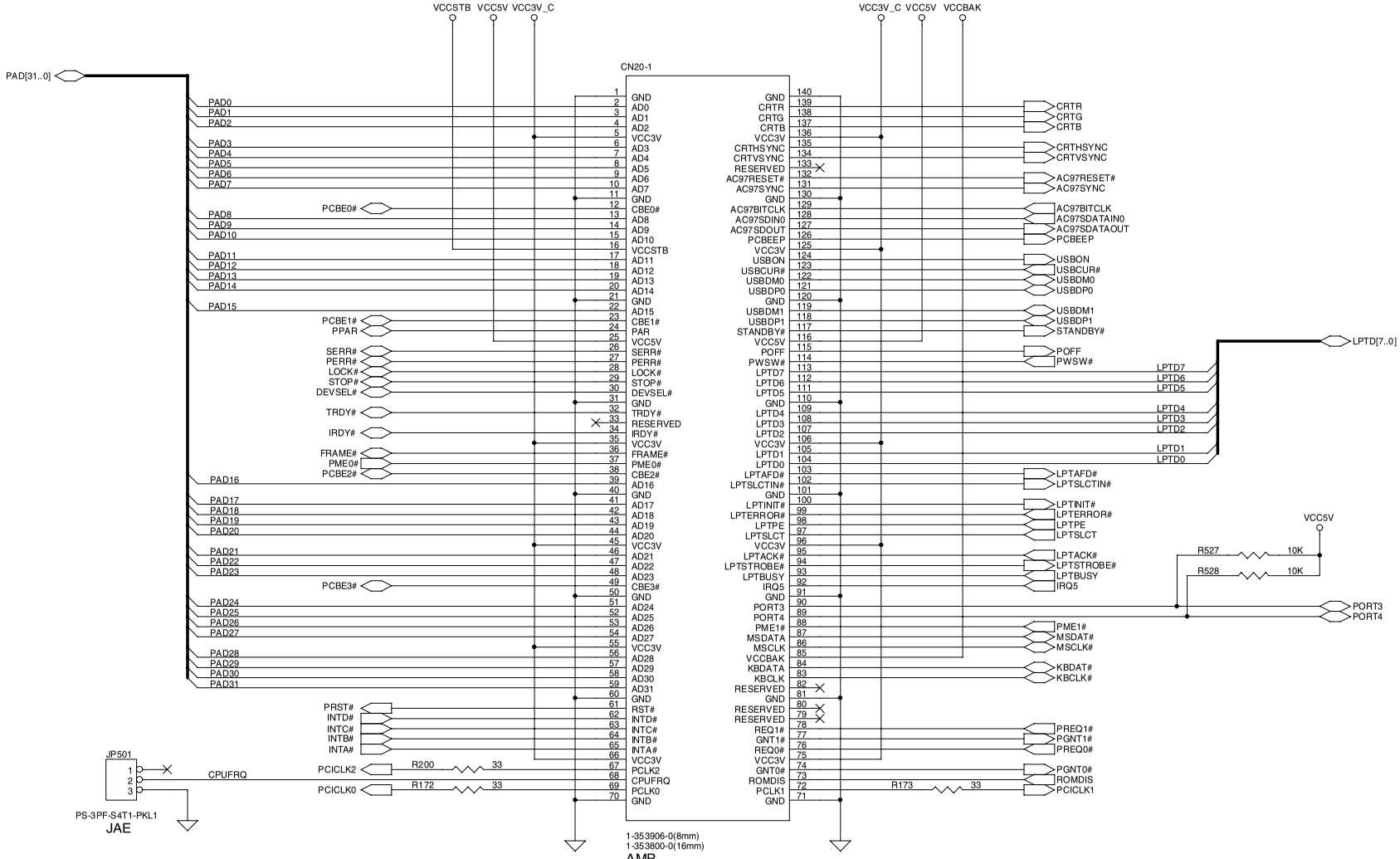
Deleted components	Added components	Function	Reason for modification
C133,C134,C137 R223,R234,R235 D12 Q7,Q8,Q10 JP[13:16],JP30 U20	C502,C503 U501	Adjust the power ON sequence of VCC3V.	To fix the circuitry meeting the requirements of power ON sequence of VCC3V.
JP[17:28]		Jumper switch for measuring consumption current	Deleted as it is not required in the circuitry for measuring the consumption current of CARD-PCI/GX in the product.
C[2:13],C[55:C59] C[61:C64],C67,C68 C[94:99],C101,C102 C115,C127,C128 R78,R85,R87,R98,R99 R101,R[149:154],R171 R189,R190 D3,D7 JP[4:8],JP31 TP[1:4] U7 SW1,SW3 CN12,CN[23:25]		Check operations of CARD-PCI/GX itself	Deleted as it is not required in the circuitry for evaluating the circuitry operation of CARD-PCI/GX in the product.

Deleted components	Added components	Function	Reason for modification
	C501 R[501:528] L501 JP501 CN501	-	Improved based on evaluation results of the Evaluation Board
	F501	Fuse for limiting input current at the VCCCORE pin	Added to avoid excessive heat generated when CARD-PCI/GX malfunctions (See section 5.2.4 for reference.)

7.2. Reference Circuitry Diagram

The reference circuitry diagram is formed from the following total 21 sheets.

Sheet 1	CARD-PCI/GX Interface 1
Sheet 2	CARD-PCI/GX Interface 2
Sheet 3	LCD and CRT Interface
Sheet 4	Internal Primary IDE Interface
Sheet 5	External Secondary IDE Circuit
Sheet 6	FDD and USB Interface
Sheet 7	Serial Port Interface
Sheet 8	Parallel Port and Keyboard/Mouse Interface
Sheet 9 - 12	PCI BUS Slot
Sheet13	BUS Switch Circuit
Sheet14,15	Limited ISA Slot
Sheet16	ISA BUS Address Latch and Misc Circuit
Sheet17	Power In and Wake On Ring / Wake On LAN Interface
Sheet18	Switches
Sheet19	LED Circuit for debugging and Speaker
Sheet20	Extended Interface
Sheet21	ROM Writer Board Interface



Note :
JP501 refer to aCARD-PC/GX Application Note

CARD I/F

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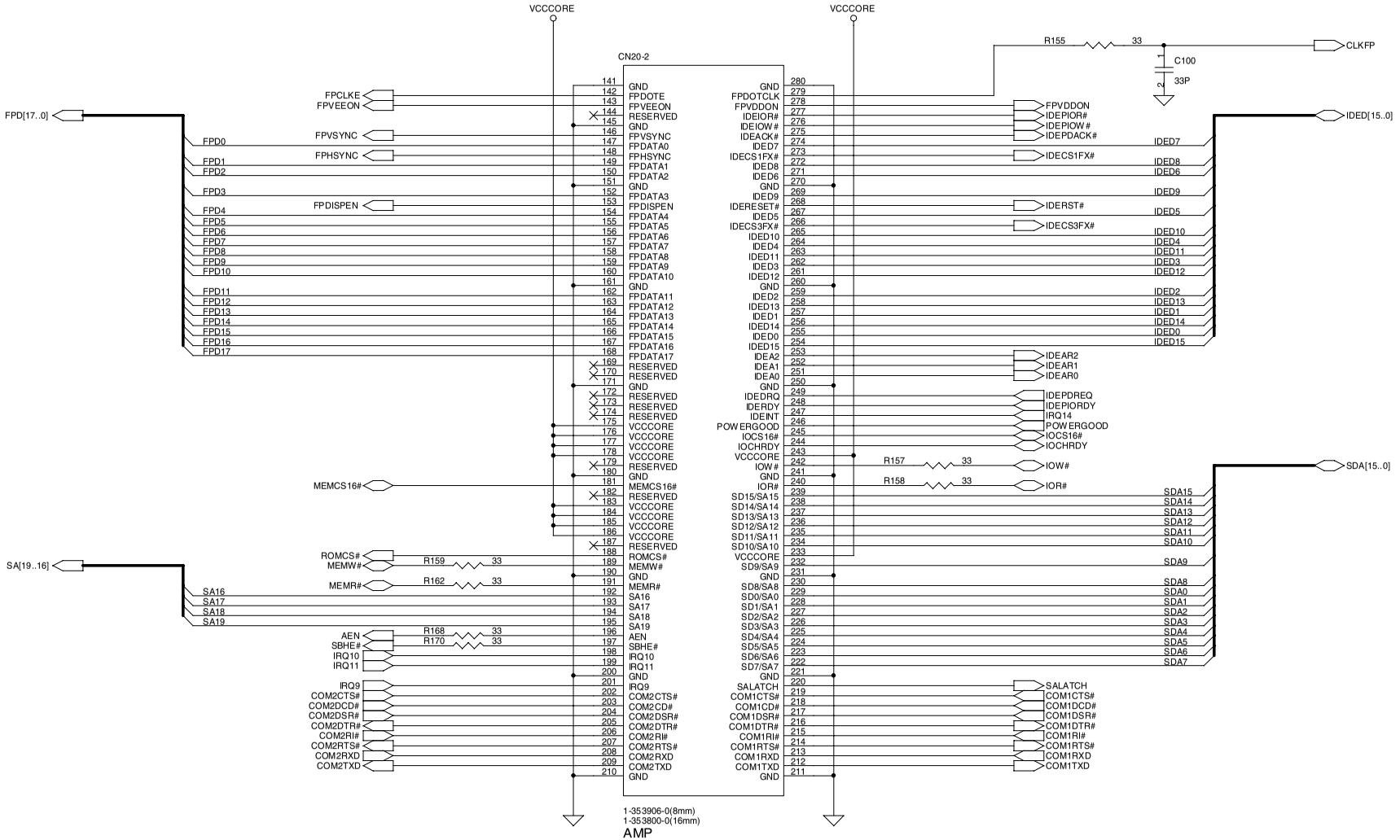
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 1 of 21	



CARD I/F

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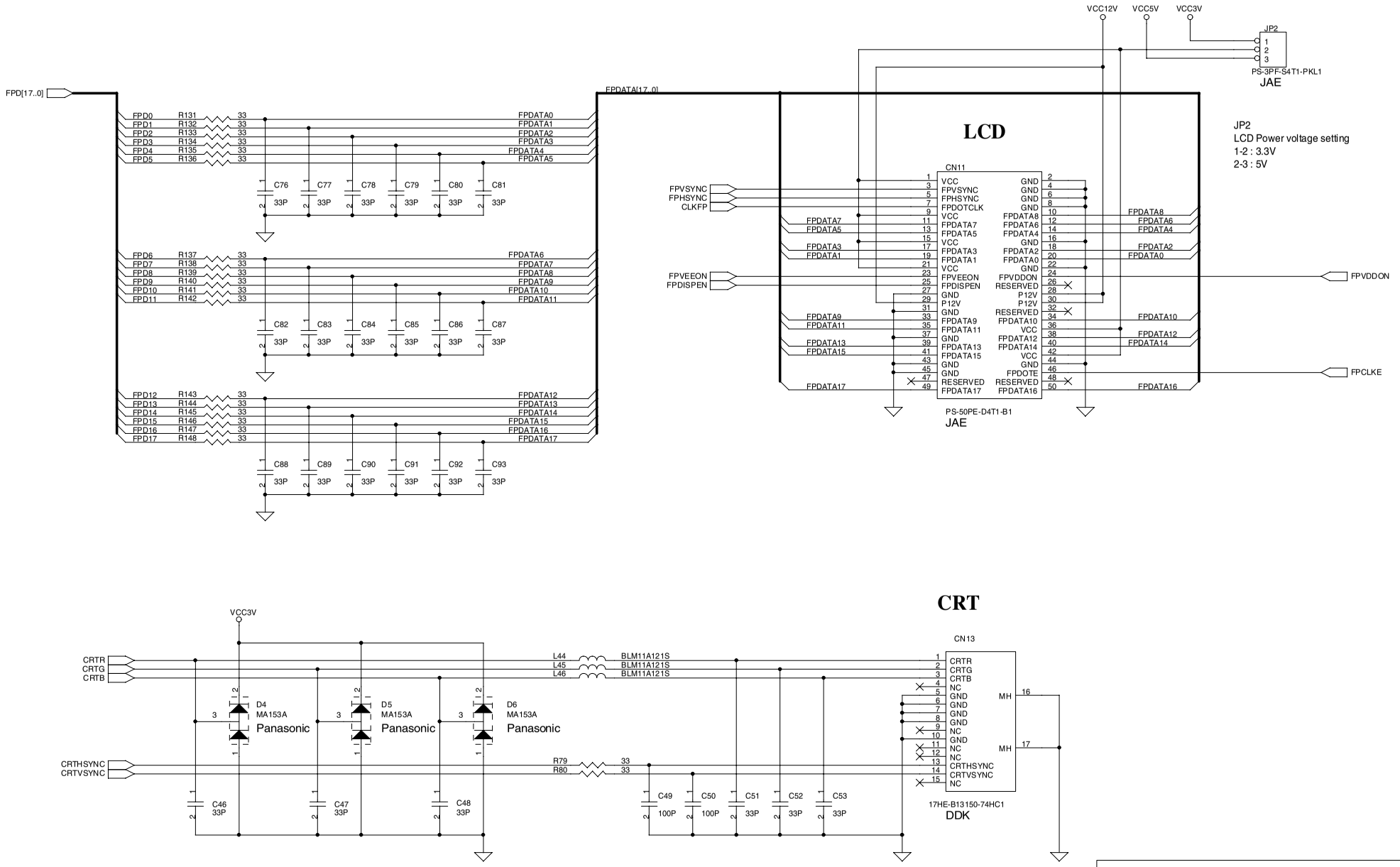

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Title: LCD and CRT Interface

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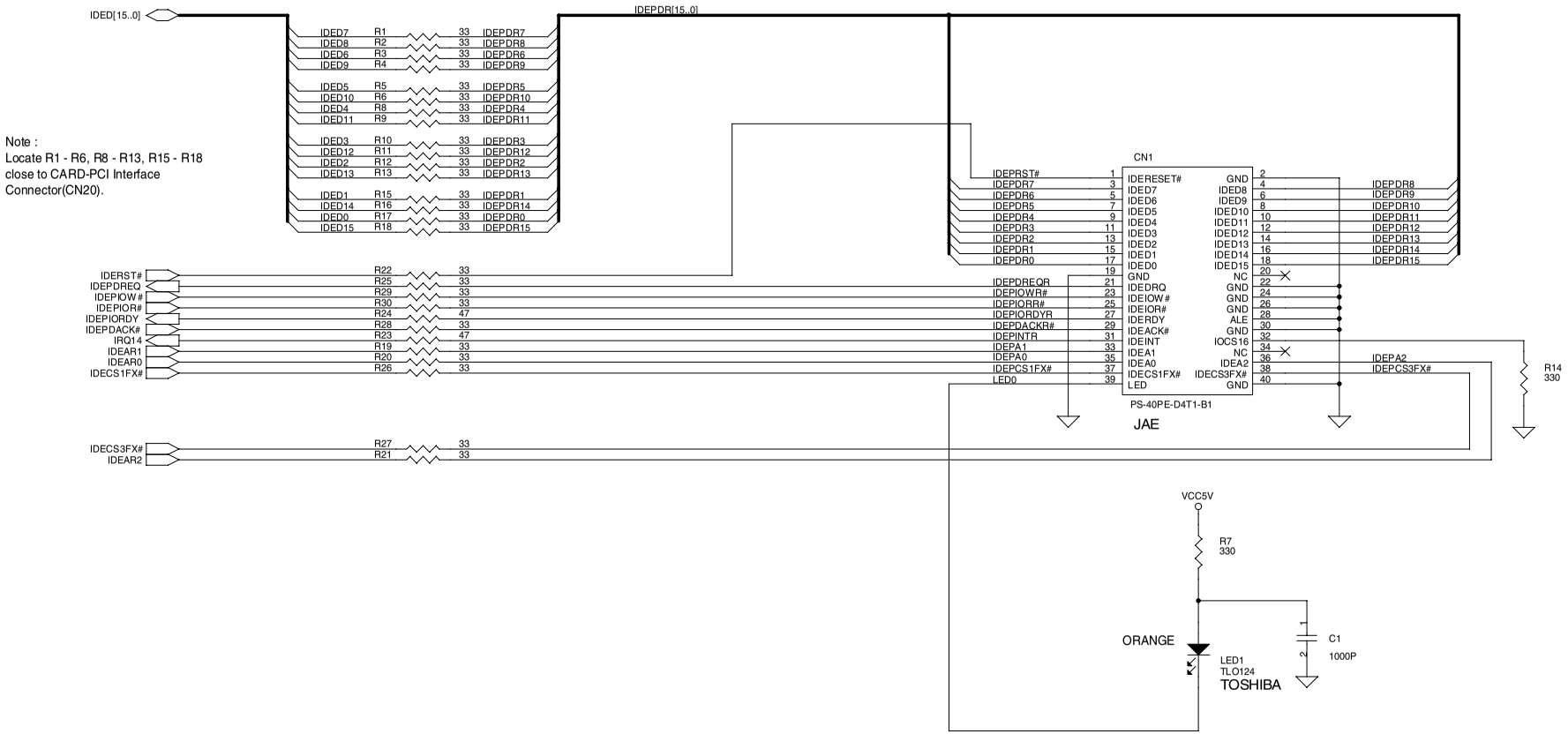
Date: Tuesday, April 25, 2000 Sheet 3 of 21

IDE



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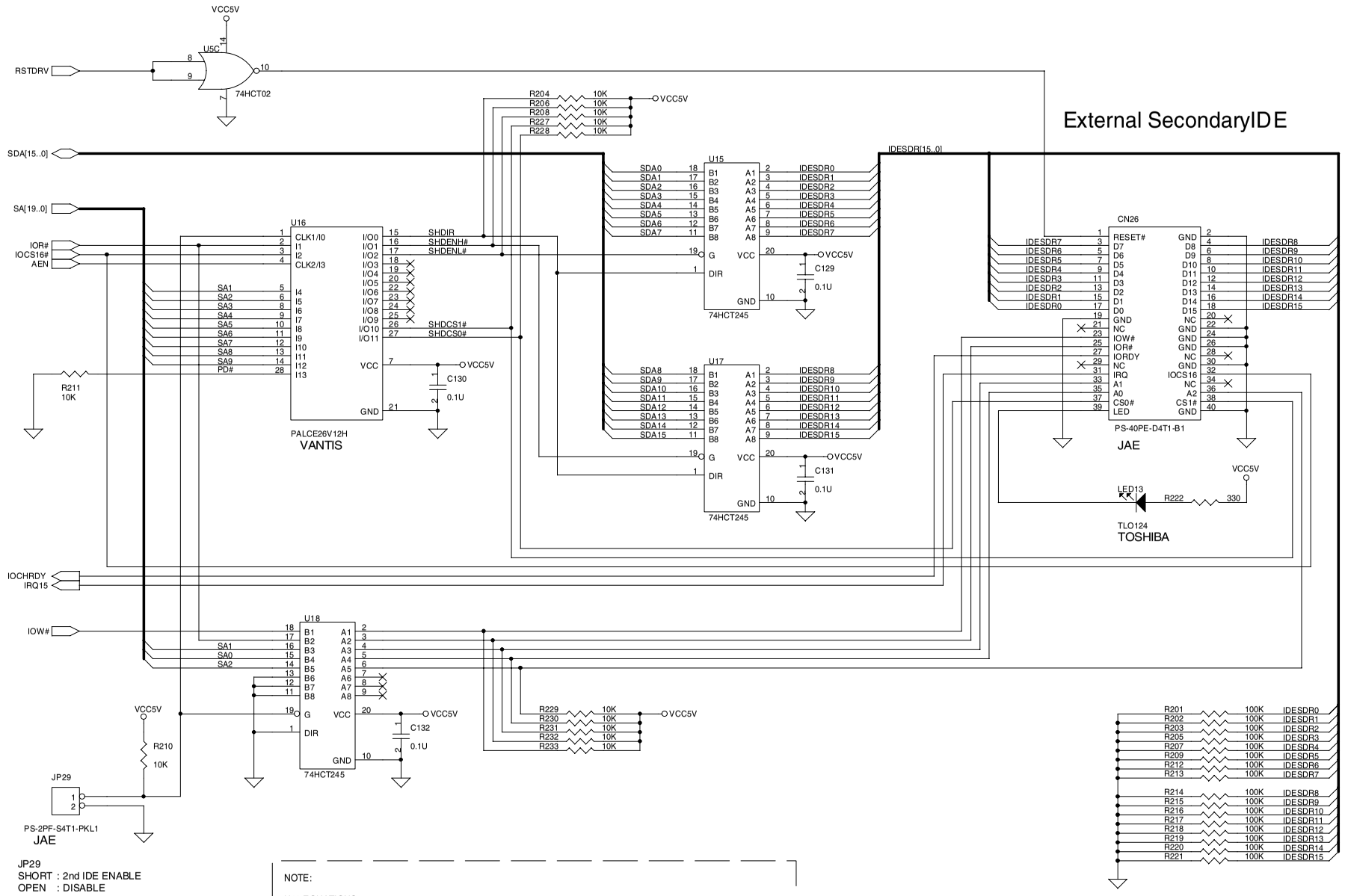
Date: Tuesday, April 25, 2000	Sheet 4 of 21	


External SecondaryIDE
VCC5V
U5C
74HCT02
RSTDRV
SDA[15..0]
SA[19..0]
IOR#
IOCS16#
AEN
IOCHRDY
IRQ15
IOW#
U16
PALCE26V12H
VANTIS
SHDIR
SHDENH#
SHDENL#
SHDCS1#
SHDCS0#
U15
U17
74HCT245
IDESDR[15..0]
CN26
PS-40PE-D4T1-B1
JAE
LED13
R222
330
TLO124
TOSHIBA
U18
R210
10K
JP29
PS-2PF-S4T1-PKL1
JAE
JP29
SHORT : 2nd IDE ENABLE
OPEN : DISABLE
NOTE:
U16 EQUATIONS
SHDIR =/IOR * (SHDCS0 + /SHDCS1)
/SHDENH = /IOCS18 * (/SHDCS0 + /SHDCS1)
/SHDENL = /SHDCS0 + /SHDCS1
/SHDCS1 = /ENA * /AEN * SA1 * SA2 * /SA3 * SA4 * SA5 * SA5 * SA6 * SA7 * SA8 * SA9 * /PD
/SHDCS0 = /ENA * /AEN * /SA3 * SA4 * SA5 * SA6 * /SA7 * SA8 * /SA9 * /PD
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Size
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Document Number
Rev
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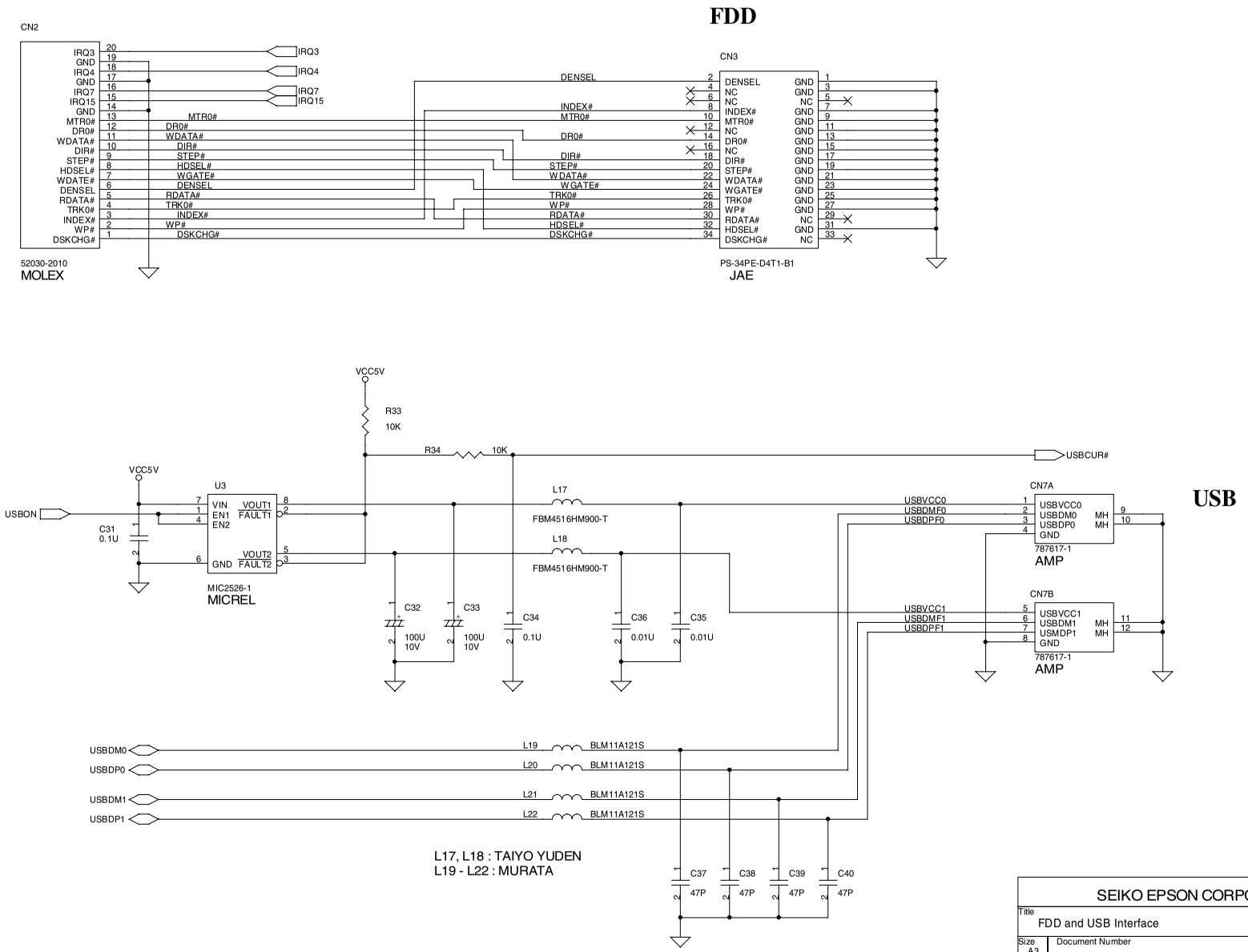
Date:
Tuesday, April 25, 2000
Sheet
5
of
21


FDD
CN2
IRQ3
GND
IRQ4
GND
IRQ7
IRQ15
GND
MTR0#
DR0#
WDATA#
DIR#
STEP#
HDSEL#
WDATE#
DENSEL
RDATA#
TRK0#
INDEX#
WP#
DSKCHG#
52030-2010
MOLEX
CN3
PS-34PE-D4T1-B1
JAE
USB
VCC5V
R33
10K
R34
10K
USBCUR#
U3
VIN
EN1
EN2
VOUT1
FAULT1
VOUT2
FAULT2
GND
MIC2526-1
MICREL
USBON
C31
0.1U
L17
FBM4516HM900-T
L18
FBM4516HM900-T
C32
100U
10V
C33
100U
10V
C34
0.1U
C36
0.01U
C35
0.01U
CN7A
CN7B
USBVCC0
USBDM0
USBDP0
GND
USBVCC1
USBDM1
USMDP1
787617-1
AMP
USBDM0
USBDP0
USBDM1
USBDP1
L19
L20
L21
L22
BLM11A121S
L17, L18 : TAIYO YUDEN
L19 - L22 : MURATA
C37
47P
C38
47P
C39
47P
C40
47P
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Document Number
Rev
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Date:
Tuesday, April 25, 2000
Sheet
6
of
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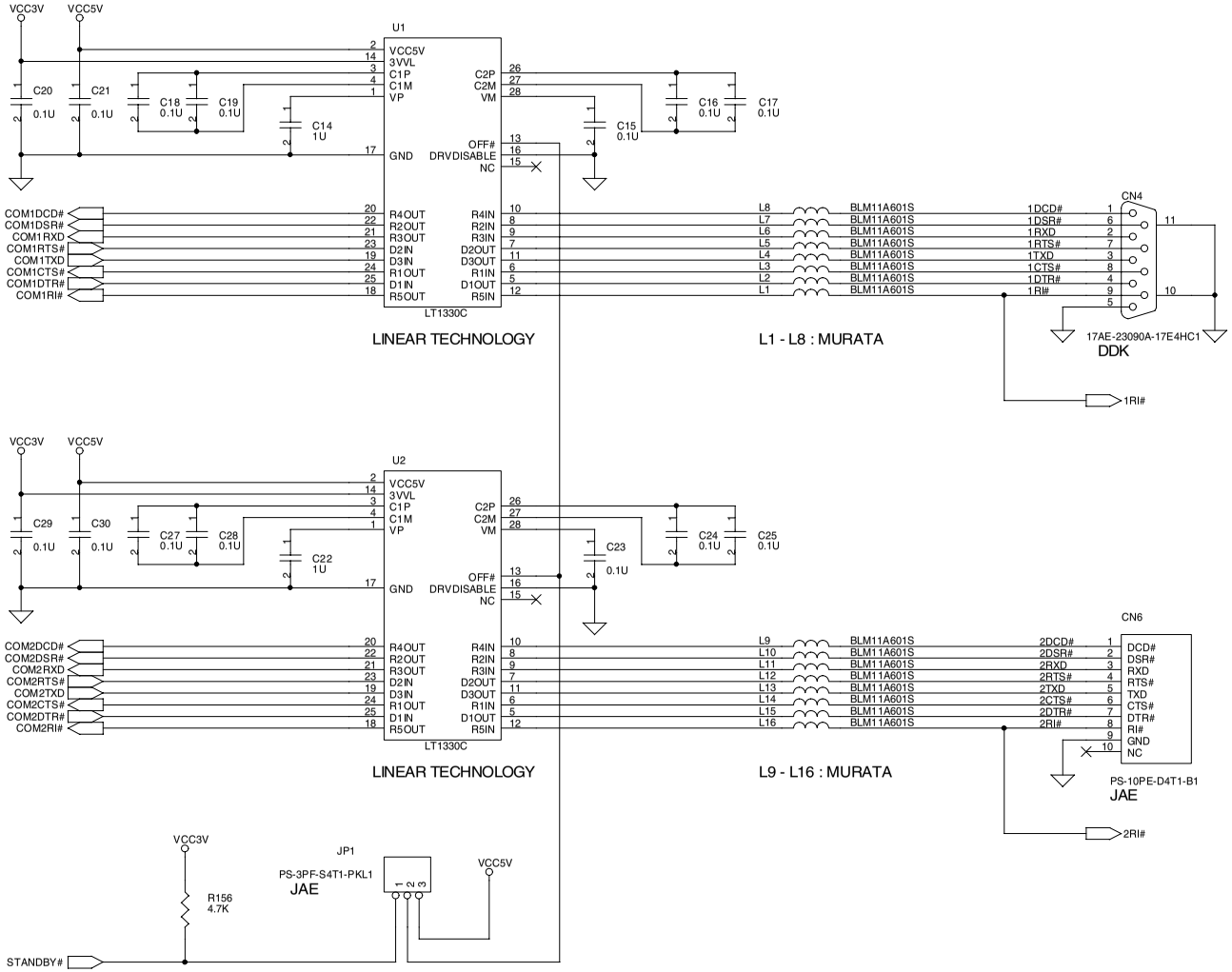

SERIAL-1

SERIAL-2

JP1 U1, U2 operating mode control

JP1	STANDBY#	Operating mode
1 - 2	Low	Shutdown mode
	High	Normal mode
2 - 3	X	Normal mode

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Title: Serial Port Interface

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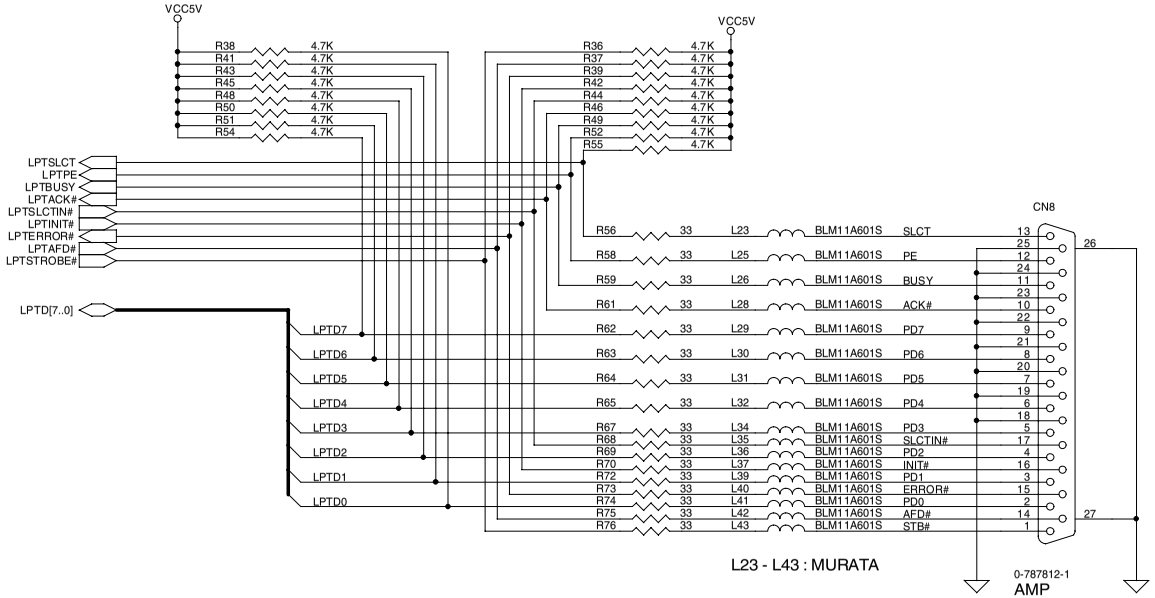
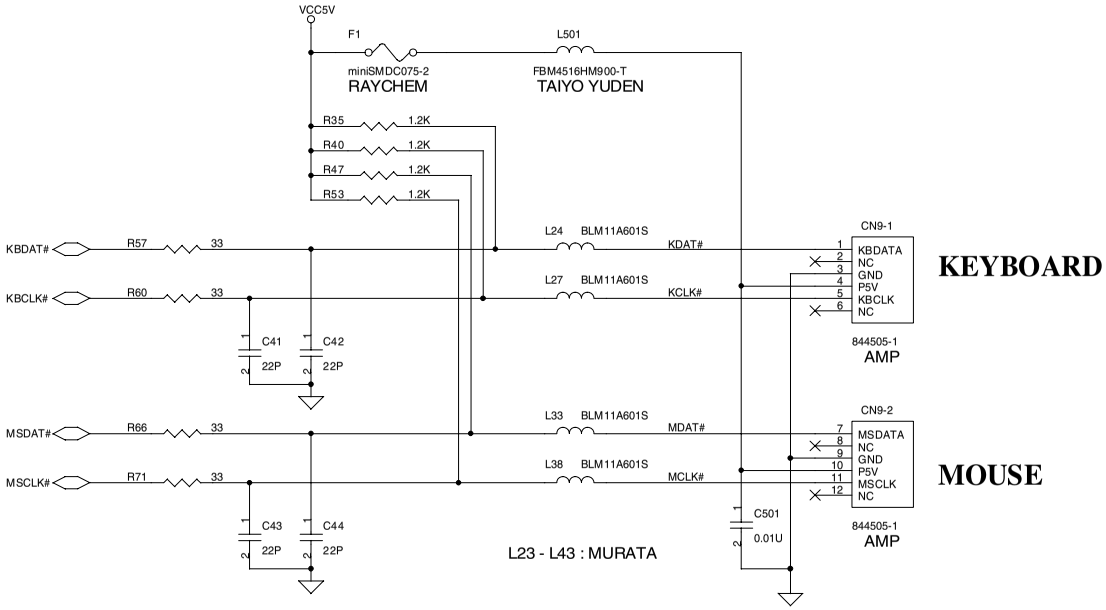
Date: Tuesday, April 25, 2000 | Sheet 7 of 22



PARALLEL



KEYBOARD

MOUSE

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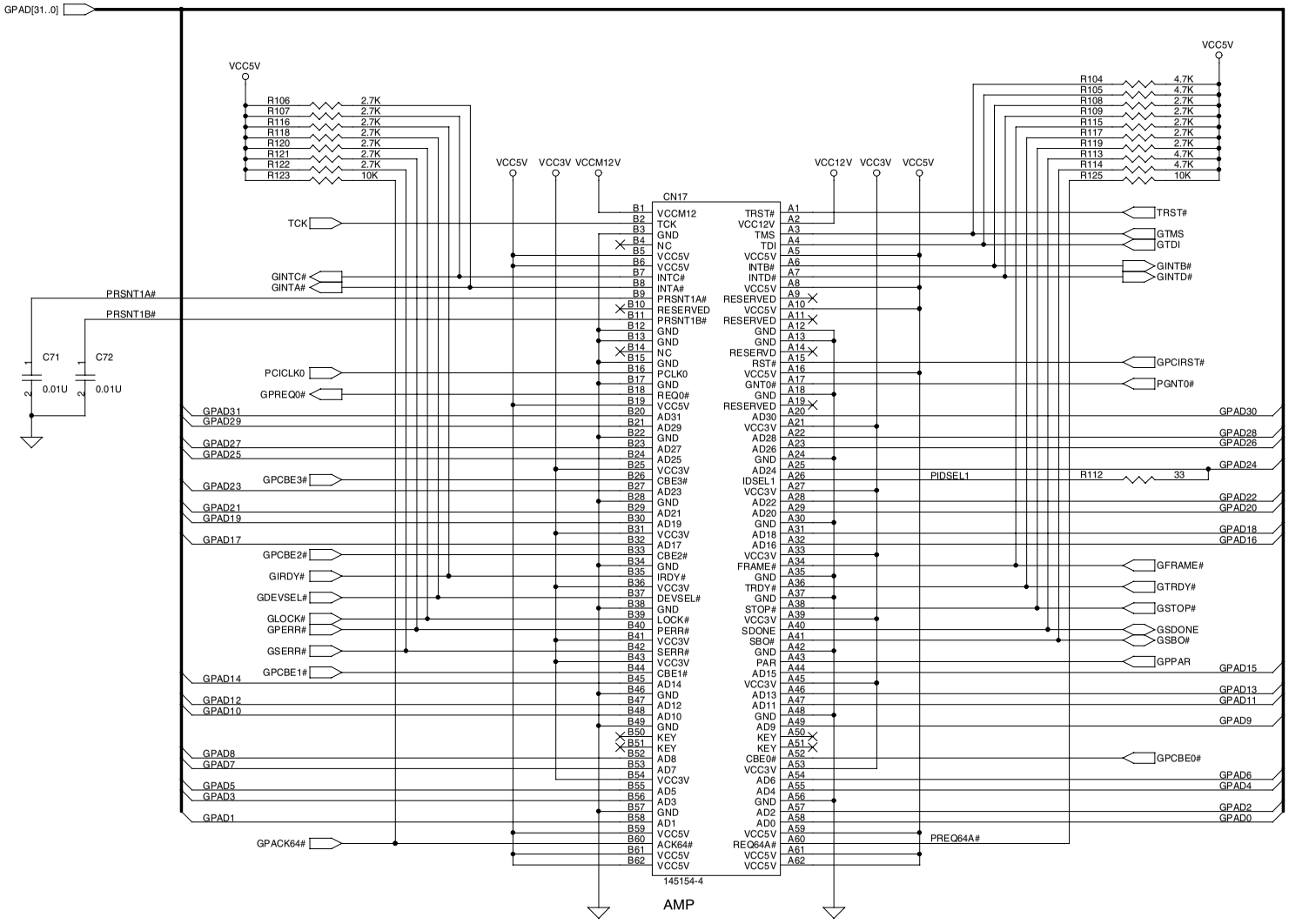
Title: Parallel Port and Keyboard/Mouse Interface		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 8 of 21	

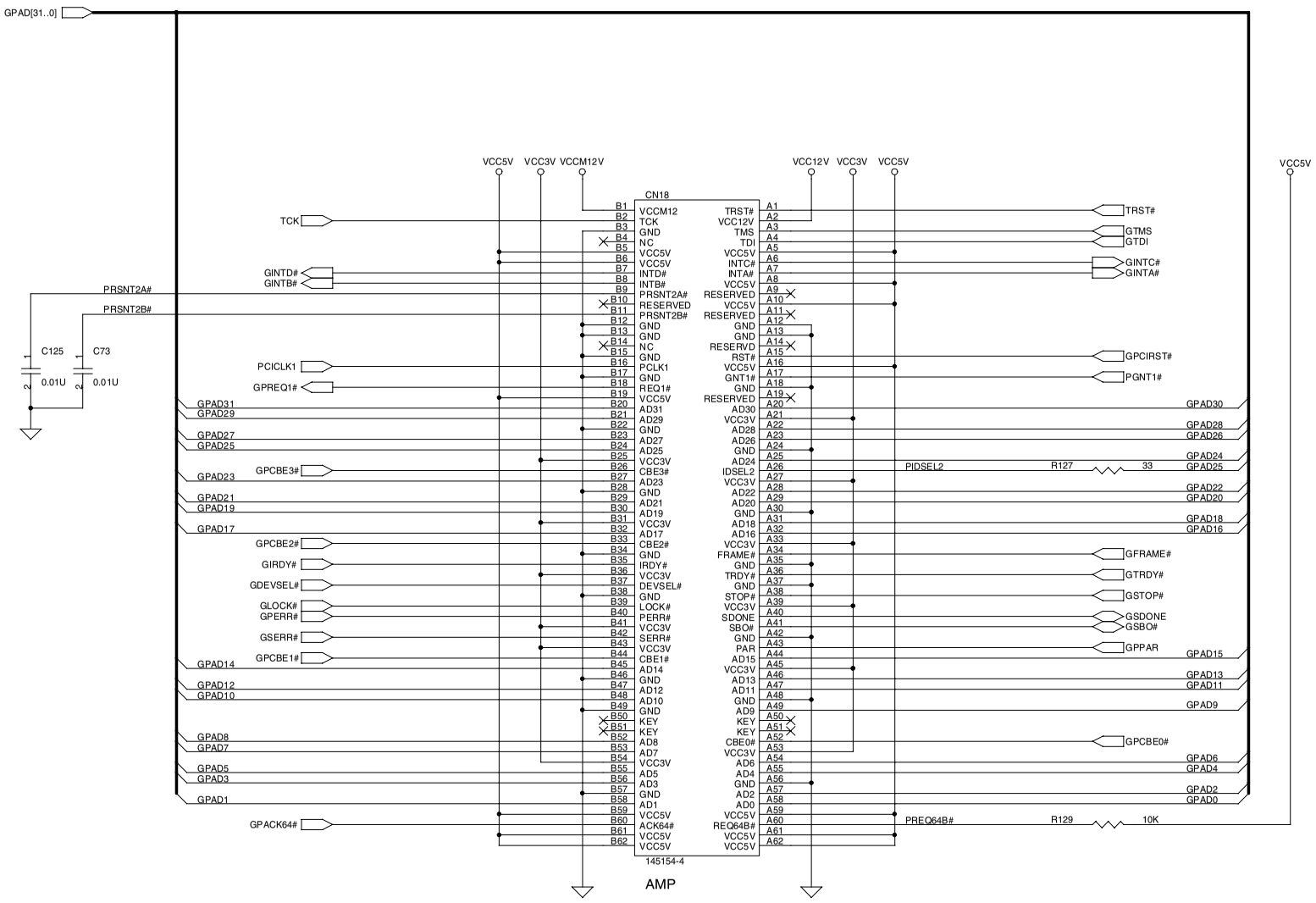


PCI - SLOT 1
(5V)

(DEVICE 0Eh)

IDSEL= PAD24

SEIKO EPSON CORPORATION		
Title: PCI BUS Slot		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 9 of 21	

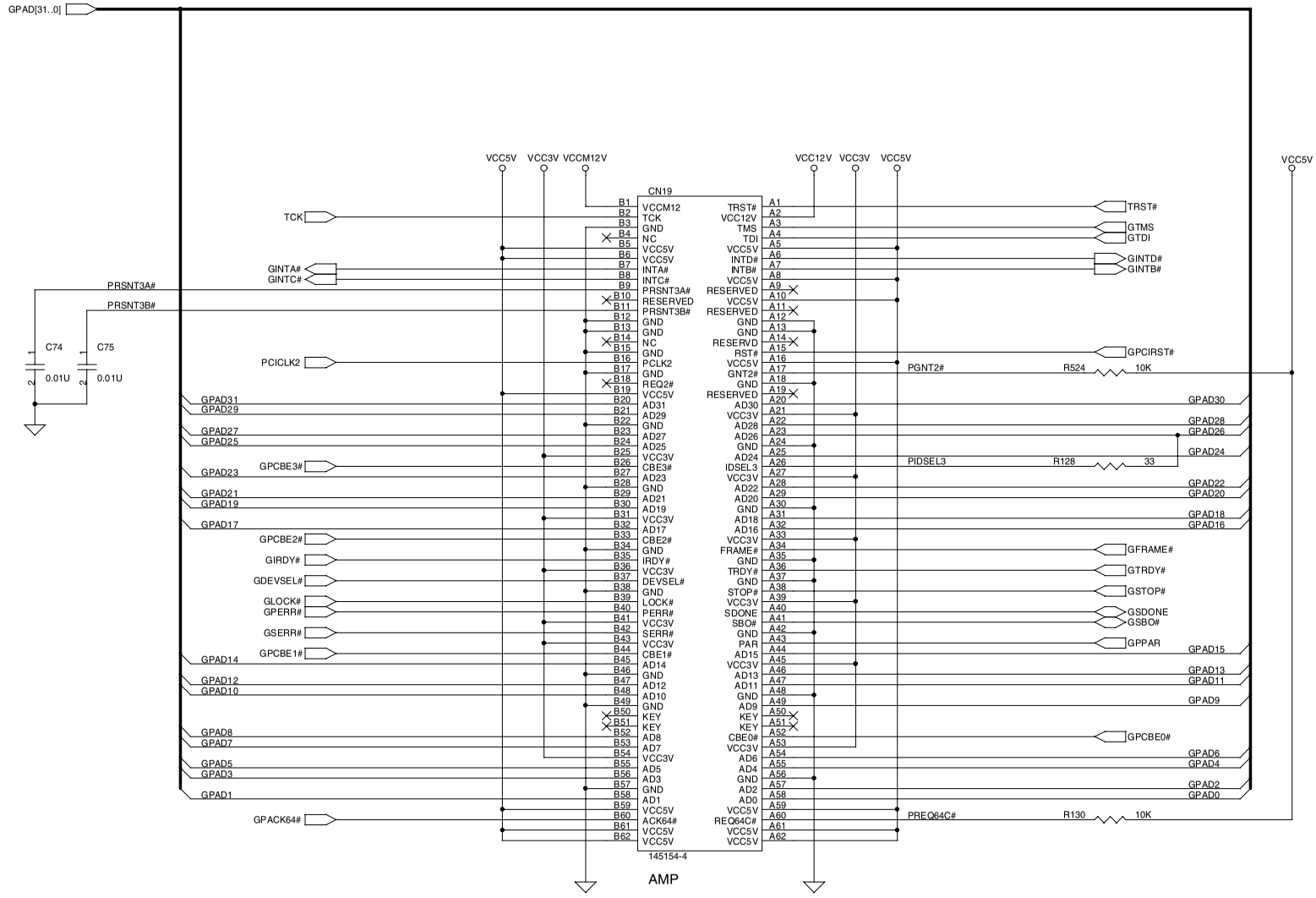


PCI - SLOT 2
(5V)

(DEVICE 0Fh)

IDSEL= PAD25

SEIKO EPSON CORPORATION	
Title: PCI BUS Slot	
Size: A3	Document Number:	Rev: A
Date: Tuesday, April 25, 2000	Sheet 10 of 21

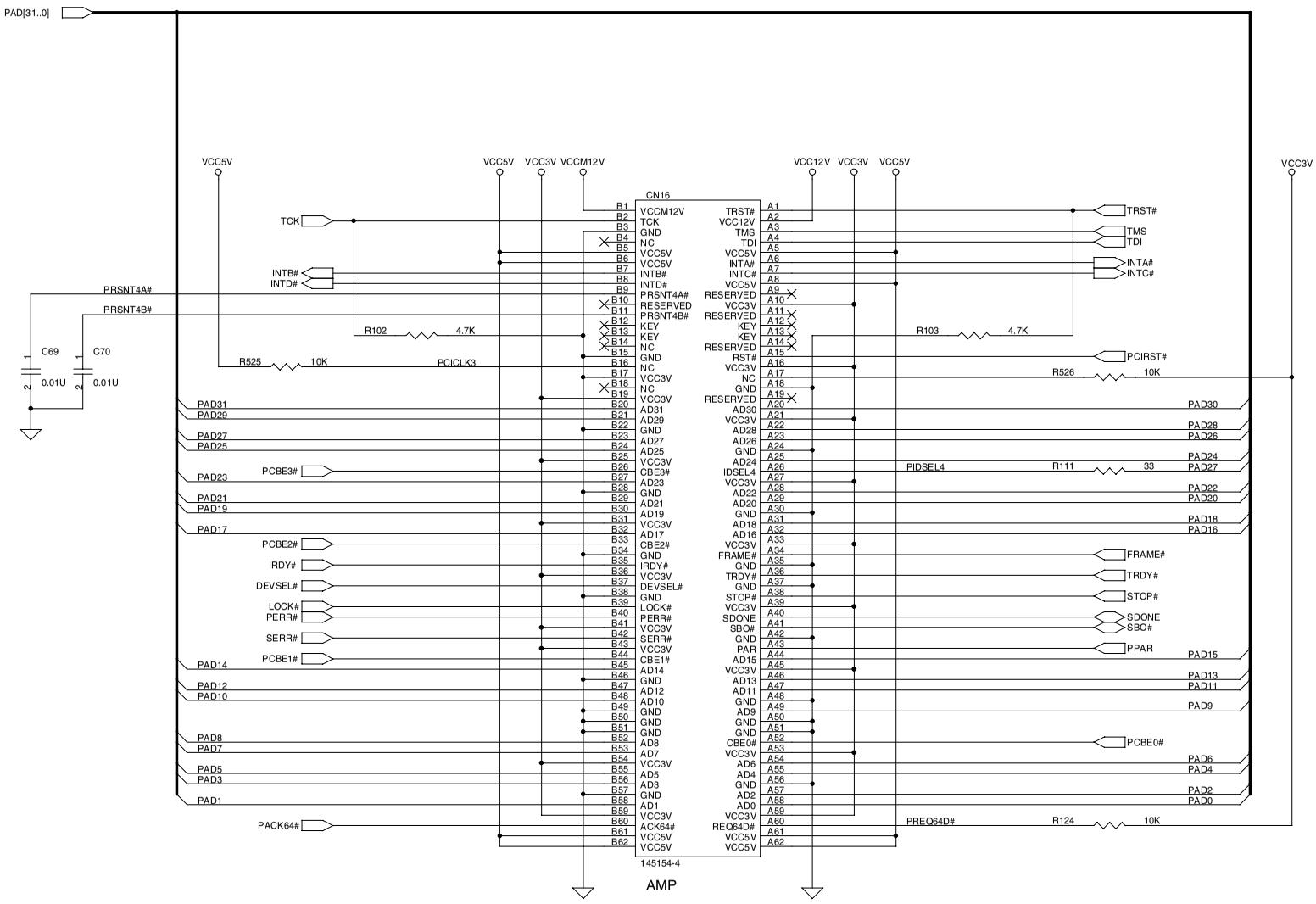


PCI - SLOT 3
(5V)

(DEVICE 10h)

IDSEL= PAD26

	SEIKO EPSON CORPORATION
Title	PCI BUS Slot
Size A3	Document Number
Rev	A
Date:	Tuesday, April 25, 2000
Sheet	11 of 21

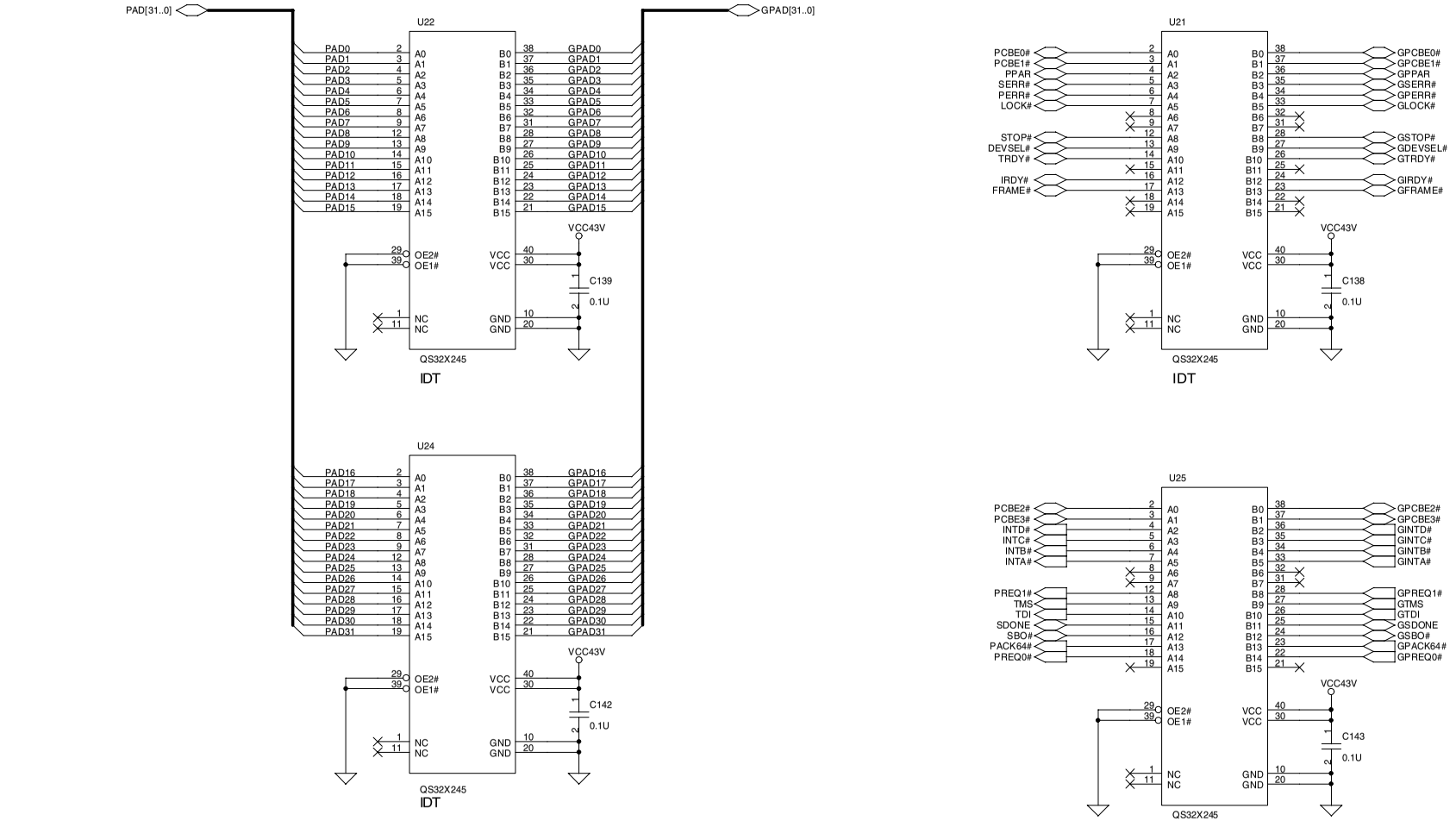


PCI - SLOT 4 (3.3V)
Debug perpose Only

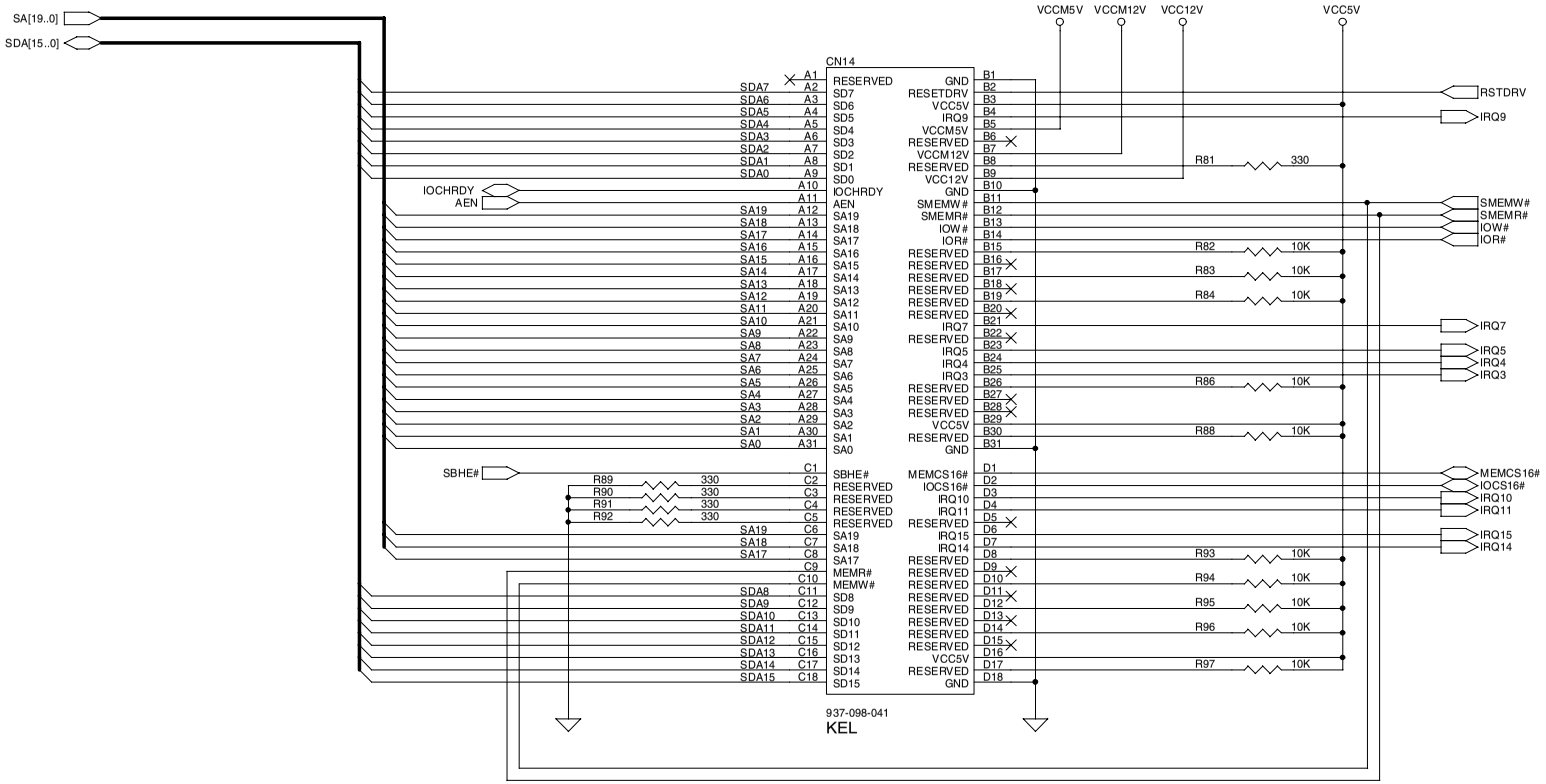
(DEVICE 11h)

IDSEL= PAD27

SEIKO EPSON CORPORATION		
Title: PCI BUS Slot		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 12 of 21	

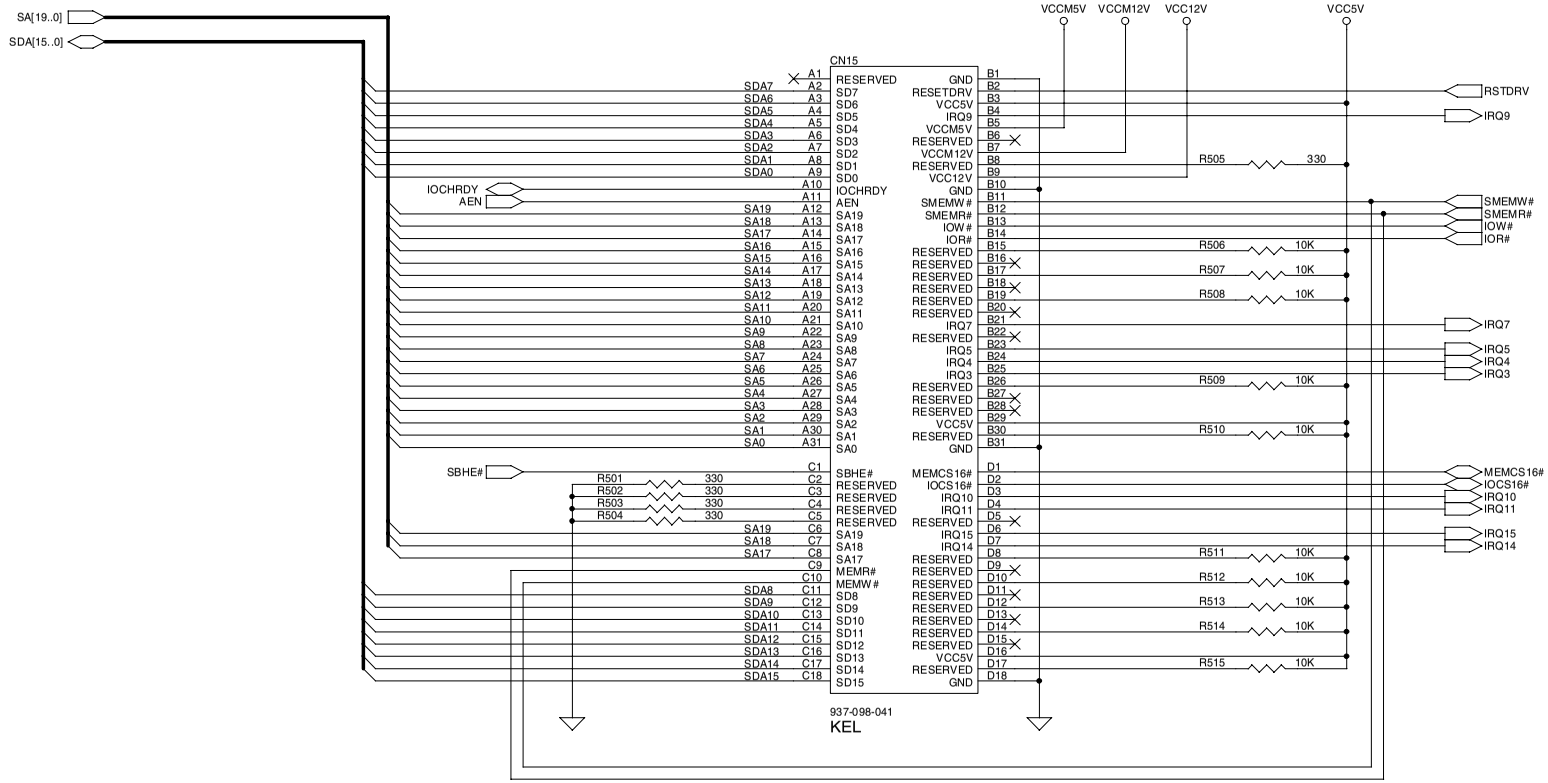


SEIKO EPSON CORPORATION		
Title: BUS Switch Circuit		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 13 of 21	



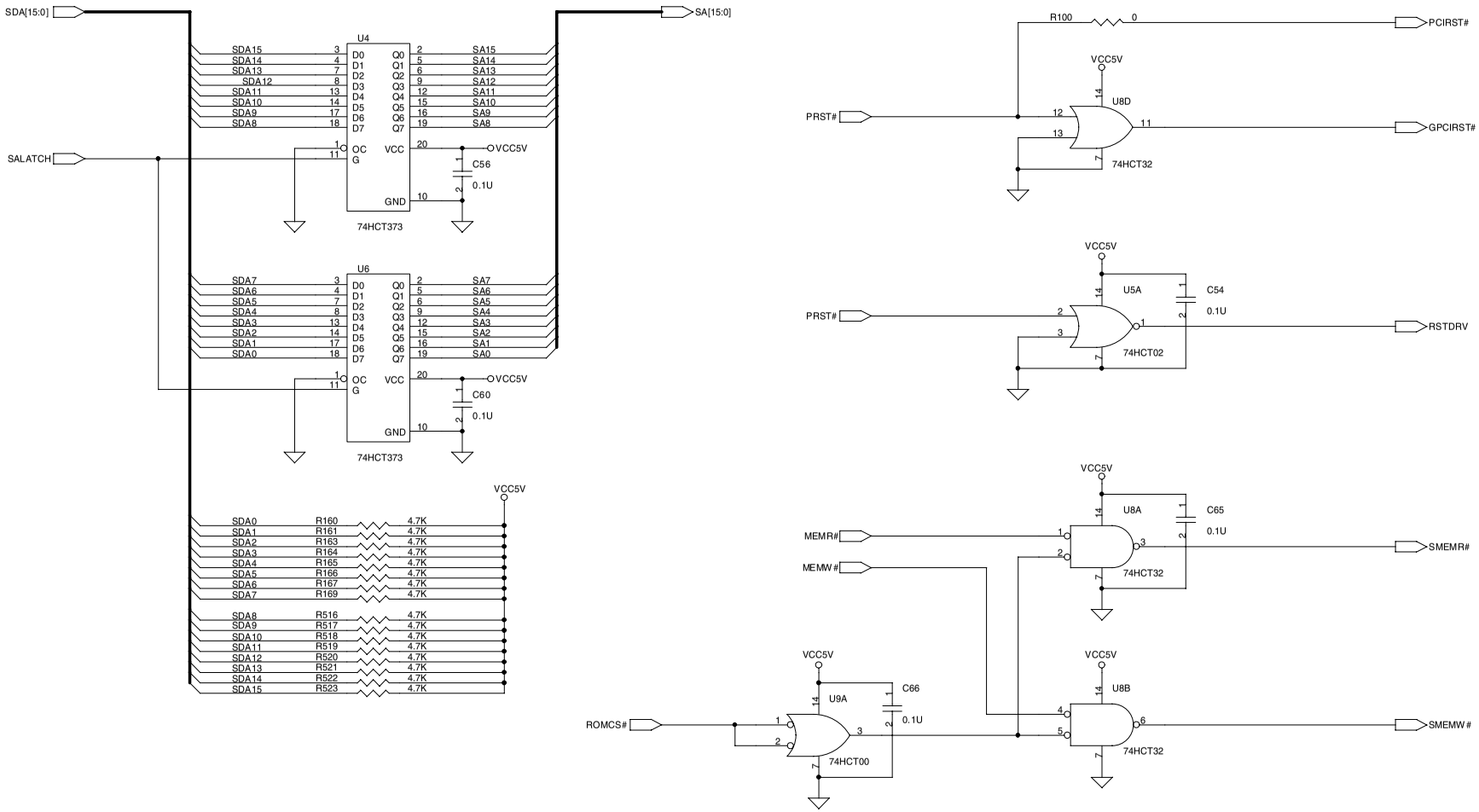
LIMITED ISA
SLOT-1

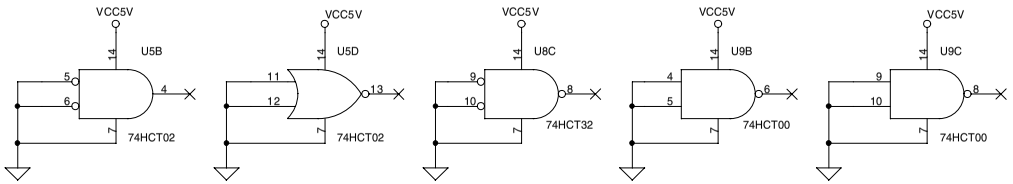
SEIKO EPSON CORPORATION		
Title: Limited ISA Slot		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 14 of 21	



LIMITED ISA SLOT-2

SEIKO EPSON CORPORATION			
Title: Limited ISA Slot			
Size: A3	Document Number		Rev: A
Date: Tuesday, April 25, 2000	Sheet 15 of 21		





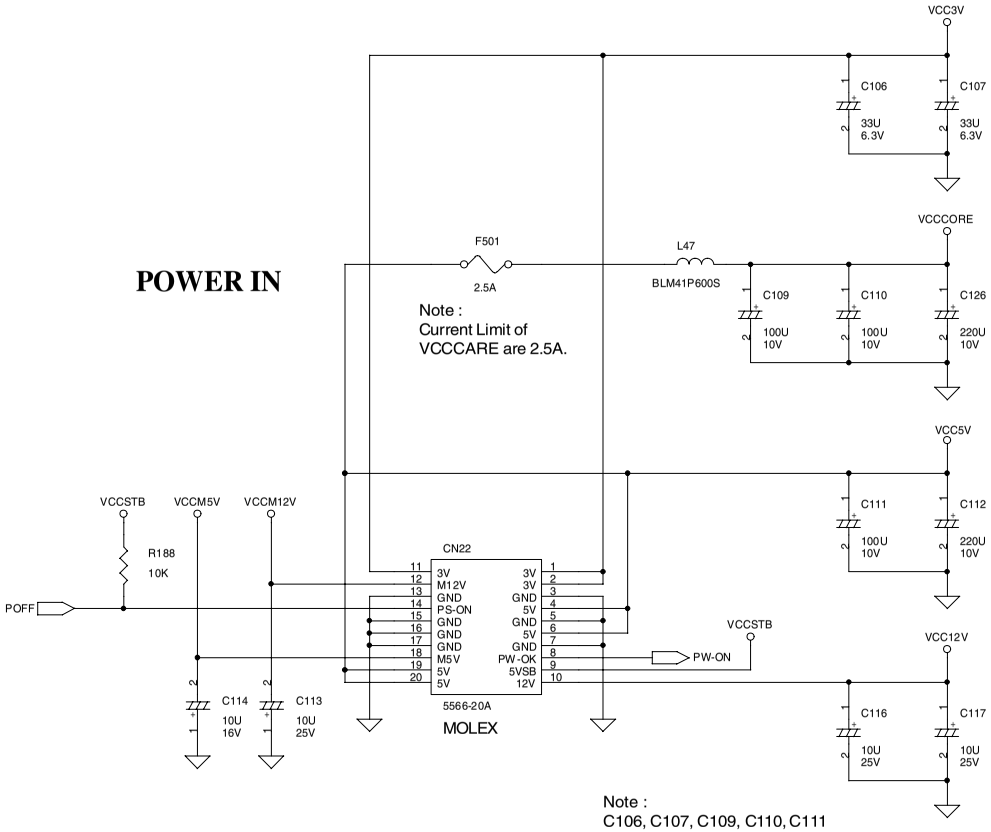
SEIKO EPSON CORPORATION

Title: ISA BUS Address Latch and Misk Circuit

Size	Document Number	Rev
A3		A

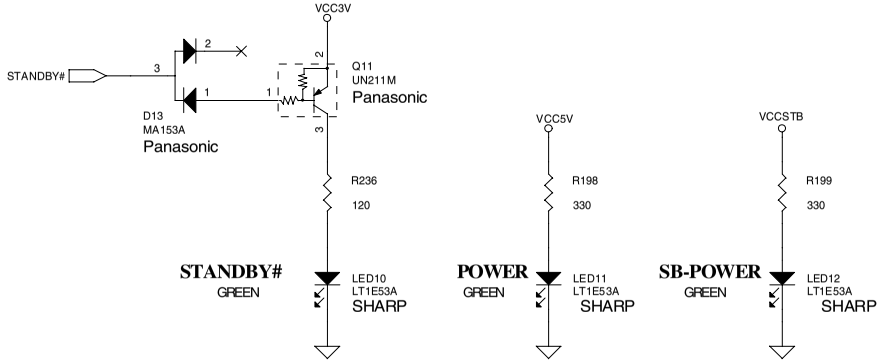
Date: Tuesday, April 25, 2000 Sheet 16 of 21

POWER IN

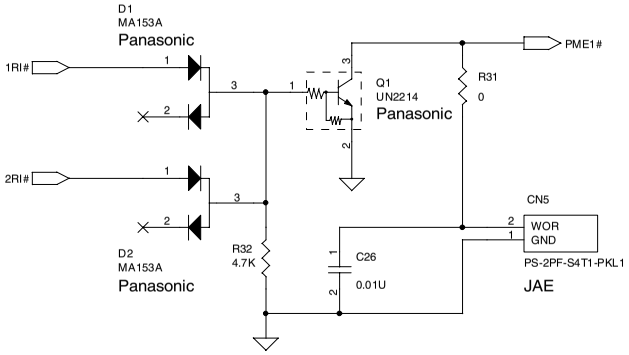


Note :
Current Limit of
VCCCARE are 2.5A.

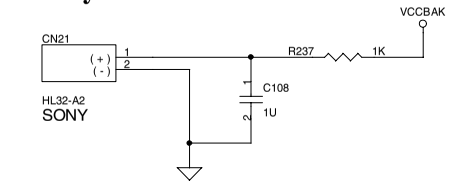
Note :
C106, C107, C109, C110, C111
OS-CON (SANYO)



Wake on Ring

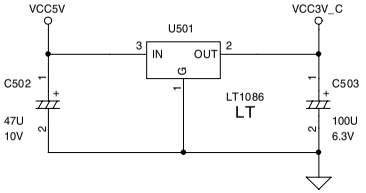


Battery Holder



NOTE :
Coin Lithum Battery CR2032

R237 is protection resistor
for preventing reverse current

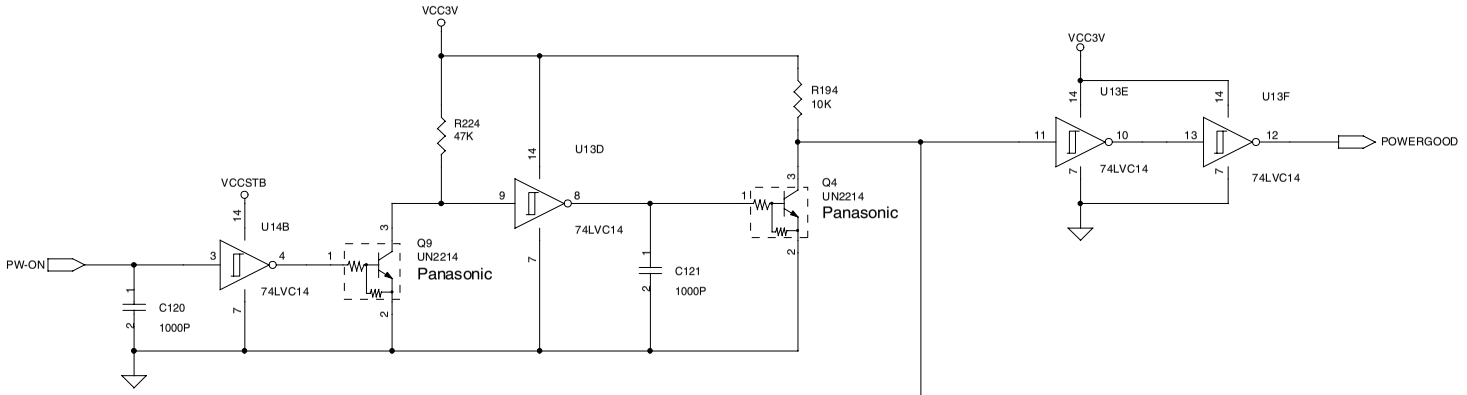


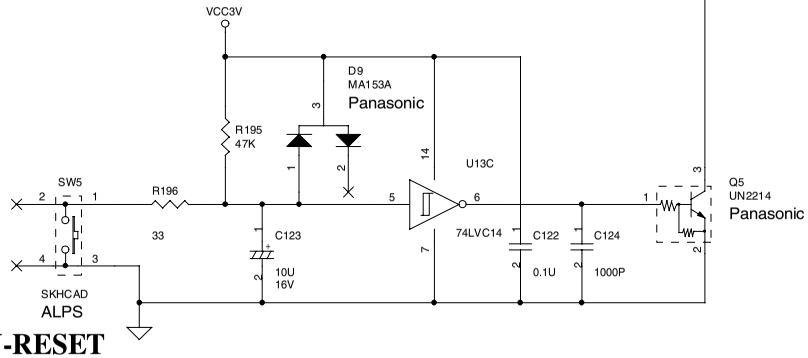
Note :
VCC3V_C is 3.3V power supply for CARD-PCI/GX.

LT : LINEAR TECHNOLOGY

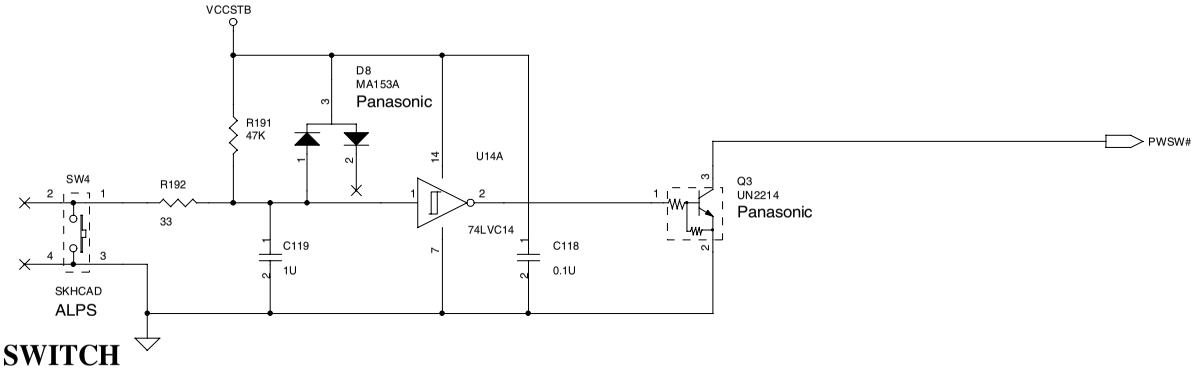
Wake On Lan

SEIKO EPSON CORPORATION		
Title: Power In and Wake On Ring/Wake On LAN Interface		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 17 of 21	

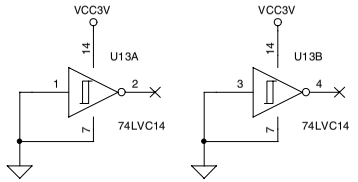


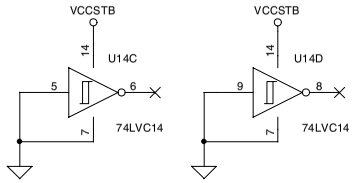


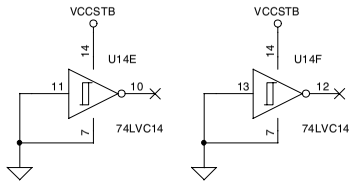
PON-RESET



POWER SWITCH

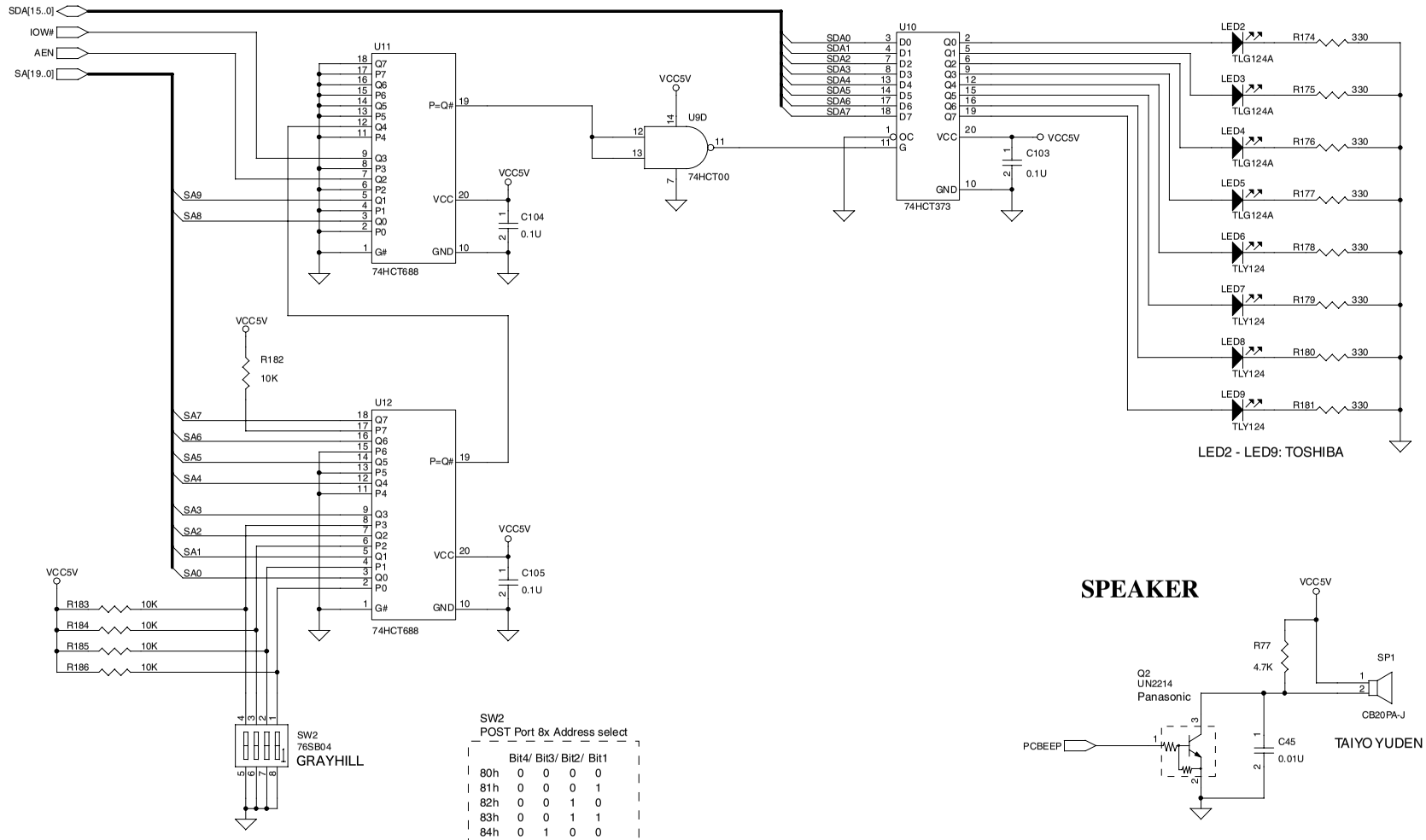






SEIKO EPSON CORPORATION

Title: Switches		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 18 of 21	



SPEAKER

SW2
POST Port 8x Address select

	Bit4/	Bit3/	Bit2/	Bit1
80h	0	0	0	0
81h	0	0	0	1
82h	0	0	1	0
83h	0	0	1	1
84h	0	1	0	0
85h	0	1	0	1
86h	0	1	1	0
87h	0	1	1	1
88h	1	0	0	0
89h	1	0	0	1
8Ah	1	0	1	0
8Bh	1	0	1	1
8Ch	1	1	0	0
8Dh	1	1	0	1
8Eh	1	1	1	0
8Fh	1	1	1	1

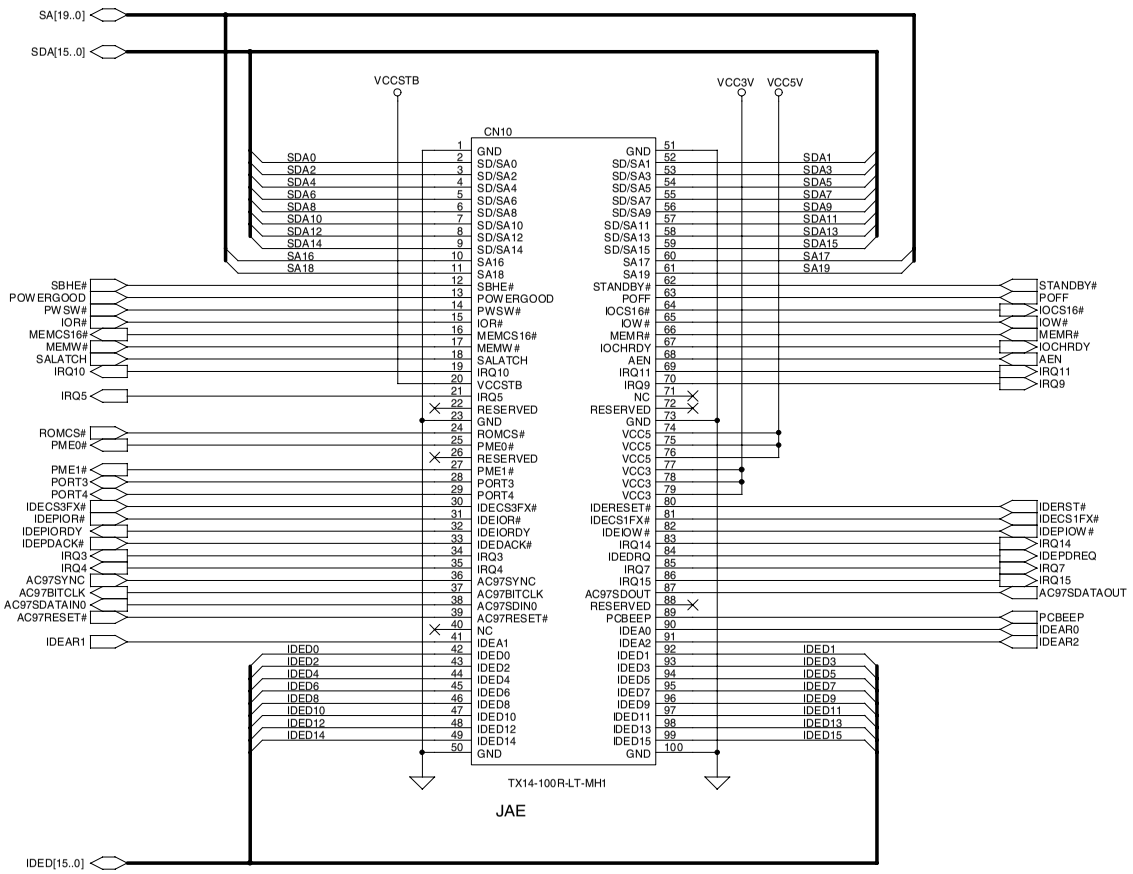
(0=SW-ON, 1=SW-OFF)

SEIKO EPSON CORPORATION

Title: LED Circuit for debugging and Speaker

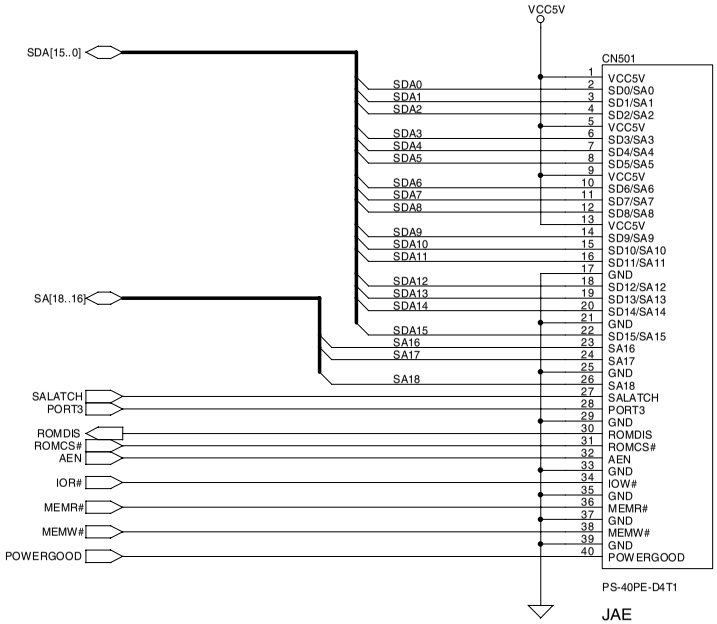
Size: A3 | Document Number | Rev: A

Date: Tuesday, April 25, 2000 | Sheet 19 of 21



EXTENDED

SEIKO EPSON CORPORATION		
Title: Extended Interface		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 20 of 21	



NOTE :
Select the connector which is most suitable for your system.

SEIKO EPSON CORPORATION		
Title: ROM Writer Board Interface		
Size: A3	Document Number	Rev: A
Date: Tuesday, April 25, 2000	Sheet 21 of 21	

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CARD-PCI/GX
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