MF1286-02

EPSON

CARD-PCI/GX

Hardware Manual

SEIKO EPSON CORPORATION

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1. Overview

SCE8720Cxx (CARD/PCI/GX) is the first product in SEIKO EPSON's CARD-PCI series equipped with the PCI bus. With the PCI bus, ability of enhancement, which enables various PCI devices to be connected, is realized.

By utilizing the Geode 200 MHz low voltage product, which comprises CPU core, and the companion chip manufactured by National Semiconductor, low power consumption, low cost and high quality display (CRT1280 × 1024, 256-color) are all realized. Especially, this low power consumption capability is one of the most important aspects to realize fan-less, which is required in applications requiring high liability.

All these capabilities are provided within a compact size of 101.6 ± 1.0 × 63.5 ± 0.3 × 16.0 ± 1.0 (mm) with 280-pin and 20-pin interface connectors.

Because SCE8720C can easily enable the core capabilities of IBM PC/AT, including BIOS, users can drastically decrease system development manpower and period.

In addition, future CARD-PCI series will also be able to be used with the same main board only requiring consideration on the card's mounting area and power supply.

1.1 System Overview

SCE8720Cxx (CARD-PCI/GX) is provided with almost all the functions usually equipped on a mother board. These functions are accessed via the 280-pin main connector and 20-pin connector.

As for 280-pin connector, manufacturer's genuine part is utilized. Functions accessed via the 280-pin connector are PCI extended bus, CRT or TFT LCD panel display, 2-channel USB, primary IDE, LIMITED ISA extended bus (*1), keyboard and mouse, 2-channel serial/parallel port and AC97 interface. FDD and a part of interrupt of ISA are accessed via the 20-pin connector.

SCE8720Cxx has Geode GX-LV 200MHz (CPU CHIP), Geode CS5530 (Companion chip), 97317 (Super IO) all built-in. As the main memory, SCE8720Cxx has a 32MB or 64MB of synchronous D-RAM and has utilized the unified memory method, in which a part of the synchronous D-RAM is used as the display memory. Generally, it is said that the unified memory method results in low-performance. However, with SCE8720Cxx, high performance is realized by compressing the data for display refreshing. In addition, SCE8720Cxx has a built-in CPU core power regulator (VRM) and a built-in CLOCK generator with built-in PLL. (*1: LIMITED ISA = ISA with limited capability)

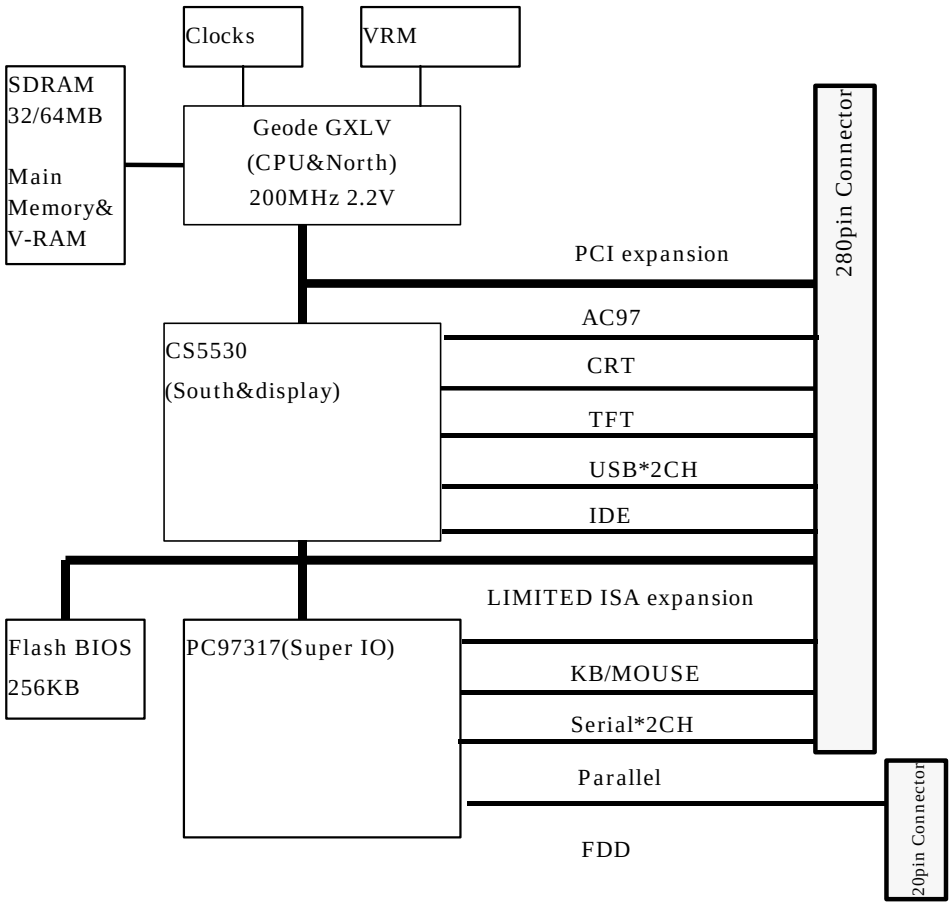
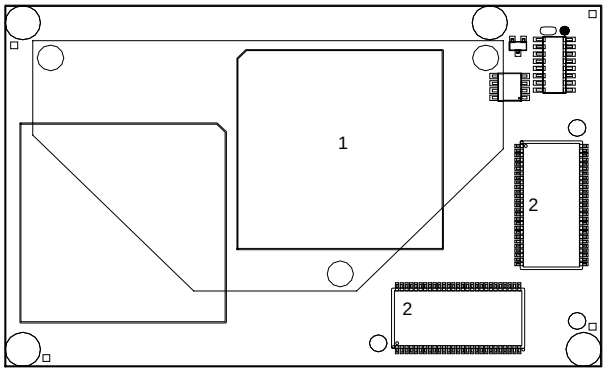


Figure1.1 Block diagram of SCE8720Cxx

1.2 Basic Specification

Item		Specifications
CPU		Geode GXLV 200MHz (Manufactured by National Semiconductor) (Cache memory 16KB built-in, FPU built-in)
Main memory		Synchronous DRAM 32MB/64MB
System ROM		256KB (System BIOS + VGA BIOS + Power management BIOS)
Companion chip		Geode CS5530 (Manufactured by National Semiconductor) (Graphic control, IDE AC97 etc.)
Graphic function		RAM Maximum 4MB (using a part of synchronous DRAM) CRT 60Hz (Max. XGA: 64K-color or SXGA: 256-color) TFT 18/12/9-bit TFT panel support (Max. XGA 64K-color) STN cannot be used.
I/O interface		
	PCI	3.3V PCI Version 2.1 Compliance (33MHz) PCI device 3 PCI master 2
	LIMITED ISA	No DMA or Master function provided. As for AB0-15, multiplex output to DB. Some signals have been deleted as well.
	Parallel	1-port SPP, ECP, EPP (rev1.9/1.7) supported.
	Serial	2-port (16550 compatible) Max.1.5Mbaud
	HDD(IDE)	1 device (ANSI ATA_4 Compliant)
	FDD	1 device (720/1.44MB 2mode, 3.5”)
	Keyboard	1PS/2-compatible
	Mouse	1PS/2-compatible
	USB	2-port, USB Revision 1.0 compliant
	Speaker	PC beep
	AC97	Version 2.0
Super I/O		PC97317 (Manufactured by National Semiconductor)
RTC		MC146818A-compatible, built in Super I/O.
Clock buffer		MK1491-06 (Manufactured by ICS)
Outside dimensions		101.6±1.0×63.5±0.3×16.0±1.0 (mm)
Weight		Approx. 82g

Operation environment (temperature ranges)
Maximum temperature [Tc = 75°C right above the heat sink, and Ta = 70°C around the SDRAM]
Minimum temperature Ta = 0°C



1: Heat sink on CPU
2: Ta around DRAM (peripheral temperature)

Figure 1.2 Temperature measurement position

Storage environment	Temperature	-20 to 75°C (no condensation)
	Humidity	0 to 90% (no condensation)
Current consumption	Maximum rating	7.1W

Power supply specifications (the following power supply is required.)
The following operational values are measured when Windows 98 is running and desktop is displayed.

CPU_VRM power supply (V_{CCCORE}) 5V

Current consumption	Typ.	408mA
Standby current	Typ.	17.2 mA

System power (V_{CC3V}) 3.3V

Current consumption	Typ.	620 mA
Standby current	Typ.	230 mA

ISA bus power supply (V_{CC5V}) 5V

Current consumption	Typ.	17.1 mA
Standby current	Typ.	11.5 mA

5V standby power (V_{CCSTB}) 5V

(Power of 5V is always supplied regardless of the ON/OFF of the power supply.)

Current consumption	Typ.	0.35 mA

Backup power (V_{CCBAK}) 2.7 to 3.6V (voltage supplied by battery)

Current consumption	Typ.	1.2 μA

(When holding the C-MOS memory contents by the battery)

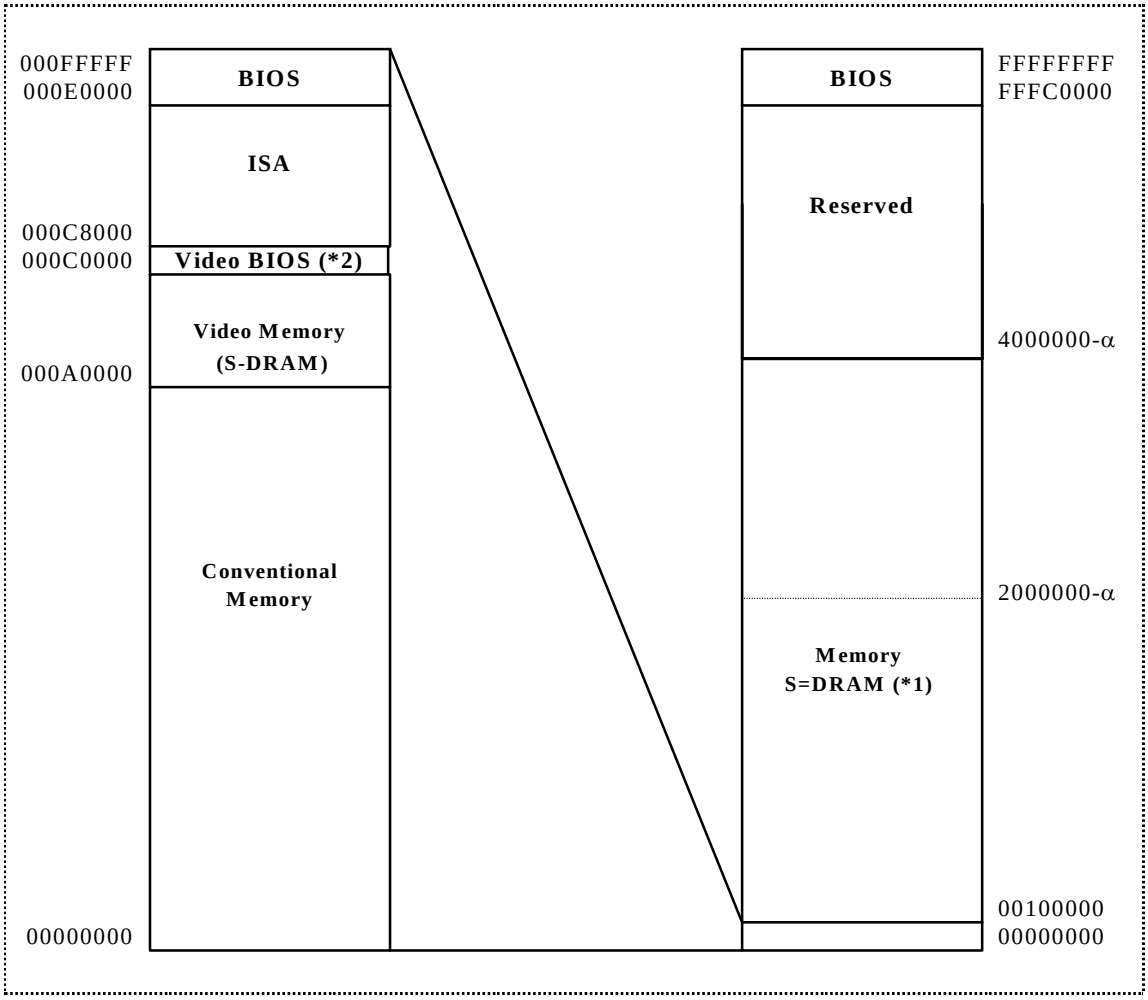
• Power management

Power ON (PME0#, 1#, power SW)
Power OFF (Soft OFF)
Standby mode

1.3 BIOS

SCE8720C has adopted AWARD BIOS manufactured by Phoenix. It has the power management and plug-and-play functions. With the BIOS setup menu, many configuration parameters can be set.
The Video BIOS is also stored in the same ROM.

1.4 Memory map



*1: Memory size can be 32MB or 64MB, depending on the model.

*2: With some types of Video, C0000h to CBFFFh can be occupied as VIDEO BIOS.

α : Area for the video memory: Max. 4MB

Figure 1.3 Memory map

1.5 I/O map

The I/O addresses 000h to 0FFh are assigned to the basic I/O. Although the addresses from 100h to 3FFh are for the ISA bus, SCE8720C has pre-built-in I/O.

These I/O addresses cannot be used when additionally setting I/O. I/O map is as follows:

Table 1.1 I/O map

I/O Address	Register		Function
000h-01Fh	00h RW	DMA Channel 0 Base and Current Address	DMA Controller 1 (82C37A equivalent)
	01h RW	DMA Channel 0 Base and Current Word	
	02h RW	DMA Channel 1 Base and Current Address	
	03h RW	DMA Channel 1 Base and Current Word	
	04h RW	DMA Channel 2 Base and Current Address	
	05h RW	DMA Channel 2 Base and Current Word	
	06h RW	DMA Channel 3 Base and Current Address	
	07h RW	DMA Channel 3 Base and Current Word	
	08h WO	Command Resister	
	08h RO	Status Register	
	09h WO	Request Register	
	0Ah WO	Single-Mask Register	
	0Bh WO	Mode Register	
	0Ch WO	Clear Byte Pointer	
	0Dh RO	Master Clear	
	0Dh WO	Temporary Register	
	0Eh WO	Clear Mask Register	
	0Fh WO	Write all Mask Register	
020h-021h	20h WO	Initialization Control Word ICW1	Interrupt Controller 1 (82C59A equivalent)
	20h WO	Operation Control Word OCW2	
	20h WO	Operation Control Word OCW3	
	20h RO	Interrupt Service Resister	
	20h RO	Interrupt Request Resister	
	21h WO	Initialization Control Word ICW2	
	21h WO	Initialization Control Word ICW3	
	21h WO	Initialization Control Word ICW4	
	21h RW	Operation Control Word OCW1	
	21h RW	Interrupt Mask Resister	

I/O Address	Register		Function
022h-2Dh	22h WO	Configuration Index Register	Geode GX-LV
	23h RW	Configuration Data Register	
O2Eh-03Fh	2Eh RW	Plug&Play Index Register	Plug&Play
	2Fh RW	Plug&Play Data Register	
040h-04Fh	40h RW	Channel 0 Count	Timer Counter 1 (8254 equivalent)
	41h RW	Channel 1 Count	
	42h RW	Channel 2 Count	
	43h RW	Command Register	
060h-06Fh	60h R	Keyboard controller Data Input Buffer	Keyboard Controller
	60h W	Keyboard controller Data Output Buffer	
	61h RW	Port B	
	62h RW	Keyboard controller mailbox Register	Keyboard Controller
	64h WO	Keyboard controller Command Register	
	64h RO	Keyboard Controller Status Register	
070h-07Fh	70h WO	RTC/CMOS RAM Address Port and NMI Mask	RTC/CMOS RAM
	71h RW	RTC/CMOS RAM Data port	
080h-09Fh	80h RW	Reserved	DMA Memory Address Mapper Page Register
	81h RW	Channel 2	
	82h RW	Channel 3	
	83h RW	Channel 1	
	84h RW	Reserved	
	85h RW	Reserved	
	86h RW	Reserved	
	87h RW	Channel 0	
	88h RW	Reserved	
	89h RW	Channel 6	
	8Ah RW	Channel 7	
	8Bh RW	Channel 5	
	8Ch RW	Reserved	
	8Dh RW	Reserved	
	8Eh RW	Reserved	
	8Fh RW	Refresh	
	92h RW	Port 92	

I/O Address	Register		Function
0A0h-BFh	A0h WO	Initialization Control Word ICW1	Interrupt Controller 2 (82C59A equivalent)
	A0h WO	Operation Control Word OCW2	
	A0h WO	Operation Control Word OCW3	
0A0h-BFh	A0h RO	Interrupt Service Resister	Interrupt Controller 2 (82C59A equivalent)
	A0h RO	Interrupt Request Resister	
	A1h WO	Initialization Control Word ICW2	
	A1h WO	Initialization Control Word ICW3	
	A1h WO	Initialization Control Word ICW4	
	A1h RW	Operation Control Word OCW1	
	A1h RW	Interrupt Mask Resister	
0C0h-0DFh	C0h RW	DMA Channel 4 Base and Current Address	DMA Controller 2 (82C37A equivalent)
	C2h RW	DMA Channel 4 Base and Current Word	
	C4h RW	DMA Channel 5 Base and Current Address	
	C6h RW	DMA Channel 5 Base and Current Word	
	C8h RW	DMA Channel 6 Base and Current Address	
	CAh RW	DMA Channel 6 Base and Current Word	
	CCh RW	DMA Channel 7 Base and Current Address	
	CEh RW	DMA Channel 7 Base and Current Word	
	D0h W0	Command Register	
	D0h RO	Status Register	
	D2h WO	Request Register	
	D4h WO	Mask Register	
	D6h WO	Mode Register	
	D8h WO	Clear Byte Pointer	
0F0h-0FFh	DAh RO	Master Clear	
	DAh WO	Temporary Register	
	DCh WO	Clear Mask Register	
	DEh WO	Write all Mask Register	
	F0h,F1h WO	Mathematical Co-processor Resister	
100h-1EFh	---	---	Usable with ISA bus

I/O Address	Register		Function
170h-177h	170h RW	Data Register	Hard Disk Controller
	171h RO	Error Register	
	172h RW	Sector Count	
	173h RW	Sector Number	
	174h RW	Cylinder HIGH	
	175h RW	Cylinder LOW	
	176h RW	SDH Register	
	177h RO	Status Register	
	177h WO	Command Register	
1F0h-1F7h	1F0h RW	Data Register	Hard Disk Controller
	1F1h RO	Error Register	
	1F2h RW	Sector Count	
	1F3h RW	Sector Number	
	1F4h RW	Cylinder HIGH	
	1F5h RW	Cylinder LOW	
	1F6h RW	SDH Register	
	1F7h RO	Status Register	
	1F7h WO	Command Register	
1F8h-277h	---	---	Usable with ISA bus
278h-27Fh	278h RW	LPT2 Data Port	Parallel Port 2
	279h RO	LPT2 Status Port	
	27Ah RW	LPT2 Control	
	27Bh RW	Automatic Address Strobe Register	
	27Ch RW	Automatic Data Strobe Register	
	27Dh RW	Automatic Data Strobe Register	
	27Eh RW	Automatic Data Strobe Register	
	27Fh RW	Automatic Data Strobe Register	
280h-2F7h	---	---	Usable with ISA bus
2F8h-2FFh	2F8h RO	Receiver Buffer	Serial Port 2
	2F8h WO	Transmit Holding Buffer	
	2F8h RW	Divider Latch Least Significant Byte	
	2F9h RW	Divider Latch Most Significant Byte	
	2F9h RW	Interrupt Enable Register	
	2FAh RO	Interrupt Register	
	2FBh RW	Line Controller Register	
	2FCh RW	MODEM Control Register	
	2FDh RO	Status Register	
	2FEh RO	MODEM Status Register	
	2FFh RW	Scratch Register	

I/O Address	Register		Function
300h-377h	---	---	Usable with ISA bus
378h-37Fh	378h RW	LPT1 Data Port	Parallel Port 1
	379h RO	LPT1 Status Port	
	37Ah RW	LPT1 Control	
	37Bh RW	Automatic Address Strobe Register	
	37Ch RW	Automatic Data Strobe Register	
	37Dh RW	Automatic Data Strobe Register	
	37Eh RW	Automatic Data Strobe Register	
	37Fh RW	Automatic Data Strobe Register	
380h-3B3h	---	---	Usable with ISA bus
3B4h-3BAh	3B4h RW	CRT Controller Index	VGA Controller (monochrome)
	3B5h RW	CRT Controller Data	
	3BAh W	Feature Control	
	3BAh R	Input Status Register	
3BBh-3BFh	---	---	Usable with ISA bus
3C0h-3CFh	3C0h W	Attribute Controller Index/Data	VGA Controller
	3C1h R	Attribute Controller Index/Data	
	3C2h W	Miscellaneous Output	
	3C2h R	Input Status Register	
	3C3h RW	VGA Enable	
	3C4h RW	Sequencer Index	
	3C5h RW	Sequencer Data	
	3C6h RW	Video DAC Pixel Mask,Hidden DAC Register	
3C0h-3CFh	3C7h W	Pixel Address Read Mode	VGA Controller
	3C7h R	DAC Status	
	3C8h RW	Pixel Mask Write Mode	
	3C9h RW	Pixel Data	
	3CAh R	Future Control Readback	
	3CCh R	Miscellaneous Output Readback	
	3CEh RW	Graphics Controller Index	
	3CFh RW	Graphics Controller Data	
3D0h-3DFh	3D4h RW	CRT Controller Index	VGA Controller (color)
	3D5h RW	CRT Controller Data	
	3DAh W	Feature Control	
	3DAh R	Input Status Register	
3E0h-3EFh	---	---	Usable with ISA bus

I/O Address	Register		Function
3F0h-3F7h	3F0h RW	Status Register A	FDD Controller
	3F1h RW	Status Register B	
	3F2h WO	Digital Output Register	
	3F3h RW	Tape Drive Register	
	3F4h RW	Main Status Register	
	3F5h RW	Data Register	
	3F6h RW	Alternate Status, Device Control	IDE
	3F7h RO	Digital Input Resister (Shared with Hard Disk Controller)	IDE 1 section FDD
3F8h-3FFh	3F7h WO	Diskette Control Register	FDD Controller
	3F8h RO	Receiver Buffer	Serial Port 1
	3F8h WO	Transmit holding Buffer	
	3F8h RW	Divider Latch Least Significant Byte	
	3F9h RW	Divider Latch Most Significant Byte	
	3F9h RW	Interrupt Enable Register	
	3FAh RO	Interrupt ID Register	
	3FBh RW	Line Control Register	
	3FCh RW	MODEM Control Register	
	3FDh RO	Status Register	
	3FEh RO	MODEM Status Register	
	3FFh RW	Scratch Register	

1.6 DMA controller

SCE8720C is provided with 2 DMA controllers (82C37A equivalent) used as follows. With SCE8720C, DMA is not available from users, as the ISA bus only has limited functions.

Table 1.2 DME controller 1

Channel No.	Device
CH0	Not available (cannot be used by user)
CH1	Not available (cannot be used by user)
CH2	Floppy disk
CH3	Not available (cannot be used by user)

Table 1.3 DME controller 2

Channel No.	Device
CH4	Cascade connection of controller 1.
CH5	Not available (cannot be used by user)
CH6	Not available (cannot be used by user)
CH7	Not available (cannot be used by user)

Controller 1, including CH0 to CH3, is used for 8-bit data transfer. Up to 64KB block transfer is possible between 8-bit I/O and 8-bit memory or 16-bit memory.
Controller 2, including CH4 to CH7, is mainly used for 16-bit data transfer, and among them CH4 is used for cascade connection of controller 1. CH5 to CH7 are not used.
Controller 2, including CH4 to CH7, is mainly used for 16-bit data transfer, and among them CH4 is used for cascade connection of controller 1. CH5 to CH7 are not used.

Table 1.4 DMA page register

Page register	I/O address
DMA channel 0	0087h
DMA channel 1	0083h
DMA channel 2	0081h
DMA channel 3	0082h
DMA channel 5	008Bh
DMA channel 6	0089h
DMA channel 7	008Ah
REFRESH	008Fh

1.7 System interrupts

The causes of interrupts on SCE8720C are shown below:

Table 1.5 Causes of interrupts

Level	Functions
SMI	External system management interrupt Power management VSA
IRQ	Interrupts by interrupt controller

IRQ interrupts are triggered by the 2 interrupt controllers (82C59 equivalent). The causes of interrupts by interrupt controllers are shown below:

Table 1.6 Levels of interrupts by interrupt controller

Controller 1	Controller 2	Device
IRQ0		Timer out 0
IRQ1		Keyboard
IRQ2		Cascade connection from controller 2
	IRQ8	Real time clock
	IRQ9	Usable with ISA bus
	IRQ10	Serial port (*)
	IRQ11	Serial port (*)
	IRQ12	Mouse
	IRQ13	Co-Processor
	IRQ14	HDD
	IRQ15	Usable with ISA bus
IRQ3		Serial port 2 (*)
IRQ4		Serial port 1 (*)
IRQ5		Parallel port 2 (*)
IRQ6		FDD
IRQ7		Parallel port 1 (*)

*: SCE8720C has 2 serial ports and 1 parallel port built-in. Serial port interrupts are selected from IRQ3, 4, 10 or 11, and parallel port interrupts are selected from IRQ5 or 7. Interrupts not used by the built-in serial or parallel port can then be used with ISA bus.

Also, when not using HDD, IRQ14 can be used with ISA bus.

1.8 Timer counter

SCE8720C has a 8254-equivalent timer counter and 3 independent timers. Their usage and inputs are shown below:

Table 1.7 Timer 1 settings

Channel 0 System timer	GATE 0	Fixed to ON
	CLK IN 0	1.19MHz
	CLK OUT 0	Connected to IRQ0 of interrupt controller 1.
Channel 1 Refresh request	GATE 1	Fixed to ON
	CLK IN 1	1.19MHz
	CLK OUT 1	Refresh request
Channel 2 Speaker interface	GATE 2	Controlled by I/O port 61h.
	CLK IN 2	1.19MHz
	CLK OUT 2	Used to drive the speaker interface.

1.9 Real time clock and C-MOS RAM

SCE8720C has a real time clock which provides clock and calendar functions and CMOS RAM used to hold system configuration information. The real time clock is compatible with 146818.

Power must be supplied constantly to the V_{CCBAK} in order to maintain the operation of the real time clock and the contents of CMOS RAM.

When V_{CCSTB} is supplied even while the system power is OFF, power from the V_{CCSTB} is used for backup. When both the system power and V_{CCSTB} is OFF, battery power from the V_{CCBAK} is used.

2. Mechanical specifications

2.1 Dimensions and weight

Dimensions

Width	101.6±1.0	(mm)
Depth	63.5±0.3	(mm)
Height	16.0±1.0	(mm)
Weight	Approx. 82g	

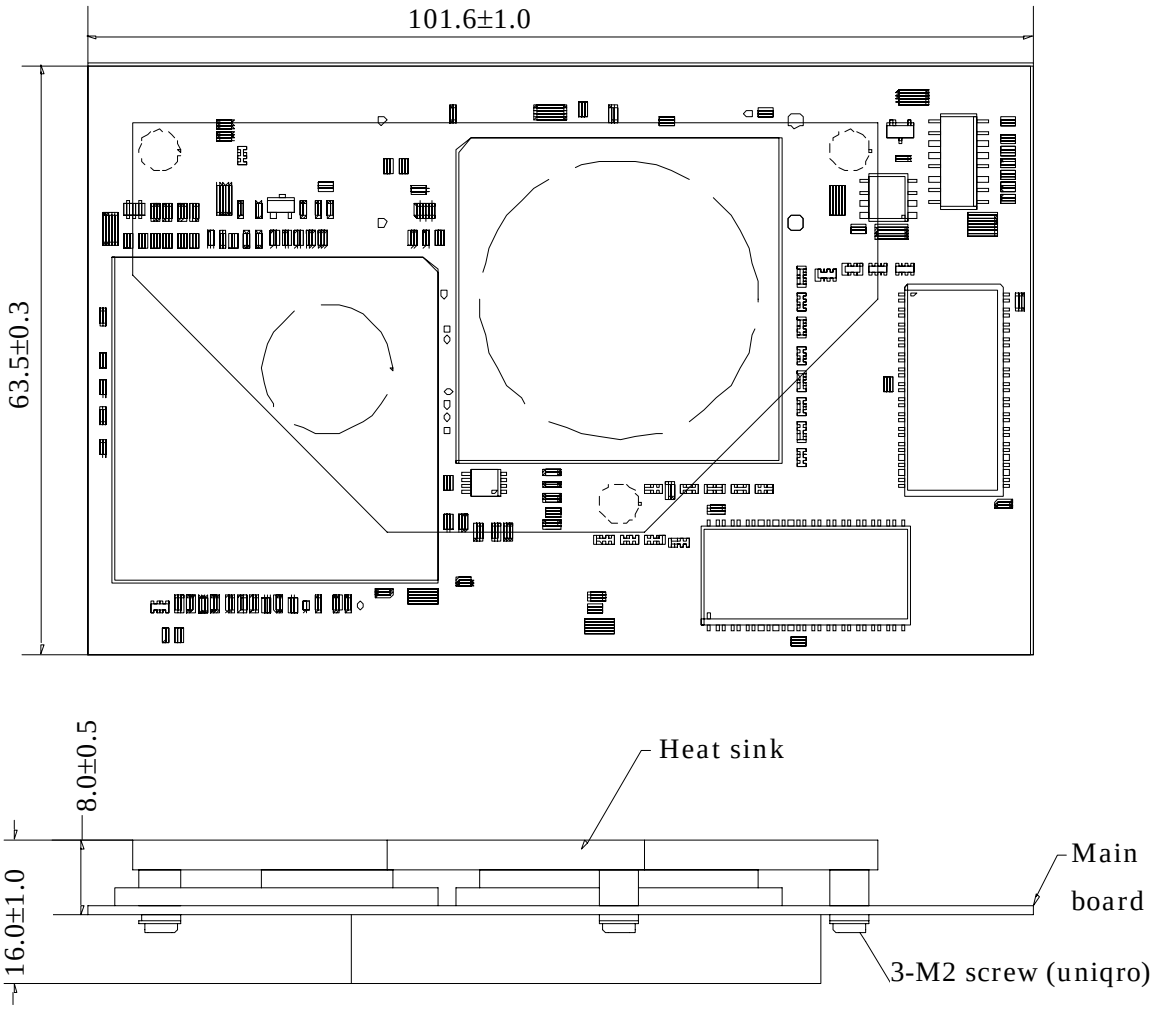


Figure 2.1 Dimensional Diagram

2.2 Installation method

CARD-PCI installation connector
280-pin connector product name 1-353906-0 Manufactured by AMP
20-pin connector product name 52030-2010 (ZIF, DIP) Manufactured by Molex

For more information about installation, refer to the application note.

3. Interface specifications

3.1 Pin configuration

Pin configurations for the 20-pin connector (mainly FDD signal) and 280-pin connector of SCE8720C are shown in the figure.

In the figure, 280-pin connector is viewed from the rear side. Connector pin configurations on the main board, on which SCE8720C is installed, are shown in the figure. (Note that the 1 pin mark on the connector is different.)

Since the 20-pin connector is connected using the flexible flat cable (FFC), pin configurations on the receiving side board vary depending on the connector's installation method.

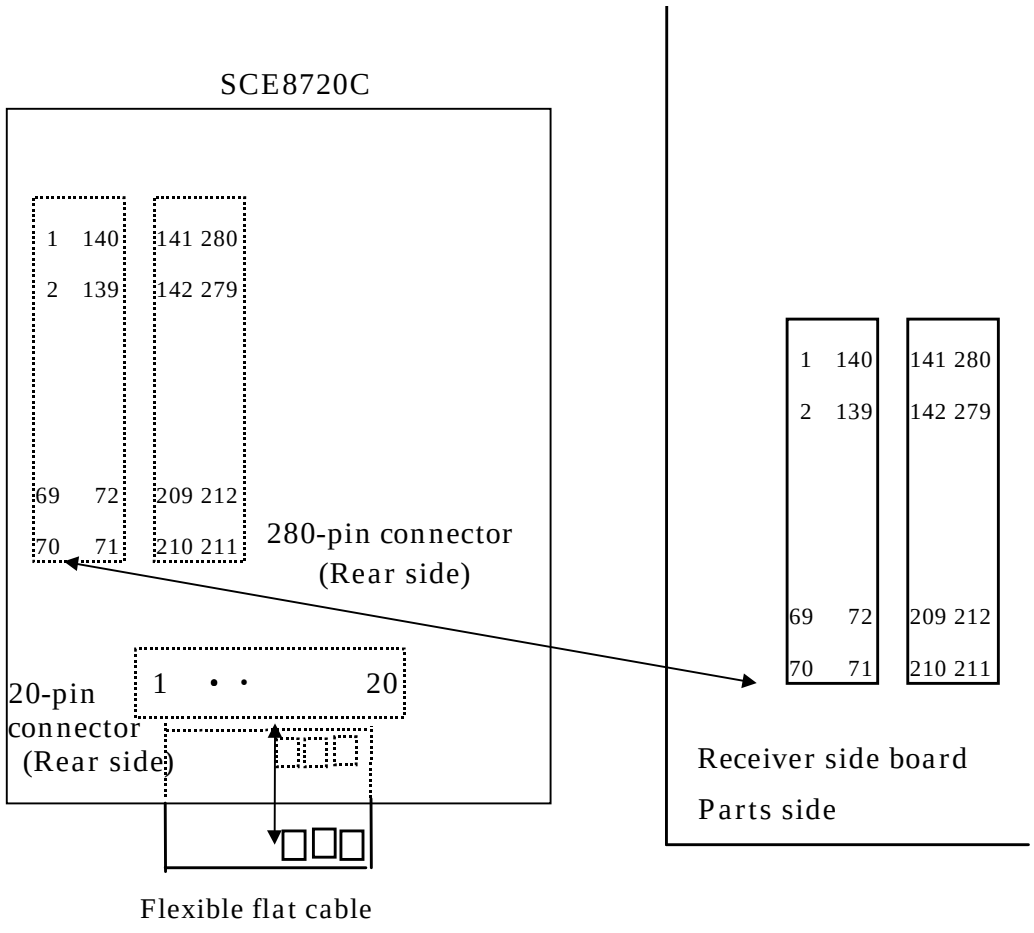


Figure 3.1 Connector pin configuration

* 280-pin connector

  Most of the signals and powers of SCE8720C are connected via this connector. It consists of 2 140-pin connectors.

* 20-pin connector

  Connector for the flexible flat cable.

  Signals for FDD and ISA bus interrupt signals are connected to this connector. When not using such signals, this connector is unconnected.

3.1.1 280-pin connector pin configuration

Table 3.1 280-pin connector pin configuration

No.	Signal Name	Block	No.	Signal Name	Block	No.	Signal Name	Block	No.	Signal Name	Block
1	GND	PWR	140	GND	PWR	141	GND	PWR	280	GND	PWR
2	AD0	PCI	139	CRTR	CRT	142	FPDOTE	FP	279	FPDOTCLK	FP
3	AD1	PCI	138	CRTG	CRT	143	FPVEEON	FP	278	FPVDDON	FP
4	AD2	PCI	137	CRTB	CRT	144	RESERVED	Video	277	IDEIOR#	IDE
5	VCC3V	PWR	136	VCC3V	PWR	145	GND	PWR	276	IDEIOW#	IDE
6	AD3	PCI	135	CRTHSYNC	CRT	146	FPVSYNC	FP	275	IDEACK#	IDE
7	AD4	PCI	134	CRTVSYNC	CRT	147	FPDATA0	FP	274	IDED7	IDE
8	AD5	PCI	133	RESERVED	AC97	148	FPHSYNC	FP	273	IDECS1FX#	IDE
9	AD6	PCI	132	AC97RESET#	AC97	149	FPDATA1	FP	272	IDED8	IDE
10	AD7	PCI	131	AC97SYNC	AC97	150	FPDATA2	FP	271	IDED6	IDE
11	GND	PWR	130	GND	PWR	151	GND	PWR	270	GND	PWR
12	CBE0#	PCI	129	AC97BITCLK	AC97	152	FPDATA3	FP	269	IDED9	IDE
13	AD8	PCI	128	AC97SDIN0	AC97	153	FPDISPEN	FP	268	IDERESET#	IDE
14	AD9	PCI	127	AC97SDOUT	AC97	154	FPDATA4	FP	267	IDED5	IDE
15	AD10	PCI	126	PCBEEP	MISC	155	FPDATA5	FP	266	IDECS3FX#	IDE
16	VCCSTB	PWR	125	VCC3V	PWR	156	FPDATA6	FP	265	IDED10	IDE
17	AD11	PCI	124	USBON	USB	157	FPDATA7	FP	264	IDED4	IDE
18	AD12	PCI	123	USBCUR#	USB	158	FPDATA8	FP	263	IDED11	IDE
19	AD13	PCI	122	USBDM0	USB	159	FPDATA9	FP	262	IDED3	IDE
20	AD14	PCI	121	USBDP0	USB	160	FPDATA10	FP	261	IDED12	IDE
21	GND	PWR	120	GND	PWR	161	GND	PWR	260	GND	PWR
22	AD15	PCI	119	USBDM1	USB	162	FPDATA11	FP	259	IDED2	IDE
23	CBE1#	PCI	118	USBDP1	USB	163	FPDATA12	FP	258	IDED13	IDE
24	PAR	PCI	117	STANDBY#	PM	164	FPDATA13	FP	257	IDED1	IDE
25	VCC5V	PWR	116	VCC5V	PWR	165	FPDATA14	FP	256	IDED14	IDE
26	SERR#	PCI	115	POFF	PM	166	FPDATA15	FP	255	IDED0	IDE
27	PERR#	PCI	114	PWSW#	PM	167	FPDATA16	FP	254	IDED15	IDE
28	LOCK#	PCI	113	LPTD7	LPT	168	FPDATA17	FP	253	IDEA2	IDE
29	STOP#	PCI	112	LPTD6	LPT	169	RESERVED	MISC	252	IDEA1	IDE
30	DEVSEL#	PCI	111	LPTD5	LPT	170	RESERVED	MISC	251	IDEA0	IDE
31	GND	PWR	110	GND	PWR	171	GND	PWR	250	GND	PWR
32	TRDY#	PCI	109	LPTD4	LPT	172	RESERVED	MISC	249	IDEDRQ	IDE
33	RESERVED	MISC	108	LPTD3	LPT	173	RESERVED	MISC	248	IDERDY	IDE
34	IRDY#	PCI	107	LPTD2	LPT	174	RESERVED	MISC	247	IDEINT	IDE
35	VCC3V	PWR	106	VCC3V	PWR	175	VCCCORE	PWR	246	POWERGOOD	PM
36	FRAME#	PCI	105	LPTD1	LPT	176	VCCCORE	PWR	245	IOCS16#	ISA
37	PME0#	PM	104	LPTD0	LPT	177	VCCCORE	PWR	244	IOCHRDY	ISA
38	CBE2#	PCI	103	LPTAFD#	LPT	178	VCCCORE	PWR	243	VCCCORE	PWR
39	AD16	PCI	102	LPTSLCTIN#	LPT	179	RESERVED	MISC	242	IOW#	ISA
40	GND	PWR	101	GND	PWR	180	GND	PWR	241	GND	PWR
41	AD17	PCI	100	LPTINIT#	LPT	181	MEMCS16#	ISA	240	IOR#	ISA
42	AD18	PCI	99	LPTERROR#	LPT	182	RESERVED	MISC	239	SD15/SA15	ISA
43	AD19	PCI	98	LPTPE	LPT	183	VCCCORE	PWR	238	SD14/SA14	ISA
44	AD20	PCI	97	LPTSLCT	LPT	184	VCCCORE	PWR	237	SD13/SA13	ISA
45	VCC3V	PWR	96	VCC3V	PWR	185	VCCCORE	PWR	236	SD12/SA12	ISA
46	AD21	PCI	95	LPTACK#	LPT	186	VCCCORE	PWR	235	SD11/SA11	ISA
47	AD22	PCI	94	LPTSTROBE#	LPT	187	RESERVED	MISC	234	SD10/SA10	ISA
48	AD23	PCI	93	LPTBUSY	LPT	188	ROMCS#	ISA	233	VCCCORE	PWR
49	CBE3#	PCI	92	IRQ5	ISA	189	MEMW#	ISA	232	SD9/SA9	ISA
50	GND	PWR	91	GND	PWR	190	GND	PWR	231	GND	PWR
51	AD24	PCI	90	PORT3	GPIO	191	MEMR#	ISA	230	SD8/SA8	ISA
52	AD25	PCI	89	PORT4	GPIO	192	SA16	ISA	229	SD0/SA0	ISA
53	AD26	PCI	88	PME1#	PM	193	SA17	ISA	228	SD1/SA1	ISA
54	AD27	PCI	87	MSDATA	KB/MS	194	SA18	ISA	227	SD2/SA2	ISA
55	VCC3V	PWR	86	MSCLK	KB/MS	195	SA19	ISA	226	SD3/SA3	ISA
56	AD28	PCI	85	VCCBAK	PWR	196	AEN	ISA	225	SD4/SA4	ISA
57	AD29	PCI	84	KBDATA	KB/MS	197	SBHE#	ISA	224	SD5/SA5	ISA
58	AD30	PCI	83	KBCLK	KB/MS	198	IRQ10	ISA	223	SD6/SA6	ISA
59	AD31	PCI	82	RESERVED	MISC	199	IRQ11	ISA	222	SD7/SA7	ISA
60	GND	PWR	81	GND	PWR	200	GND	PWR	221	GND	PWR
61	RST#	PCI	80	RESERVED	MISC	201	IRQ9	ISA	220	SALATCH	ISA
62	INTD#	PCI	79	RESERVED	MISC	202	COM2CTS#	COM2	219	COM1CTS#	COM1
63	INTC#	PCI	78	REQ1#	PCI	203	COM2CD#	COM2	218	COM1CD#	COM1
64	INTB#	PCI	77	GNT1#	PCI	204	COM2DSR#	COM2	217	COM1DSR#	COM1
65	INTA#	PCI	76	REQ0#	PCI	205	COM2DTR#	COM2	216	COM1DTR#	COM1
66	VCC3V	PWR	75	VCC3V	PWR	206	COM2RI#	COM2	215	COM1RI#	COM1
67	PCLK2	PCI	74	GNT0#	PCI	207	COM2RTS#	COM2	214	COM1RTS#	COM1
68	CPUFRQ	MISC	73	ROMDIS	MISC	208	COM2RXD	COM2	213	COM1RXD	COM1
69	PCLK0	PCI	72	PCLK1	PCI	209	COM2TXD	COM2	212	COM1TXD	COM1
70	GND	PWR	71	GND	PWR	210	GND	PWR	211	GND	PWR

3.1.2 20-pin connector pin configuration

Table 3.2 20-pin connector pin configuration

Pin No.	Signal name	Block
1	DSKCHG#	FDD
2	WP#	FDD
3	INDEX#	FDD
4	TRK0#	FDD
5	RDATA#	FDD
6	DENSEL	FDD
7	WGATE#	FDD
8	HDSEL#	FDD
9	STEP#	FDD
10	DIR#	FDD
11	WDATA#	FDD
12	DR0#	FDD
13	MTR0#	FDD
14	GND	PWR
15	IRQ15	ISA
16	IRQ 7	ISA
17	GND	PWR
18	IRQ4	ISA
19	GND	PWR
20	IRQ3	ISA

3.2 Signal characteristics

This section describes characteristics of each signal. Characteristic factors are as follows:

- I/O Type of signal input/output.
- Voltage Input: Indicates the voltage level that can be input.
  Output: Indicates the voltage level that can be output.
- pull-up /down
  Indicates whether or not the signal is pulled-up or pulled-down inside SCE8720C.
- I_{OL}/I_{OH} Indicates drive ability of the output buffer sink current and source current.
- Reference PU/PD Reference value of required pull-up or pull-down resistance.
  (When using all the IO port.)
- pull-up /down when not used
  Indicates whether or not pull-up or pull-down is required when not using signals.

Descriptions on symbols indicating these factors are shown below:

Symbol description

Item	Symbol	Description
I/O	I/O	Input/output
	s/t/s	Sustained tri-state (reference PCI v2.1))
	I/OD	Input and open drain output
	I	Input only
	O	Output only
	OD	Open drain output
	programmable	Input/output is set by software.
Voltage	3.3V	Output is 0 to 3.3V. Input must be 0 to 3.3V.
	3.3V ,5VT	Output is 0 to 3.3V. Input can be 0 to 5V. (5V input is TTL level.)
	5VSTB	V_{CCSTB} is supplied to the input/output element power supply.
	5V	Both input and output is 0 to 5.0V (5V input is TTL level.)
pull-up /down	XpU(5V)	Pulled-up to 5V by resistance of xΩ inside SCE8720C.
	xPU(3.3V)	Pulled-up to 3.3V by resistance of x Ω inside SCE8720C.
	xPU(5VSTB)	Pulled-up to V_{CCSTB} by resistance of x Ω inside SCE8720C.
	xPD	Pulled-down by resistance of x Ω inside SCE8720C.
	weak-PU	Pulled-up to 5V by Approx. 40kΩ resistance.
	Weak-PD	Pulled-down by Approx. 40kΩ resistance.
I_{OL}/I_{OH}	x/-y	Output drivability: sink current x, source current y
Refe- rence PU/PD	xPU(5V)	Pulled-up to 5V by x Ω resistance.
	XPU(5VSTB)	Pulled-up to V_{CCSTB} by x Ω resistance.
	XPU(3.3V)	Pulled-up to 3.3V by x Ω resistance.
pull-up /down when not used	PU	Even when not using the signal in the system, some kind of pull-up is necessary. NC is not available.

Signal characteristics

Table 3.3 PCI signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
AD[31:0],CBE[3:0]#,PAR	37	PCI	I/O	3.3V	---	5mA	-2mA	---	---
FRAME#,IRDY#,TRDY#, STOP# ,DEVSEL#,LOCK# ,PERR#	7	PCI	s/t/s	3.3V	20kPU (3.3V)	5mA	-2mA	8.2kPU (3.3V)	---
SERR#	1	PCI	I/OD	3.3V	20kPU (3.3V)	5mA	---	8.2kPU (3.3V)	---
RST#	1	PCI	O	3.3V	---	16mA	-16mA	---	---
REQ[1:0]#	2	PCI	I	3.3V	20kPU (3.3V)	---	---	---	---
GNT[1:0]#	2	PCI	O	3.3V	---	5mA	-2mA	---	---
PCLK[2:0]	3	PCI	O	3.3V	---	8mA	-8mA	---	---
INTA#,INTB#, INTC#,INTD#	4	PCI	I	3.3V	---	---	---	2.7kPU (3.3V)	PU

Table 3.4 ISA signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
SD/SA[15:8]	8	ISA	I/O	3.3V, 5VT	20kPU (3.3V)	8mA	-8mA	---	---
SD/SA[7:0]	8	ISA	I/O	3.3V, 5VT	20kPU (3.3V)	8mA	-8mA	4.7kPU (5V)	---
SA[19:16],SBHE#	5	ISA	O	3.3V	20kPU (3.3V)	8mA	-8mA	---	---
MEMR#,MEMW#,IOR#, IOW#	4	ISA	O	3.3V, 5VT	4.7kPU (5V)	8mA	-8mA	---	---
SALATCH	1	ISA	O	3.3V	---	4mA	-4mA	---	---
AEN	1	ISA	O	3.3V	---	8mA	-8mA	---	---
ROMCS#	1	ISA	O	3.3V	---	4mA	-4mA	---	---
MEMCS16#,IOCS16#	2	ISA	I	3.3V, 5VT	1kPU (5V)	---	---	---	---
IOCHRDY	1	ISA	I	3.3V, 5VT	1kPU (5V)	---	---	---	---
IRQ[5,9,10,11]	4	ISA	I	3.3V, 5VT	10kPU (5V)	---	---	---	---

Table 3.5 CRT, LCD signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
CRTHSYNC,CRTVSYNC	2	CRT	O	3.3V	---	16mA	-16mA	---	---
FPHSYNC,FPVSYNC FPDATA[17:0] FPDOTCLK,FPDOTE, FPDISPEN, FPVEEON,FPVDDON	25	FP	O	3.3V	---	8mA	-8mA	---	---
CRTR,CRTG,CRTB	3	CRT	O	Ana -log	75PD	---	---	---	---

Table 3.6 IDE signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
IDED[15:8] IDED[6:0]	15	IDE	I/O	3.3V, 5VT	---	8mA	-8mA	---	---
IDED7	1	IDE	I/O	3.3V, 5VT	10kPD	8mA	-8mA	---	---
IDEA[2:0],IDEIOR#,IDEIOW#,IDEACK#, IDECS1FX#,IDECS3FX#, IDERESET#	9	IDE	O	3.3V	---	8mA	-8mA	---	---
IDERDY	1	IDE	I	3.3V, 5VT	1kPU (5V)	---	---	---	---
IDEINT(IRQ14)	1	IDE	I	3.3V, 5VT	10kPU (5V)	---	---	---	---
IDEDRQ	1	IDE	I	3.3V, 5VT	10kPD	---	---	---	---

Table 3.7 USB signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
USBDM1, USBDP1 USBDM0, USBDP0	4	USB	I/O	3.3V	15kPD	---	---	---	---
USBON	1	USB	O	3.3V	---	4mA	-4mA	---	---
USBCUR#	1	USB	I	3.3V, 5VT	---	---	---	10kPU (5V)	PU

Table 3.8 Serial port signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
COM1RXD,COM1CTS#, COM1DSR#,COM1CD#, COM2RXD,COM2CTS#, COM2DSR#,COM2CD#, COM1RI#,COM2RI#	10	COM1,2	I	5V	---	---	---	---(*6)	PU
COM1TXD, COM2TXD, COM2RTS#	3	COM1,2	O	5V	---	12mA	-6mA	(*6)	---
COM1RTS#, COM1DTR#, COM2DTR#	3	COM1,2	O	5V	10kPU (5V)	12mA	-6mA	(*6)	---

Table 3.9 Parallel port signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
LPTD[7:0]	8	LPT	IOD	5V	---	14mA	---	4.7kPU (5V)	---
LPTBUSY,LPTSLCT	2	LPT	I	5V	weak-PD	---	---	4.7kPU (5V)	---
LPTPE	1	LPT	I	5V	weak-PD/PU	---	---	4.7kPU (5V)	---
LPTACK#,LPTERROR#	2	LPT	I	5V	weak-PU	---	---	4.7kPU (5V)	---
LPTINIT#,LPTSTROBE#, LPTAFD#,LPTSLCTIN#	4	LPT	I/OD	5V	---	14mA	---	4.7kPU (5V)	PU

Table 3.10 KB signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
KBDATA,KBCLK,MSDATA,MSCLK	4	KB/MS	I/OD	5V	---	16mA	---	2kPU (5V)	PU

Table 3.11 AC97 signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
AC97SDIN0,AC97BITCLK	2	AC97	I	3.3V 5VT	15kPD	---	---	---	---
AC97SDOUT,AC97SYNC, PCBEEP	3	AC97	O	3.3V	---	4mA	-4mA	---	---
AC97RESET#	1	AC97	O	3.3V	---	16mA	-16mA	---	---

Table 3.12 PM signal characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
POFF	1	PM	OD	5VSTB (*5)	---	14mA	---	10kPU (5VSTB)	(*1)
PWSW#	1	PM	I	5VSTB (*5)	1MPU (5VSTB)	---	---	---	---
STANDBY#	1	PM	OD	5V	---	16mA	---	4.7kPU (3.3V)	---
POWERGOOD	1	PM	I	3.3V	---	---	---	---	(*1)
PME0#	1	PM	I	5VSTB (*5)	4.7kPU (5VSTB)	---	---	---	---
PME1#	1	PM	I	5VSTB (*5)	4.7kPU (5VSTB)	---	---	---	---
PORT[4:3]	2	GPIO	Programmable	5V	Programmable	2mA	-2mA	---	- or PU (*2)
CPUFRQ	1	MISC	I	3.3V	10kPU	---	---	---	---
ROMDIS	1	MISC	I	5V	10kPD	---	---	---	--- (*3)
RESERVE	14	MISC	---	---	---	---	---	---	--- (*4)

Table 3.13 Power supply characteristics

Signal name 280-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
V_{CCCORE}	10	Power supply	---	5.0V ±5%	---	---	---	---	---
V_{CC3V}	10	Power supply	---	3.3V ± 0.15V	---	---	---	---	---
V_{CC5V}	2	Power supply	---	5.0V ±5%	---	---	---	---	---
V_{CCSTB}	1	Power supply	---	5.0V ±5%	---	---	---	---	---
V_{CCBAK}	1	Power supply	---	2.7~ 3.6V	---	---	---	---	---

♦ 20-pin connector

Table 3.14 FDD signal characteristics

Signal name 20-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
INDEX#,TRK0#,RDATA#, WP#,DSKCHG#	5	FDD	I	5V	1kPU	---	---	---	---
DENSEL,WDATA#, WGATE#,DIR#, STEP#,HDSEL#,DR0#, MTR0#	8	FDD	O	5V	---	40mA	-4mA	---	---

Table 3.15 ISA interrupt signal characteristics

Signal name 20-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
IRQ[3,4,7,15]	4	ISA	I	3.3V, 5VT	10kPU	---	---	---	---

Signal name 20-pin connector	No. of pins	Block	I/O	Vol-tage	pull-up/ down	I_{OL}	I_{OH}	Reference PU/PD	When not used PU/PD
GND	3	Power supply	---	0V	---	---	---	---	---

20 total

*1: Circuits corresponding these signals are essential and therefore cannot be unused.
*2: If the ports corresponding to these signals in SCE8720C are set to output, pull-up resistance is not necessary. If the ports are set to input, pull-up resistance is necessary.
*3: When set to NC, the ROM in the card (SCE8720C) is selected.
*4: Keep all the RESERVED pins unconnected.
*5: Signals of POFF, PWSW#, PME0# (Wake On LAN), PME1# (Wake On Ring) operates with V_{CCSTB} controlling ON/OFF of the power supply. It is recommended that signal inputs of PWSW#, PME0# and PME1# are set to low or high impedance for compatibility with other cards (so that other cards can also use the same main circuit).
*6: For RS232C driver receiver on the evaluation board to be connected to the COM1 and COM2 interfaces, use one that operates at 5V, or that operates at 3.3V and is 5V-tolerant.

3.3 Descriptions on signal functions

3.3.1 PCI bus

PCI bus of SCE8720C complies with the PCI2.1..

Signal name (57 pins in total)	I/O	Function description
AD[31:0]	I/O	Address and data bus signals. Transfers addresses and data by time division.
CBE[3:0]#	I/O	Bus command and byte enable. Transfers by time division.
PAR	I/O	parity data of 36-bit of AD[31:0] and CBE[3:0]#.
FRAME#	S/T/S	Signal indicating the cycle frame.
IRDY#	S/T/S	Ready signal of the initiator.
TRDY#	S/T/S	Ready signal of the target.
STOP#	S/T/S	Signal from target requesting transaction canceleration.
DEVSEL#	S/T/S	Signal from the PCI slave indicating that it is selected.
LOCK#	S/T/S	Signal used when exclusively accessing the target.
SERR#	I/OD	Signal indicating that a fatal error has occurred.
PERR#	S/T/S	Parity error signal.
RST#	O	PCI reset signal.
REQ[1:0]#	I	Bus request signal.
GNT[1:0]#	O	Permission signal to use bus.
PCLK[2:0]	O	PCI clock
INT[A,B,C,D]#	I	PCI interrupt signal.

3.3.2 LIMITED ISA bus

SCE8720C's LIMITED ISA bus is different from standard ISA and its capability is limited. For details, refer to section 4.10.

For interrupt signals, IRQ5, 9, 10, 11 and 14(IDEINT) for the 280-pin connector, and IRQ3, 4, 7 and 15 for the 20-pin connector are assigned.

280-pin connector		
Signal name (35 pins in total)	I/O	Function description
SD/SA[15:0]	I/O	Address/data bus. Address and data are multiplexed. Address can be latched by SALATCH signal.
SA[19:16]	O	Standard ISA signal. The upper 4 bits of the 20-bit address. The lower 16 bits latch and generate SD/SA[15:0].
SALATCH	O	Signal to latch address from SD/SA[15:0].
AEN	O	Address enable. Signal which indicates that the current cycle is DMA or refresh cycle.
SBHE#	O	System byte enable Active low Signal which indicates that SD[15:8] is enabled.
ROMCS#	O	Signal which becomes active at ROM access. Active low
MEMR#	O	Memory read Active low Signals which request the memory device on the ISA bus to output data to SD[15:8] or SD[7:0]. This gets active when the memory address area on the ISA bus, 000000H to FFFFFFH (all of the 16-MB area) is accessed. This command applies only if ROMCS#=H when connecting to the memory device on the ISA bus.
MEMW#	O	Memory write Active low Signals which request the memory device on the ISA bus to accept data from SD[15:8] or SD[7:0]. This gets active when the memory address area on the ISA bus, 000000H to FFFFFFH (all of the 16-MB area) is accessed. This command applies only if ROMCS#=H when connecting to the memory device on the ISA bus.

Signal name (35 pins in total)	I/O	Function description
IOR#	O	I/O read Active low Signal which requests the I/O device on the ISA bus to output data to SD[15:8] or SD[7:0].
IOW#	O	I/O write Active low Signal which requests the I/O device on the ISA bus to accept data from SD[15:8] or SD[7:0].
MEMCS16#	I	Memory chip select 16 Active low Signal which lets the memory device on the ISA bus indicate the SCE8720C that 16-bit transfer is possible by the current memory cycle.
IOCS16#	I	I/O chip select 16 Active low Signal which lets the I/O device on the ISA bus indicate the SCE8720C that 16-bit transfer is possible by the current I/O cycle.
IOCHRDY	I	I/O channel ready Active high Signal which terminates the ISA bus cycle. When the memory or the I/O device on the ISA bus wants to extend the bus cycle, it can extend the cycle by setting this signal to low immediately after detecting an effective address and command. SCE8720C continues the bus cycle until this signal becomes high.
IRQ[5,9,10,11]	I or O	Interrupt request Active high Signals which request SCE8720C for interruption. When being used by the serial interface inside SCE8720C, IRQ11 and 10 become outputs. When being not used, they become inputs and can be used on the ISA bus. When being used by the parallel interface inside SCE8720C, IRQ5 becomes output. When being not used, they become inputs and can be used on the ISA bus.

20-pin connector		
Signal name (4 pins in total)	I/O	Function description
IRQ[3,4,7,15]	I or O	Interrupt request Active high Signals which request SCE8720C for interruption. When being used by the serial interface inside SCE8720C, IRQ4 and 3 become outputs. When being not used, they become inputs and can be used on the ISA bus. When being used by the parallel interface inside SCE8720C, IRQ7 becomes output. When being not used, they become inputs and can be used on the ISA bus.

3.3.3 LCD

With SCE8720C, only TFT panel can be used as LCD panel. STN panel cannot be used. LCD data is 18-bit (FPDATA17~0).

Signal name (25 pins in total)	I/O	Function description
FPHSYNC, FPVSYNC	O	Horizontal and vertical synchronous signals for flat panel (TFT).
FPDATA[17:0]	O	Dot data for flat panel (TFT). 6 bits for R, G and B each.
FPDISPEN	O	Display enable
FPDOTCLK	O	Dot clock
FPDOTE	O	Extended signal for flat panel. Even clock for LVDS is output.
FPVEEON	O	Enable signal for back light power supply.
FPVDDON	O	Enable signal for V_{DD} power supply (logic system).

3.3.4 CRT

Signal name (6 pins in total)	I/O	Function description
CRTR,CRTG,CRTB	O	R, G and B signals for CRT.
CRTHSYNC, CRTVSYNC	O	Horizontal and vertical synchronous signals for CRT.

3.3.5 Hard disk (IDE)

Signal name (28 pins in total)	I/O	Function description
IDED[15:0]	I/O	IDE data bus (*)
IDEA[2:0]	O	IDE address bus
IDEIOR#,IDEIOW#	O	IO read or write signal for IDE.
IDECS1FX#,IDECS3FX#	O	Chip select signal for IDE.
IDERDY	I	IO ready signal for IDE.
IDEINT(IRQ14)	I	IDE interrupt signal.
IDEDRQ	I	DMA transfer request signal for IDE.
IDEACK#	O	DMA acknowledge signal for IDE.
IDERESET#	O	Reset signal for IDE.

*: No pull-up resistance is required for IDE[15:0].

3.3.6 USB

SCE8720C supports 2 ports of USB complying with the Open HCI.

Signal name (6 pins in total)	I/O	Function description
USB DP1, USBDM1	I/O	Plus and minus data of USB port 1.
USB DP0, USBDM0	I/O	Plus and minus data of USB port 0.
USBON	O	Power supply control signal of USB (Power-ON)
USBCUR#	I	Over-current detection signal of USB.

3.3.7 Serial interfaces

SCE8720C supports 2 ports of serial interfaces by 16550-compatible UART.

Signal name (16 pins in total)	I/O	Function description
COM1CD# COM2CD#	I	Data carrier detect Active low Signal which indicates that the modem or data terminal has detected the carrier.
COM1DTR# COM2DTR#	O	Data terminal ready Active low Signal which indicates that SCE8720 is ready for data transmission with respect to the modem or data terminal.
COM1DSR# COM2DSR#	I	Data set ready Active low Signal which indicates that the modem or data terminal is ready for data transmission with respect to SCE8720C..
COM1RTS# COM2RTS#	O	Request to send Active low Signal which indicates that SCE8720 has transmission data ready, and indicates a request to transmit data with respect to the modem or data terminal.
COM1CTS# COM2CTS#	I	Clear to send Active low Signal which indicates that the modem or data terminal has become ready to receive for the SCE8720C's request to send.
COM1RI# COM2RI#	I	Ring indicator Active low Signal which indicates that the modem or data terminal has detected a telephone ringing signal. Alternatively, this signal can be used in SCE8720C as a wake-up signal from the suspend state.
COM1TXD COM2TXD	O	Serial data transmission Output pin for the asynchronous serial data.
COM1RXD COM2RXD	I	Serial data receive Input pin for the asynchronous serial data.

3.3.8 Parallel interfaces

SCE8720C supports 1 parallel port complying with IEE1284.

ECP, EPP and SPP modes are supported.

Signal name (17 pins in total)	I/O	Function description
LPTSTROBE#	I/OD	Line printer strobe Active low Signals used as a strobe for a peripheral on the parallel interface to read the data.
LPTAFD#	I/OD	Line printer auto feed Active low When this signal is active, a parallel printer inserts a line feed after every line.
LPTBUSY	I	Line printer busy Active high Signal which indicates that the printer is not able to accept data from SCE8720C.
LPTACK#	I	Line printer acknowledge Active low Signal which indicates that data transfer has been completed and also prepared for the next transfer.
LPTERROR#	I	Line printer error Active low Input signal which notifies SCE8720C of errors in peripheral devices.
LPTPE	I	Line printer paper end Active high Input signal which notifies SCE8720C that the printer is out of paper.
LPTINIT#	I/OD	Line printer initialize Active low Initialization signal for the printer.
LPTSLCTIN#	I/OD	Line printer select in Active low Signal used to select the peripheral device currently connected to the parallel port.
LPTSLCT	I/OD	Line printer selected Active high Status signal sent to SCE8720C by a peripheral device in order to confirm that SCE8720C has selected the device.
LPTD[7:0]	IOD	Line printer data bus A data bus between SCE8720C and the printer.

Parallel ports support SPP, ECP and EPP modes. In each mode, signal definition varies as follows. The pin Nos. are the ones on the D-TYPE connector.

Pin No.	Signal name	SPP	ECP	EPP
1	LPTSTROBE#	LPTSTROBE#	LPTSTROBE#	WRITE#
2-9	LPTD[7:0]	LPTD[7:0]	LPTD[7:0]	LPTD[7:0]
10	LPTACK#	LPTACK#	LPTACK#	LPTACK#
11	LPTBUSY	LPTBUSY	LPTBUSY	WAIT#
12	LPTPE	LPTPE	LPTPE	LPTPE
13	LPTSLCT	LPTSLCT	LPTSLCT	LPTSLCT
14	LPTAFD#	LPTAFD#	LPTAFD#	DSTRB#
15	LPTERROR#	LPTERROR#	LPTERROR#	LPTERROR#
16	LPTINIT#	LPTINIT#	LPTINIT#	LPTINIT#
17	LPTSLCTIN#	LPTSLCTIN#	LPTSLCTIN#	ASTRB#

3.3.9 Keyboard/mouse

Signal name (4 pins in total)	IO	Function description
KBCLK	IOD	Keyboard clock. Clock signal for a PS/2-style keyboard interface.
KBDATA	IOD	Keyboard data. Data signal for a PS/2-style keyboard interface.
MSCLK	IOD	Mouse clock. Clock signal for a PS/2-style mouse interface.
MSDATA	IOD	Mouse data. Data signal for a PS/2-style mouse interface.

3.3.10 AC97 interfaces

SCE8720C provides audio CODEC interface complying AC97 Version 2.0.

By adding CODEC and using the dedicated driver, high-quality audio is easily achieved.

There's only 1 channel for AC97 serial data.

Signal name (6 pins in total)	I/O	Function description
AC97SDIN0	I	Audio serial data input (from CODEC)
AC97SDOUT	O	Audio serial data output (to CODEC)
AC97SYNC	O	Serial bus synchronous signal
AC97RESET#	O	Reset signal for AC97.
AC97BITCLK	I	Audio bit clock input
PCBEEP	O	Legacy PC/AT speaker output

3.3.11 Power management

SCE8720C provides the following signals in order to achieve power supply control complying ACPI.
Other than these signals, SCE8720C also provides signals to use BIOS ROM (ROMDIS).

Signal name (22 pins in total)	I/O	Function description
POFF	OD	Output signal which controls ON/OFF of the power supply. Power OFF at HIGH, and ON at LOW.
PWSW#	I	Input signal of the power ON/OFF switch.
STANDBY#	OD	Output signal which represents standby status. Standby at LOW.
POWERGOOD	I	Input power good signal which indicates that the power is properly supplied. When this signal is LOW, the card is initialized.
PME1#	I	Wake on RING input
PME0#	I	Power management input signal usually assigned to Wake on LAN signal.
PORT4	programmable	General-purpose input/output signal. (GPIO13 of PC97317)
PORT3	programmable	General-purpose input/output signal. (GPIO12 of PC97317)
CPUFRQ	I	Input signal. Set it to NC with SCE8720Cxx.
ROMDIS	I	Input signal. Disable signal of ROM inside SCE8720C. CPU accesses the external ROM when the signal is HIGH, and internal ROM when LOW.
RESERVED	---	RESERVED pin. Set it to NC.

3.3.12 Power supply

Signal name (57 pins in total)	Function description
GND	Ground.
V_{CCCORE}	Power to the regulator for CPU core power supply. Power of 5V should be supplied. This is not connected to V_{CC5V} inside the card.
V_{CC3V}	3.3V power supply.
V_{CC5V}	5V power supply, for ISA bus.
V_{CCSTB}	5V standby power supply signal supplied to the power supply control circuit inside the card. Power of 5V is always supplied when AC line of the power supply is connected.
V_{CCBAK}	power supply for RTC backup.

3.3.13 FDD

SCE8720C supports 1 unit of 3.5” floppy disk drive. 2 modes, 720KB and 1.44MB, are available.

Signal name	I/O	Function description
DSKCHG#	I	Disk Change
WP#	I	Write Protect
INDEX#	I	Index
TRK0#	I	Track 0
RDATA#	I	Read Data
DENSEL	O	Density Select
WGATE#	O	Write Gate
HDSEL#	O	Head Select
STEP#	O	Step
DIR#	O	Direction
WDATA#	O	Write Data
DR0#	O	Drive Select 0
MTR0#	O	Motor Select 0

4. Detailed description of interfaces

4.1 CRT, LCD

With SCE8720C, display is controlled by Geode CPU and companion chip (Geode CS5530). It supports CRT and TFT panel display, but not STN panel.

The display controller supports standard VGA and high resolution display.

For driver, use Windows 95-98 driver or Windows NT 4.0 driver by National Semiconductor Corporation.

Display resolution and No. of colors of CRT and TFT are as follows. (Adjustment of display frequency and position to suit the panel must be done from the utility software.):

Table 3.16 TFT display mode

Resolution	No. of colors	Panel type
640×480	8BPP 256 colors from palette.	9 bits
		12 bits
		18 bits
	16BPP 64K colors R = 5 bits, G = 6 bits and B = 5 bits	9 bits
		12 bits
		18 bits
800×600	8BPP 256 colors from palette.	9 bits
		12 bits
		18 bits
	16BPP 64K colors R = 5 bits, G = 6 bits and B = 5 bits	9 bits
		12 bits
		18 bits
1024×768	8BPP 256 colors from palette.	9 bits
		12 bits
		18 bits
	16BPP 64K colors R = 5 bits, G = 6 bits and B = 5 bits	9 bits
		12 bits
		18 bits

In 640 × 480 and 800 × 600 modes, simultaneous display with CRT is available.

Table 3.17 CRT display mode

Resolution	No. of colors
640×480	8BPP, 256 colors from palette.
	16BPP, 64K colors R = 5 bits, G = 6 bits and B = 5 bits
800×600	8BPP, 256 colors from palette.
	16BPP, 64K colors R = 5 bits, G = 6 bits and B = 5 bits
1024×768	8BPP, 256 colors from palette.
	16BPP, 64K colors R = 5 bits, G = 6 bits and B = 5 bits
1280×1024	8BPP, 256 colors from palette.

Connection method of TFT signal and panel is shown below.
(R5: Red MSB, G5: Green MSB, B5: Blue MSB):

Table 3.18 TFT display data assignment

Signal name	18-bit TFT	12-bit TFT	9-bit TFT		
			640×480	1024×768	
FPDATA17	R5	R5	R5	R5	Even
FPDATA16	R4	R4	R4	R4	pixel
FPDATA15	R3	R3	R3	R3	
FPDATA14	R2	R2		R5	Odd
FPDATA13	R1			R4	pixel
FPDATA12	R0			R3	
FPDATA11	G5	G5	G5	G5	Even
FPDATA10	G4	G4	G4	G4	pixel
FPDATA9	G3	G3	G3	G3	
FPDATA8	G2	G2		G5	Odd
FPDATA7	G1			G4	pixel
FPDATA6	G0			G3	
FPDATA5	B5	B5	B5	B5	Even
FPDATA4	B4	B4	B4	B4	pixel
FPDATA3	B3	B3	B3	B3	
FPDATA2	B2	B2		B5	Odd
FPDATA1	B1			B4	pixel
FPDATA0	B0			B3	

4.2 Hard disk

SCE8720C only supports primary IDE. Up to 2 hard disks, master and slave, can be controlled. IDE interface complies with ANSI ATA-4 (ultra DMA/33), (Refer to ANSI ATA-4 for detailed specifications of I.F) Therefore, it can operate in PIO mode 1, 2, 3 or 4, or Ultra DMA/33. Connection method of HDD is shown below. If secondary IDE is needed, extend to the ISA bus:

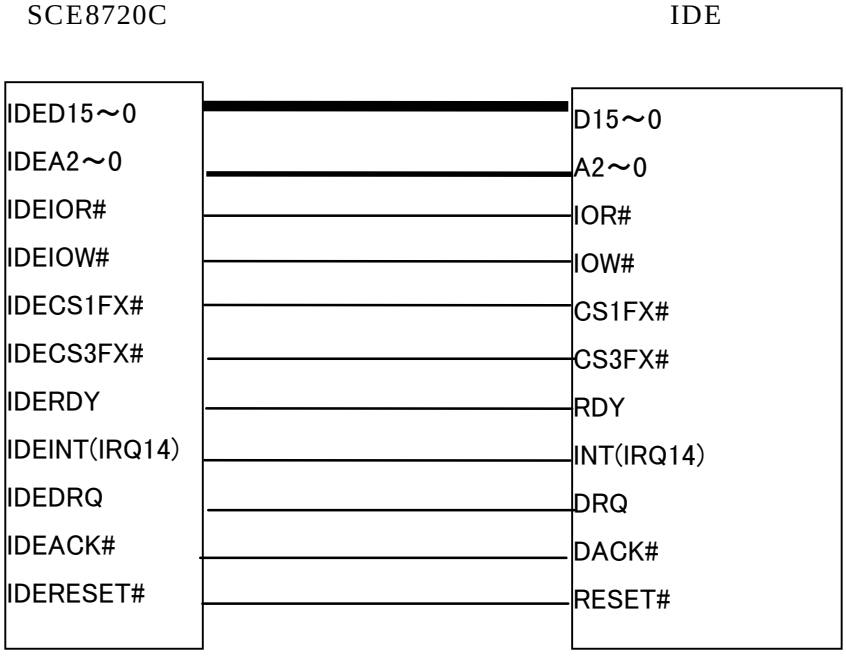


Figure 4.1 IDE interface connection

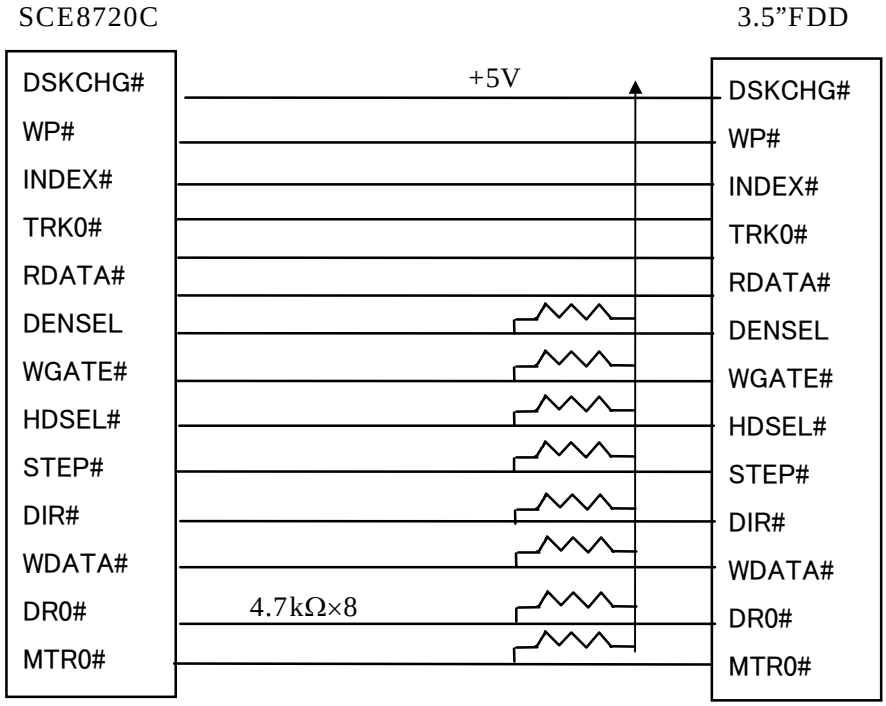
Each signal of IDE can be directly connected to IDE with no problem. However, it is sometimes better to add serial dumping resistances of 33Ω or so in order for countermeasure against noises.

Output level of each IDE signal is 3.3V, and input level is 5V-tolerant. No pull-up or pull-down is required.

4.3 FDD

1 unit of 3.5” FDD can be connected. 2 modes, 720KB and 1.44MB, are available.

Connection method of FDD is shown below.



Resistance of 4.7kΩ × 8 is not necessary when built into FDD.

Figure 4.2 FDD interface connection

4.4 Keyboard/mouse

The keyboard/mouse interfaces can be connected to IBM/PS2 type keyboard and mouse. Connection method is shown below.

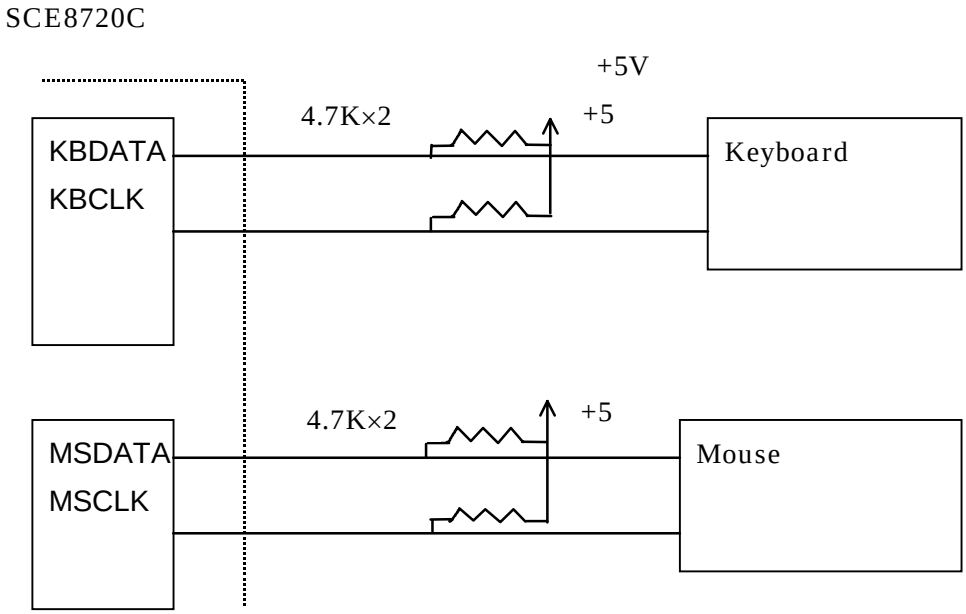


Figure 4.3 Keyboard/mouse interface connection

All the keyboard and mouse signals require pull-up resistance of 4.7kΩ or so.
Pull-up resistance of 100kΩ or so is required even when not in use.

4.5 Parallel port

SCE8720C supports 1 parallel port complying with IEE1284.
This port can be used in ECP, EPP or SPP mode.

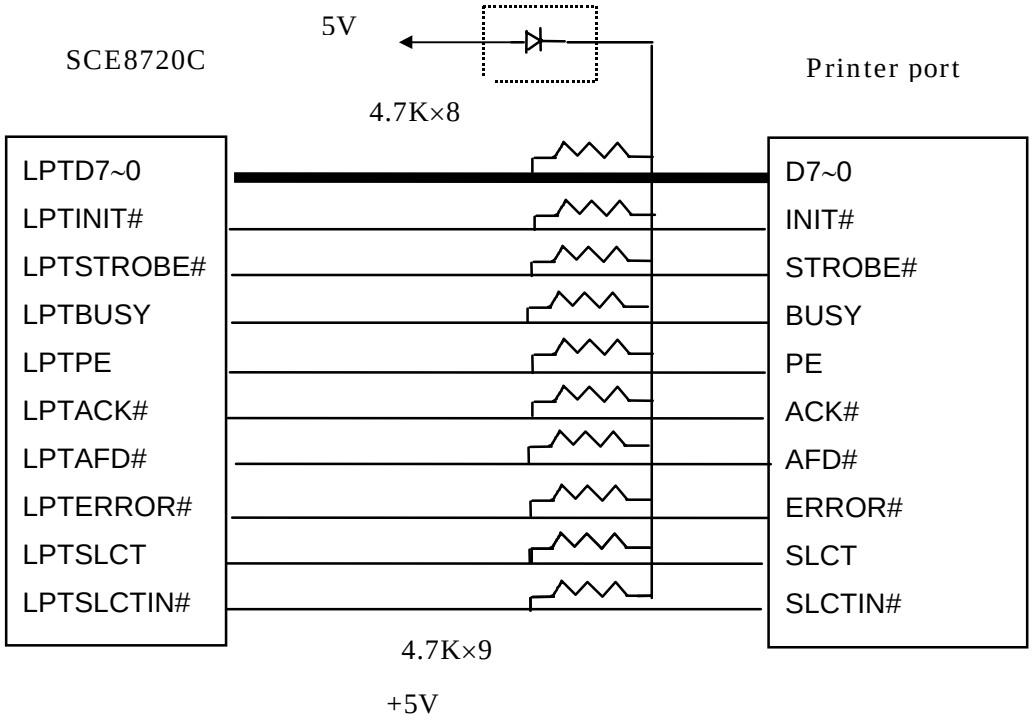


Figure 4.4 Parallel interface connection

All the parallel port signals require pull-up resistance of 4.7kΩ or so.

Even when the parallel port is not in use, the LPTD[7:0],LPTINIT#,LPTSTROBE#, PTAFD#,LPTSLCTIN# signals require pull-up resistance of 100kΩ or so.
The diode in the dotted rectangular is for preventing troubles from happening due to current flowing from the printer signal to the 5V of the system when the power of the system including SCE8720C is OFF and the power of the printer is ON. This is essential for such system which mis-operates when +5V becomes 1 to 2V. Place it as necessary.

4.6 Serial port

SCE8720C supports 2 ports of serial interfaces by 16550-compatible UART.

When sending/receiving data at a high speed, use sufficient RS232C driver.

4.7 USB

By connecting the USB signal of SCE8720C directly to the USB connector, 2-channel USB port becomes available.

When the overcurrent detector of the USB detects an overcurrent, USB port can be disabled in order to protect the circuit. In this case, even if only one port is detected as an overcurrent, both USBs are disabled. Connection example is shown below.

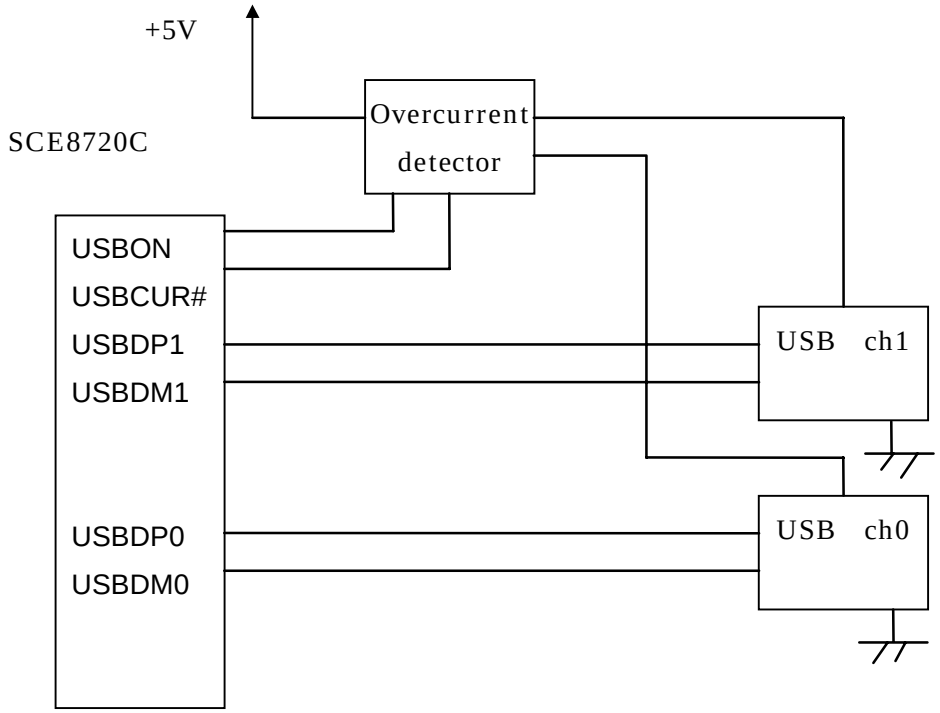


Figure 4.5 USB interface connection

4.8 Speaker

PCBEEP signal is used to drive the piezoelectric loudspeaker by logical pulse signal. Circuit example is shown below.

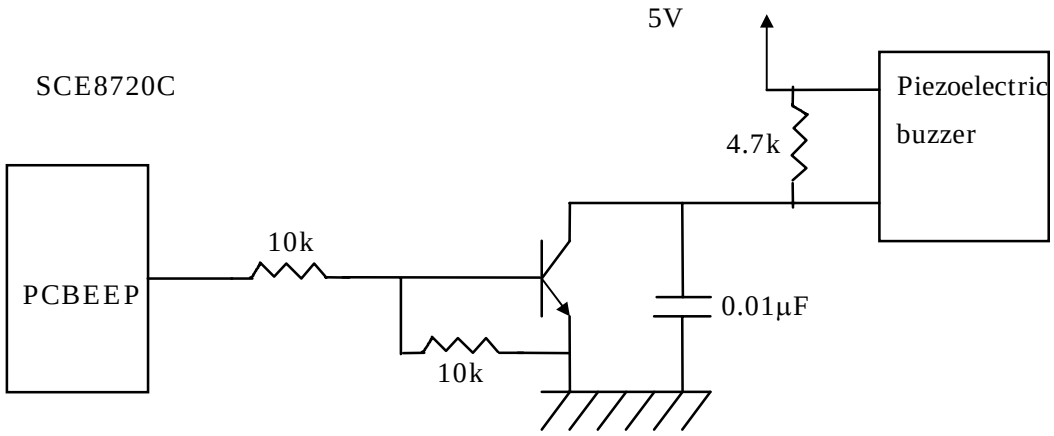


Figure 4.6 Piezoelectric buzzer connection

4.9 PCI

PCI bus of SCE8720C complies with the PCI2.1, but the power voltage is limited to 3.3V. Up to 3 PCI devices can be connected. (also limited by the number of PCICLKs.) Among these, up to 2 PCI devices can be connected as master. (limited by the numbers of REQ and GNT.)

If you wish to connect a 5V PCI device, or PCI devices of more than 3, refer to the reference circuit in Appendix A.

4.10 LIMITED ISA

SCE8720C's LIMITED ISA bus is different from standard ISA as follows.

1) No master function provided.
2) Memory area is only 1MB, from 0000h to FFFFFh.
3) No DMA function provided. (However, for FDD access, DMA is used.)
4) The lower 16-bit address (SA0-15) is multiplexed to the data bus SD/SA[15:0] to be output. Therefore, in order to obtain SA[15:0], SD/SA[15:0] must be latched by the latch signal (SALATCH).
5) The following signals are not supported.
   BALE, SCLK, OSC, REFRESH#, IOCHK#, 0WS#
   (SMEMW# can be generated from other signals.)
6) SCE8720C's ISA output is 3.3V max.
   Since the IC power supply, which drives the ISA bus, is 3.3V, SCE8720C's ISA output level is 3.3V maximum. Input signal level is 5V-tolerant.
7) IRQ5, 9, 10 and 11 for the 280-pin connector, and IRQ3, 4, 7 and 15 for the 20-pin connector are supported.

Reference 8.2 IO extension of ISA bus

4.11 RTC

MC146818A-compatible RTC function is built in the Super IO inside SCE8720C.

When V_{CCSTB} is supplied, it is supplied to the RTC power supply, and when V_{CCSTB} is OFF, the power supply is switched to the battery power supply, V_{CCBAK}. Since this switching circuit is inside SCE8720C, connect V_{CCBAK} and V_{CCSTB} directly to SCE8720.

Protection resistance applying to UL is also built-in.

5. Power management

This chapter describes SCE8720C's power-saving functions and power-related matters. The power-saving function is precisely specified in the BIOS setup menu. SCE8720C's power-saving function not only minimizes the system power consumption, but also minimizes the CPU heat-up to control and protect the temperature.

5.1 Power ON/OFF

The system can select whether or not to control the power supply by software or external control signals PM0# and PM1#.

When controlling by software or PM0# and PM1# signals, power can be turned ON by signal from LAN, RING signal or PWSW# signal, and be turned OFF from the software. For each reference circuit, refer to Appendix A.

5.2 Standby mode

In case of no input from Windows' keyboard or mouse for a certain period of time, or PWSW# signal (pulse) input within 4 seconds, the system gets into the standby mode. In standby mode, the display is turned OFF and the peripheral devices also get into the power-saving mode. (motors of HDD and FDD are turned OFF.) To return to the standard operation mode from the standby mode, the power switch input within 4 seconds or keyboard/mouse input is effective. However, whether or not the operation mode is resumed is determined by the BIOS settings.

5.3 Power supply

- V_{CC3V} (3.3V)

  Supplied to the IO power supply of the CPU chip (Geode GX-LV), companion chip (Geode CS5530) and S-DRAM.

- V_{CCCORE} (5V)

  Power supply for the DC-DC converter, which generates the CPU's core power supply. Input the same power supply as V_{CC5V}. Power consumption is highest of all.

- V_{CC5V} (5V)

  Mainly supplied to the Super IO (PC97317).

- V_{CCSTB}

  Supplied to the circuit which controls ON/OFF of the power supply. In SCE8720C, it is supplied to the power supply control circuit of the Super I/O (PC97317). When ATX power supply is used, it is always supplied from the power supply unit when the AC cord is connected.

  When V_{CCSTB}-equivalent power cannot be obtained due to the power supply unit not capable of ON/OFF control of the power supply, connect V_{CC5V} instead.

- V_{CCBAK}

  Supplied in order to maintain the RTC and C-MOS RAM when no V_{CCSTB} is supplied as the power is OFF.

5.4 Power sequence

5.4.1 Power sequence (for power supply which is turned ON/OFF from the software)

Follow the power ON/OFF sequence shown below.

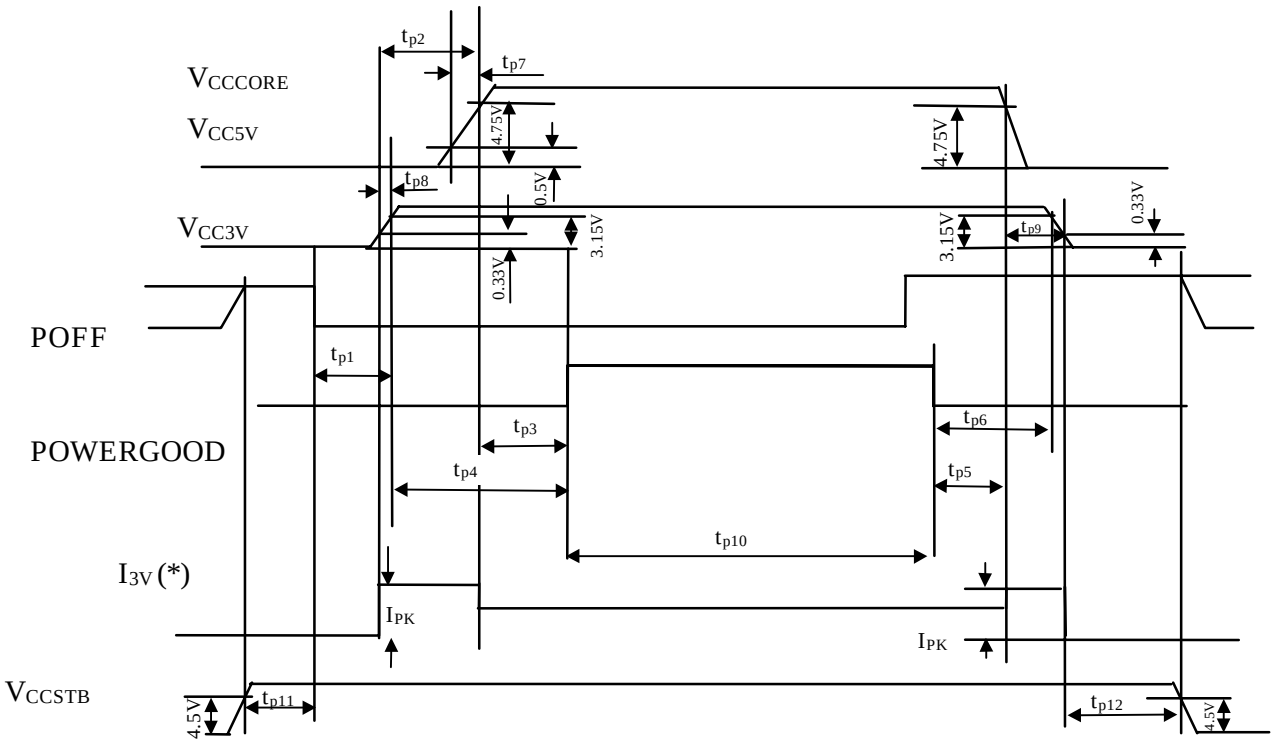


Figure 5.1 Power sequence (for power supply which is turned ON/OFF from the software)

*: I_{3V} is the current of V_{CC3V} supplied to SCE8720Cxx.

If V_{CCORE} starts up after V_{CC3V}, or if V_{CCORE} shuts down before V_{CC3V}, peak current such as I_{PK} is supplied to V_{CC3V}. (typical I_{PK}=1.8A)

As a system power supply, it must be designed so that it is not damaged if a peak current is supplied. For that, the following measures are available.

1) Suppress the peak current from the current control circuit. Voltage drop due to this measure is acceptable.
2) Increase the current capacity.

Symbol	Parameter	Min.	Max.	Unit
t_{p1}	POFF inactive to V_{CC3V}=3.15V	0	---	ms
t_{p2}	V_{CC3V}=0.33V to V_{CCCORE} & V_{CC5V} =4.75V	-100	80	ms
t_{p3}	V_{CCCORE} & V_{CC5V} =4.75V to POWERGOOD active	10	---	ms
t_{p4}	V_{CC3V}=3.15V to POWERGOOD active	10	---	ms
t_{p5}	POWERGOOD inactive to V_{CCCORE} & V_{CC5V} =4.75V	0	---	ms
t_{p6}	POWERGOOD inactive to V_{CC3V}=3.15V	0	---	ms
t_{p7}	V_{CCCORE} & V_{CC5V} rise time		20	ms
t_{p8}	V_{CC3V} rise time	---	20	ms
t_{p9}	V_{CCCORE} & V_{CC5V} =4.75V to V_{CC3V}=0.33V	-100	80	ms
t_{p10}	Width of POWERGOOD	10	---	---
t_{p11}	V_{CCSTB}=4.5V to POFF inactive	500	---	---
t_{p12}	POFF active to V_{CCSTB}=4.5V	500	---	ms

5.4.2 Power sequence (for power supply which is not turned ON/OFF from the software)

Follow the power ON/OFF sequence shown below.

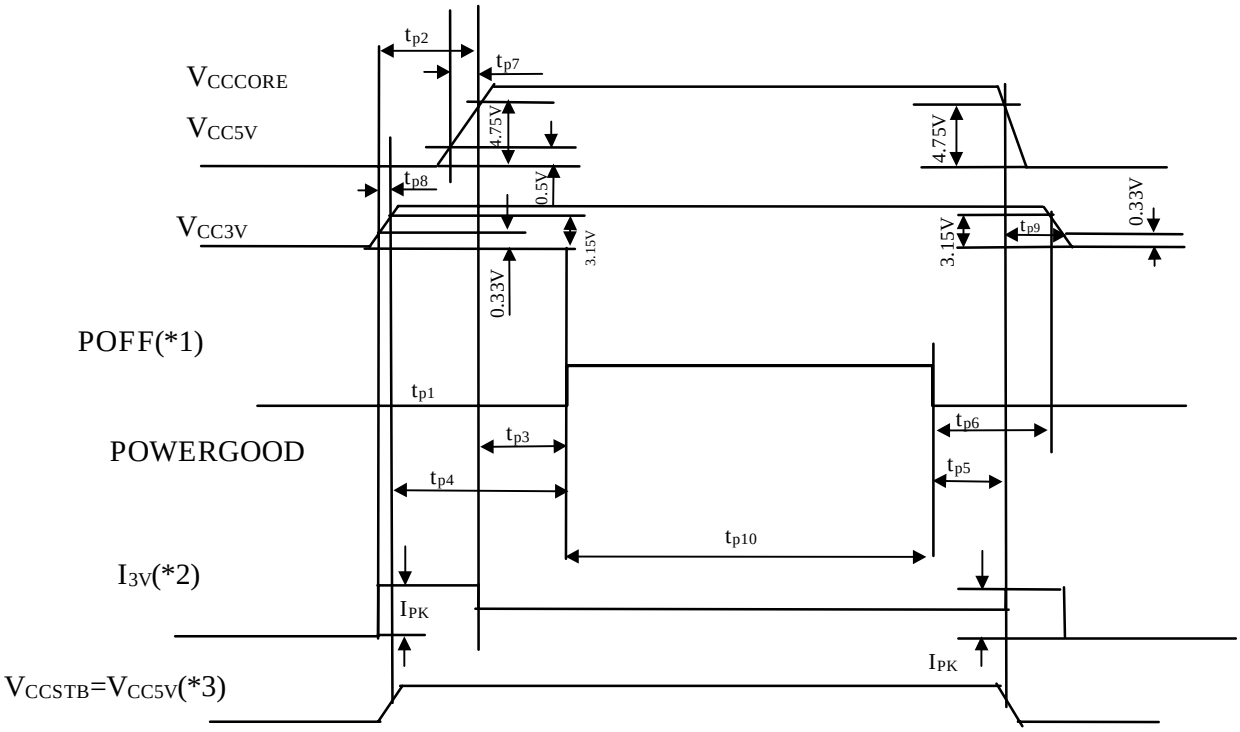


Figure 5.2 Power sequence (for power supply which is not turned ON/OFF from the software)

*1: POFF is not used. (Set it to NC.)

*2: I_{3V} is the current of V_{CC3V} supplied to SCE8720Cxx.

If V_{CCORE} starts up after V_{CC3V}, or if V_{CCORE} shuts down before V_{CC3V}, peak current such as I_{PK} is supplied to V_{CC3V}. (typical I_{PK}=1.8A)

As a system power supply, it must be designed so that it is not damaged if a peak current is supplied. For that, the following measures are available.

1) Suppress the peak current from the current control circuit. Voltage drop due to this measure is acceptable.
2) Increase the current capacity.

*3: Connect V_{CCSTB} to V_{CC5V}.

6. Electrical characteristics

6.1 Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC3V}	0	4.0	V
	V_{CC5V}	-0.5	6.5	V
	V_{CCSTB}	-0.5	6.5	V
	V_{CCBAK}	-0.5	6.5	V
Votage on pin	CPUFRQ	-0.5	V_{CC3V}+0.5	V
	PCLK[2:0]	-0.5	V_{CC3V}+0.5	V
	Other pins	-0.5	(*1)	V

*1: Lower voltage between 5.5V and V_{CC5V} + 0.5V.

6.2 Recommended operating condition

Symbol	Min.	Max.	Unit	Current Limit (*2)
V_{CCCORE}	4.75	5.25	V	2.5A
V_{CC5V}	4.75	5.25	V	---
V_{CC3V}	3.15	3.45	V	3A
V_{CCSTB}	4.5	5.5	V	---
V_{CCBAK}	2.7	3.6	V	---

*2: Even if any part defect occurred in SCE8720Cxx, do not supply current over the current limit in order to suppress abnormal heating of SCE8720Cxx.

6.3 DC characteristics (under recommended operating condition)

6.3.1 PCI bus

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	$0.3*V_{CC3V}$	V	---
V_{IH}	Input high voltage	---	2.0	$V_{CC3V}+0.5$	V	---
V_{OL}	Output low voltage	I_{OL}=5mA	---	0.4	V	---
V_{OH}	Output high voltage	I_{OH}=-2mA	2.4	---	V	---
I_{LL1}	Input leakage current	V_{IN}=0.35V	-400	---	μA	(*1)
I_{LL2}	Input leakage current	V_{IN}=0.35V	-20	+20	μA	(*2)
I_{LL3}	Input leakage current	V_{IH}=2.4V	-20	+20	μA	---

*1: Input leak current of FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR# and REQ[2:0]# signals.

*2: Input leak current of signals other than FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR# and REQ[2:0]# signals.

6.3.2 LIMITED ISA bus

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	---
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	---
V_{OL1}	Output low voltage	I_{OL}=8mA	---	0.4	V	(*1)
V_{OL2}	Output low voltage	I_{OL}=4mA	---	0.4	V	(*2)
V_{OH1}	Output high voltage	I_{OL}=8mA	2.4	---	V	(*1)
V_{OH2}	Output high voltage	I_{OL}=4mA	2.4	---	V	(*2)
I_{LL1}	Input leakage current	V_{IN}=0.35V	-400	---	μA	(*3)
I_{LL2}	Input leakage current	V_{IN}=0.35V	-1.1	---	mA	(*4)
I_{LL3}	Input leakage current	V_{IN}=0.35V	-5.5	---	mA	(*5)
I_{LL4}	Input leakage current	V_{IN}=0.35V	-550	---	μA	(*6)
I_{LL5}	Input leakage current	V_{IN}=0.35V	-20	---	μA	(*6)
I_{LL6}	Input leakage current	V_{IN}=V_{CC5V}	---	+20	μA	---

*1: ISA output signals other than SALATCH and ROMCS# signals (including bi-directional bus)

*2: SALATCH and ROMCS# signals.

*3: SBHE#, SA[19:16] and SD/SA[15:0] signals. (20kΩ pull-up)

*4: IOR#, IOW#, MEMR# and MEMW# signals. (4.7kΩ pull-up)

*5: MEMCS16#, IOCS16# and IOCHRDY (1kΩ pull-up)

*6: IRQ[3,4,5,7,9,10,11 and 15] (10kΩ pull-up)

*7: SALATCH, AEN and ROMCS#

6.3.3 LCD

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{OL}	Output low voltage	I_{OL}=8mA	---	0.4	V	---
V_{OH}	Output high voltage	I_{OH}=-8mA	---	0.4	V	---

6.3.4 CRT

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{OL1}	Output low voltage	I_{OL}=16mA	---	0.4	V	(*1)
V_{OH1}	Output high voltage	I_{OH}=-16mA	2.4	---	V	(*1)
V_{OL2}	Output low voltage	---	---	---	V	(*2)
V_{OH2}	Output high voltage	---	---	---	V	(*2)

*1: CRTHSYNC,CRTVSYNC

*2: CRTR,CRTG,CRTB

6.3.5 FDD

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL}	Output low voltage	I_{OL}=40mA	---	0.4	V	(*2)
V_{OH}	Output low voltage	I_{OH}=-4mA	2.4	---	V	(*2)
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	+10	μA	---
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA	---

*1: INDEX#,TRK0#,RDATA#,WP#,DSKCHG#

*2: DENSEL,WDATA#,WGATE#,DIR#, STEP#,HDSEL#,DR0#,MTR0#

6.3.6 IDE

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL}	Output low voltage	I_{OL}=8mA	---	0.4	V	(*2)
V_{OH}	Output high voltage	I_{OH}=-8mA	2.4	---	V	(*2)
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	5.5	mA	(*3)
I_{LL2}	Input leakage current	$V_{IN}=V_{CC5V}$	---	5.5	mA	(*4)
I_{LL3}	Input leakage current	$V_{IN}=V_{SS}$	-5.5	---	mA	(*5)
I_{LL4}	Input leakage current	$V_{IN}=V_{SS}$	-550	---	μA	(*6)
I_{LL5}	Input leakage current	$V_{IN}=V_{CC5V}$	---	+10	μA	(*7)
I_{IL6}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA	(*7)

*1: IDED[15:0], IDERDY, IDEINT(IRQ14), IDEDRQ

*2: IDED[15:0], IDEA[2:0], IDEIOR#, IDEIOW#, IDEACK#, IDECS1FX#, IDECS3FX#, IDERESET#

*3: IDED7

*4: IDEDRQ

*5: IDERDY

*6: IDEINT(IRQ14)

*7: IDED[15:0](other than IDED7)

6.3.7 Serial port

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL}	Output low voltage	I_{OL}=12mA	---	0.4	V	(*2)
V_{OH}	Output low voltage	I_{OH}=-6mA	2.4	---	V	(*2)
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	+10	μA	---
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA	---

*1: COM1RXD,COM1CTS#,COM1DSR#,COM1CD#, COM2RXD,COM2CTS#,
COM2DSR#,COM2CD#, COM1RI#,COM2RI#

*2: COM1TXD,COM1RTS#,COM1DTR#, COM2TXD,COM2RTS#,COM2DTR#

6.3.8 Parallel port

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL}	Output low voltage	I_{OL}=14mA	---	0.4	V	(*2)
V_{OH}	Output high voltage	I_{OH}=-14mA	2.4	---	V	(*2)
I_{LL1}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA	(*3)
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-120	---	μA	(*4)
I_{LL3}	Input leakage current	$V_{IN}=V_{CC5V}$	---	120	μA	(*3)
I_{LL4}	Input leakage current	$V_{IN}=V_{CC5V}$	---	10	μA	(*4)

*1: All the parallel port signals.
(LPTD[7:0], LPTINIT#,LPTSTROBE#, LPTAFD#,LPTSLCTIN#
LPTBUSY,LPTSLCT, LPTPE, LPTACK#,LPTERROR#)

*2: LPTD[7:0],LPTINIT#,LPTSTROBE#, LPTAFD#,LPTSLCTIN#

*3: LPTBUSY, LPTSLCT, LPTPE (*3 or *4 depending on the software settings)

*4: LPTACK#, LPTERROR#, LPTPE (*3 or *4 depending on the software settings)

6.3.9 Keyboard/mouse

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL}	Output low voltage	I_{OL}=16mA	---	0.4	V	(*1)

*1: KBDATA, KBCLK, MSDATA and MSCLK are all open-collector output.

6.3.10 USB

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V	(*1)
V_{OL1}	Output low voltage	I_{OL}=4mA	---	0.4	V	(*2)
V_{OL2}	Output low voltage	---	---	0.3	V	(*3)
V_{OH1}	Output high voltage	I_{OH}=-4mA	2.4	---	V	(*2)
V_{OH2}	Output high voltage	---	2.8	3.6	V	(*4)

*1: USBCUR#

*2: USBON

*3 :USBDM1, USBDP1, USBDM0, USBDP0

(1.5kΩ of pull-up resistance is added outside SCE8720C.)

*4: USBDM1, USBDP1, USBDM0, USBDP0

(15kΩ of pull-up resistance is added outside SCE8720C.)

6.3.11 Power management signal

PME0# signal (For compatibility with other cards, input should be set to low or high impedance.)

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	---
V_{IH}	Input high voltage	---	2	---	V	---
I_{LL1}	Input leakage current	V_{IN}=V_{CC5V}	---	+10	μA	---
I_{LL2}	Input leakage current	V_{IN}=V_{SS}	-1.2	---	mA	---

PME1# signal (For compatibility with other cards, input should be set to low or high impedance.)

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	---
V_{IH}	Input high voltage	---	2	V_{CCSTB}	V	---
I_{LL1}	Input leakage current	V_{IN}=V_{CC5V}	---	+10	μA	---
I_{LL2}	Input leakage current	V_{IN}=V_{SS}	-1.2	---	mA	---

POWERGOOD# signal (this signal is not 5V-tolerant.)

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	---
V_{IH}	Input high voltage	---	2	1.1* V_{CC3V}	V	---
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	-10	+10	μA	---
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-10	+10	μA	---

PWSW1# signal (For compatibility with other cards, input should be set to low or high impedance.)

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.5	0.8	V	---
V_{IH}	Input high voltage	---	2 2	---	V	---
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$		+10	μA	---
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-1.2	---	mA	---

POFF signal (open-collector)

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{OL1}	Output low voltage	I_{OL}=14mA	---	0.4	V	---

STANDBY# signal

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{OL1}	Output low voltage	I_{OL}=16mA	---	0.4	V	---

6.3.12 AC97

Symbol	Parameter	Condition	Min.	Max.	Unit	Note
V_{IL}	Input low voltage	---	-0.3	0.8	V	(*1)
V_{IH}	Input high voltage	---	2.0	5.5	V	(*1)
V_{OL1}	Output low voltage	I_{OL}=4mA	---	0.4	V	(*2)
V_{OL2}	Output low voltage	I_{OL}=16mA	---	0.4	V	(*3)
V_{OH1}	Output high voltage	I_{OH}=-4mA	2.4	---	V	(*2)
V_{OH2}	Output high voltage	I_{OL}=-16mA	2.4	---	V	(*3)

*1: AC97SDIN0,AC97BITCLK

*2: AC97SDOUT,AC97SYNC,PCBEEP

*3: AC97RESET#

6.3.13 Other signals

PORT3 signal

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input low voltage	---	-0.5	0.8	V
V_{IH}	Input high voltage	---	2.0	V_{CC5V}	V
V_{OL}	Output low voltage	I_{OL}=2mA	---	0.4	V
V_{OH}	Output high voltage	I_{OH}=-2mA	2.4	---	V
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	+10	μA
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-100	---	μA

PORT4 signal

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input low voltage	---	-0.5	0.8	V
V_{IL}	Input high voltage	---	2.0	V_{CC5V}	V
V_{OL}	Output low voltage	I_{OL}=14mA	---	0.4	V
V_{OH}	Output high voltage	I_{OH}=-2mA	2.4	---	V
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	+10	μA
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-550	---	μA

CPUFRQ signal (this signal is not 5V-tolerant.)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input low voltage	---	---	$0.3*V_{CC3V}$	V
V_{IH}	Input high voltage	---	$0.7*V_{CC3V}$	---	V
I_{LL1}	Input leakage current	$V_{IN}=V_{CC3V}$	---	3.6	mA
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA

ROMDIS signal

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input low voltage	---	---	$0.3*V_{CC5V}$	V
V_{IH}	Input high voltage	---	$0.7*V_{CC5V}$	---	V
I_{LL1}	Input leakage current	$V_{IN}=V_{CC5V}$	---	5.5	mA
I_{LL2}	Input leakage current	$V_{IN}=V_{SS}$	-10	---	μA

6.4 Current consumption

6.4.1 Maximum current value

Measurement method: Startup Windows 98, and measure each maximum current in the process of operating the screen saver (pipe). Each maximum current cannot be measured simultaneously, these values must be taken into account when designing the power supply.

(Memory side: 64MB Display 1280 × 1024, 256-color CRT)

Item	Symbol	Typ.	Max.	Unit	Note
Current	V_{CCCORE} (*1)	500	750	mA	V_{CCCORE}=5V
	V_{CC5V} (*1)	20	30	mA	V_{CC5V}=5V
	V_{CC3V} (*2)	640	960	mA	V_{CC3V}=3.3V
	V_{CCSTB}	1	1.5	mA	V_{CCSTB}=5V
	V_{CCBAK}	1.2	---	μA	V_{CCBAK}=3V
Power(total)	---	4717	7075.5	mW	---

*1: At Windows 98 startup. *2: Screen saver (pipe)

6.4.2 Typical current value 1

Measurement method: Startup Windows 98 and measure while nothing is being executed by the application.APM(Advanced Power Management)=OFF

(Memory side: 64MB Display 1280 × 1024, 256-color CRT)

Item	Symbol	Typ.	Unit	Note
Current	V_{CCCORE}	408	Ma	V_{CCCORE}=5V
	V_{CC5V}	17.1	mA	V_{CC5V}=5V
	V_{CC3V}	621	mA	V_{CC3V}=3.3V
	V_{CCSTB}	0.35	mA	V_{CCSTB}=5V
	V_{CCBAK}	0	μA	V_{CCBAK}=3V
Power(total)	---	4176.6	mW	---

6.4.3 Typical current value 2

Measurement method: Startup Windows 98 and measure while nothing is being executed by the application.

APM(Advanced Power Management)=ON Therefore, Windows 98's power management is activated.

(Memory side: 64MB Display 1280 × 1024, 256-color CRT)

Item	Symbol	Typ.	Unit	Note
Current	V_{CCCORE}	110	mA	V_{CCCORE}=5V
	V_{CC5V}	17.1	mA	V_{CC5V}=5V
	V_{CC3V}	530	mA	V_{CC3V}=3.3V
	V_{CCSTB}	0.35	mA	V_{CCSTB}=5V
	V_{CCBAK}	0	μA	V_{CCBAK}=3V
Power(total)	---	2386.3	Mw	---

6.4.4 Standby current

Measurement method: Measure in the standby mode.

(Memory size: 64MB)

Item	Voltage	Typ.	Unit	Note
Current	V_{CCCORE}	17.2	mA	V_{CCCORE}=5V
	V_{CC5V}	11.5	mA	V_{CC5V}=5V
	V_{CC3V}	230	mA	V_{CC3V}=3.3V
	V_{CCSTB}	0.35	mA	V_{CCSTB}=5V
	V_{CCBAK}	0	μA	V_{CCBAK}=3V
Power(total)	---	904.25	mW	---

7. AC characteristics

7.1 PCI timing

Since the PCI timing is based on the PCI BUS Specification rev2.1, refer to the PCI BUS Specification 2.1 for details.

7.2 USB timing

Since the PCI timing is based on the PCI BUS Specification rev2.1, refer to the PCI BUS Specification 2.1 for details.

7.3 LIMITED ISA timing

ISA signals comply with the ISA specifications.

7.3.1 Memory, I/O read cycle timing

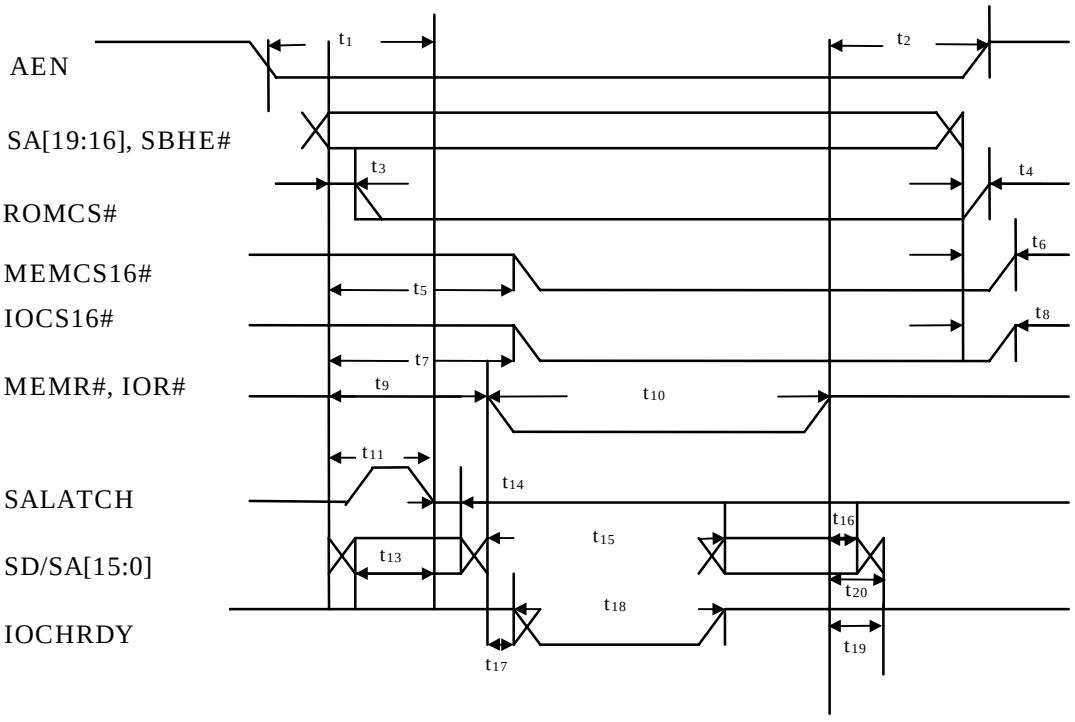


Figure 7.1 Memory, I/O read cycle timing

Symbol	Parameter	Min.	Max.	Unit	Note
t_1	AEN active to falling edge of SALATCH	56	---	ns	---
t_2	AEN inactive from command	30	---	ns	---
t_3	ROMCS# active from SA[19:16]	---	24	ns	---
t_4	ROMCS# inactive from SA[19:16]	---	10	ns	---
t_5	MEMCS16# active from SA[19:16]	---	72	---	---
t_6	MEMCS16# inactive from SA[19:16]	---	58	---	---
t_7	IOCS16# active from SA[19:16]	---	95	---	---
t_8	IOCS16# inactive from SA[19:16]	---	69	---	---
t_9	Read command active from SA[19:16]	162	---	ns	8 bits
		102	---	ns	16 bits
t_{10}	Memory read command pulse width	509	---	ns	8 bits
		209	---	ns	16 bits
t_{10}	IO read command pulse width	509	---	ns	8 bits
		147	---	ns	16 bits
t_{11}	SA[19:16] to falling edge of SALATCH	28	---	ns	---
t_{13}	SA(onSD/SA) active to SALATCH inactive	13	---	ns	---
t_{14}	SA(onSD/SA) inactive to SALATCH inactive	5	---	ns	---
t_{15}	Valid read DATA from M-read command	---	460	ns	8 bits
		---	161	ns	16 bits
t_{15}	Valid read DATA from I-read command	---	462	ns	8 bits
		---	103	ns	16 bits
t_{16}	Read data valid hold to read Command inactive	0	---	ns	---
t_{17}	IOCHRDY inactive from active command	---	344	ns	8 bits
		---	54	ns	16 bits
t_{18}	IOCHRDY inactive pulse width	0.120	15.6	μS	---
t_{19}	IOCHRDY active hold from inactive command	0	---	ns	---
t_{20}	Read command inactive to SD tristate	---	30	ns	---

7.3.2 Memory, I/O write cycle timing

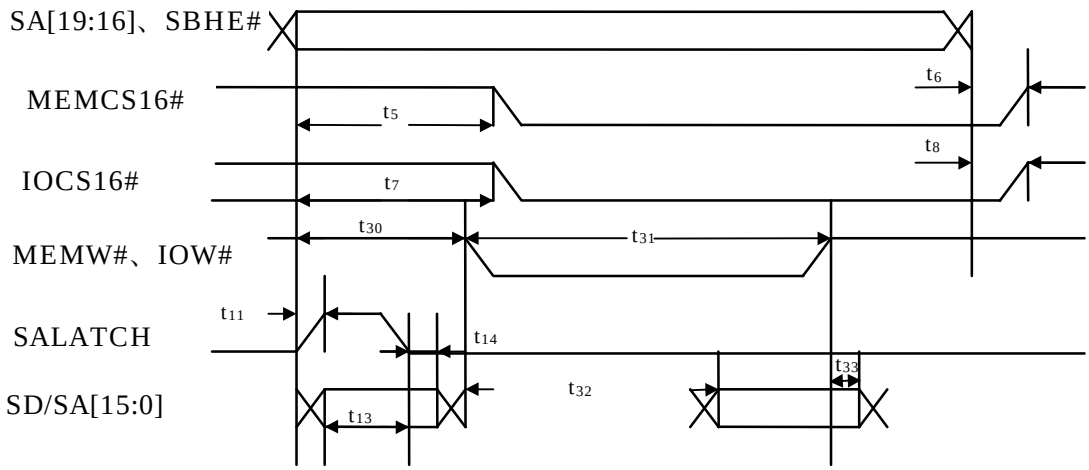


Figure 7.2 Memory, I/O write cycle timing

Symbol	Parameter	Min.	Max.	Unit	Note
t_{30}	Write Command active from SA[19:16]	162	---	ns	8 bits
		102	---	ns	16 bits
t_{31}	Memory write command pulse width	509	---	ns	8 bits
		209	---	ns	16 bits
t_{31}	IO write command pulse width	509	---	ns	8 bits
		147	---	ns	16 bits
t_{32}	Write data valid from write command	---	61	ns	8 bits
		---	47	ns	16 bits
t_{33}	Valid data from write command	25	---	ns	---

7.4 AC97 timing

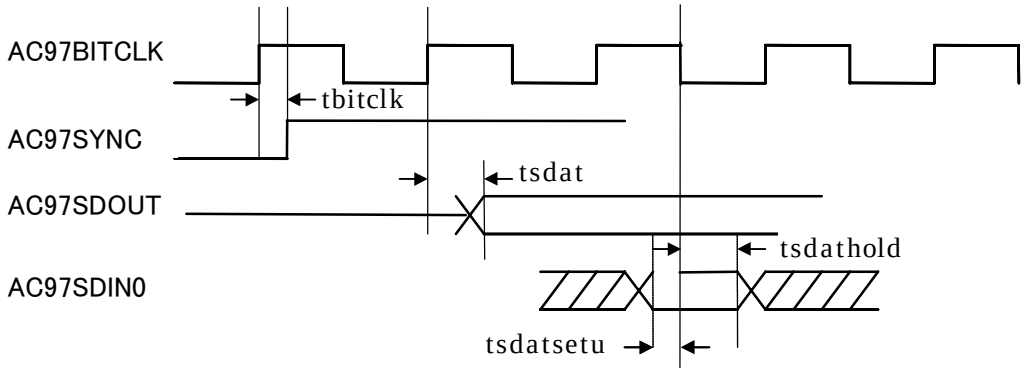


Figure 7.3 AC97 timing

Symbol	Parameter	Min.	Max.	Unit	Note
tbitclk	Rising BITCLK to SYNC	5	16	ns	---
tsdat	Rising BITCLK to SDOUT	5	17	ns	---
tsdatsetup	SDIN0 setup to falling BITCLK	15	---	ns	---
tsdathold	SDIN0 hold from falling BITCLK	5	---	ns	---

7.5 TFT timing

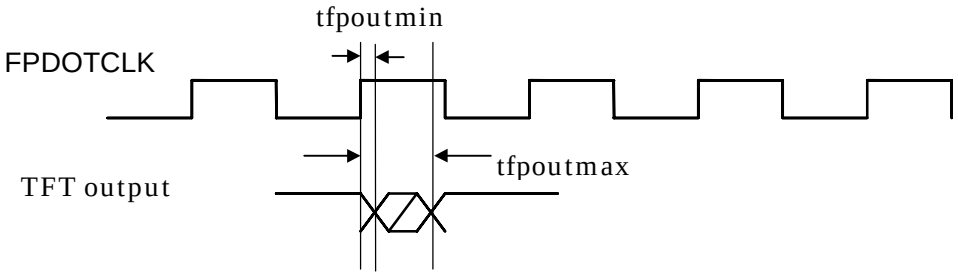


Figure 7.4 TFT timing

Symbol	Parameter	Min.	Max.	Unit	Note
tfpoutmin	TFT output Delay from	0.1	---	ns	---
(Min Delay)	FPDOTCLK	---	---	---	---
	FPDATA[17:0]	---	---	---	---
tfpoutmax	FPHSYNC,FPVSYNC	---	---	---	---
(Max Delay)	FPDISPEN,FPDOTE	---	5.2	---	---
	FPVEEON,FPVDDON	---	---	---	---

8. Cautions on use

1) Touching SCE8720Cxx (CARD-PCI/GX) while it is in operation or right after it is turned off may result in a burn because its surface temperature is high. Take the following countermeasures.
   - Notify those who might contact SCE8720Cxx while it is in operation or right after it is turned off, such as service personnel, of the heat on the surface.
   - If necessary, indicate a caution regarding surface temperature somewhere on SCE8720Cxx after it is installed on device.
   - Also if necessary, put a cover so that SCE8720Cxx cannot be touched.
2) If any part defect occurred in SCE8720Cxx, do not supply current over the current limit (6.1.1) in order to suppress abnormal heating of SCE8720Cxx. If current over the current limit is supplied to SCE8720Cxx while it is in the error mode, safety of SCE8720Cxx cannot be guaranteed.
3) Because of its structural limitation, SCE8720Cxx requires countermeasure against electrostatic noise in customer's system.
4) Do not touch the pin section of SCE8720Cxx with hand or metal.
5) Do not bend, drop or give shock to SCE8720Cxx.
6) Avoid heat, humidity and direct sunlight.
7) Do not insert or remove SCE8720Cxx while its power is turned on.
8) Do not copy or modify BIOS without permission.
9) When designing any product using SCE8720Cxx, refer to the application note as well.

Appendix A. Peripheral circuit design

A.1 IO extension of PCI bus

A.1.1 Number of PCI devices

Up to 3 devices can be connected to the PCI bus of SCE8720C (excluding Geode CS5530). Among them, up to 2 devices can be used as masters.

To connect more devices, PCICLK can be divided as shown below. In this case, it is necessary to confirm the waveform of PCICLK using an actual circuit. Also, determine whether or not a terminal circuit of PCICLK is needed. Since loads of other signals are also increased, these signals must be checked as well. When using divided PCICLK, do not use PCICLK for the extended slot. More than 1 device might be connected in a board Connected to extended slot.

Note that customization of BIOS is needed in order to increase the number of PCI Devices.

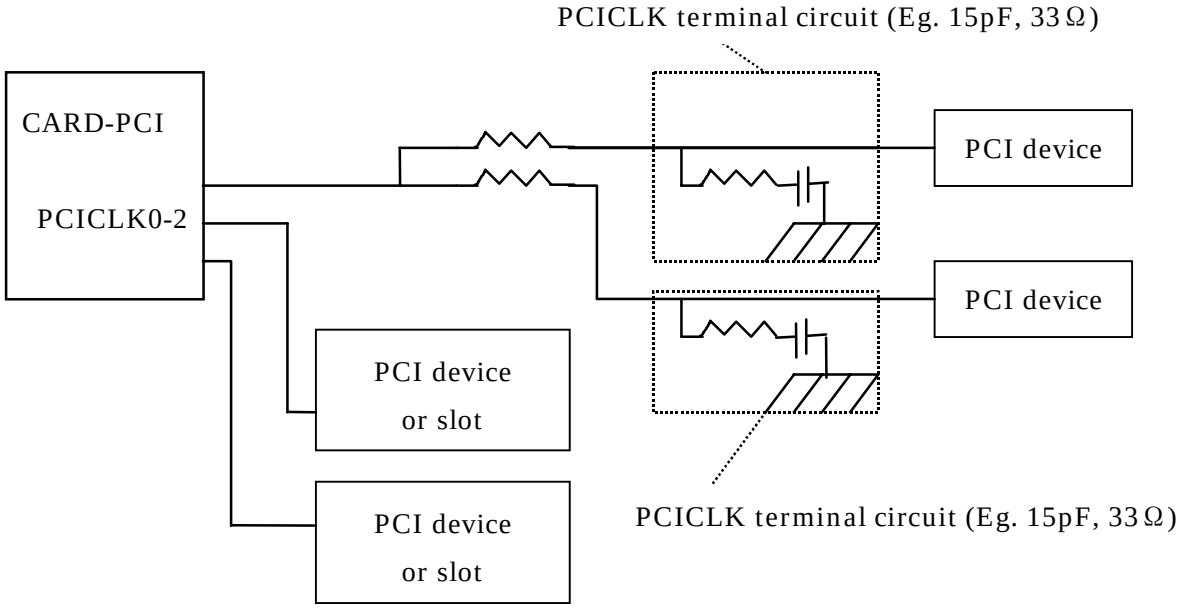


Figure A.1 PCICLK division

A.1.2 PCI device No. and wiring method for interrupts

Each device on the PCI bus must have a unique device No. The device No. is determined by which AD[11:31] signal is connected to IDSEL signals. There are 21 device Nos. in total, but among them AD28 and 29 are used inside SCE8720C.
How IDSELs are connected is shown in the table below. Connection of the PCI devices 1 to 3 cannot be changed. Customization of BIOS is needed in order to change them.
(A wiring example of interrupt and IDSEL is shown in the figure below.)

Table A.1 PCI device No. assignment

PCI device	IDSEL	Device No.
Chipset (inside Geode CS5530)	AD28	18 (12h)
USB (inside Geode CS5530)	AD29	19 (13h)
PCI device 1	AD24	14 (Eh)
PCI device 2	AD25	15 (Fh)
PCI device 3	AD26	16 (10h)

Wire the interrupt cables for each slot, so that load is put equally on each of INTA# to INTD# on the PCI device. Customization of BIOS is needed in order to change them as well.
(Note that sharing of interrupts is not available with Windows-CE.)

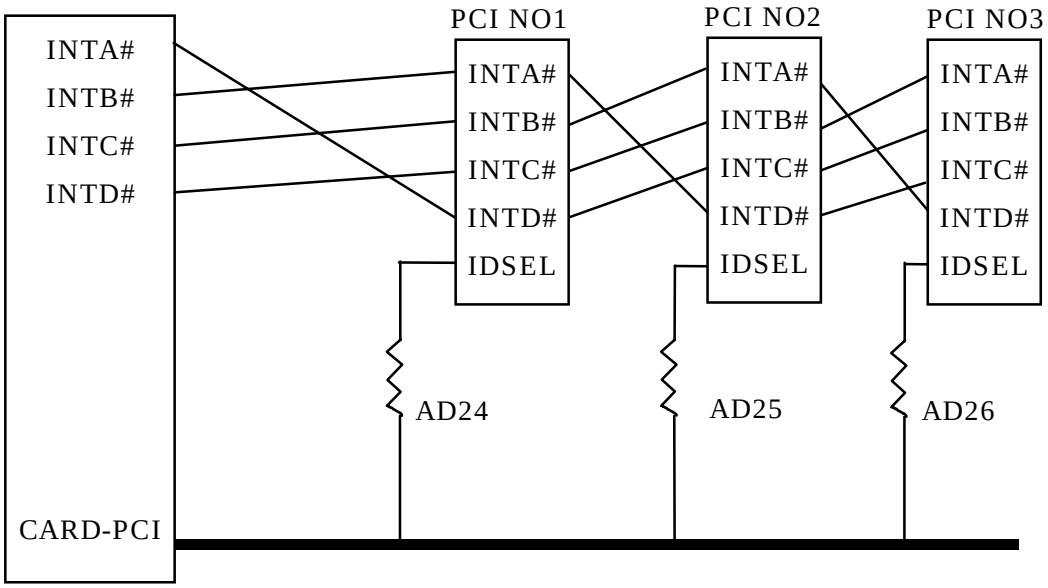


Figure A.2 Wiring of interrupts

A.1.3 Connection of 5V device to PCI bus

SCE8720C only supports the 3.3V PCI bus. Therefore, 5V PCI bus cannot be connected to the PCI bus. To connect a 5V PCI device, use the level converter which converts signals from 5V device to 3.3V, as shown in the circuit below.

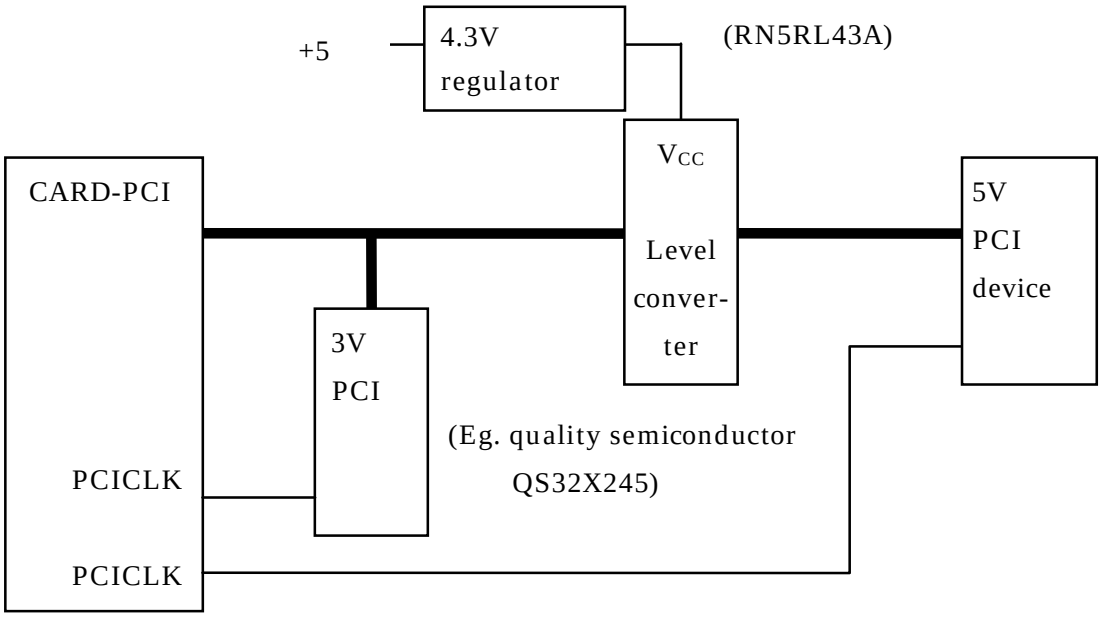


Figure A.3 Connection method of 5V PCI device

A.2 IO extension of LIMITED ISA bus

A.2.1 Address decoding

The IO addresses that can be used outside SCE8720C are the ones not used by the system, within the range from 100h to 3FFh. (refer to the IO map in the section 1.6.) When decoding, the conditions SA0-9 and AEN=0 must be set to input.

A.2.2 Pull-up of SD/SA[7:0]

Pull-up SD/SA[7:0] by a resistance of 4.7kΩ or so. Otherwise, the software cannot detect empty space in the memory area.

A.2.3 SA[15:0] latch

Since SA[15:0] are multiplexed by SD/SA[15:0] to be output, they must be externally latched by SALATCH signal. Circuit example is shown below.

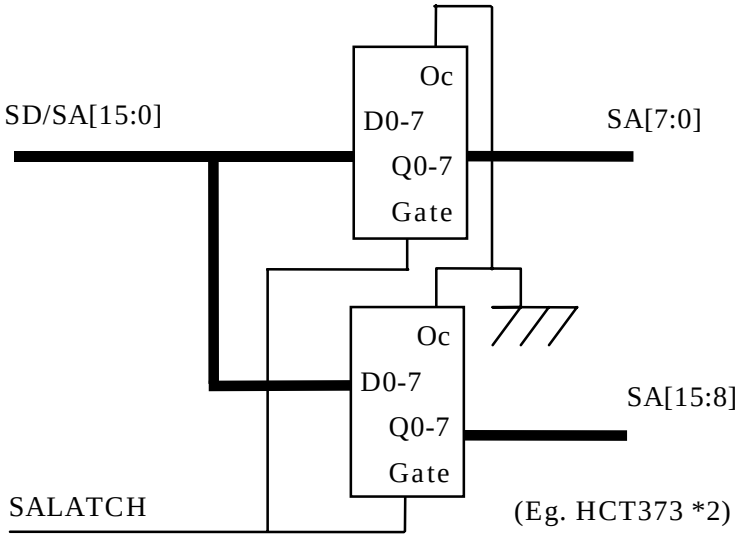


Figure A.5 Latch method of SA0-15 signals

A.2.4 Number of ISA slots

2 slots are assumed. However, condition varies depending on the type of load (CMOS, TTL, LSTTL) and wiring length. Therefore, design must be done by calculating the load, wiring length, fine-in and fine-out (refer to 6.3).

A.2.5 Pull-up resistance of IOCHRDY

Since IOCHRDY sample timing is fixed, devices on the ISA must change the signal within the fixed timing. This signal might be delayed due to increased load capacity, so externally add a pull-up resistance when load is heavy. Of course, this resistance must be within the range that can be driven by the device on the ISA.

A.2.6 SMEMR# and SMEMW# generation

As described in 4.10, SCE8720C's LIMITED ISA bus does not have SMEMR# or SMEMW# signal. However, they can easily be generated in the circuit as shown below.

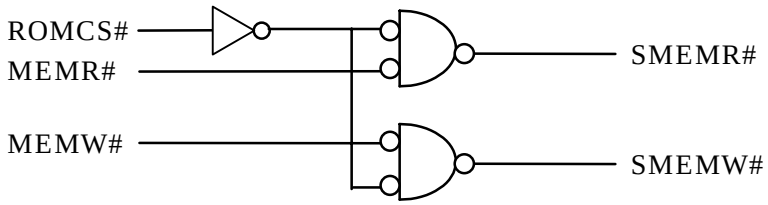


Figure A.6 Circuit to generate SMEMR# and SMEMW#

A.2.7 MEMCS16# generation

To generate MEMCS16#, the condition ROMCS#=1 (BIOS ROM is not selected) is necessary. If this condition is absent, error such as improper overwrite on BIOS ROM might occur. Circuit example is shown below.

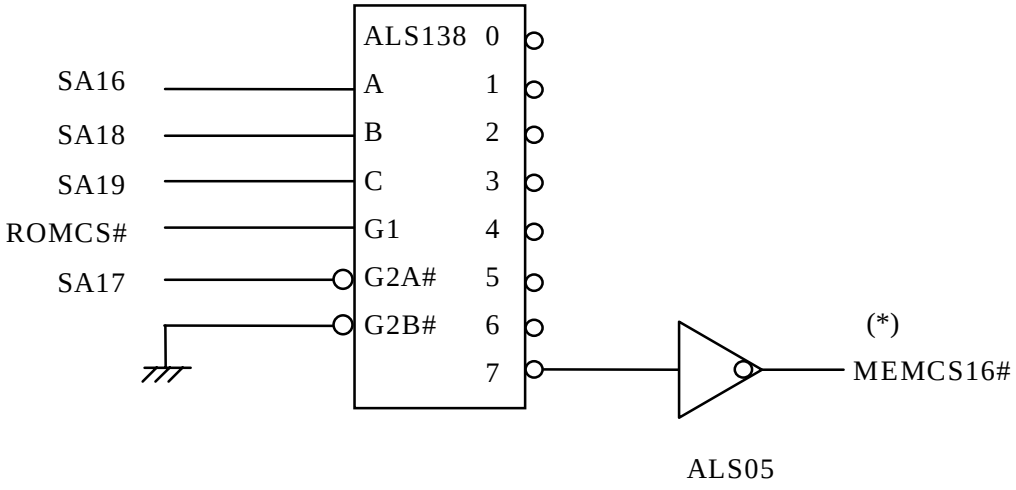


Figure A.7 Circuit to generate ROMCS16#

*: MEMCS16# is active at D0000 to DFFFF.

A.3 Power supply design: Power control circuit

Standard power voltage specifications

To guarantee liability of SCE8720C, V_{CC5V}, V_{CCCORE} and V_{CC3V} requires power quality shown below.

Ripple : 100mVp-p

Spike noise : 200mVp-p

A.3.1 Power not requiring ON/OFF by software

With systems not requiring powering-off by OS shutting down, Wake on LAN nor Wake on RING, power control is much easier not requiring V_{CCSTB}.

Block diagram is shown below. If the power ON/OFF switch cannot be used as the switch to suspend, the switch to suspend is separately required.

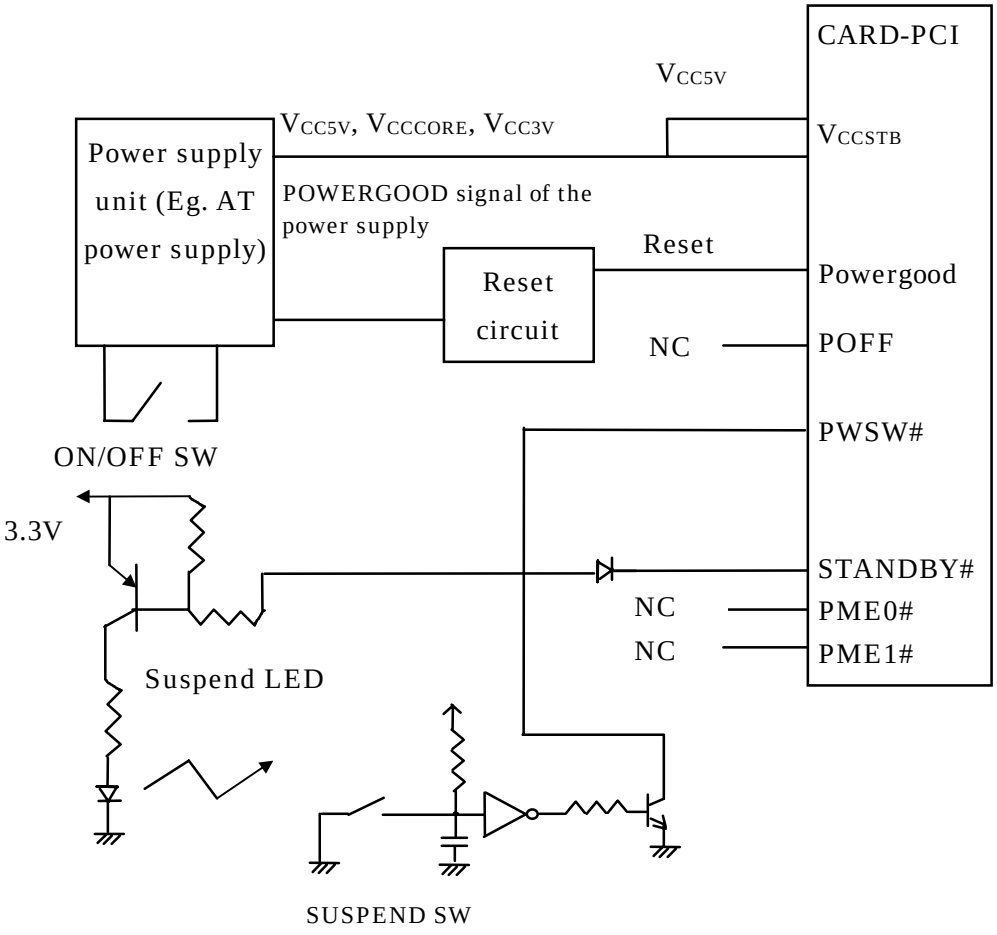


Figure A.7 Example of peripheral circuit for power not controlled by software

Note) Connect V_{CC5V} to V_{CCSTB}.

A.3.2 Power requiring ON/OFF by software

Block diagram of power control circuit, which can realize powering-off by OS shutting down, Wake on LAN or Wake on RING, is shown below. The PON/OFF SW, Wake on LAN and Wake on RING circuits must be operated by V_{CCSTB}.

When the PON/OFF switch (power switch) is held down for less than 4 seconds while the power is on, it transits to the suspend status. Holding down the switch for more than 4 seconds, the power is turned off.

In this case, a separate suspend switch is not necessary.

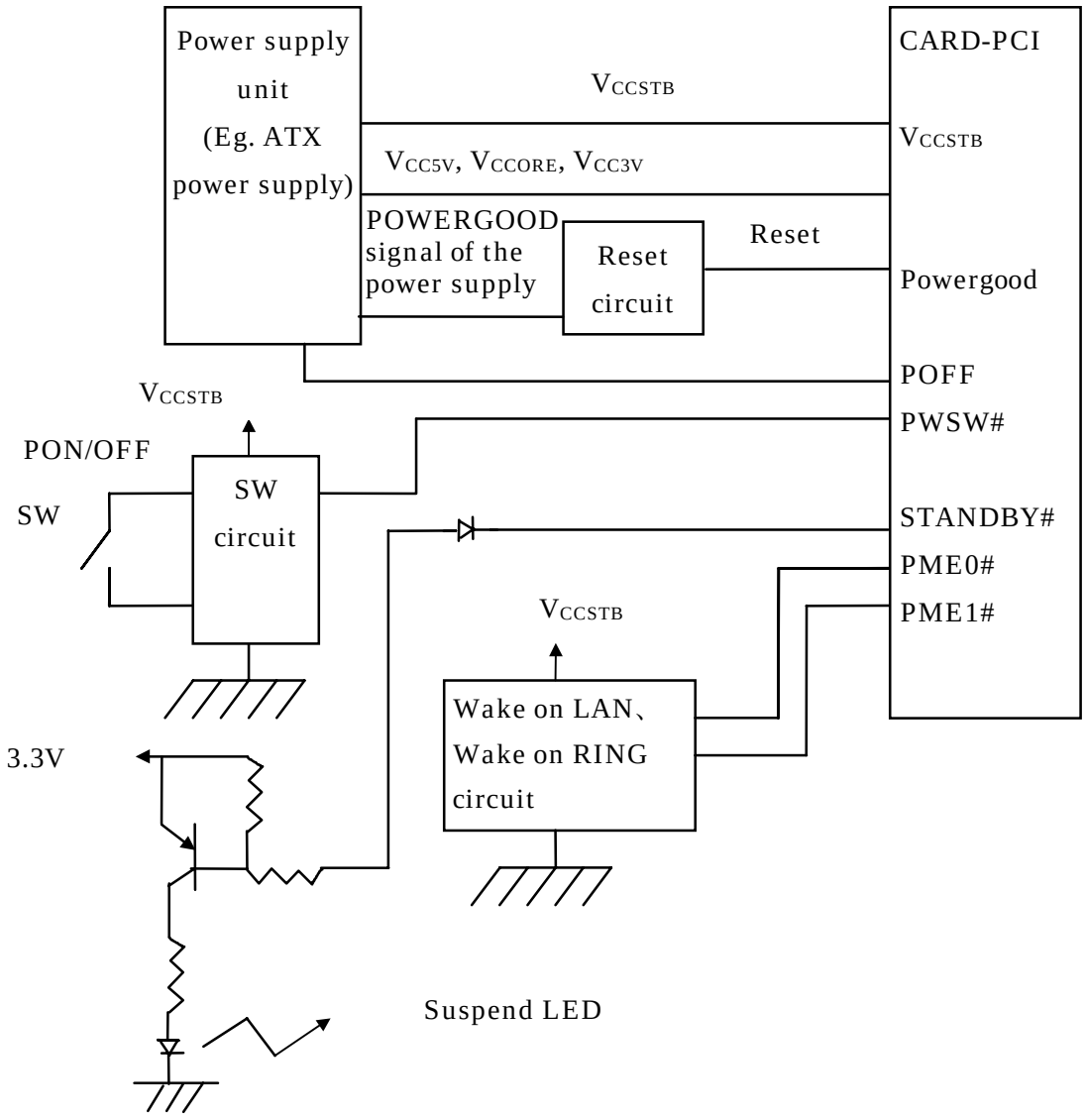


Figure A.8 Example of peripheral circuit for power controlled by software

A.3.3 Cautions on compatibility of CARD-PCI

It is recommended that signal inputs of PWSW#, PME0# and PME1# are set to low or high impedance for compatibility with other CARD-PCIs (so that other cards can also use the same main circuit). Also, STANDBY# signal is driven with open drain with SCE8720C, but with other cards, it is driven HIGH/LOW at 3.3V. Therefore design the circuit to support both, as shown in Figure A.7 and A.8.

A.3.4 Wake on LAN signal

PME0# signal is used for Wake on LAN. With PCI version 2.2, this signal is assigned to A19 pin of the PCI option connector. However, SCE8720C's PCI is version 2.1, so do not connect PME0# signal to the PCI connector. For Wake on LAN using PME0# signal, use another connector. (There are connectors specified as "semi-standard".)

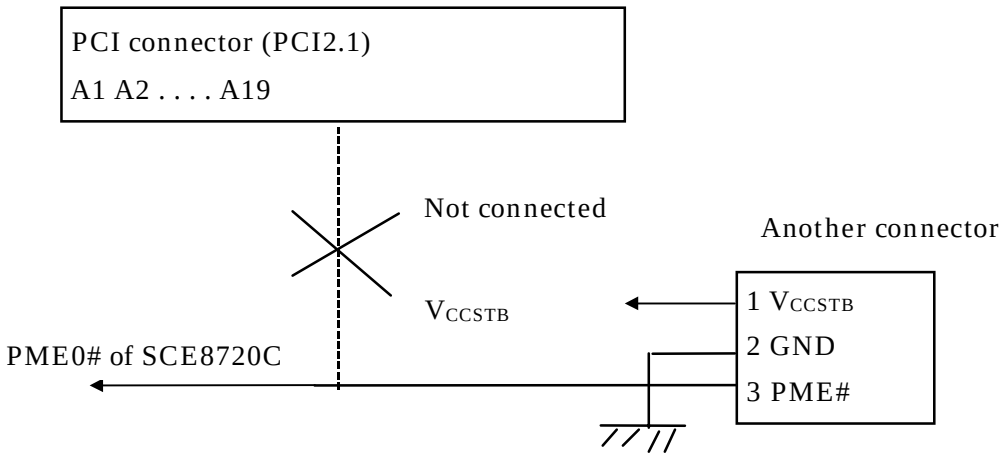


Figure A.9 Wiring example of PME0#

A.4 Cautions on artwork design

A.4.1 Power supply line

To stabilize voltages supplied to SCE8720C, place an appropriate decoupling capacitor at each power supply line close to SCE8720C connector. Recommended values are shown below.

Power supply line	Type of capacitor	Quantity
V_{CCCORE}-GND	220µF - 10V electrolytic capacitor 0.01µF ceramic capacitor	1 (*1) 2
V_{CC5V}-GND	220µF - 10V electrolytic capacitor 0.01µF ceramic capacitor	1 (*2) Large quantity (*3)
V_{CC3V}-GND	100µF - 10V electrolytic capacitor 0.01µF ceramic capacitor	1 Large quantity (*3)
V_{CCSTB}-GND	10µF - 10V electrolytic capacitor 0.01µF ceramic capacitor	1 2~ (*3)
V_{CCBAK}	1µF laminated ceramic	1

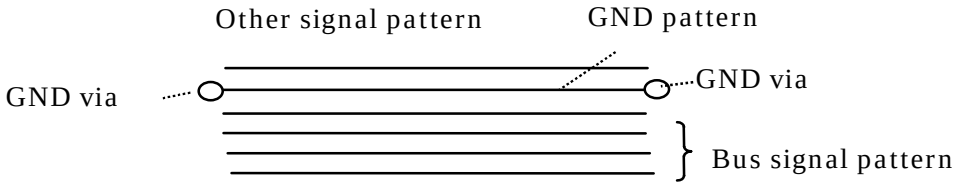
*1: V_{CCORE} is input voltage of DC-DC converter which generates the core voltage (2.2V) of CPU. Although SCE8720C has a built-in capacitor, another capacitor is needed on the system side as peak current flows anyway. Since the voltage is 5V, it is possible to use the common power supply with V_{CC5V}. However, as peak current flows as mentioned above, countermeasure such as use of separate power supply line on the board is needed.

*2: In order to avoid variation of voltage when accessing HDD or CompactFlash, put a capacitor of required value to V_{CC5V}.

*3: 0.5 to 1 ceramic capacitor per IC is recommended.

A.4.2 Address bus and data bus

The address and data busses, such as AD0-31 of PCI, SD0-15 and SA0-19 of ISA, should be grouped by bus type for wiring. (Do not mix with other signals.) To avoid crosstalk, do not wire these busses and other signals in parallel. If wiring in parallel, put GND between the signals and busses.

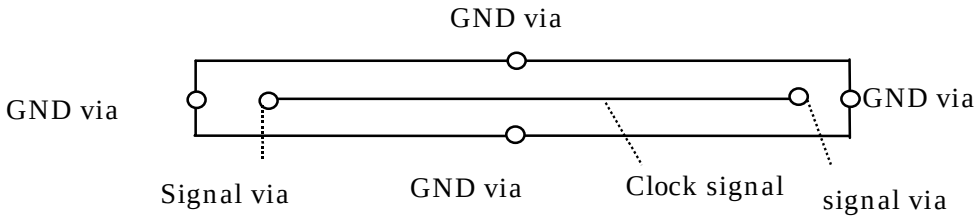


A.4.3 PCI signal

Avoid making the PCI signal wiring too long since the PCI signal speed is higher than those of ISA. If long wiring cannot be avoided or load is heavy, be sure to confirm the waveform.

A.4.4 Clock signal

High speed clock signal are likely to negatively affect other signals by crosstalk or be affected by other signals, resulting in trouble. To avoid such troubles, guard it using GND patter as shown below.



Clock signals requiring attention is shown below.

Clock signal name	Frequency
PCICLK0-2	33MHz
FPDOTCLK	25MHz~65MHz
FPDOTE	12.5MHz~32.5MHz
AC97BITCLK	12.288MHz (varies depending on Codec specifications)

A.4.5 CRT RGB signal

When noise is present on CRTR, CRTG or CRTB signal, display quality drops. To avoid this make the wiring as short and far from other signals as possible so that no crosstalk occurs.

A.4.6 Reset signal

Use the RST# signal for resetting the system (other than SCE8720C).
Do not make the signal wiring too long. If long wiring cannot be avoided, add a buffer or a capacitor to remove noise.
Also, POWERGOOD signal should not be used to reset the system circuit (other than SCE8720C). This is fine from the logical viewpoint, but it does raise the possibility to extract noise, resulting in decreased liability.

Appendix B. Timing examples of power management signals

1. Powering-ON by PWSW# or PME0, 1/Powering-OFF by PWSW#

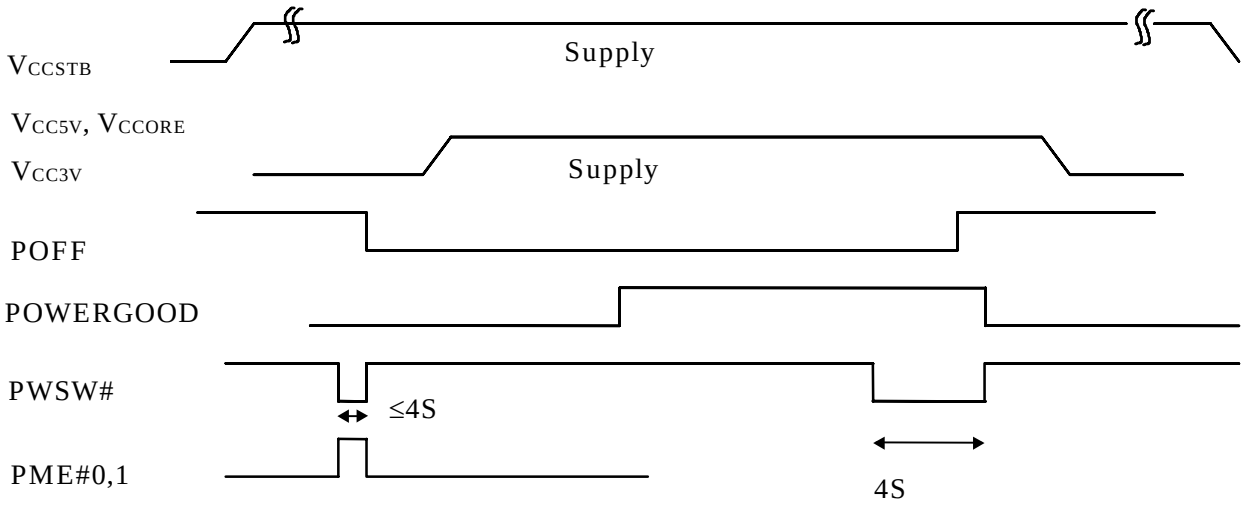
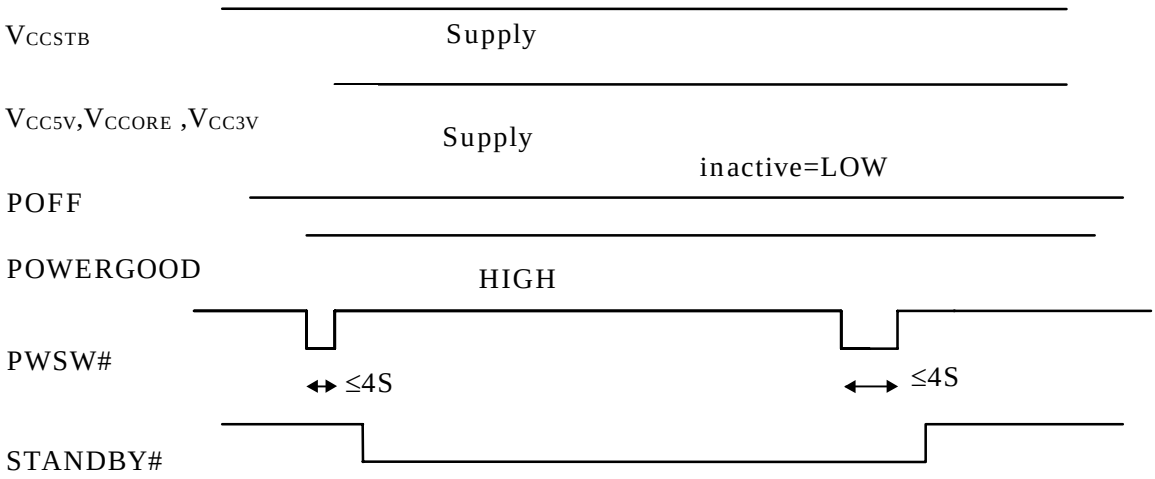


Figure B.1 PM signal operation timing example 1

2. Transit to/from the standby mode by PWSW#



Note) Do not supply V_{CC5V} when V_{CCSTB} is OFF.

Figure B.2 PM signal operation timing example 2

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