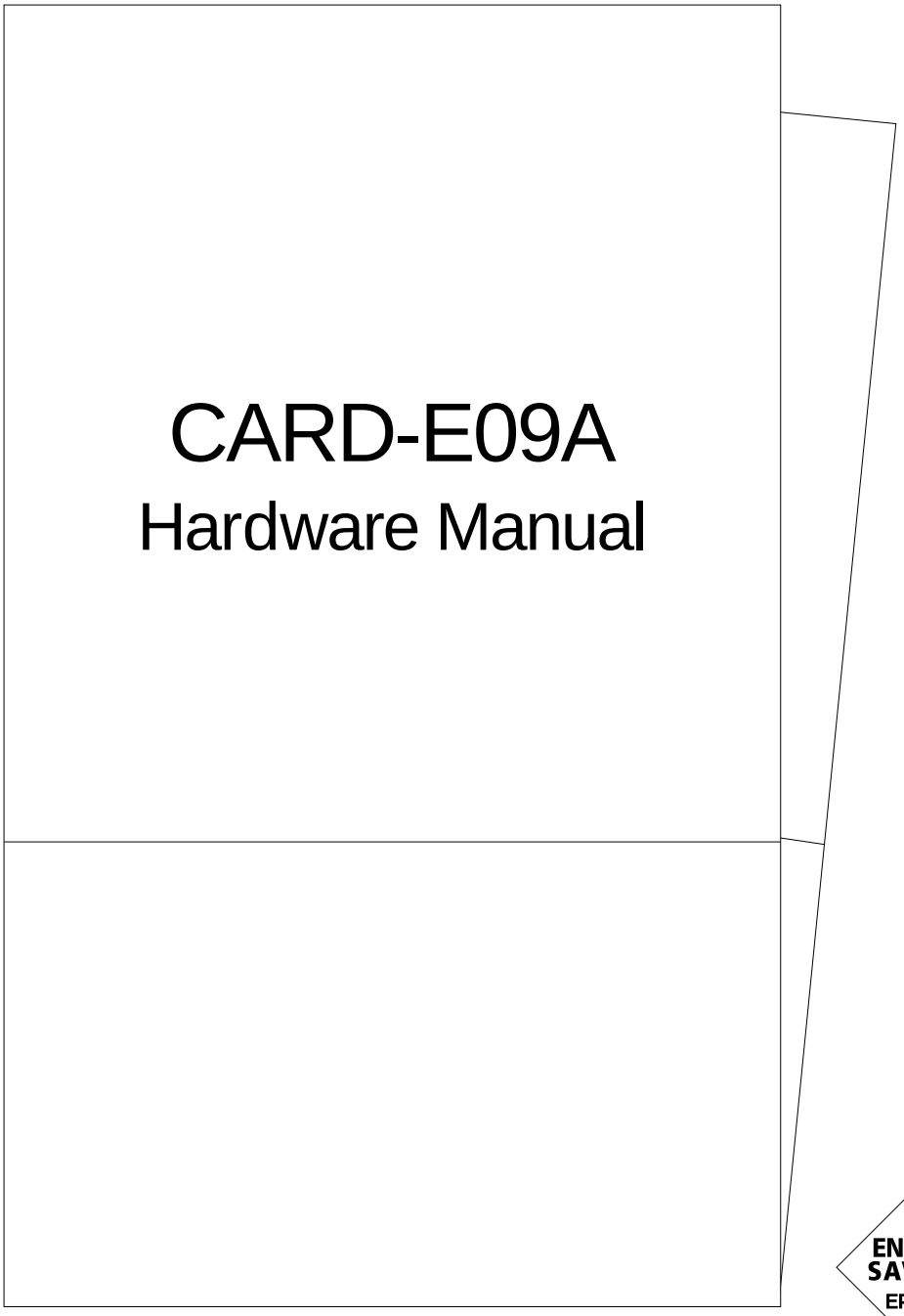
MF1193-04

EPSON

CARD-E09A

Hardware Manual



ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

NOTICE

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

Table of contents

1 BASIC SPECIFICATIONS 1

1.1 Block diagram 2

2 MECHANICAL SPECIFICATION 3

2.1 External dimensions 3

2.2 Weight 3

2.3 Connector 3

2.4 Installation 3

2.5 CompactFlash connector 3

3 PIN ASSIGNMENT 4

4 FUNCTION OF PINS 7

5 FUNCTION DESCRIPTION 13

5.1 Memory map 13

5.2 SDRAM 17

5.3 Flash ROM 17

5.4 Interrupt 18

5.4.1. IRQ0 18
5.4.2. Registers 20

5.5 DMA 23

5.6 Timer 24

5.7 RTC 25

5.8 Power Management 26

5.8.1. SH7709A 26
5.8.2. SDRAM 26
5.8.3. SED1355 26
5.8.4. Companion Chip 26
5.8.5. Suspend/resume 27
5.8.6. Power-off 34

5.9 Serial Communication Interface 35

5.10 Parallel Interface 37

5.10.1. Registers 37

5.10.2 Enhanced parallel port 39
5.10.3 Interrupt 41
5.10.4 Circuitry example 41
5.11 Keyboard/Mouse Interface 42
5.11.1 Registers 43
5.11.2 Data reception 45
5.11.3 Data transmission 45
5.11.4 Programming 47
5.11.5 Connection example 47
5.12 PCMCIA/CompactFlash Interface 48
5.12.1 PCMCIA/CompactFlash memory map 49
5.12.2 Register 50
5.12.3 Timing 56
5.12.4 Slot Power On/Off Signals 57
5.12.5 Slot Signals at Power-Off 58
5.12.6 Slot Power-On/Off Timing 58
5.12.7 Slot Auto Power-On/Off Timing 59
5.12.8 Interrupt 60
5.12.9 Connection example 61
5.12.10 CompactFlash 63
5.13 ISA Interface 64
5.13.1 Overview 64
5.13.2 Signals 64
5.13.3 ISA interface memory map 65
5.13.4 Registers 66
5.13.5 Timing 67
5.13.6 Connection example 69
5.14 CRT/LCD Interface 71
5.15 AD/DA 73
5.16 Port 74
5.17 SH7709A Bus 75
5.18 Baud Rate Generator 77
5.18.1 Registers 78
5.18.2 Setting the output frequency 82
6 ENVIRONMENTAL CHARACTERISTICS 84
6.1 Temperature 84
6.2 Humidity 84
7 ELECTRICAL CHARACTERISTICS 85
7.1 Absolute maximum rating 85
7.2 Recommended operating condition 85
7.3 Current Consumption 86
7.4 Pin characteristics 87

8 AC CHARACTERISTICS 103

9 CAUTIONS ON HANDLING 116

Figure

Figure 1-1 CARD-E09A Block Diagram....2
Figure 2-2 CARD-E09A External Dimension Diagram....3
Figure 3-1 CARD-E09A Pin No. 4
Figure 3-2 CompactFlash Connector Pin No. 6
Figure 5-1 CARD-E09A Memory Map 13
Figure 5-2 Area 4 Memory Map 14
Figure 5-3 Area 5 Memory Map 14
Figure 5-4 Area 6 Memory Map 15
Figure 5-5 Flash ROM Mapping....17
Figure 5-6 Interrupt Block Diagram 18
Figure 5-7 IRQ0 Block Diagram 19
Figure 5-8 DMA Block Diagram 23
Figure 5-9 Timer Block Diagram....24
Figure 5-10 RTC Block Diagram....25
Figure 5-11 VBK Power Switching Circuitry Example 25
Figure 5-12 Serial Communication Interface Block Diagram....35
Figure 5-13 Parallel Interface Diagram....37
Figure 5-14 EPP Read Cycle 40
Figure 5-15 EPP Write Cycle 40
Figure 5-16 Parallel Port Interrupt....41
Figure 5-17 Parallel Port Interface Example....41
Figure 5-18 Keyboard Controller Block Diagram 42
Figure 5-19 Keyboard Data Receiving/Transmitting Timing 46
Figure 5-20 Keyboard/Mouse Interface Example 47
Figure 5-21 PCMCIA/CompactFlash Interface Block Diagram 48
Figure 5-22 PCMCIA Bus Memory Map 49
Figure 5-23 PCMCIA Memory Read Timing 56
Figure 5-24 PCMCIA Memory Write Timing 56
Figure 5-25 PCMCIA Power-On/Off Timing 59
Figure 5-26 PCMCIA Auto Power-On Timing....60
Figure 5-27 PCMCIA Auto Power-Off Timing 60
Figure 5-28 PCMCIA Connection Example 62
Figure 5-29 ISA Bus Interface Diagram 65
Figure 5-30 ISA Bus Memory Map 66
Figure 5-31 ISA Read Timing 67
Figure 5-32 ISA Write Timing....68
Figure 5-33 Memory Device Connection Example....69
Figure 5-34 SMEMR# & SMEMW# Generation Example 69
Figure 5-35 I/O Device Connection Example 70
Figure 5-36 CRT/LCD Interface System Diagram....71
Figure 5-37 SH7709A Memory Map (SED1355)....72
Figure 5-38 AD/DA Block Diagram....73
Figure 5-39 Analog Input Pin Protection Circuitry Example....73
Figure 5-40 Port Diagram....74
Figure 5-41 SH7709A Bus Diagram....75
Figure 5-42 WAIT# Example 76
Figure 5-43 BRG Block Diagram (1) 77
Figure 5-44 BRG Block Diagram (2) 77
Figure 8-1 CKIO Timing 103
Figure 8-2 EXTCLKI Timing....103
Figure 8-3 SH-Bus Timing 105
Figure 8-4 ISA Interface Timing (IOCHRDY Asserted) 106
Figure 8-5 ISA Interface Timing (IOCHRDY Deasserted)....107
Figure 8-6 PCMCIA Memory Timing (WAIT# Deasserted) 108
Figure 8-7 PCMCIA Memory Timing (WAIT# Asserted) 109
Figure 8-8 PCMCIA I/O Timing (WAIT# Deasserted) 110

Figure 8-9 PCMCIA I/O Timing (WAIT# Asserted)....111
Figure 8-10 EPP Read Timing (BUSY Deasserted)....112
Figure 8-11 EPP Read Timing (BUSY Asserted)....112
Figure 8-12 EPP Write Timing (BUSY Deasserted)....113
Figure 8-13 EPP Write Timing (BUSY Asserted)....113
Figure 8-14 Keyboard/Mouse Receiving Data Timing....114
Figure 8-15 Keyboard/Mouse Sending Data Timing....114
Figure 8-16 Power On/Off Timing....115

Table

Table 5-1 Pin Status....29
Table 5-2 Pin Status (CompactFlash Connector)....33
Table 5-3 Parallel Port Control Register (EPP Mode)....39
Table 5-4 PCMCIA Memory Read/Write Timing....57
Table 5-5 PCMCIA Power Control....57
Table 5-6 PCMCIA Power Control....61
Table 5-7 ISA Read/Write Timing....68
Table 5-8 SH7709A Port Assignment....72
Table 5-9 BRG Register Value....83
Table 8-1 CKIO A.C Specification....103
Table 8-2 EXTCLKI A.C Specification....103
Table 8-3 H-Bus A.C Specification....104
Table 8-4 ISA Interface A.C Specification....106
Table 8-5 PCMCIA A.C Specification (Memory)....108
Table 8-6 PCMCIA A.C Specification (I/O)....110
Table 8-7 EPP A.C Specification....112
Table 8-8 Keyboard/Mouse Interface A.C Characteristics....114
Table 8-9 Power On/Off A.C Specification....115

1 BASIC SPECIFICATIONS

The SCE8700C series (referred to as "CARD-E09A" throughout this document) uses SH7709A as its CPU, and contains the PCMCIA interface, serial interface, keyboard/mouse interface, and parallel interface, all in a card-size structure. Its basic configuration is described as follows:

CPU	SH7709A	133MHz
Companion chip	ISP0110	PCMCIA interface Serial interface (16550-compatible x 2) PS/2 keyboard interface PS/2 mouse interface Parallel interface ISA bus interface
Memory	SDRAM	16 MB or 32 MB
	Flash ROM	256 KB
Video	SED1355	CRT LCD
	VRAM	2 MB

List of CARD-E09A models

Model	CPU Clock	SDRAM
SCE8700C01	133MHz	16MB
SCE8700C02	133MHz	32MB

1.1 Block diagram

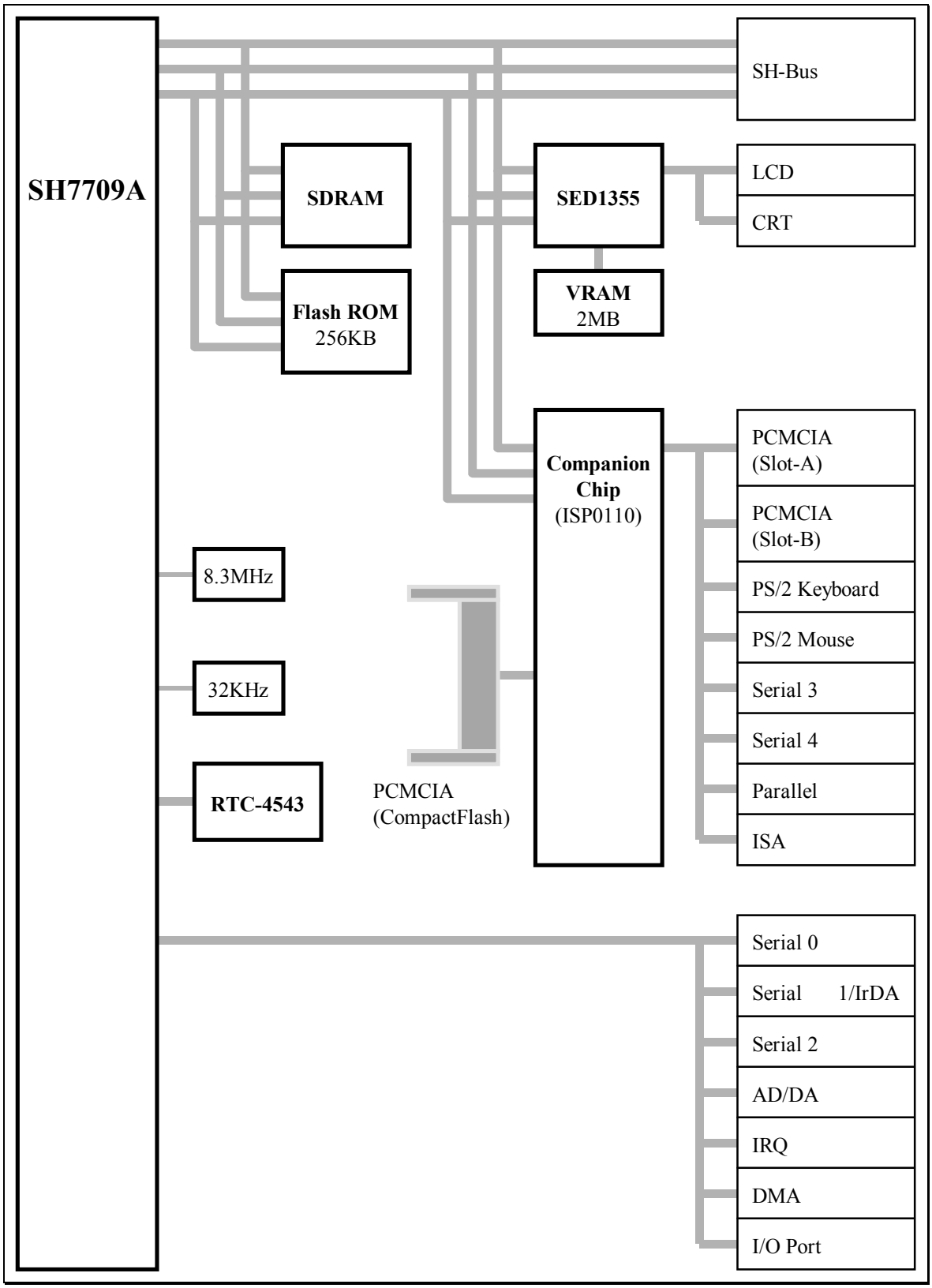


Figure 1-1 CARD-E09A Block Diagram

2 MECHANICAL SPECIFICATION

2.1 External dimensions

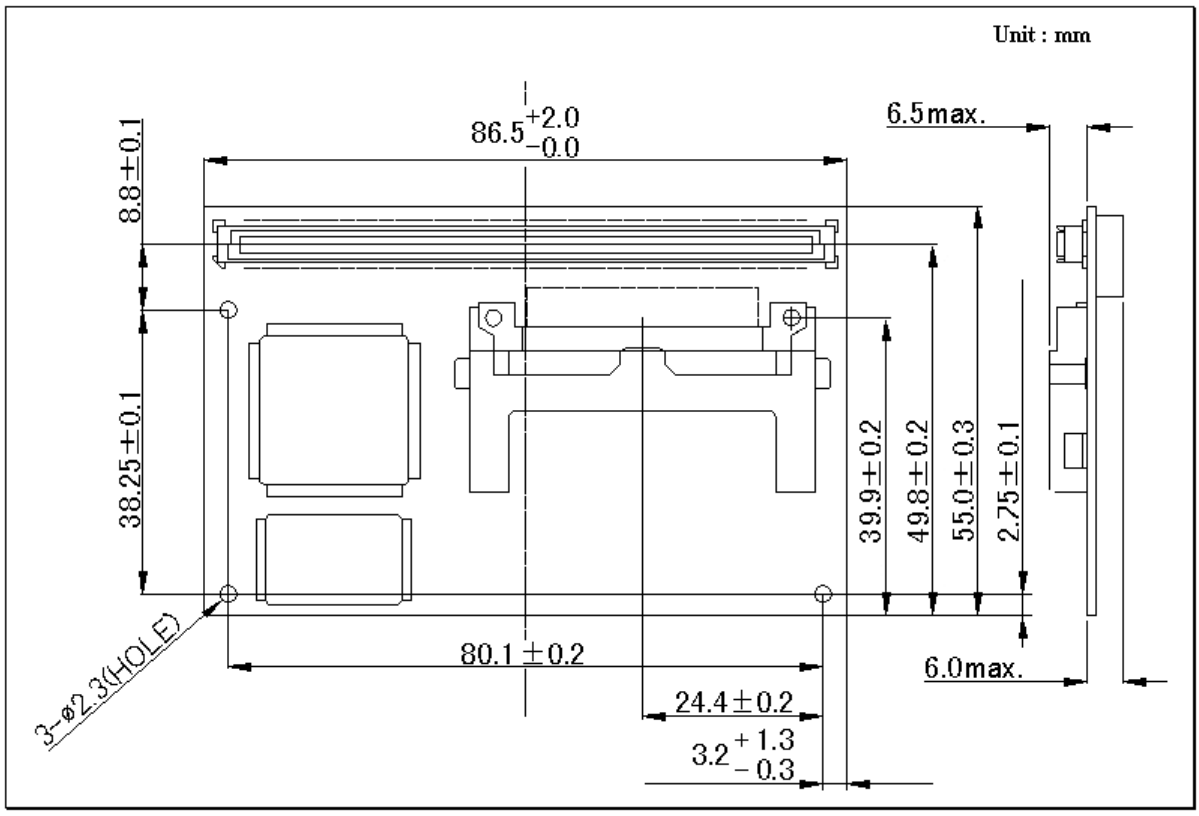


Figure 2-2 CARD-E09A External Dimension Diagram

2.2 Weight

About 26.5g

2.3 Connector

Molex 52760 (240V)

2.4 Installation

Either Molex 53467 (240V) or 53481(240V) can be used as the receiving connector on the card.

2.5 CompactFlash connector

Fujitsu FCN-568H050-G/A1 is used.
When a CompactFlash card is plugged into this connector, the edge of the CompactFlash card extends 2.0mm (max.) beyond the edge of the CARD-E09A.

3 PIN ASSIGNMENT

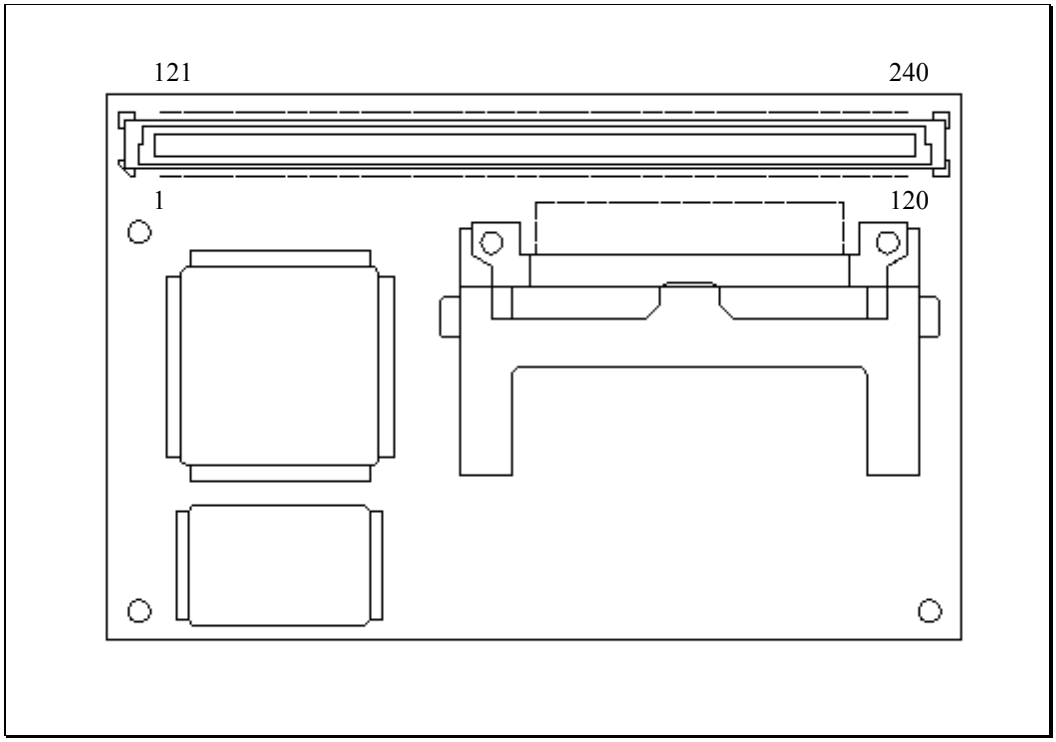


Figure 3-1 CARD-E09A Pin No.

No.	Signal	No.	Signal	No.	Signal	No.	Signal
1	GND	61	GND	121	GND	181	GND
2	BCD1#	62	CKIO	122	ACD1#	182	AN5
3	BCE1#	63	TCLK	123	ACE1#	183	DA1
4	BCE2#	64	RESETP#	124	ACE2#	184	DA0
5	BOE#	65	RESETM#	125	AOE#	185	TXD1
6	SLOT_B_VCC	66	WAIT#	126	SLOT_A_VCC	186	RXD1
7	BVS1	67	CS2#	127	AVS1	187	TXD2
8	BIORD#	68	CS0#	128	AIORD#	188	RXD2
9	BIOWR#	69	RD/WR#	129	AIOWR#	189	RTS2#
10	BWE#	70	WE1#	130	AWE#	190	CTS2#
11	BRDY_IRQ#	71	WE0#	131	ARDY_IRQ#	191	PWOFF#
12	BVS2	72	RD#	132	AVS2	192	SRBTN#
13	BRESET	73	BS#	133	ARESET	193	FPVCCON
14	BWAIT#	74	A25	134	AWAIT#	194	PTC7/PINT7
15	VCC	75	A24	135	VCC	195	PTC6/PINT6
16	BREG#	76	A23	136	AREG#	196	PTC5/PINT5
17	BBVD2_SPKR	77	VCC	137	ABVD2_SPKR	197	VCC
18	BBVD1_STSCHG#	78	A22	138	ABVD1_STSCHG#	198	PTC4/PINT4
19	BWP_IOIS16#	79	A21	139	AWP_IOIS16#	199	PTC3/PINT3
20	GND	80	A20	140	GND	200	PTC2/PINT2
21	BCD2#	81	A19	141	ACD2#	201	PTC1/PINT1
22	BADRENA#	82	GND	142	AADRENA#	202	GND
23	BDATAENA#	83	A18	143	ADATAENA#	203	DACK0#
24	BVPPPGM	84	A17	144	AVPPPGM	204	DREQ0#
25	BVPPVCC	85	A16	145	AVPPVCC	205	DACK1#
26	BVCC5#	86	A15	146	AVCC5#	206	DREQ1#
27	BVCC3#	87	A14	147	AVCC3#	207	NMI
28	KBCLK	88	A13	148	CA25	208	IRQ1
29	KBDATA	89	A12	149	CA24	209	IRQ2
30	MSCLK	90	A11	150	CA23	210	IRQ3
31	MSDATA	91	A10	151	SLCT	211	IRQ4
32	RESETDRV	92	A9	152	PE	212	VSYNC
33	IOCHRDY	93	A8	153	BUSY	213	HSYNC
34	IOW#	94	A7	154	ACK#	214	B
35	IOR#	95	A6	155	LPTD7	215	G
36	MEMCS16#	96	A5	156	LPTD6	216	R
37	SBHE#	97	A4	157	LPTD5	217	FPDAT15
38	IOCS16#	98	A3	158	LPTD4	218	FPDAT14
39	MEMR#	99	A2	159	LPTD3	219	FPDAT13
40	MEMW#	100	A1	160	SLCTIN#	220	FPDAT12
41	GND	101	GND	161	GND	221	GND
42	ISADATAENA#	102	A0	162	LPTD2	222	FPDAT11
43	RI4#	103	D15	163	INIT#	223	FPDAT10
44	DTR4#	104	D14	164	LPTD1	224	FPDAT9
45	VCORE	105	D13	165	VCORE	225	FPDAT8
46	VCORE	106	VCC	166	VBK	226	VCC
47	CTS4#	107	D12	167	ERROR#	227	FPDAT7
48	TXD4	108	D11	168	LPTD0	228	FPDAT6
49	RTS4#	109	D10	169	AFD#	229	FPDAT5
50	RXD4	110	D9	170	STROBE#	230	FPDAT4
51	DSR4#	111	D8	171	STANDBY#	231	FPDAT3
52	DCD4#	112	D7	172	ROMDIS#	232	FPDAT2
53	RI3#	113	D6	173	RESERVE	233	FPDAT1
54	DTR3#	114	D5	174	EXTCLKI	234	FPDAT0
55	CTS3#	115	D4	175	RESERVE	235	DOTCLK
56	TXD3	116	D3	176	CA22	236	MOD
57	RTS3#	117	D2	177	TXD0	237	FPVEEON
58	RXD3	118	D1	178	SCK0	238	LINE
59	DSR3#	119	D0	179	RXD0	239	FRAME
60	DCD3#	120	GND	180	AN4	240	GND

The CompactFlash connector has the following pin assignment.

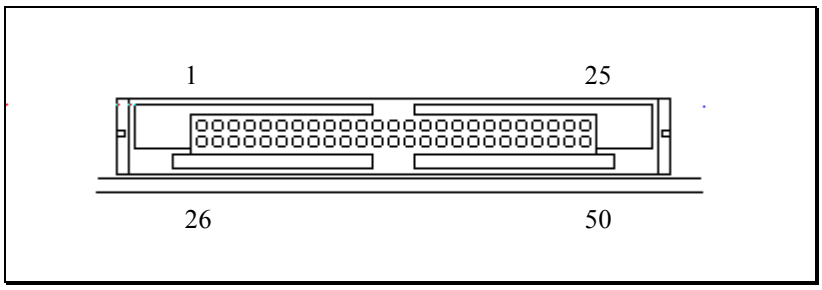


Figure 3-2 CompactFlash Connector Pin No.

No.	Signal	No.	Signal
1	GND	26	RESERVE (*)
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D17
7	CCE1#	32	CCE2#
8	A10	33	RESERVE (*)
9	COE#	34	CIORD#
10	A9	35	CIOWR#
11	A8	36	CWE#
12	A7	37	CRDY_IREQ#
13	CVCC	38	CVCC
14	A6	39	RESERVE (*)
15	A5	40	RESERVE (*)
16	A4	41	RESET
17	A3	42	CWAIT#
18	A2	43	RESERVE (*)
19	A1	44	CREG#
20	A0	45	RESERVE (*)
21	D0	46	CBVD1_STSCHG#
22	D1	47	D8
23	D2	48	D9
24	CWP_IOIS16#	49	D10
25	RESERVE (*)	50	GND

(*) The RESERVE pin is not connected inside the CARD-E09A.

4 FUNCTION OF PINS

This section briefly describe function of pins in each of the interfaces.
The following symbols are used in the Type column of the tables.

I	-	Input pin
O	-	Output pin
O OD	-	Output pin (open drain output)
Tri	-	Output pin (3-state output)
I/O	-	Input/output pin
I/O OD	-	Input/output pin (open drain output)

SH7709A bus

Pin	Type	Description
A[0..25]	O	Address
D[0..15]	I/O	Data bus
CKIO	O	System clock
BS#	O	Bus cycle start signal
RD#	O	Read strobe signal
RD/WR#	O	Read/write toggle signal
WE0#	O	Write strobe signal for D[0..7]
WE1#	O	Write strobe signal for D[8..15]
WAIT#	I	Wait state request signal
CS2#	O	Area 2 chip select signal

PCMCIA interface

Pin	Type	Description
CA[23..25]	O	Upper 3 bits of address of PCMCIA card.
AREG# BREG#	Tri	For memory card, this signal indicates either the attribute memory or common memory is accessed. When this signal is LOW, the attribute memory is accessed. The signal becomes LOW during I/O card access.
ACE1# BCE1#	Tri	Indicates even addresses are valid at the card select signal.
ACE2# BCE2#	Tri	Indicates odd addresses are valid at the card select signal.
AOE# BOE#	Tri	This is the read strobe signal of memory card.
AWE# BWE#	Tri	This is the write strobe signal to memory card
AIORD# BIORD#	Tri	This is the read strobe signal of I/O card.
AIOWR# BIOWR#	Tri	This is the write strobe signal to I/O card.
AWP_IOIS16# BWP_IOIS16#	I	In the memory card mode, this signal indicates the state of the write protect switch of the card. In the I/O card mode, it indicates whether the I/O port on the interface allows 16-bit access.
ARDY_IREQ# BRDY_IREQ#	I	In the memory card mode, they become the ready signals from the card. In the I/O card mode, they become the interrupt request signals from the card.
AWAIT# BWAIT#	I	This is the signal the PCMCIA card uses to delay ending the current cycle. The CARD-E09A does not end the cycle until this signal becomes HIGH.
ACD[1..2]# BCD[1..2]#	I	This signal indicates whether a PCMCIA card is inserted or not.
ARESET	Tri	This is the initialization signal of a PCMCIA card.

Pin	Type	Description
BRESET		
ABVD2_SPKR BBVD2_SPKR	I	In the memory card mode, these input signals indicate the voltage of the battery on the card. In the I/O card mode, these input signals have no meaning because the CARD-E09A does not support digital audio input.
ABVD1_STSCHG# BBVD1_STSCHG#	I	In the memory card mode, these signals indicate the state of the voltage of the battery on the card. In the I/O card mode, these input signals indicates the state of the card, such as ready/busy, write-protect.
AVS[1..2] BVS[1..2]	I	These pins detect voltage of the power source requested by the PCMCIA card.
AVPPVCC BVPPVCC	O	These pins control the power source (VPP) of the PCMCIA card. When the signal becomes HIGH, a circuitry is required to supply power to the VPP of the card, using the same power source of VCC of the card.
AVPPPGM BVPPPGM	O	These pins control the power source (VPP) of the PCMCIA card. When the signal becomes HIGH, a circuitry is required to supply the program power (usually 12V) to the VPP of the card,
AVCC3# BVCC3#	O	These pins control the power source (VCC) of the PCMCIA card. When the signal becomes LOW, a circuitry is required to supply a 3.3V power to the VCC of the card,
AVCC5# BVCC5#	O	These pins control the power source (VCC) of the PCMCIA card. When the signal becomes LOW, a circuitry is required to supply a 5V power to the VCC of the card,
AADRENA# BADRENA#	O	These pins indicate the address to the PCMCIA card is valid. They control the address buffer gate connected between the CARD-E09A and the card.
ADATAENA# BDATAENA#	O	These pins indicate the PCMCIA card data is valid. They controls the data buffer gate connected between the CARD-E09A and the card.

Serial interface

Pin	Type	Description
SCK0	O	This is the clock output pin of Serial 0.
TXD0 TXD1 TXD2 TXD3 TXD4	O	They are asynchronous serial data output pins. When infrared communication is used, TXD1 becomes the data transmission output pin.
RXD0 RXD1 RXD2 RXD3 RXD4	I	They are asynchronous serial data input pins. When infrared communication is used, RXD1 becomes the data reception input pin.
DCD3# DCD4#	I	They are input signals to indicate the modem or the data terminal has detected a carrier.
DTR3# DTR4#	O	They are output signals to indicate the modem or the data terminal is ready for communication with the CARD-E09A.
DSR3# DSR4#	I	They are input signals to indicate the modem or the data terminal is ready for communication with the CARD-E09A.
RTS2# RTS3# RTS4#	O	They are output signals to indicate the CARD-E09A is ready to send data to the modem or the data terminal.
CTS2# CTS3# CTS4#	I	They are input signals to indicate the modem or the data terminal is ready to receive data from the CARD-E09A, in response to the CARD-E09A's request to send.
RI3# RI4#	I	They are input signals to indicate the modem or the data terminal has detected the telephone ring.

Keyboard/mouse interface

Pin	Type	Description
KBCLK	I/O OD	This pin contains the clock signal of the PS/2 keyboard interface.
KBDATA	I/O OD	This pin contains the data signal of the PS/2 keyboard interface.
MSCLK	I/O OD	This pin contains the clock signal of the PS/2 mouse interface.
MSDATA	I/O OD	This pin contains the data signal of the PS/2 mouse interface.

Parallel interface

Pin	Type	Description
STROBE#	I/O OD	This signal instructs to get data from the parallel peripheral device. In the EPP model, this signal becomes indicates the write cycle.
AFD#	I/O OD	When this signal becomes active, the parallel printer adds line feed into each line. In the EPP mode, this signal becomes the data strobe.
BUSY	I	This input signal indicates the peripheral device is not ready yet to receive data from the CARD-E09A.
ACK#	I	This input signal indicates data transmission is finished and the peripheral device is ready for the next data.
ERROR#	I	This input signal sent from the peripheral device to the CARD-E09A indicates an error has occurred.
PE	I	This input signal indicates the printer has successfully used the paper.
INIT#	I/O OD	This is a signal to initialize the peripheral device.
SLCTIN#	I/O OD	This signal selects the peripheral device connected to the parallel port. In the EPP mode, this signal becomes the address strobe.
SLCT	I	This input signal is a status signal sent from the peripheral device to the CARD-E09A to confirm the CARD-E09A has made a selection.
LPTD[0..7]	I/O OD	This pin serves as the data bus between the CARD-E09A and the peripheral device.

ISA bus interface

Pin	Type	Description
CA[22..23]	O	Upper 2 bits of the ISA bus address.
SBHE#	O	This signal indicates the data's upper 8 bits are valid.
IOR#	O	This signal is sent to the I/O device on the ISA bus to request for data output.
IOW#	O	This signal is sent to the I/O device on the ISA bus to request for data loading.
IOCS16#	I	This signal indicates the I/O device on the ISA bus can perform 16-bit transfer of I/O cycle to the CARD-E09A.
MEMR#	O	This signal is sent to the memory device on the ISA bus to request for data output.
MEMW#	O	This signal is sent to the memory device on the ISA bus to request for data loading.
MEMCS16#	I	This signal indicates the memory device on the ISA bus can perform 16-bit transfer of memory cycle to the CARD-E09A.
IOCHRDY	I	This is the signal for ending the ISA bus cycle. If the memory or I/O device on the ISA bus wants to lengthen the cycle, it turns this signal to LOW immediately when a valid address and command is detected. This method enables the bus cycle to be lengthened. The CARD-E09A does not end the cycle until the signal is turned to HIGH.
RESETDRV	O	This signal requests for initialization of a device on the ISA bus.
ISADATAENA#	O	This signal indicates data on the ISA bus is valid. It controls the gate of the data buffer connected between the CARD-E09A and ISA.

CRT/LCD interface

Pin	Type	Description
VSYNC	O	This is the vertical sync signal of the CRT device.
HSYNC	O	This is the horizontal sync signal of the CRT device.
R	O	This is the color signal (red) to send to the CRT device.
G	O	This is the color signal (green) to send to the CRT device.
B	O	This is the color signal (blue) to send to the CRT device.
FPDAT[0..15]	O	This is the flat panel display data.
DOTCLK	O	This is the shift clock of the display data.
EXTCLKI	I	Usually CKIO is input to CLKI of the LCD controller (SED1355). However, if the frequency of CKIO fails to meet the LCD panel specifications, this pin can be used for clock input to CLKI. The frequency of EXTCLKI is 33MHz(max.).
MOD	O	This signal contains the following functions: (1) TFT/D-TFT panel Indicates the display duration of the TFT/D-TFT panel data. Usually it is connected to the display enable (DE) of the panel. (2) Special LCD panel This is the 2nd shift clock. It is usually not used. (3) Other panel This is the communication signal.
LINE	O	This signal indicates the display start timing as well as the data latch timing in one horizontal period of the flat panel.
FRAME	O	This signal indicates the display start timing of one screen of the flat panel.
FPVEEON	O	This signal turns on the device power source of the flat panel.
FPVCCON	O	This signal turns on the logic power source of the flat panel.

AD/DA interface

Pin	Type	Description
AN5 AN4	I	This is the input pin of the AD converter.
DA1 DA0	O	This is the output pin of the DA converter.

Port/interrupt

Pin	Type	Description
PTC7/PINT7 PTC6/PINT6 PTC5/PINT5 PTC4/PINT4 PTC3/PINT3 PTC2/PINT2 PTC1/PINT1	I/O	This is a pin for the input/output port or interrupt input.

Interrupt

Pin	Type	Description
NMI	I	This is the pin for non-maskable interrupt.
IRQ[1..4]	I	This is the pin for interrupt input.

DMA

Pin	Type	Description
DREQ1# DREQ0#	I	This is the pin for input of DMA transfer request.
DACK1# DACK0#	O	This is the pin for output of the DMA transfer strobe to an external device.

Power management

Pin	Type	Description
STANDBY#	O	This signal indicates the CARD-E09A has entered the suspend mode.
PWOFF#	O	This signal permits the CARD-E09A to cut off the power.
SRBTN#	I	This is the signal to request suspend or resume of the CARD-E09A.

Timer

Pin	Type	Description
TCLK	I	This pin enables input of the clock of the timer built into SH7709A.

Reset

Pin	Type	Description
RESETP#	I	This pin is for input of request for power-on reset.
RESETM#	I	This pin is for input of request for manual reset.

Flash ROM

Pin	Type	Description
ROMDIS#	I	The flash ROM inside the CARD-E09A can be disabled by activating this signal (LOW).
CS0#	O	This is the area 0 select signal for output from SH7709A.

Power source

Pin	Type	Description
V_{CORE}	-	SH7709A core power source.
V_{CC}	-	Power voltage (3V±0.3V)
SLOT_A_V_{CC}	-	Be sure to input the same power source as PCMCIA slot A.
SLOT_B_V_{CC}	-	Be sure to input the same power source as PCMCIA slot B.
V_{BK}	-	RTC-4543 power source.
GND	-	Ground (0V)

Other

Pin	Type	Description
RESERVE	-	Make sure all of these pins are not connected. They are reserved for future use.

CompactFlash connector

Pin	Type	Description
A[0..10]	O	Address bus
D[0..15]	I/O	Data bus
CCE1#	O	This is a CompactFlash select signal and indicates the even address is valid.
CCE2#	O	This is a CompactFlash select signal and indicates the odd address is valid.
CREG#	O	This is the signal for selecting the attribute memory or the common memory. When this signal is LOW, the attribute memory is accessed. The signal becomes LOW during I/O card access.
COE#	O	This is the memory read strobe signal.
CWE#	O	This is the memory write strobe signal.
CIORD#	O	This is the I/O read strobe signal.
CIOWR#	O	This is the I/O write strobe signal.
CWP_IOIS16#	I	In the memory card mode, this signal indicates the state of the write protect switch of the card. In the I/O card mode, it indicates whether the I/O port on the interface allows 16-bit access.
CRDY_IREQ#	I	In the memory card mode, this is the ready signal from the card. In the I/O card mode, this is the interrupt request signal from the card.
CWAIT#	I	This is the signal the CompactFlash card uses to delay ending the current cycle. The CARD-E09A does not end the cycle until this signal becomes HIGH.
CRESET	O	This signal initializes the CompactFlash card.
CBVD1_STSCHG#	I	In the memory card mode, this signal indicates the state of the voltage of the battery on the card. In the I/O card mode, this signal indicates the state of the card, such as ready/busy, write-protect.
CVCC	-	This is the power source of the CompactFlash card. This power source is same as VCC.
GND	-	Ground (0V)

5 FUNCTION DESCRIPTION

This chapter describes the basic functions of the CARD-E09A.
For detailed information on SH7709A and SED1355, refer to their respective manuals.

5.1 Memory map

Figure 5-1 is SH7709A memory map for the CARD-E09A.

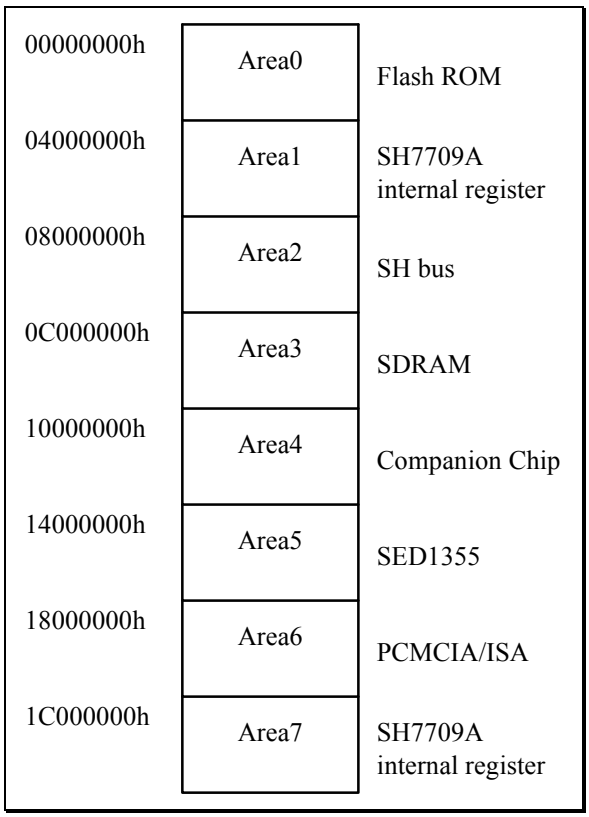


Figure 5-1 CARD-E09A Memory Map

Figure 5-2 indicates the composition of area 4. Area 4 uses Companion Chip.

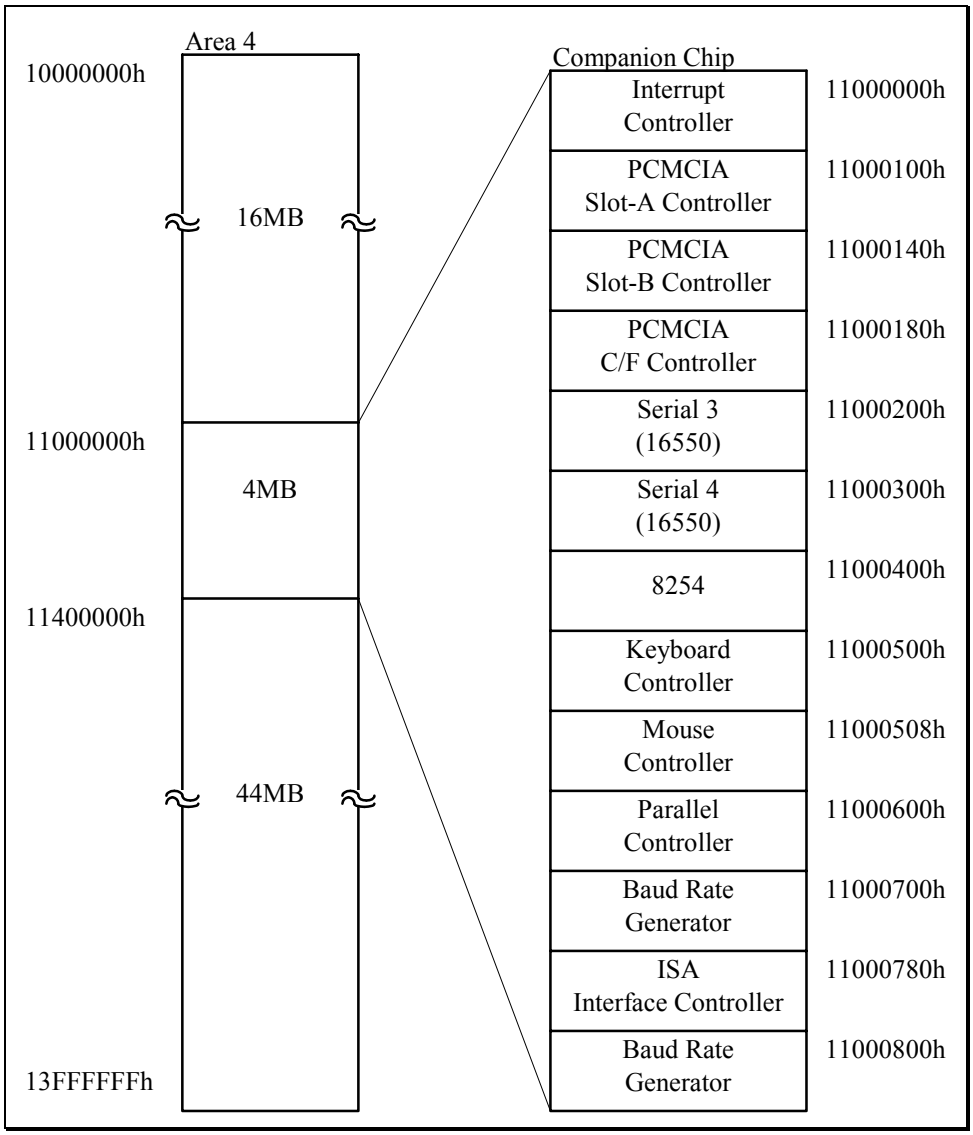


Figure 5-2 Area 4 Memory Map

Figure 5-3 indicates the composition of area 5. Area 5 uses SED1355.

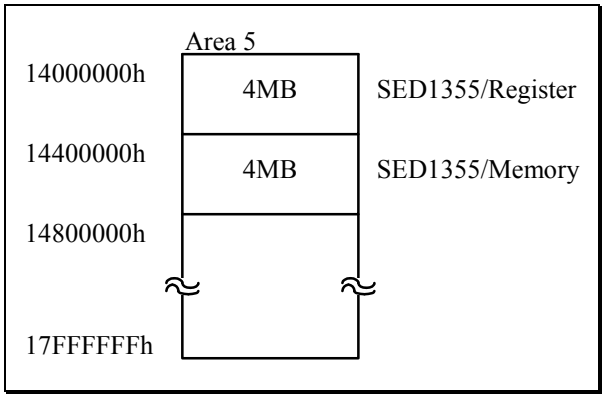


Figure 5-3 Area 5 Memory Map

Figure 5-4 indicates the composition of area 6. PCMCIA provides three slots: Slot-A, Slot-B and CompactFlash. The memory space of each of the slots can be selected from PCMCIA-0, -1, and -2 as shown in the illustration. The I/O space can be selected from PCMCIA-4, -5, or -6. For memory space and I/O space of the ISA bus, each of them is fixed in the ranges from 1B800000h to 1BBFFFFFh and from 1BC00000h to 1BFFFFFFh, respectively.

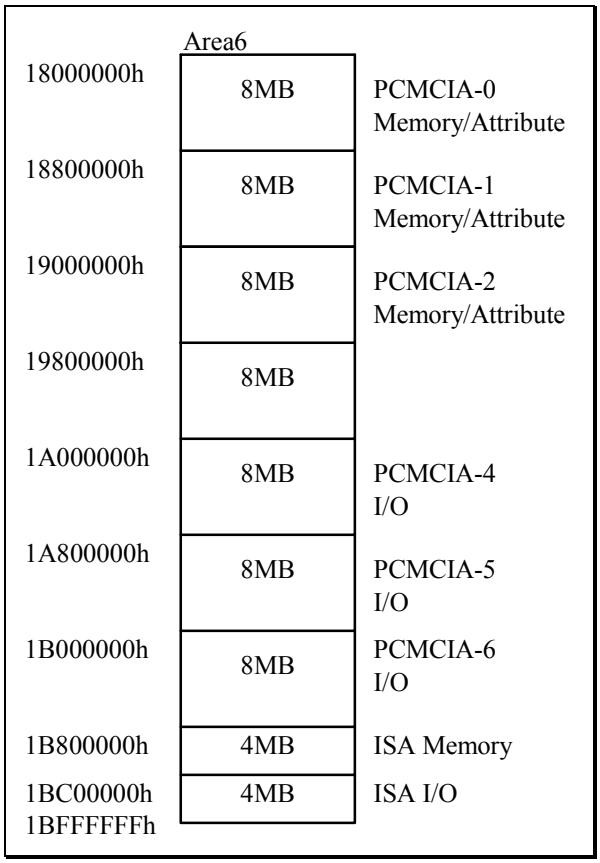


Figure 5-4 Area 6 Memory Map

The settings of the wait number of each area of SH7709A are listed below.

For all areas

Endian	Little Endian

Area 0 setting

Access method	Normal memory
Bus width	16 bits (fixed by hardware)
Wait number	4 wait insertion
Idle cycle	1 idle cycle insertion

Area 2 setting (initial value)

Access method	Normal memory
Bus width	16 bits
Wait number	3 wait insertion
Idle cycle	1 idle cycle insertion

Area 3 setting

Access method	SDRAM
Bus width	32 bits
CAS# latency	2
Idle cycle	1 idle cycle insertion

Area 4 setting

Access method	Normal memory
Bus width	16 bits
Wait number	2 wait insertion
Idle cycle	1 idle cycle insertion

Area 5 setting

Access method	Normal memory
Bus width	16 bits
Wait number	2 wait insertion
Idle cycle	1 idle cycle insertion

Area 6 setting

Access method	PCMCIA
Bus width	16 bits
Wait number	2 wait insertion
Idle cycle	2 idle cycle insertion
Address-OE#/WE# asserted delay	1.5 cycle delay
OE#/WE# negate address delay	3.5 cycle delay

5.2 SDRAM

The CARD-E09A comes with either 16 MB (64 Mbits, 4Mx16-bit, 2pcs.) or 32 MB (128 Mbits, 8Mx16-bit, 2pcs.) of SDRAM built in. This SDRAM is connected to area 3 of SH7709A, and controlled by BSC (bus state controller).

5.3 Flash ROM

The CARD-E09A has 256 KB (2Mbit, 128Kx16 bits) of flash ROM built in. This flash ROM is connected to area 0 of SH7709A, and controlled by BSC (bus state controller). By turning ROMDIS# to LOW, the built-in flash ROM's mapping can be changed from area 0 to the leading 8 MB of area 4. In this situation, because area 0is now available for use outside the CARD-E09A, CS0# and RD# can be used to connect to external ROM so that the external ROM can start the CARD-E09A.

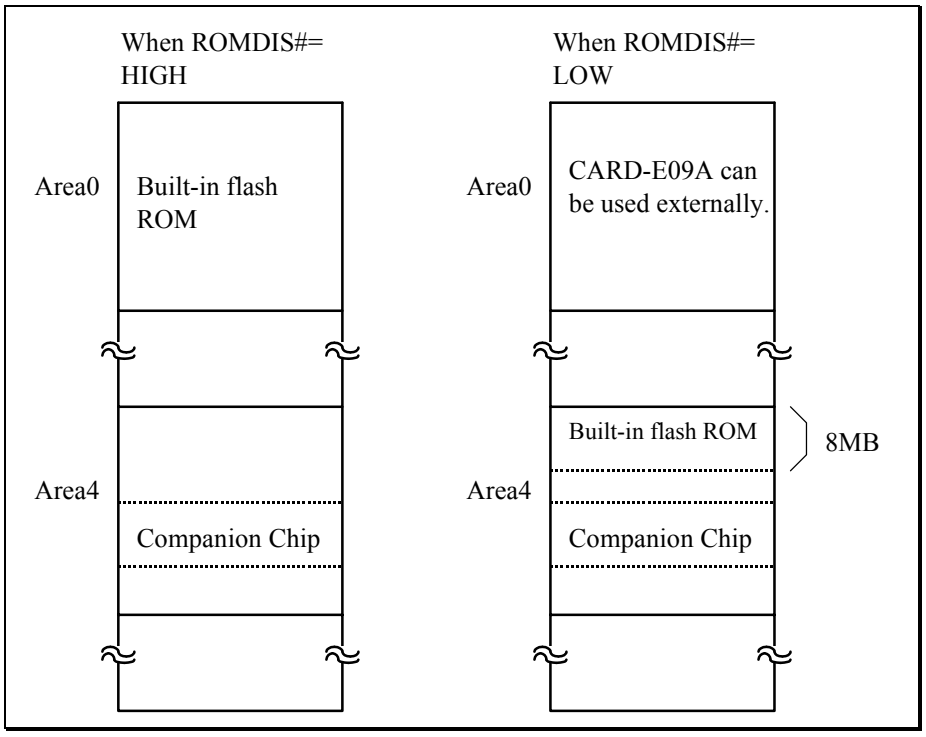


Figure 5-5 Flash ROM Mapping

5.4 Interrupt

There are five causes of SH7709A interrupt: NMI, IRQ, IRL, PINT, and SH7709A internal module. Figure 5-6 shows that the CARD-E09A supports only NMI, IRQ, PINT, and SH7709A internal module. The Companion Chip interrupt request is entered into IRQ0. Interrupt requests that can be used outside the CARD-E09A are NMI, IRQ[1..4] and PINT[1..7].

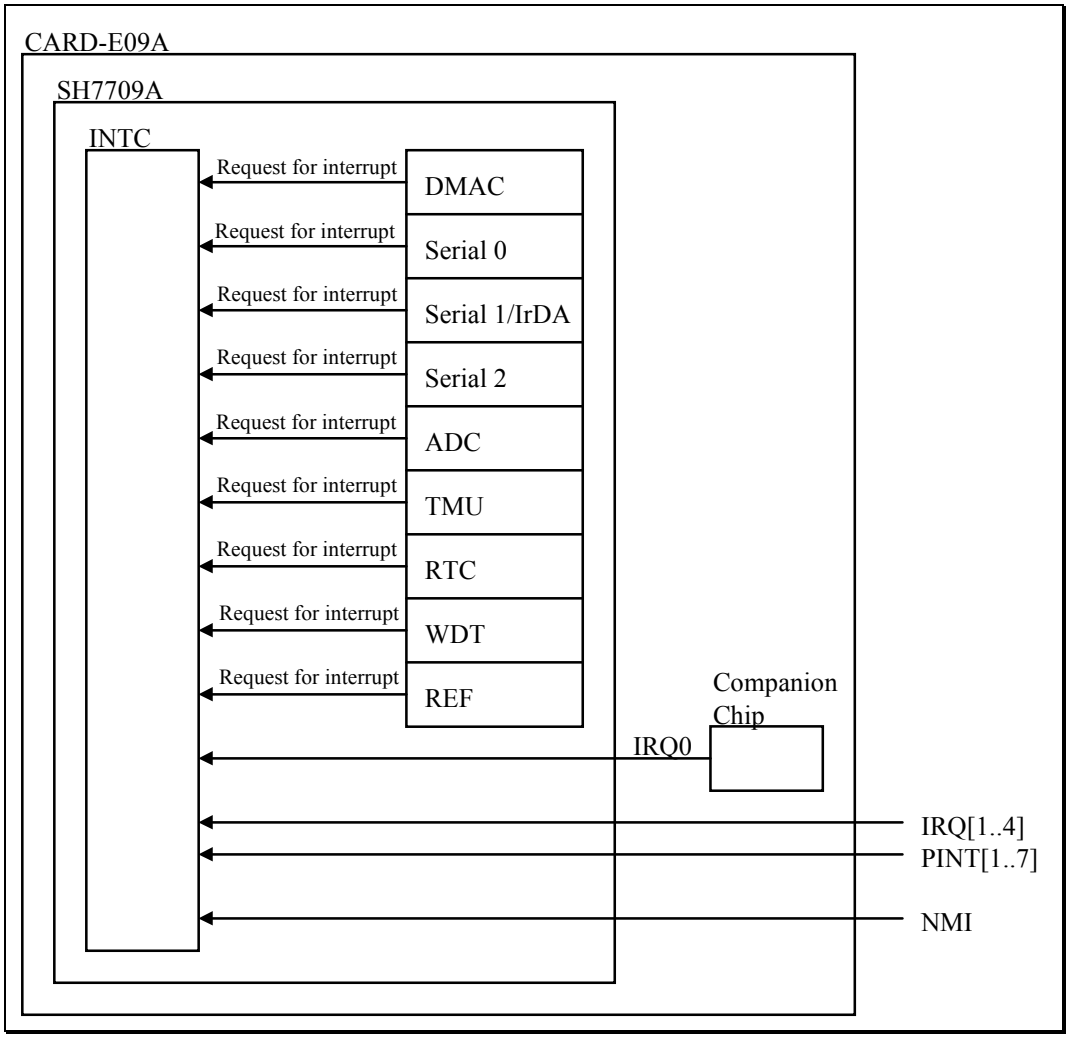


Figure 5-6 Interrupt Block Diagram

5.4.1 IRQ0

The interrupt request inside the Companion Chip is output to IRQ0 via the Interrupt Controller inside Companion Chip. This interrupt may be triggered by any of the following sixteen causes.

1. 8254 Ch0 (OUT0)
2. 8254 Ch1 (OUT1)
3. 8254 Ch2 (OUT2)
4. Parallel
5. Serial 3
6. Serial 4
7. PCMCIA Slot-A Status Change
8. PCMCIA Slot-B Status Change
9. PCMCIA CompactFlash Status Change
10. PCMCIA Slot-A IREQ

11. PCMCIA Slot-B IREQ
12. PCMCIA CompactFlash IREQ
13. Keyboard Data Receiving Complete
14. Keyboard Data Transmitting Complete
15. Mouse Data Receiving Complete
16. Mouse Data Transmitting Complete

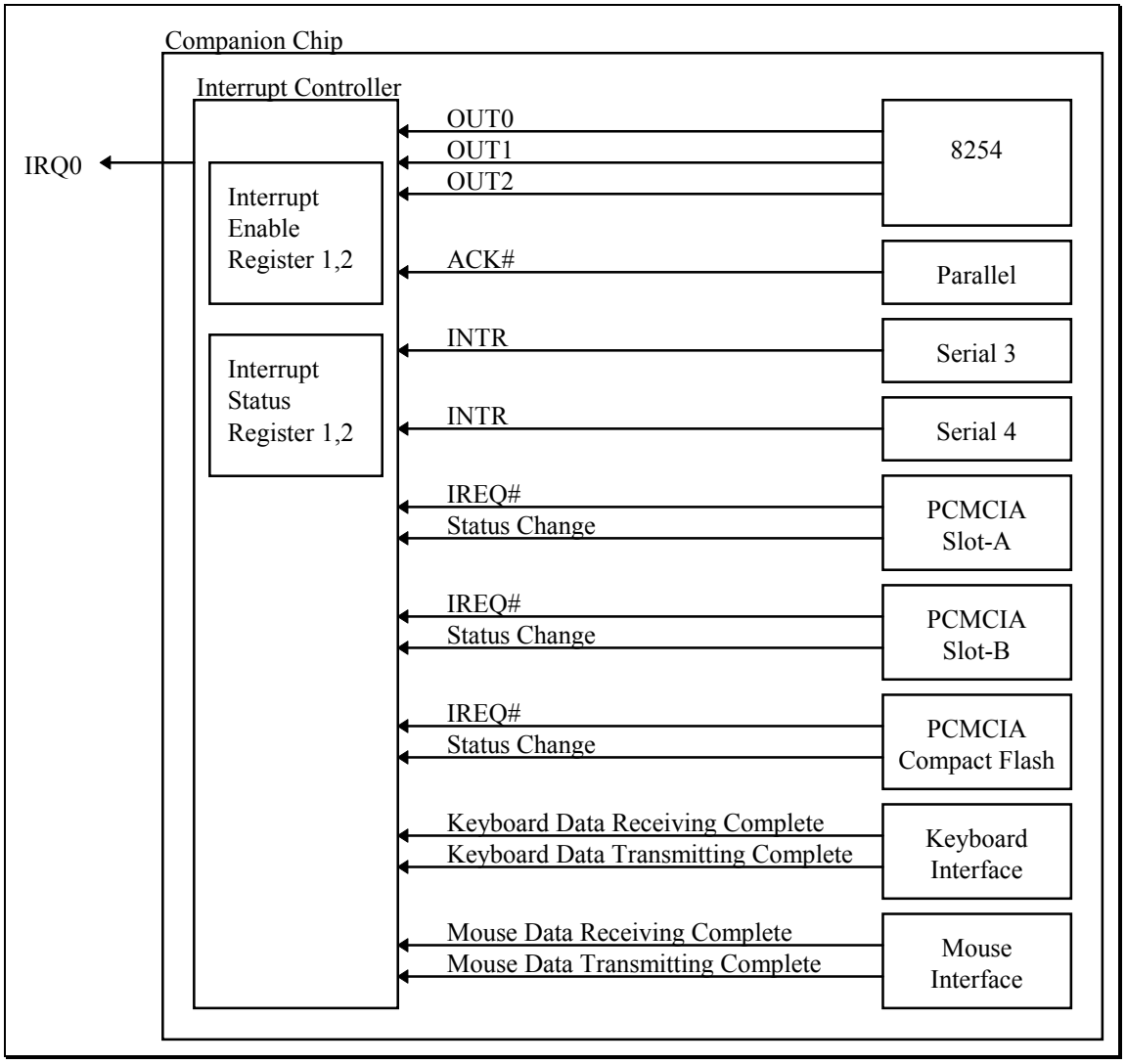


Figure 5-7 IRQ0 Block Diagram

When an interrupt occurs, be sure to use the Interrupt Status Registers 1 and 2 to determine the cause of the interrupt. Because these interrupts are level interrupts, the cause of the interrupt must be cleared in the interrupt handler. For IRQ0 of SH7709A, set it up at "Interrupt Detect at LOW Level".

5.4.2 Registers

Interrupts from the Companion Chip are controlled by the following registers.

Interrupt Enable Register 1

Address = 11000000h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CF IREQ Enable	CF Status Change Interrupt Enable	Serial 4 Interrupt Enable	Serial 3 Interrupt Enable	Parallel Port Interrupt Enable	8254 Ch2 Interrupt Enable	8254 Ch1 Interrupt Enable	8254 Ch0 Interrupt Enable

bit	Name	R/W	Description
0	8254 Ch0 Interrupt Enable	R/W	This bit enables 8254 Ch0 interrupt (raised edge of OUT0).
1	8254 Ch1 Interrupt Enable	R/W	This bit enables 8254 Ch1 interrupt (raised edge of OUT1).
2	8254 Ch2 Interrupt Enable	R/W	This bit enables 8254 Ch2 interrupt (raised edge of OUT2).
3	Parallel Port Interrupt Enable	R/W	This bit enables parallel port interrupt (edge when ACK# is raised).
4	Serial 3 Interrupt Enable	R/W	This bit enables interrupt at Serial 3. The INT signal of Serial 3 becomes the interrupt signal.
5	Serial 4 Interrupt Enable	R/W	This bit enables interrupt at Serial 4. The INT signal of Serial 4 becomes the interrupt signal.
6	CF Status Change Interrupt Enable	R/W	This bit enables use of interrupt caused by change in the state of the CompactFlash card. The logical sum of bits 2 and 0 of Card Status Change Register CF becomes the interrupt signal.
7	CF IREQ Enable	R/W	This bit enables interrupt based on the CompactFlash card. The RDY_IREQ# signal of the CompactFlash card becomes the interrupt signal.

Interrupt Enable Register 2

Address = 11000002h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Mouse Data Transmitting Complete Interrupt Enable	Mouse Data Receiving Complete Interrupt Enable	Keyboard Data Transmitting Complete Interrupt Enable	Keyboard Data Receiving Complete Interrupt Enable	Slot-B IREQ Enable	Slot-B Status Change Interrupt Enable	Slot-A IREQ Enable	Slot-A Status Change Interrupt Enable

bit	Name	R/W	Description
0	Slot-A Status Change Interrupt Enable	R/W	This bit enables interrupt based on change of the state of Slot-A. The logical sum of bits 3 to 0 of Card Status Change Register A becomes the interrupt signal.
1	Slot-A IREQ Enable	R/W	This bit enables interrupt based on Slot-A. The RDY_IREQ# signal of Slot-A becomes the interrupt signal.
2	Slot-B Status Change Interrupt Enable	R/W	This bit enables interrupt based on change of the state of Slot-B. The logical sum of bits 3 to 0 of Card Status Change Register B becomes the interrupt signal.
3	Slot-B IREQ Enable	R/W	This bit enables interrupt based on Slot-B. The RDY_IREQ# signal of Slot-B becomes the interrupt signal.
4	Keyboard Data Receiving Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data reception from the keyboard is finished.The Keyboard Data Receiving Completed flag becomes the interrupt signal.
5	Keyboard Data Transmitting Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data transmission to the keyboard is finished. The Keyboard Data Transmitting Completed flag becomes the interrupt signal.
6	Mouse Data Receiving Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data reception from the mouse is finished. The Mouse Data Receiving Completed flag becomes the interrupt signal.
7	Mouse Data Transmitting Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data transmission to the mouse is finished. The Mouse Data Transmitting Completed flag becomes the interrupt signal.

Interrupt Status Register 1

Address = 11000004h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CF IREQ	CF Status Change Interrupt	Serial 4 Interrupt	Serial 3 Interrupt	Parallel Port Interrupt	8254 Ch2 Interrupt	8254 Ch1 Interrupt	8254 Ch0 Interrupt

bit	Name	R/W	Description
0	8254 Ch0 Interrupt	R/W	This bit indicates there is an interrupt request (raised edge of OUT0) at 8254 Ch0. The interrupt request can be removed by writing "0" to this bit.
1	8254 Ch1 Interrupt	R/W	This bit indicates there is an interrupt request (raised edge of OUT1) at 8254 Ch1. The interrupt request can be removed by writing "0" to this bit.
2	8254 Ch2 Interrupt	R/W	This bit indicates there is an interrupt request (raised edge of OUT2) at 8254 Ch2. The interrupt request can be removed by writing "0" to this bit.
3	Parallel Port Interrupt	R/W	This bit indicates there is an interrupt request (raised edge of ACK#) at the parallel port. The interrupt request can be removed by writing "0" to this bit.
4	Serial 3 Interrupt	R	This bit indicates there is an request for interrupt at Serial 3.
5	Serial 4 Interrupt	R	This bit indicates there is an request for interrupt at Serial 4.
6	CF Status Change Interrupt	R	This bit indicates there is an request for interrupt based on change of the state of the CompactFlash card.
7	CF IREQ	R	This bit indicates there is an request for interrupt based on the CompactFlash card.

Interrupt Status Register 2

Address = 11000006h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Mouse Data Transmitting Complete Interrupt	Mouse Data Receiving Complete Interrupt	Keyboard Data Transmitting Complete Interrupt	Keyboard Data Receiving Complete Interrupt	Slot-B IREQ	Slot-B Status Change Interrupt	Slot-A IREQ	Slot-A Status Change Interrupt

bit	Name	R/W	Description
0	Slot-A Status Change Interrupt	R	This bit indicates there is an request for interrupt based on change of the state of Slot-A.
1	Slot-A IREQ	R	This bit indicates there is an request for interrupt based on Slot-A.
2	Slot-B Status Change Interrupt	R	This bit indicates there is an request for interrupt based on change of the state of Slot-B.
3	Slot-B IREQ	R	This bit indicates there is an request for interrupt based on Slot-B.
4	Keyboard Data Receiving Complete Interrupt	R	This bit indicates there is an request for interrupt which occurs when data reception from the keyboard is finished.
5	Keyboard Data Transmitting Complete Interrupt	R	This bit indicates there is an request for interrupt which occurs when data transmission to the keyboard is finished.
6	Mouse Data Receiving Complete Interrupt	R	This bit indicates there is an request for interrupt which occurs when data reception from the mouse is finished.
7	Mouse Data Transmitting Complete Interrupt	R	This bit indicates there is an request for interrupt which occurs when data transmission to the mouse is finished.

Even if interrupt is prohibited with Interrupt Enable Registers 1 and 2, if an interrupt occurs, the bits for Interrupt Status Registers 1 and 2 are set to "1".

5.5 DMA

SH7709A has an internal DMA controller with 4 channels. Request for DMA transfer to channel 0 and channel 1 can be made from outside. As this external transfer request signal and its acknowledge signal are connected to the connectors of the CARD-E09A, the external device can directly send transfer request to SH7709A.

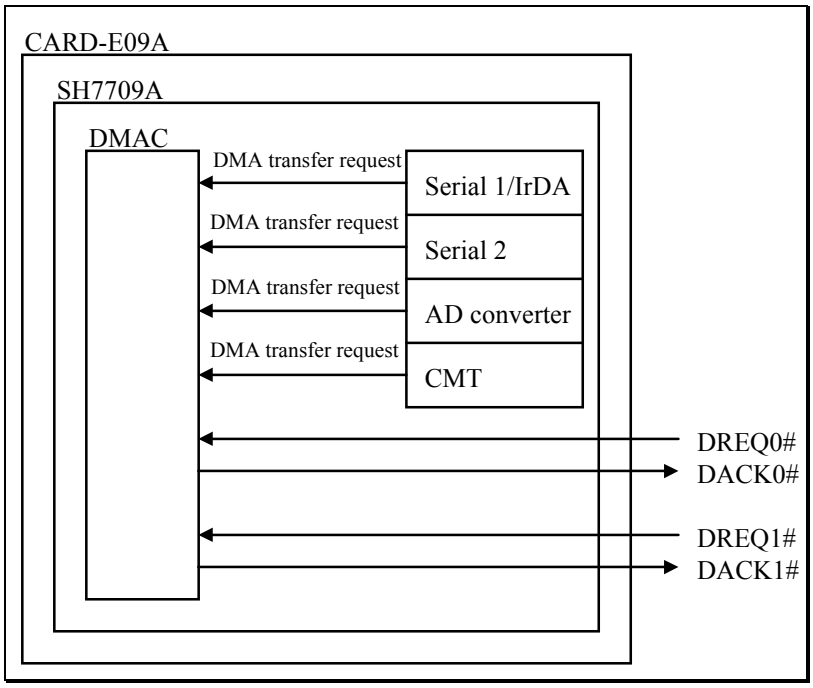


Figure 5-8 DMA Block Diagram

5.6 Timer

The CARD-E09A comes with a timer (TMU) for the three channels inside SH7709A and a timer (8254) for the three channels inside the Companion Chip.

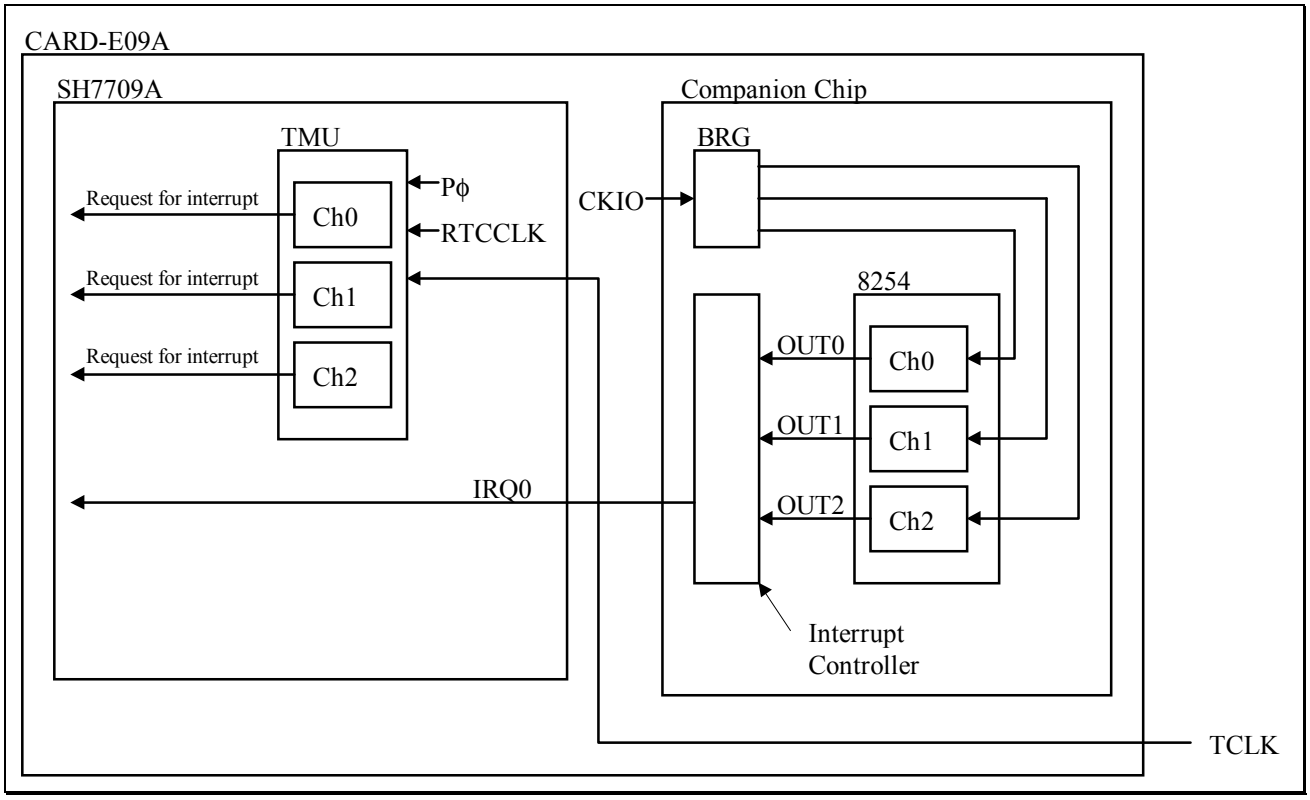


Figure 5-9 Timer Block Diagram

The 8254 clock inside the Companion Chip is generated by BRG (Baud Rate Generator). (For detailed information on BRG, see the "5.18 Baud Rate Generator" section.)

The 8254 address is as follows.

Register	Address
Counter 0	11000400h
Counter 1	11000402h
Counter 2	11000404h
Control Word Register	11000406h

5.7 RTC

The CARD-E09A contains an RTC (real time clock) built into SH7709A, as well as the RTC-4543 which can be backed up.

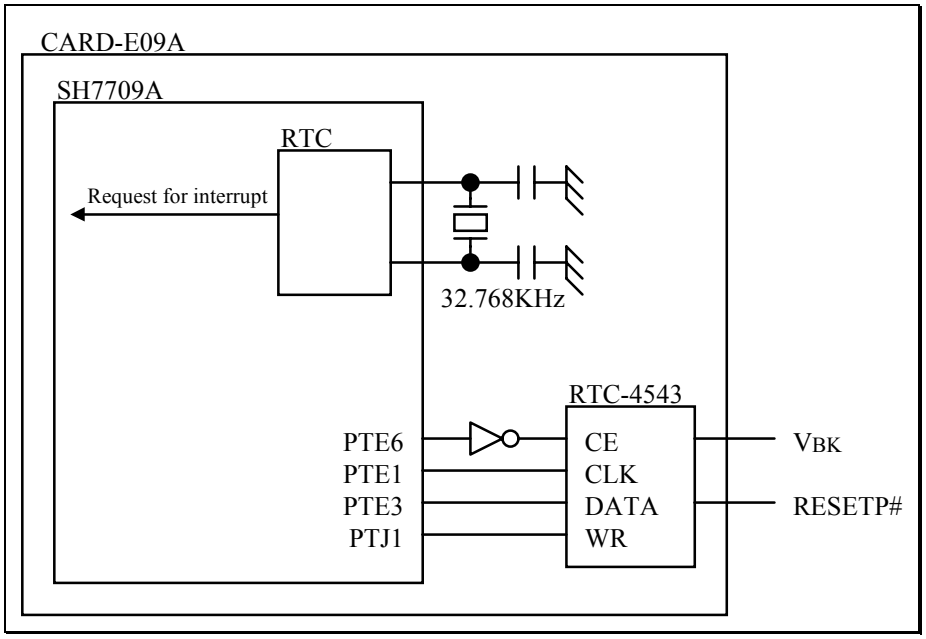


Figure 5-10 RTC Block Diagram

Because the RTC built into SH7709A uses VCC as its power source, it does not run when the power is turned off. On the other hand, RTC-4543 uses VBK as its power source and therefore can continue to run as long as power is supplied to VBK, even when VCC is turned off. When supplying power to the CARD-E09A (while operating), be sure to supply the same power as VCC. When backing up the RTC-4543, be careful with the timing so that the backup power (lithium battery, etc.) is supplied as the power of the CARD-E09A is turned off.
RESETP# is used for separating, electrically, the RTC-4543 from other circuitries. For this reason, when the RTC-4543 runs on the backup power, RESETP# must be set to LOW.

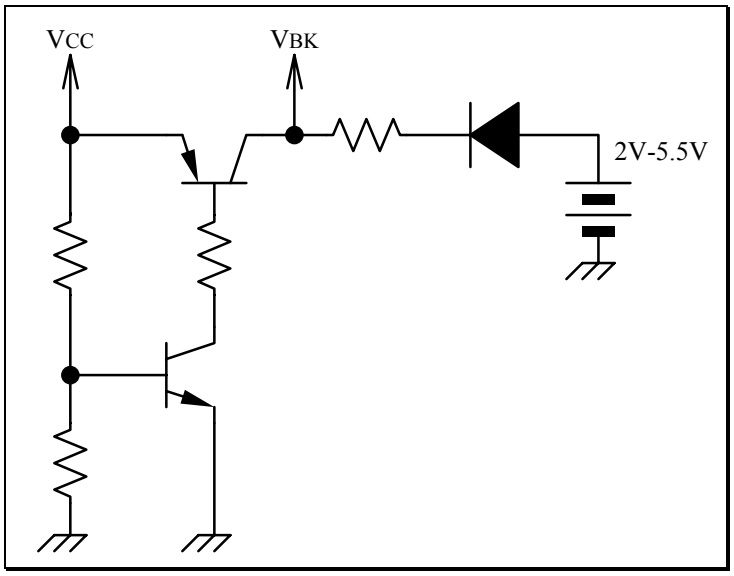


Figure 5-11 VBK Power Switching Circuitry Example

5.8 Power Management

This section describes the low power consumption mode supported by the CARD-E09A.

5.8.1 SH7709A

SH7709A has four low power consumption modes: sleep mode, standby mode, module standby mode, and hardware standby mode. The CARD-E09A supports all of the modes except the hardware standby mode.

5.8.2 SDRAM

SDRAM mounted on the CARD-E09A supports the self refresh function. By setting SH7709A's BSC (bus state controller) to use self refresh, the consumed current of SDRAM can be reduced.
In the standby mode, because SH7709A's clock stops, the self refresh must be used to keep the data in SDRAM. Simply setting SH7709A to the standby mode does not enable self refresh. Self refresh must be enabled before the standby mode is set. Once self refresh is enabled, all access to SDRAM becomes impossible. For this reason, these programs must be run from ROM.

5.8.3 SED1355

Display off, software-based suspend, and hardware-based suspend supported by the SED1355 can be used. To use hardware-based suspend, LOW must be output from PTE7 of SH7709A.
FRAME and LINE signals of SED1355 become inactive. On TFT panels, etc., when these signals are in active LOW, they will be driven to HIGH even in the low power consumption mode. Because the power of the LCD panel is turned off in the low power consumption mode, problem will occur, solution based on hardware or software must be formulated.
(For detailed information on SED1355's low power consumption mode and its problem and solution, refer to the SED1355 manual.)
Turning PTD3 of SH7709A to HIGH in effect turns off the IREF fixed current circuity of SED1355. For CRT display off, software-based suspend, or hardware-based suspend, turn PTD3 to HIGH.

5.8.4 Companion Chip

In the Companion Chip, the following registers can be used to stop the clock of each of the modules.

Power Management Register

Address = 11000700h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8254 Ch2 Clock Standby	8254 Ch1 Clock Standby	8254 Ch0 Clock Standby	PCMCIA/ CompactFlash Interface Standby	Mouse Controller Standby	Keyboard Controller Standby	Serial 4 Standby	Serial 3 Standby

bit	Name	R/W	Description
0	Serial 3 Standby	R/W	This bit stops the clock of Serial 3.
1	Serial 4 Standby	R/W	This bit stops the clock of Serial 4.
2	Keyboard Controller Standby	R/W	This bit stops the clock of the keyboard controller.
3	Mouse Controller Standby	R/W	This bit stops the clock of the mouse controller.
4	PCMCIA/CompactFlash Interface Standby	R/W	This bit stops the clock of the PCMCIA/CompactFlash controller.
5	8254 Ch0 Clock Standby	R/W	This bit stops the clock of 8254 Ch0.
6	8254 Ch1 Clock Standby	R/W	This bit stops the clock of 8254 Ch1.
7	8254 Ch2 Clock Standby	R/W	This bit stops the clock of 8254 Ch2.

To enter or exit SH7709A's standby mode, set the Companion Chip as follows:
To enter the standby mode:

① Use Power Management Register to stop the clocks of all of the following: Serial 3, Serial 4, keyboard controller, mouse controller, PCMCIA/CompactFlash controller, 8254 Ch0, 8254 Ch1, and 8254 Ch2.
② Use SCP5 of SH7709A to output the LOW signal. This causes the Companion Chip to enter the suspend mode. From this moment on, the Companion Chip can no longer be accessed.
③ Use the SLEEP command to change SH7709A to the standby mode.

To exit the standby mode

① Use SCP5 of SH7709A to output the HIGH signal and cause the Companion Chip to exit the suspend mode.
② Restart the clocks of any of the following as required: Serial 3, Serial 4, keyboard controller, mouse controller, PCMCIA/CompactFlash controller, 8254 Ch0, 8254 Ch1, and 8254 Ch2.

5.8.5 Suspend/resume

The CARD-E09A can resume to where it was before the suspend operation. In a suspend operation, all of the CARD-E09A devices enter the low power consumption mode and only a minimum amount of power is used to keep the system going. The suspend/resume operations require support from software. The following example illustrates how to implement the functions, including use of software.

<<Entering the suspend mode>>
Here the SRBTN# pin acts as a trigger to entering the suspend mode. Because the SRBTN# pin of the CARD-E09A is connected to PTC0/PINT0 of SH7709A, PINTO port interrupt occurs when the SRBTN# pin becomes LOW. When this interrupt occurs, the software must perform the following tasks.

- Turn SED1355 into the suspend mode using either software or hardware.
  Turn PTD3 of SH7709A to HIGH, and turn off the IREF fixed current circuitry.
- Perform task on the PCMCIA card as required.
  Turn off the power of the PCMCIA interface.
- Set up the port, registers, etc.
- Stop clocks of all modules inside the Companion Chip.
  Turn SCPT5 of SH7709A to LOW, and turn the Companion Chip into the suspend mode
- Move to ROM execution and turn SDRAM into the self refresh mode.

After the above tasks are performed, run the SLEEP command of SH7709A to turn the CARD-E09A into the suspend mode and the STANDBY# pin to LOW.

<<Resume>>
The SRBTN# pin also acts as a trigger to recovering from the suspend mode. Like entering the suspend mode, when the SRBTN# pin becomes LOW, the PINT0 port interrupt occurs and SH7709A returns from the suspend mode. At this moment, since SDRAM is in the self refresh mode, the interrupt handling routine must be executed from ROM. When this interrupt occurs, the software must perform the following tasks.

- Turn SDRAM to the auto refresh mode.
  Subsequently execution from RAM becomes possible.
- Turn SCPT5 of SH7709A to HIGH, and restore the Companion Chip from the suspend mode.
  Re-start the clocks of all modules inside the Companion Chip.
- Set up the port, registers, etc.
- Turn on the power of the PCMCIA interface.
  Perform task on the PCMCIA card as required.
- Turn PTD3 of SH7709A to HIGH, and turn on the IREF fixed current circuitry.
  Restore SED1355 from the suspend mode.

States of the pins during a suspend operation
The following table lists the states of the pins of the CARD-E09A during a suspend operation. Note that by using the registers, it is possible to change the state of some pins during a suspend operation.

Type	Indicates types of pins. I : Input O : Output Tri : 3-State output I/O : Bi-directional I/OD : Bi-directional open-drain output Power : Power
Termination	Indicates the internal terminator resistance of the pin. HOLD : Has bus holder xxPU : Pulled-up at xx Ω resistance xxPD : Pulled-down at xx Ω resistance External : Pull-up resistance outside the CARD-E09A is required.
Reset Suspend	Indicates state of pin during a reset or suspend operation. Input : The state is input. It is necessary to input HIGH or LOW from outside the CARD-E09A and then check the input level. However, if the CARD-E09A contains a bus holder or pull-up resistance, then such checking is not required. Hi-Z : The state is input. There is no need to check the input level. Input(High) : Input of HIGH is required. Input(Low) : Input of LOW is required. High : Outputs HIGH. Low : Outputs LOW. Drive : Outputs HIGH or LOW. Z : High impedance is in effect. Off : Be sure to turn off power to the PCMCIA interface.

Table 5-1 Pin Status

Pin	Group	Name	Type	Termination	Reset	Suspend
1	Power	GND	Power	-	-	-
2	Slot_B	BCD1#	I	100KPU	Input	Input
3		BCE1#	Tri	-	Z	Z
4		BCE2#	Tri	-	Z	Z
5		BOE#	Tri	-	Z	Z
6		SLOT_B_VCC	Power	-	Off	Off
7		BVS1	I	100KPU	Input	Input
8		BIORD#	Tri	-	Z	Z
9		BIOWR#	Tri	-	Z	Z
10		BWE#	Tri	-	Z	Z
11		BRDY_IRQ#	I	100K/60KPU	Hi-Z	Hi-Z
12		BVS2	I	100KPU	Input	Input
13		BRESET	Tri	-	Z	Z
14		BWAIT#	I	100K/60KPU	Hi-Z	Hi-Z
15	Power	VCC	Power	-	-	-
16	Slot_B	BREG#	Tri	-	Z	Z
17		BBVD2_SPKR	I	100K/60KPU	Hi-Z	Hi-Z
18		BBVD1_STSCHG#	I	100K/60KPU	Hi-Z	Hi-Z
19		BWP_IOIS16#	I	100K/60KPU	Hi-Z	Hi-Z
20	Power	GND	Power	-	-	-
21	Slot_B	BCD2#	I	100KPU	Input	Input
22		BADRENA#	O	-	High	High
23		BDATAENA#	O	-	High	High
24		BVPPPGM	O	-	Low	Low
25		BVPPVCC	O	-	Low	Low
26		BVCC5#	O	-	High	High
27		BVCC3#	O	-	High	High
28	KB/MS	KBCLK	I/OD	External	Low	Input or Low(*4)
29		KBDATA	I/OD	External	Low	Input or Low(*4)
30		MSCLK	I/OD	External	Low	Input or Low(*4)
31		MSDATA	I/OD	External	Low	Input or Low(*4)
32	ISA	RESETDRV	O	-	High	Low
33		IOCHRDY	I	External	Input	Input
34		IOW#	O	-	High	High
35		IOR#	O	-	High	High
36		MEMCS16#	I	External	Input	Input
37		SBHE#	O	-	Drive	Drive
38		IOCS16#	I	External	Input	Input
39		MEMR#	O	-	High	High
40		MEMW#	O	-	High	High
41	Power	GND	Power	-	-	-
42	ISA	ISADATAENA#	O	-	High	High
43	Serial 4	RI4#	I	50KPU	Input	Input
44		DTR4#	O	-	Drive	Drive
45	Power	VCORE	Power	-	-	-
46		VCORE	Power	-	-	-
47	Serial 4	CTS4#	I	50KPU	Input	Input
48		TXD4	O	-	High	High
49		RTS4#	O	-	Drive	Drive
50		RXD4	I	50KPU	Input	Input
51		DSR4#	I	50KPU	Input	Input
52		DCD4#	I	50KPU	Input	Input
53	Serial 3	RI3#	I	50KPU	Input	Input
54		DTR3#	O	-	Drive	Drive
55		CTS3#	I	50KPU	Input	Input
56		TXD3	O	-	Drive	Drive
57		RTS3#	O	-	Drive	Drive
58		RXD3	I	50KPU	Input	Input
59		DSR3#	I	50KPU	Input	Input
60		DCD3#	I	50KPU	Input	Input

Pin	Group	Name	Type	Termination	Reset	Suspend
61	Power	GND	Power	-	-	-
62	SH-Bus	CKIO	O	-	Drive	Drive
63	Timer	TCLK	I	100KPU	Input	Input
64	SH-Bus	RESETP#	I	-	Input(Low)	Input(High)
65		RESETM#	I	-	Input(High)	Input(High)
66		WAIT#	I	4.7KPU	Input	Input
67		CS2#	O	-	High	High
68		CS0#	O	-	High	High
69		RD/WR#	O	-	High	High
70		WE1#	O	-	High	High
71		WE0#	O	-	High	High
72		RD#	O	-	High	High
73		BS#	O	-	High	High
74		A25	O	HOLD	Z	Low
75		A24	O	HOLD	Z	Low
76		A23	O	HOLD	Z	Low
77	Power	VCC	Power	-	-	-
78	SH-Bus	A22	O	HOLD	Z	Low
79		A21	O	-	Z	Low
80		A20	O	-	Z	Low
81		A19	O	-	Z	Low
82	Power	GND	Power	-	-	-
83	SH-Bus	A18	O	-	Z	Low
84		A17	O	-	Z	Low
85		A16	O	-	Z	Low
86		A15	O	-	Z	Low
87		A14	O	-	Z	Low
88		A13	O	-	Z	Low
89		A12	O	-	Z	Low
90		A11	O	Hold	Z	Low
91		A10	O	Hold	Z	Low
92		A9	O	Hold	Z	Low
93		A8	O	Hold	Z	Low
94		A7	O	Hold	Z	Low
95		A6	O	Hold	Z	Low
96		A5	O	Hold	Z	Low
97		A4	O	Hold	Z	Low
98		A3	O	Hold	Z	Low
99		A2	O	Hold	Z	Low
100		A1	O	Hold	Z	Low
101	Power	GND	Power	-	-	-
102	SH-Bus	A0	O	Hold	Z	Low
103		D15	I/O	100KPU	Input	Input
104		D14	I/O	100KPU	Input	Input
105		D13	I/O	100KPU	Input	Input
106	Power	VCC	Power	-	-	-
107	SH-Bus	D12	I/O	100KPU	Input	Input
108		D11	I/O	100KPU	Input	Input
109		D10	I/O	100KPU	Input	Input
110		D9	I/O	100KPU	Input	Input
111		D8	I/O	100KPU	Input	Input
112		D7	I/O	HOLD	Input	Input
113		D6	I/O	HOLD	Input	Input
114		D5	I/O	HOLD	Input	Input
115		D4	I/O	HOLD	Input	Input
116		D3	I/O	HOLD	Input	Input
117		D2	I/O	HOLD	Input	Input
118		D1	I/O	HOLD	Input	Input
119		D0	I/O	HOLD	Input	Input
120	Power	GND	Power	-	-	-
121		GND	Power	-	-	-

Pin	Group	Name	Type	Termination	Reset	Suspend
122	Slot_A	ACD1#	I	100KPU	Input	Input
123		ACE1#	Tri	-	Z	Z
124		ACE2#	Tri	-	Z	Z
125		AOE#	Tri	-	Z	Z
126		SLOT_A_VCC	Power	-	Off	Off
127		AVS1	I	100KPU	Input	Input
128		AIORD#	Tri	-	Z	Z
129		AIOWR#	Tri	-	Z	Z
130		AWE#	Tri	-	Z	Z
131		ARDY_IRQ#	I	100K/60KPU	Hi-Z	Hi-Z
132		AVS2	I	100KPU	Input	Input
133		ARESET	Tri	-	Z	Z
134		AWAIT#	I	100K/60KPU	Hi-Z	Hi-Z
135	Power	VCC	Power	-	-	-
136	Slot_A	AREG#	Tri	-	Z	Z
137		ABVD2_SPKR	I	100K/60KPU	Hi-Z	Hi-Z
138		ABVD1_STSCHG#	I	100K/60KPU	Hi-Z	Hi-Z
139		AWP_IOIS16#	I	100K/60KPU	Hi-Z	Hi-Z
140	Power	GND	Power	-	-	-
141	Slot_A	ACD2#	I	100KPU	Input	Input
142		AADRENA#	O	-	High	High
143		ADATAENA#	O	-	High	High
144		AVPPPGM	O	-	Low	Low
145		AVPPVCC	O	-	Low	Low
146		AVCC5#	O	-	High	High
147		AVCC3#	O	-	High	High
148	PCMCIA	CA25	O	-	Drive	Drive
149		CA24	O	-	Drive	Drive
150	PCMCIA/ISA	CA23	O	-	Drive	Drive
151	Parallel	SLCT	I	External	Input	Input
152		PE	I	External	Input	Input
153		BUSY	I	External	Input	Input
154		ACK#	I	External	Input	Input
155		LPTD7	I/OD	External	Low	Input or Low(*4)
156		LPTD6	I/OD	External	Low	Input or Low(*4)
157		LPTD5	I/OD	External	Low	Input or Low(*4)
158		LPTD4	I/OD	External	Low	Input or Low(*4)
159		LPTD3	I/OD	External	Low	Input or Low(*4)
160		SLCTIN#	I/OD	External	Input	
161	Power	GND	Power	-	-	-
162	Parallel	LPTD2	I/OD	External	Low	Input or Low(*4)
163		INIT#	I/OD	External	Low	Input or Low(*4)
164		LPTD1	I/OD	External	Low	Input or Low(*4)
165	Power	VCORE	Power	-	-	-
166		VBK	Power	-	-	-
167	Parallel	ERROR#	I	External	Input	Input
168		LPTD0	I/OD	External	Low	Input or Low(*4)
169		AFD#	I/OD	External	Input	Input or Low(*4)
170		STROBE#	I/OD	External	Input	Input or Low(*4)
171	PM	STANDBY#	O	-	High	Low
172	Flash ROM	ROMDIS#	I	50KPU	Input(High)	Input(High)
173		RESERVE	-	-	-	-
174	Video	EXTCLKI	I	100KPU	Input	Input
175		RESERVE	-	-	-	-
176	ISA	CA22	O	-	Drive	Drive
177	Serial 0	TXD0	O	-	Z	Z
178		SCK0	O	-	High(*1)	Z
179		RXD0	I	100KPU	Input	Input
180		AN4	I	-	Hi-Z	Hi-Z
181	Power	GND	Power	-	-	-
182	AD/DA	AN5	I	-	Hi-Z	Hi-Z
183		DA1	O	-	Z	Z

Pin	Group	Name	Type	Termination	Reset	Suspend
184	AD/DA	DA0	O	-	Z	Z
185	Serial 1/Irda	TXD1	O	-	Z	Z
186		RXD1	I	100KPU	Input	Input
187	Serial 2	TXD2	O	-	Z	Z
188		RXD2	I	100KPU	Input	Input
189		RTS2#	O	-	High(*1)	Z
190		CTS2#	I	100KPU	Input	Input
191	PM	PWOFF#	O	-	High(*1)	High
192		SRBTN#	I	60KPU	Input	Input
193	Video	FPVCCON	O	-	High(*1)	Low
194	Port	PTC7/PINT7	I/O	60KPU	Input	Input or Output(*2)
195		PTC6/PINT6	I/O	60KPU	Input	Input or Output(*2)
196		PTC5/PINT5	I/O	60KPU	Input	Input or Output(*2)
197	Power	VCC	Power	-	-	-
198	Port	PTC4/PINT4	I/O	60KPU	Input	Input or Output(*2)
199		PTC3/PINT3	I/O	60KPU	Input	Input or Output(*2)
200		PTC2/PINT2	I/O	60KPU	Input	Input or Output(*2)
201		PTC1/PINT1	I/O	60KPU	Input	Input or Output(*2)
202	Power	GND	Power	-	-	-
203	DMA	DACK0#	O	-	High(*1)	Z
204		DREQ0#	I	100KPU	Input	Input
205		DACK1#	O	-	High(*1)	Z
206		DREQ1#	I	100KPU	Input	Input
207	Interrupt	NMI	I	100KPU	Input	Input
208		IRQ1	I	60KPU	Input	Input
209		IRQ2	I	60KPU	Input	Input
210		IRQ3	I	60KPU	Input	Input
211		IRQ4	I	60KPU	Input	Input
212	Video	VSYNC	O	-	Low	Low
213		HSYNC	O	-	Low	Low
214		B	O	150PD	-	-
215		G	O	150PD	-	-
216		R	O	150PD	-	-
217		FPDAT15	O	-	Low	Low
218		FPDAT14	O	-	Low	Low
219		FPDAT13	O	-	Low	Low
220		FPDAT12	O	-	Low	Low
221	Power	GND	Power	-	-	-
222	Video	FPDAT11	O	-	Low	Low
223		FPDAT10	O	-	Low	Low
224		FPDAT9	O	-	Low	Low
225		FPDAT8	O	-	Low	Low
226	Power	VCC	Power	-	-	-
227	Video	FPDAT7	O	-	Low	Low
228		FPDAT6	O	-	Low	Low
229		FPDAT5	O	-	Low	Low
230		FPDAT4	O	-	Low	Low
231		FPDAT3	O	-	Low	Low
232		FPDAT2	O	-	Low	Low
233		FPDAT1	O	-	Low	Low
234		FPDAT0	O	-	Low	Low
235		DOTCLK	O	-	Low	Low
236		MOD	O	-	Low	Low
237		FPVEEON	O	-	Low	Low
238		LINE	O	-	Low	Drive(*3)
239		FRAME	O	-	Low	Drive(*3)
240	Power	GND	Power	-	-	-

*1 While this is an output pin, it goes into high impedance during a reset operation, and becomes HIGH when there is a pull-up resistance. After the reset, with the software changing the registers of SH7709A, it outputs (with no pull-up resistance).

*2 Input or output, depending on the settings of the SH7709A registers.

*3 HIGH or LOW, depending on the settings of the SED1355 registers.

*4 Input or LOW, depending on the settings of the Companion Chip registers.

Table 5-2 Pin Status (CompactFlash Connector)

Pin	Group	Name	Type	Termination	Reset	Suspend
1	CompactFlash	GND	Power	-	-	-
2		D3	I/O	Hold	Input	Input
3		D4	I/O	Hold	Input	Input
4		D5	I/O	Hold	Input	Input
5		D6	I/O	Hold	Input	Input
6		D7	I/O	Hold	Input	Input
7		CCE1#	O	-	High	High
8		A10	O	-	Z	Low
9		COE#	O	-	High	High
10		A9	O	-	Z	Low
11		A8	O	-	Z	Low
12		A7	O	-	Z	Low
13		VCC	Power	-	-	-
14		A6	O	-	Z	Low
15		A5	O	-	Z	Low
16		A4	O	-	Z	Low
17		A3	O	-	Z	Low
18		A2	O	-	Z	Low
19		A1	O	-	Z	Low
20		A0	O	-	Z	Low
21		D0	I/O	Hold	Input	Input
22		D1	I/O	Hold	Input	Input
23		D2	I/O	Hold	Input	Input
24		CWP_IOIS16#	I	100KPU	Input	Input
25		RESERVE	-	-	-	-
26		RESERVE	-	-	-	-
27		D11	I/O	100KPU	Input	Input
28		D12	I/O	100KPU	Input	Input
29		D13	I/O	100KPU	Input	Input
30		D14	I/O	100KPU	Input	Input
31		D17	I/O	100KPU	Input	Input
32		CCE2#	O	-	High	High
33		RESERVE	-	-	-	-
34		CIORD#	O	-	High	High
35		CIOWR#	O	-	High	High
36		CWE#	O	-	High	High
37		CRDY_IREQ#	I	100KPU	Input	Input
38		VCC	Power	-	-	-
39		RESERVE	-	-	-	-
40		RESERVE	-	-	-	-
41		RESET	O	-	High	Low
42		CWAIT#	I	100KPU	Input	Input
43		RESERVE	-	-	-	-
44		CREG#	O	-	High	High
45		RESERVE	-	-	-	-
46		CBVD1_STSCHG#	I	100KPU	Input	Input
47		D8	I/O	100KPU	Input	Input
48		D9	I/O	100KPU	Input	Input
49		D10	I/O	100KPU	Input	Input
50		GND	Power	-	-	-

5.8.6 Power-off

Some systems may require a certain routine to run before the power of the card can be turned off. For these kinds of systems, the PWOFF# signal can be used to check if the power-off routine is finished. PTD0 of SH7709A outputs to PWOFF#. When the required routine for power-off is finished, PTD0 outputs LOW to PWOFF#; as soon as PWOFF# becomes LOW the power of the system can now be turned off.

5.9 Serial Communication Interface

The CARD-E09A contains one channel of serial communication interface (Serial 0) and four channels of FIFO-attached serial communication interface (Serial 1 to 4). Serial 0 and Serial 1 & 2 are built into SH7709A while Serial 3 & 4 are built into the Companion Chip. Serial 1 can be used as IrDA1.0. Also, Serial 3 and 4 are compatible with 16550.

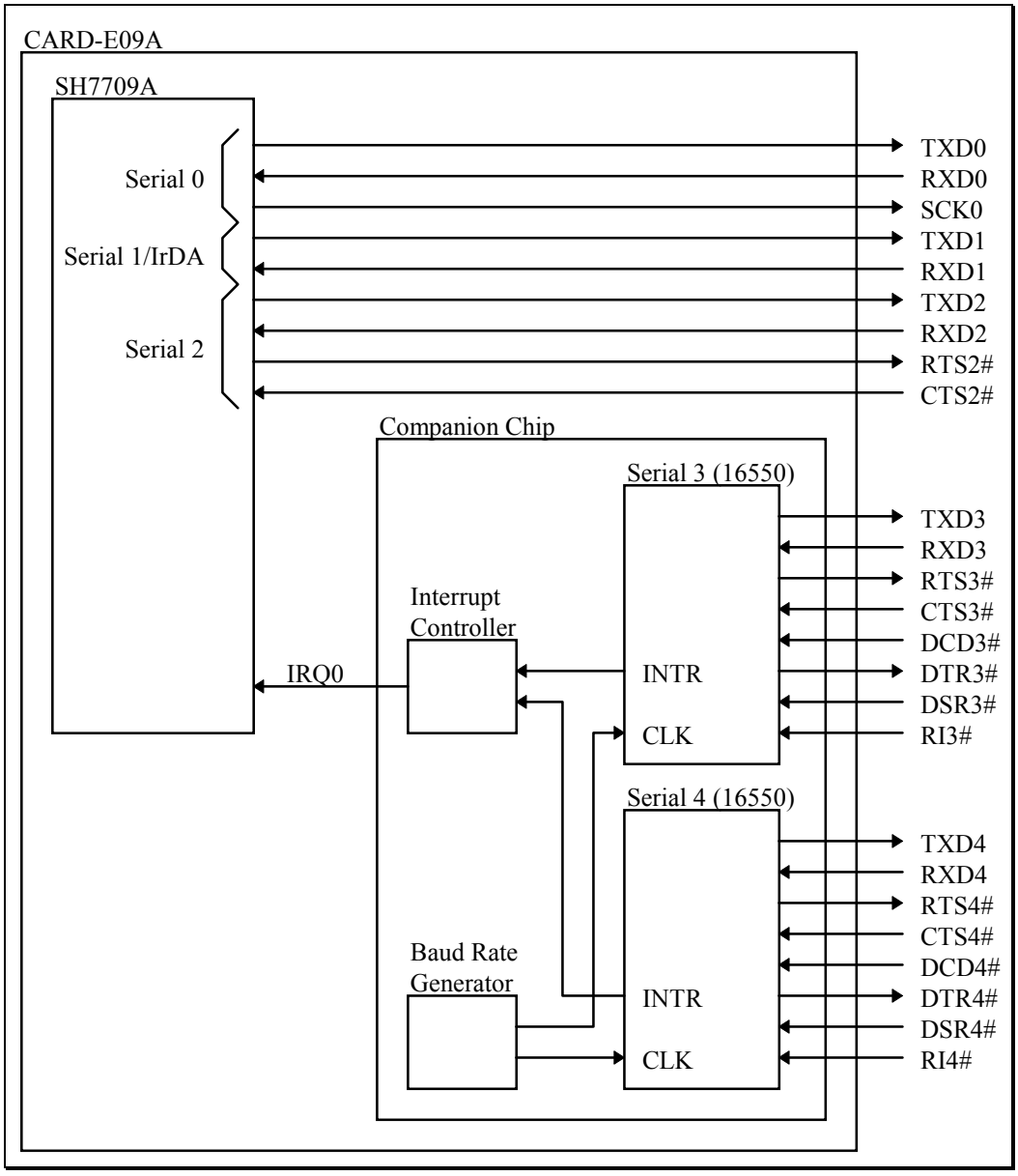


Figure 5-12 Serial Communication Interface Block Diagram

For detailed information on Serial 0 and Serial 1 & 2, refer to the SH7709A manual.

The following table shows the address of Serial 3 and 4.

Serial 3 (16550)

Register	Address
Receive buffer Send buffer Divisor latch (lower bit)	11000200h
Enable interrupt register Divisor latch (upper bit)	11000202h
Interrupt check register FIFO control register	11000204h
Line control register	11000206h
Modem control register	11000208h
Line status register	1100020Ah
Modem status register	1100020Ch
Scratch pad register	1100020Eh

Serial 4 (16550)

Register	Address
Receive buffer Send buffer Divisor latch (lower bit)	11000300h
Enable interrupt register Divisor latch (upper bit)	11000302h
Interrupt check register FIFO control register	11000304h
Line control register	11000306h
Modem control register	11000308h
Line status register	1100030Ah
Modem status register	1100030Ch
Scratch pad register	1100030Eh

The clocks of Serial 3 and 4 are generated by the Baud Rate Generator. Set the Baud Rate Generator register so that 1.8432 MHz can be supplied to Serial 3 and 4.

5.10 Parallel Interface

The CARD-E09A's parallel interface has the following characteristics. This interface supports the enhanced parallel port (EPP) in addition to PS/2 bi-directional direction parallel ports.

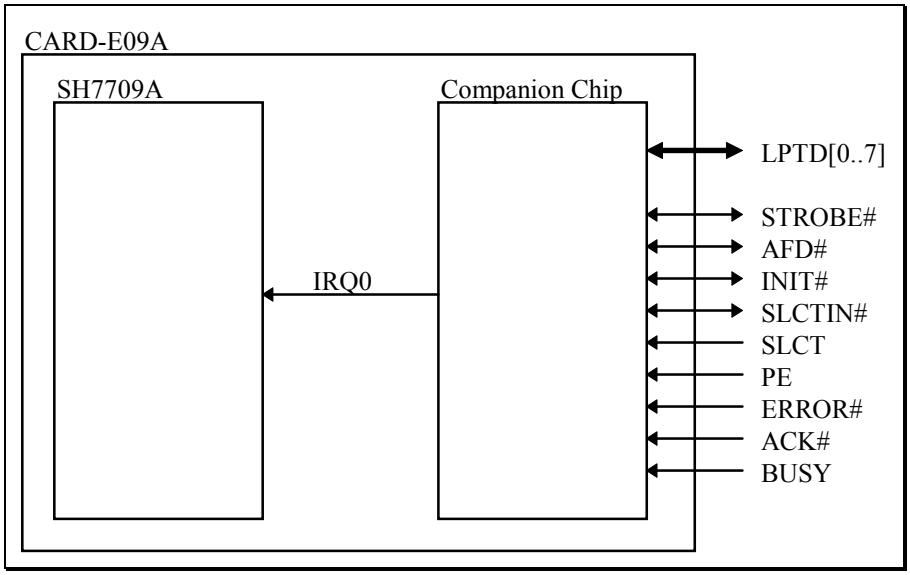


Figure 5-13 Parallel Interface Diagram

5.10.1 Registers

The following registers can be used to control the parallel port.

Parallel Port Data Register

Address = 11000600h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PPD7	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1	PPD0

bit	Name	R/W	Description
7-0	PPD7-0	R/W	In output mode **[** Write **]** The value written to this register is output from LPTD7-0 pins. **[** Read **]** LPTD7-0 pins can be read. In input mode **[** Write **]** There is no impact. **[** Read **]** LPTD7-0 pins can be read.

Parallel Port Status Register

Address = 11000602h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Printer Busy#	Acknowledge#	Out of Paper	Printer is Selected	Error#			

bit	Name	R/W	Description
2-0			
3	Error#	R	The ERROR# pin can be read.
4	Printer is Selected	R	The SLCT pin can be read.
5	Out of Paper	R	The PE pin can be read.
6	Acknowledge#	R	The ACK# pin can be read.
7	Printer Busy#	R	The reversed value of the BUSY pin can be read.

Parallel Port Control Register

Address = 11000604h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Enhanced Parallel Port Mode	Direction	Interrupt Enable	Select Printer	Initialize Printer#	Automatic Line Feed	Data Strobe

bit	Name	R/W	Description
0	Data Strobe	R/W	**[** Write **]** This bit sets the STROBE# pin. 0 : Sets the STROBE# pin to the Tri-state. 1 : Uses the STROBE# pin to output LOW. In the enhanced parallel mode, set this bit to "0". **[** Read **]** The reversed value of the STROBE# pin can be read.
1	Automatic Line Feed	R/W	**[** Write **]** This bit sets the AFD# pin. 0 : Sets the AFD# pin to the Tri-state 1 : Uses the AFD# pin to output LOW. In the enhanced parallel mode, set this bit to "0". **[** Read **]** The reversed value of the AFD # pin can be read.
2	Initialize Printer#	R/W	**[** Write **]** This bit sets the INIT# pin. 0 : Uses the INIT# pin to output LOW. 1 : Sets the INIT# pin to the Tri-state **[** Read **]** The INIT# pin can be read.
3	Select Printer	R/W	**[** Write **]** This bit sets the SLCTIN# pin. 0 : Sets the SLCTIN# pin to the Tri-state 1 : Uses the SLCTIN# pin to output LOW. In the enhanced parallel mode, set this bit to "0". **[** Read **]** The reversed value of the SLCTN# pin can be read.
4	Interrupt Enable	R/W	This bit enables or disables interrupt. 0 : Disable 1 : Enable

bit	Name	R/W	Description
5	Direction	R/W	This bit sets the LPTD70 pins to input or output mode. 0 : Output mode 1 : Input mode
6	Enhanced Parallel Port Mode	R/W	This bit selects the mode of the parallel interface. 0 : Bi-directional parallel mode 1 : Enhanced parallel mode
7			

Automatic Address Strobe Register (EPP)

Address = 11000606h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Address Strobe 7	Address Strobe 6	Address Strobe 5	Address Strobe 4	Address Strobe 3	Address Strobe 2	Address Strobe 1	Address Strobe 0

Automatic Data Strobe Register (EPP)

Address = 11000608h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Data Strobe 7	Data Strobe 6	Data Strobe 5	Data Strobe 4	Data Strobe 3	Data Strobe 2	Data Strobe 1	Data Strobe 0

5.10.2 Enhanced parallel port

When the Enhanced Parallel Port Mode bit of the Parallel Port Control Register is set to "1", the CARD-E09A's parallel port functions as an enhanced parallel port. In this situation, be sure to set the Data Strobe bit, the Automatic Line Feed bit, and the Select Printer bit to the values shown in Table 5-3. Also, make sure the Automatic Address Strobe Register as well as the Automatic Data Strobe Register are accessed only in the enhanced parallel mode.

Table 5-3 Parallel Port Control Register (EPP Mode)

bit	Function	
0	Data Strobe	Be sure to set this bit to "0".
1	Automatic Line Feed	Be sure to set this bit to "0".
2	Initialize Printer#	This bit sets the INIT# pin. 0 : Uses the INIT# pin to output "L". 1 : Turns the INIT# pin to Tri-state.
3	Select Printer	Be sure to set this bit to "0".
4	Interrupt Enable	This bit enables or disables interrupt. 0 : Disable 1 : Enable
5	Direction	don’t care
6	Enhanced Parallel Port Mode	Be sure to set this bit to "1".
7	-	-

In the enhanced parallel mode, the SLCTIN#, AFD#, and STROBE# signals are used as the data strobe signal (DSTRB#), address strobe signal (ADSTRB#), and write cycle indication signal (WRITE#) on the parallel device. Also, BUSY is used as the WAIT# signal. The other control signals remain the same as in the bi-directional parallel mode.
In the enhanced parallel mode, access is controlled by the Automatic Address Strobe Register and the Automatic Data Strobe Register.

① When there is a write to the Automatic Address Strobe Register, the data is output to LPTD[0..7]. At that moment, WRITE#(STROB#) and ADSTRB#(SLCTIN#) become active.
② When there is a read from the Automatic Address Strobe Register, LPTD[0..7] can be read in that way. At that moment, ADSTRB#(SLCTIN#) becomes active.
③ When there is a write to the Automatic Data Strobe Register, the data is output to LPTD[0..7]. At that moment, WRITE#(STROBE#) and DSTRB#(AFD#) become active.
④ When there is a read from the Automatic Data Strobe Register, LPTD[0..7] can be read in that way. At that moment, DSTRB#(AFD#) becomes active.

WAIT#(BUSY) is equivalent to IOCHRDY of the ISA bus. When the Automatic Address Strobe Register or the Automatic Data Strobe Register is accessed, if WAIT# is "L", the cycle will end after it turns to "H".

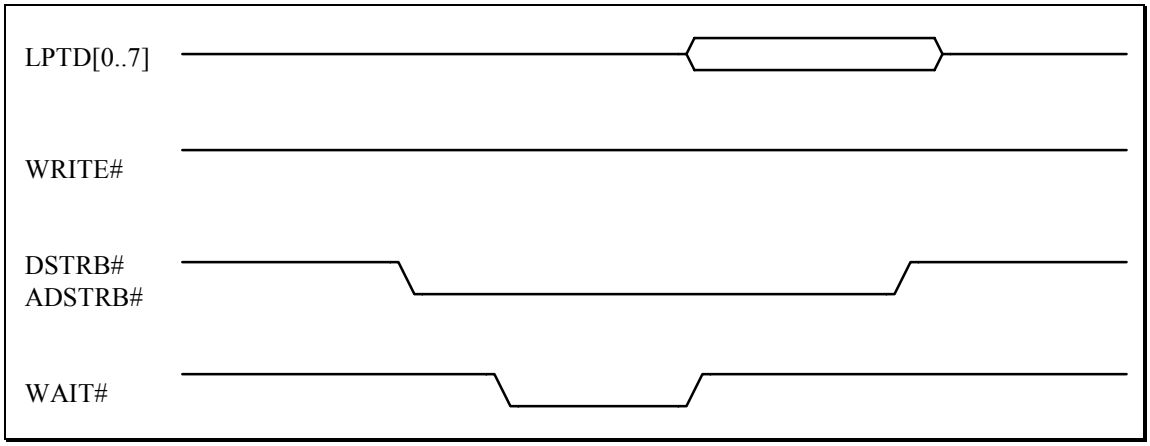


Figure 5-14 EPP Read Cycle

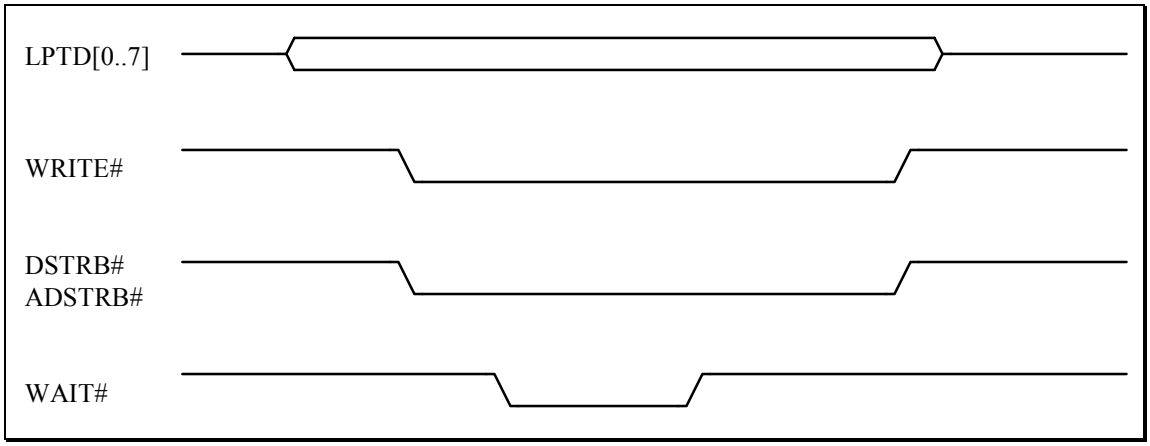


Figure 5-15 EPP Write Cycle

5.10.3 Interrupt

When interrupt is enabled by the Parallel Control Register and Interrupt Enable Register 1, the parallel port can send an interrupt to SH7709A. This interrupt detects the raised edge of ACK# and goes from the Companion Chip through IRQ0 to become the SH7709A interrupt. This interrupt signal must be cleared by using Interrupt Status Register 1.

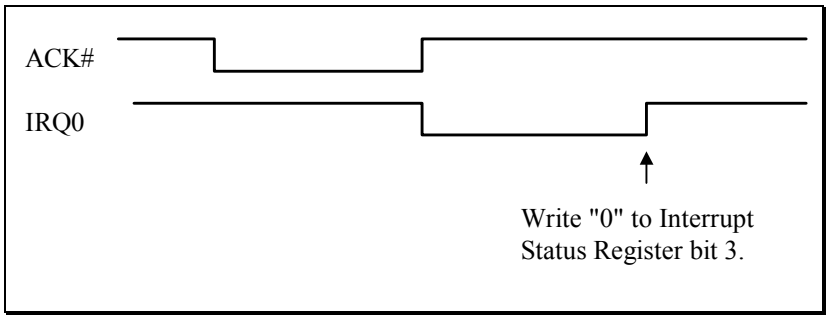


Figure 5-16 Parallel Port Interrupt

5.10.4 Circuitry example

Figure 5-17 shows a circuitry example of the parallel port. The data and control signals require pull-up resistance.

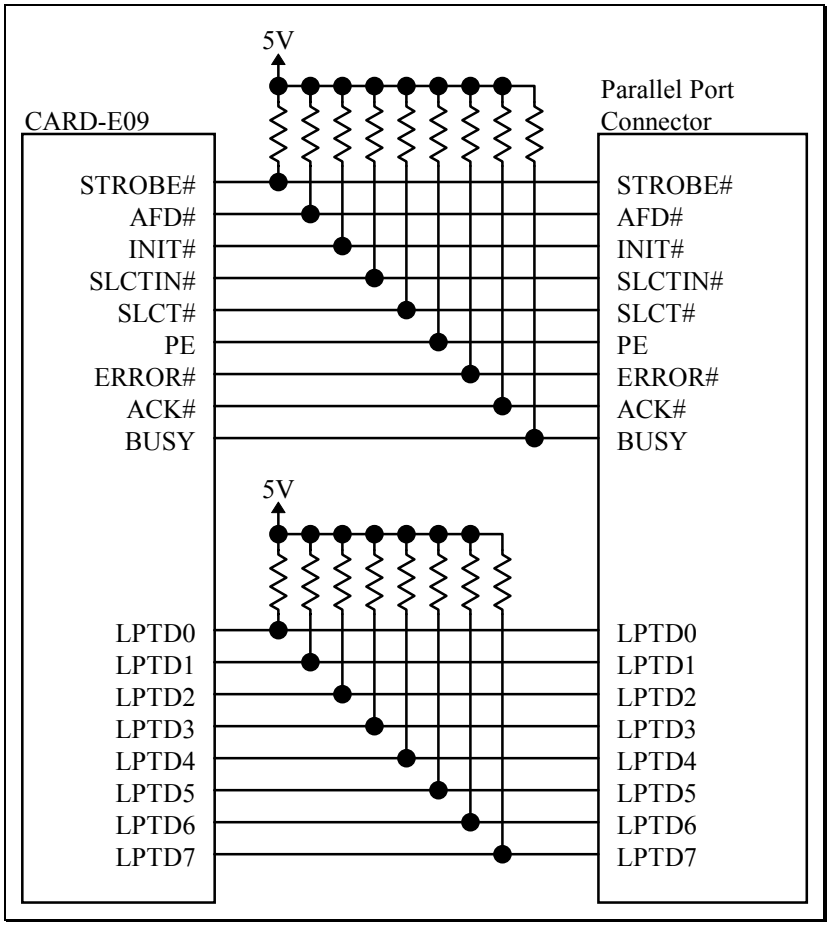


Figure 5-17 Parallel Port Interface Example

5.11 Keyboard/Mouse Interface

The CARD-E09A has a built-in control to allow use of PS/2 keyboard and mouse as they are.
Figure 5-18 is a keyboard controller block diagram. While the following discussion focuses on the keyboard, it applies to the mouse as well.

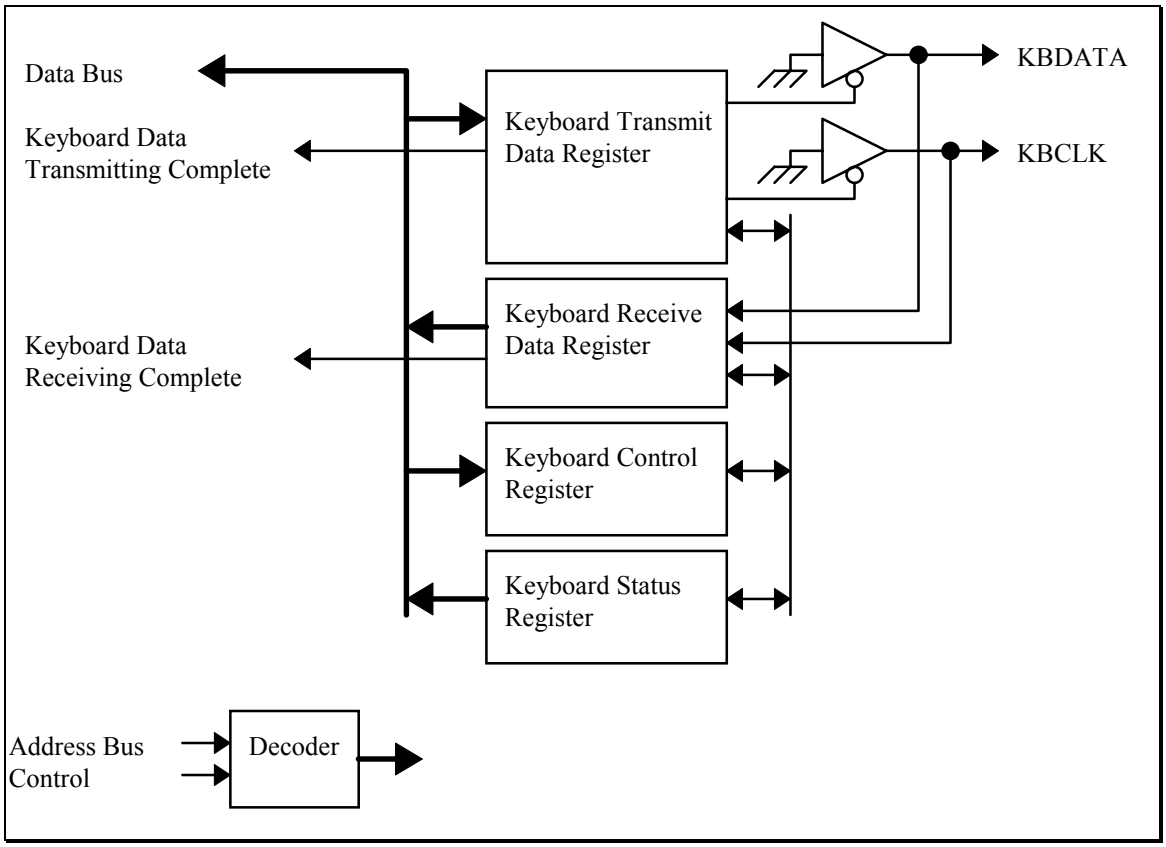


Figure 5-18 Keyboard Controller Block Diagram

5.11.1 Registers

The following registers are available in the keyboard/mouse controller.

Keyboard/Mouse Control Register

Address = 11000500h, 11000508h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		Keyboard (Mouse) Data Transmitting Complete Interrupt Enable	Keyboard (Mouse) Data Receiving Complete Interrupt Enable	KBDATA (MSDATA) forced LOW#	KBCLK (MSCLK) forced LOW#		Keyboard (Mouse) Interface RESET#

bit	Name	R/W	Description
0	Keyboard(Mouse) Interface RESET#	R/W	Setting this bit to "0" resets the communication circuit with the Keyboard(Mouse). All the flags are reset. If the unit is receiving data, the reception is stopped immediately; if the unit is sending data, the transmission is stopped immediately as well.
1			
2	KBCLK (MSCLK) forced LOW#	R/W	Setting this bit to "0" turns KBCLK (MSCLK) to LOW. This can be used to prohibit data transmission from the Keyboard(Mouse).
3	KBDATA (MSDATA) forced LOW#	R/W	Setting this bit to "0" turns KBDATA(MSDATA) to LOW.
4	Keyboard(Mouse) Data Receiving Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data reception from the Keyboard(Mouse) is finished. The Keyboard(Mouse) Data Receiving Completed flag becomes the interrupt signal.
5	Keyboard(Mouse) Data Transmitting Complete Interrupt Enable	R/W	This bit enables the interrupt which occurs when data transmission to the Keyboard(Mouse) is finished. The Keyboard(Mouse) Data Transmitting Completed flag becomes the interrupt signal.
7-6			

Keyboard/Mouse Status Register

Address = 11000502h, 1100050Ah
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
			Keyboard (Mouse) Parity Error	Keyboard (Mouse) Data Transmitting Complete	Keyboard (Mouse) Data Receiving Complete	Keyboard (Mouse) Data Transmitting	Keyboard (Mouse) Data Receiving

bit	Name	R/W	Description
0	Keyboard(Mouse) Data Receiving	R	When this bit is "1", this indicates data is being received from the Keyboard(Mouse).
1	Keyboard(Mouse) Data Transmitting	R	When this bit is "1", this indicates data is being sent to the Keyboard(Mouse). This bit is set to (1) when data is written to Keyboard(Mouse) Transmit Data Register; when data transmission is finished, it is reset to (0).
2	Keyboard(Mouse) Data Receiving Complete	R/W	When this bit is "1", this indicates data reception from the Keyboard(Mouse) is finished, and the value of Keyboard(Mouse) Receive Data Register is valid. This bit is reset when "0" is written to it. If this bit is not reset, the next data cannot be received.
3	Keyboard(Mouse) Data Transmitting Complete	R/W	When this bit is "1", this indicates data transmission to the Keyboard(Mouse) is finished, This bit is reset when "0" is written to it.
4	Keyboard(Mouse) Parity Error	R	Data communication with the Keyboard(Mouse) uses the ODD parity. If the received data has the EVEN parity, this bit is set to "1". This bit is valid only when Keyboard(Mouse) Data Receiving Complete is "1".
7-5			

Keyboard/Mouse Transmit Data Register

Address = 11000504h, 1100050Ch
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
KBDW7 (MSDW7)	KBDW6 (MSDW6)	KBDW5 (MSDW5)	KBDW4 (MSDW4)	KBDW3 (MSDW3)	KBDW2 (MSDW2)	KBDW1 (MSDW1)	KBDW0 (MSDW0)

bit	Name	R/W	Description
7-0	KBDW7-0 (MSDW7-0)	W	Data transmitted to the Keyboard(Mouse)

Keyboard/Mouse Receive Data Register

Address = 11000506h, 1100050Eh
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
KBDR7 (MSDR7)	KBDR6 (MSDR6)	KBDR5 (MSDR5)	KBDR4 (MSDR4)	KBDR3 (MSDR3)	KBDR2 (MSDR2)	KBDR1 (MSDR1)	KBDR0 (MSDR0)

bit	Name	R/W	Description
7-0	KBDR7-0 (MSDR7-0)	R	Data received from the Keyboard(Mouse) This register is valid only when Keyboard(Mouse) Data Receiving Complete is "1".

5.11.2 Data reception

This section describes how data is received from the keyboard and mouse (Figure 5-19). While the following discussion focuses on the keyboard, it applies to the mouse as well.

① When no data is sent to the keyboard and the KBDATA line is inactive (LOW), if there is a dropped edge at the KBCLK line, this data is determined as the start bit and subsequently no data is sent until the data reception is finished.
② Lower the KBCLK line and latch the 9 bits of data. These 9 bits consist of 8 data bits and 1 parity bit.
③ Lower the 11th KBCLK line to trigger the data reception complete interrupt and request data from the CPU. Change the KBCLK line to LOW and prohibit data transmission from the keyboard. No check on the stop bit is performed.
④ When SH7709A takes in the received data and clears the interrupt, the KBCLK line becomes active (HIGH) and the next data can be transferred.

5.11.3 Data transmission

This section describes how data is sent to the keyboard and mouse (Figure 5-19). While the following discussion focuses on the keyboard, it applies to the mouse as well.

① When the KBDATA line is active (HIGH) and no data is being received from the keyboard, turn the KBCLK line to become inactive (LOW). If data is being received, wait until the data reception is finished (interrupt is cleared).
② Turn the KBCLK line to become inactive (LOW). After 48 usec, turn the KBDATA line to become inactive (LOW). This means requesting for data transmission to the keyboard, and is equivalent to setting the start bit.
③ After 48 usec, return the KBCLK line to become active again (HIGH), and then wait until the KBCLK line becomes inactive (LOW).
④ When the KBCLK line becomes inactive (LOW), set the first bit at the KBDATA line. In the same way, wait for the KBCLK line to lower and then send 10 bits of data until the stop bit
⑤ If the interrupt is enabled, when the 11th clock is lowered, the data transmission complete interrupt occurs.
⑥ SH7709A clears the interrupt.

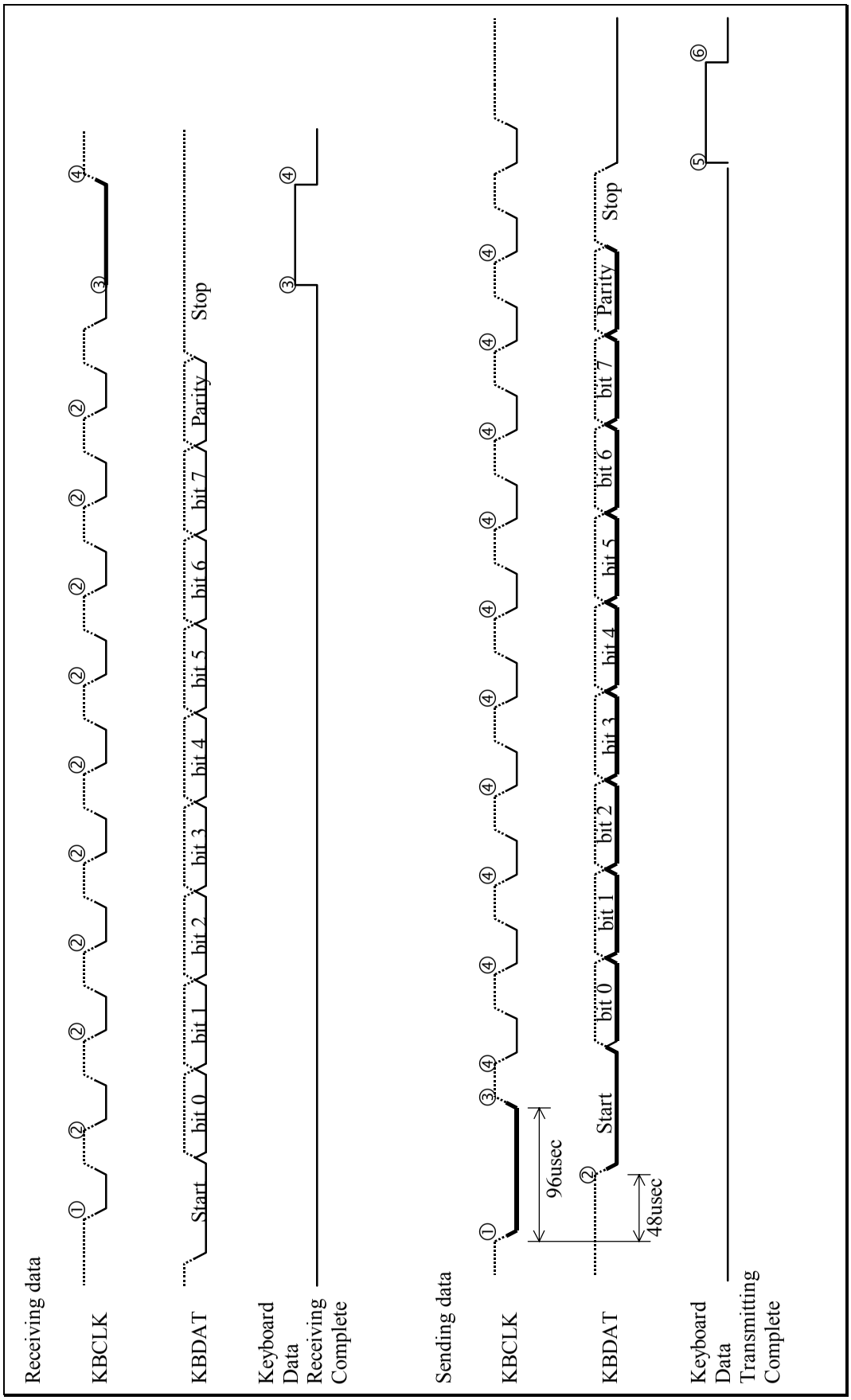


Figure 5-19 Keyboard Data Receiving/Transmitting Timing

5.11.4 Programming

The following is an example on how to program using the keyboard controller.

[Receiving data]
When each bit of data is received from the keyboard, an interrupt occurs at SH7709A. At the same time, because the Keyboard Data Receiving Complete Interrupt flag of Interrupt Status Register 2 is set, SH7709A can read the Interrupt Status Register to determine that there is a data reception interrupt. When this is confirmed, data read is performed using the Keyboard Receive Data Register, and if necessary the
Keyboard Parity Error flag of the Keyboard Status Register is also read. When this is finished, "0" must be written to the Keyboard Data Receiving Complete of the Keyboard Status Register. This write operation clears the interrupt and allows for reception of the next data.

[Sending data]
When the Keyboard Data Transmitting flag of the Keyboard Status Register is "0", by writing data to the Keyboard Transmit Data Register, the data is sent to the keyboard.

5.11.5 Connection example

Figure 5-20 shows a connection example on keyboard/mouse. Usually the keyboard/mouse requires an operating voltage of 5V, so a 5V power must be supplied to the keyboard/mouse. Also, KBCLK, KBDATA, MSCLK and MSDATA must be pulled up at 5V. Even though the operating voltage of the CARD-E09A is 3.3V, input of 5V signal at KBCLK, KBDATA, MSCLK and MSDATA does not cause any problem.

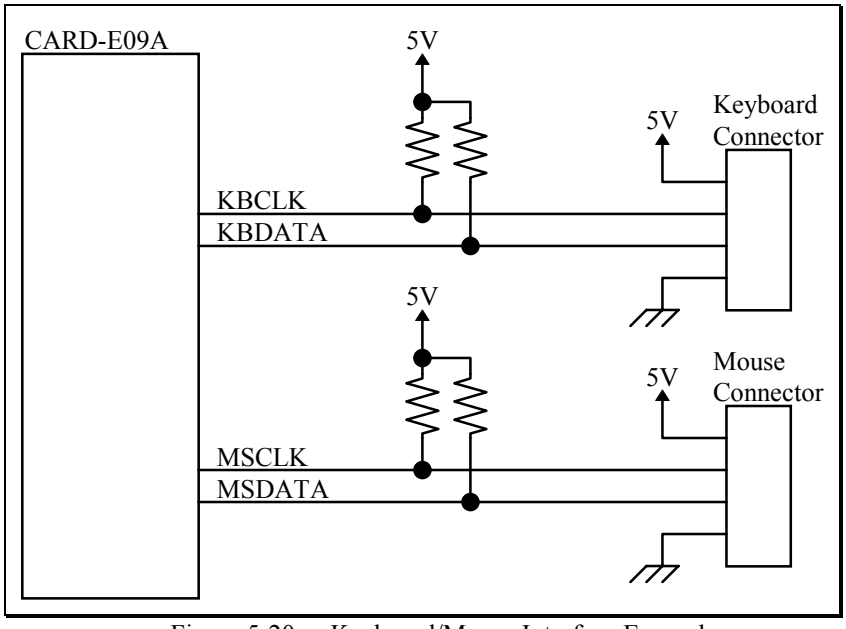


Figure 5-20 Keyboard/Mouse Interface Example

5.12 PCMCIA/CompactFlash Interface

SH7709A can set Area 6 as the PCMCIA interface. The CARD-E09A makes the 3-channel PCMCIA interface possible through using this feature of SH7709A as well as the Companion Chip. The two channels can be used outside the CARD-E09A and one channel for internal use of the CARD-E09A to connect a CompactFlash card.

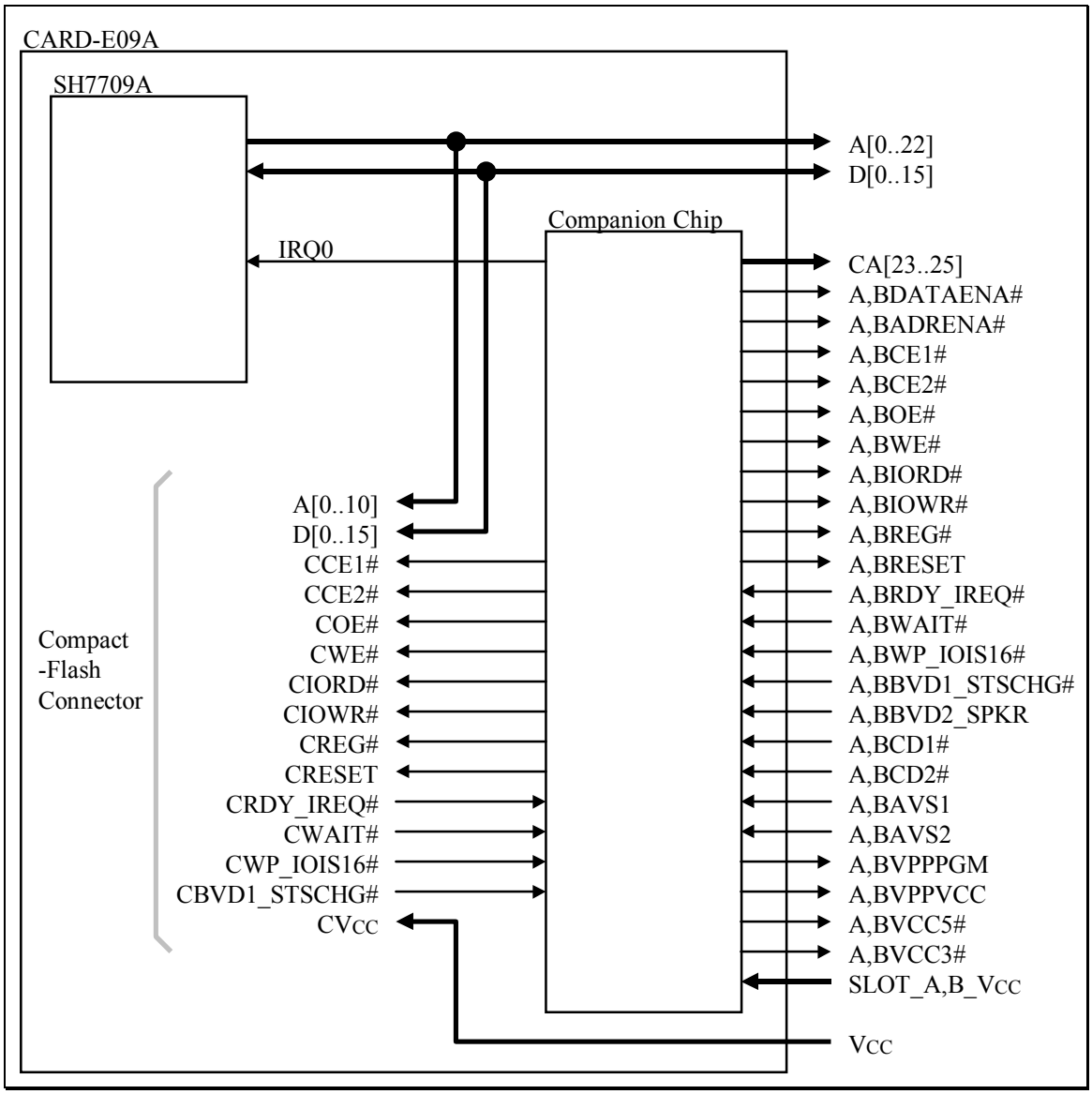


Figure 5-21 PCMCIA/CompactFlash Interface Block Diagram

5.12.1 PCMCIA/CompactFlash memory map

The PCMCIA memory space is 64 MB. On the CARD-E09A, access is via 8 MB of an area of SH7709A (Figure 5-22). It can be selected from the following three areas, by using the Memory Area Select bit of the Slot Configuration Register.

① 8000000h to 187FFFFFh
② 8800000h to 18FFFFFFh
③ 9000000h to 197FFFFFh

The upper 3 bits are specified by the Slot Memory Address bit of the Slot Address Register.

Like the memory space, the PCMCIA I/O space memory can be selected from the following three areas, by using the I/O Area Select bit of the Slot Configuration Register.

① A000000h to 1A7FFFFFh
② A800000h to 1AFFFFFFh
③ A000000h to 1A7FFFFFh

The upper 3 bits are specified by the I/O Address bit of the Slot Address Register.

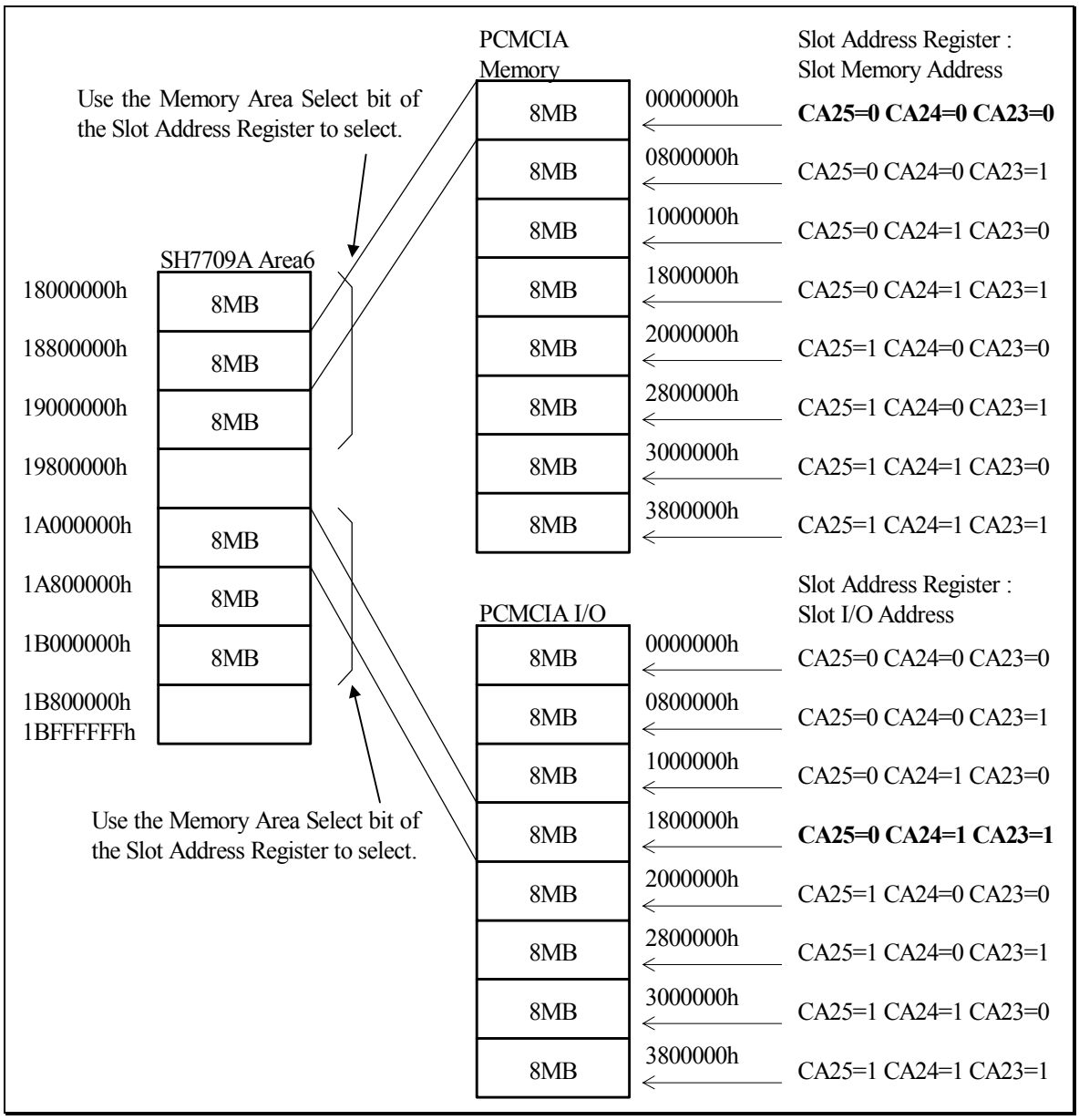


Figure 5-22 PCMCIA Bus Memory Map

5.12.2 Register

The following indicates the registers of the PCMCIA/CompactFlash interface.

Slot Configuration Register A,B,CF

Address = 11000100h, 11000140h, 11000180h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		I/O Area Select bit 1	I/O Area Select bit 0		Memory Area Select bit 2	Memory Area Select bit 1	Memory Area Select bit 0

bit	Name	R/W	Description
2,1,0	Memory Area Select bit 1,0	R/W	These bits specify the SH7709A address for the PCMCIA Slot (Memory Area). bit2 bit1 bit0 0 0 0 : Memory Interface Disable 0 0 1 : Do not change it. 0 1 0 : Do not change it. 0 1 1 : 18000000h-187FFFFFh 1 0 0 : 18800000h-18FFFFFFh 1 0 1 : 19000000h-197FFFFFh 1 1 0 : Memory Interface Disable 1 1 1 : Memory Interface Disable
3			
5,4	I/O Area Select bit 1,0	R/W	These bits specify the SH7709A address for the PCMCIA Slot (I/O Area). bit1 bit0 0 0 : I/O Interface Disable 0 1 : 1A000000h-1A7FFFFFh 1 0 : 1A800000h-1AFFFFFFh 1 1 : 1B000000h-1B7FFFFFh
7,6			

Slot Address Register A,B,CF

Address = 11000102h, 11000142h, 11000182h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Slot I/O Address CA25	Slot I/O Address CA24	Slot I/O Address CA23		Slot Memory Address CA25	Slot Memory Address CA24	Slot Memory Address CA23

bit	Name	R/W	Description
2,1,0	Slot Memory Address	R/W	These bit specify the upper 3 bits of the PCMCIA Slot (Memory Area) address. CompactFlash They are ignored.
3			
6,5,4	Slot I/O Address	R/W	These bit specify the upper 3 bits of the PCMCIA Slot (I/O Area) address. CompactFlash They are ignored.
7			

Slot Status Register A,B,CF

Address = 11000104h, 11000144h, 11000184h
Reset = Not fixed

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VS2	VS1	READY/ BUSY#	WP	CD2	CD1	BVD2	BVD1

bit	Name	R/W	Description
1,0	BVD2, BVD1	R	These bits can be used to read the states of the BVD2_SPKR and BVD1_STSCHG# pins. BVD2_SPKR BVD1_STSCHG# : BVD2 bit BVD1 bit LOW LOW : 0 0 LOW HIGH : 0 1 HIGH LOW : 1 0 HIGH HIGH : 1 1 CompactFlash Only the state of the BVD1_STSCHG# pin can be read. The BVD2 bit is always read as "1".
3,2	CD2,1	R	These bits can be used to read the reverse of the states of the CD1# and CD2# pins. CD2# pin CD1# pin : CD2 bit CD1 bit HIGH HIGH : 0 0 No card HIGH LOW : 0 1 No card LOW HIGH : 1 0 No card LOW LOW : 1 1 Has card CompactFlash The CD1 and CD2 bits are always read as "1".
4	WP	R	This bit can be used to read the state of the WP_IOIS16# pin. In the memory card mode, the state of the write protect switch on the card can be read. In the I/O card mode, the value thus read has no meaning.

bit	Name	R/W	Description
5	READY/BUSY#	R	This bit can be used to read the state of the RDY_IREQ# pin. In the memory card mode, it can read the state to see whether new data transmission of the card is possible. In the I/O card mode, the value thus read has no meaning.
7,6	VS2,1	R	These bits can be used to read the states of the VS1 and VS2 pins. VS2 pin VS1 pin : VS2 bit VS1 bit LOW LOW : 0 0 LOW HIGH : 0 1 HIGH LOW : 1 0 HIGH HIGH : 1 1 CompactFlash The VS1 and VS2 bit are always read as "0".

Power Control Register A,B,CF

Address = 11000106h, 11000146h, 11000186h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Card Enable		Auto Power		VCC3.3V	VCCPower	VPPPower1	VPPPower 0

bit	Name	R/W	Description
1,0	VPPPower1,0	R/W	These bits controls the power (VPP) of the card. CompactFlash Be sure to always set them to "01".
2	VCCPower	R/W	This bit controls the power (VCC) on/off of the card. CompactFlash Be sure to always set it to "1".
3	VCC3.3V	R/W	This bit specifies the voltage of the card's power (VCC). 0 : 5V 1 : 3.3V CompactFlash Be sure to always set it to "1".
4			
5	Auto Power	R/W	When this bit is "0", regardless of the states of the CD1# and CD2# pins, the power of the card can be controlled by using the four bits mentioned above. When this bit is "1", the power of the card can be controlled by using the four bits mentioned above only if both the CD1# and CD2# pins are LOW. If either of CD1# or CD2# becomes HIGH, the power of the card is always off. (The control signal becomes inactive.) CompactFlash Be sure to always set it to "0".
6			

bit	Name	R/W	Description
7	Card Enable	R/W	When this bit is "0", the following signals are in high impedance: CE2#, CE1#, IORD#, IOWR#, OE#, WE#, REG# and RESET. Also, buffer control signals change in the following way so that the address data go into high impedance: ADRENA#="HIGH" DATAENA#="HIGH" Even when this bit is "1", as long as the card's power is not turned on with CD2#= LOW and CD1# = LOW, the above signal cannot be driven. CompactFlash Be sure to always set it to "1".

General Control Register A,B,CF

Address = 11000108h, 11000148h, 11000188h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Card Reset#	I/O Card Mode				Write Protect	REG Setting

bit	Name	R/W	Description
0	REG Setting	R/W	This bit sets up the REG# pin for the PCMCIA Slot. 0 : REG# = "HIGH" (Common Memory) 1 : REG# = "LOW" (Attribute Memory) When the I/O Area is accessed, REG# becomes LOW.
1	Write Protect	R/W	When this bit is set to "1", no write cycle occurs at the Memory Area. This bit has no relationship with the state of the WP_IOIS16# pin. For the memory card, even if the WP_IOIS16# pin is active, as long as this bit is "0", no write cycle occurs. Also, write to I/O Area cannot be prohibited.
4-2			
5	I/O Card Mode	R/W	When this bit is set to "1", the PCMCIA controller goes into the I/O card mode; when this bit is set to "0", the controller goes into the memory card mode.
6	Card Reset#	R/W	When this bit is set to "0", the RESET pin becomes active (HIGH).
7			

Card Status Change Register A,B,CF

Address = 1100010Ah, 1100014Ah, 1100018Ah

Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
			Card Remove	Card Insert	Ready Change	Battery Warning	Battery Dead or STSCHG

bit	Name	R/W	Description
0	Battery Dead or STSCHG	R/W	In the memory card mode: This bit is set to "1" when the BVD1_STSCHG# pin changes from HIGH to LOW. This bit is reset when "0" is written to it. In the I/O card mode: This bit functions in the same way as in the memory card mode.
1	Battery Warning	R/W	In the memory card mode: This bit is set to "1" when the BVD2_SPKR pin changes from HIGH to LOW. This bit is reset when "0" is written to it. In the I/O card mode: This bit is always read as "0". CompactFlash This bit can always be read as "0".
2	Ready Change	R/W	In the memory card mode: This bit is set to "1" when the RDY_IREQ# pin changes from LOW to HIGH. This bit is reset when "0" is written to it. In the I/O card mode: This bit is always read as "0".
3	Card Insert	R/W	This bit is set to "1" when both the CD1# and CD2# pins become LOW. This bit is reset when "0" is written to it. CompactFlash This bit has no meaning.
4	Card Remove	R/W	This bit is set to "1" when either the CD1# or CD2# pin become HIGH. This bit is reset when "0" is written to it. CompactFlash This bit has no meaning.
7-5			

Management Interrupt Configuration Register A,B,CF

Address = 1100010Ch, 1100014Ch, 1100018Ch

Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
			Card Remove Interrupt Enable	Card Insert Interrupt Enable	Ready Change Interrupt Enable	Battery Warning Interrupt Enable	Battery Dead or STSCHG Interrupt Enable

bit	Name	R/W	Description
0	Battery Dead or STSCHG Interrupt Enable	R/W	If this bit is set to "1", when the Battery Dead or STSCHG bit becomes "1", interrupt occurs.
1	Battery Warning Interrupt Enable	R/W	If this bit is set to "1", when the Battery Warning bit becomes "1", interrupt occurs. CompactFlash Be sure to always set this bit to "0".
2	Ready Change Interrupt Enable	R/W	If this bit is set to "1", when the Ready Change bit becomes "1", interrupt occurs.
3	Card Insert Interrupt Enable	R/W	If this bit is set to "1", when the Card Insert bit becomes "1", interrupt occurs. CompactFlash Be sure to always set this bit to "0".
4	Card Remove Interrupt Enable	R/W	If this bit is set to "1", when the Card Remove bit becomes "1", interrupt occurs. CompactFlash Be sure to always set this bit to "0".
7-5			

The PCMCIA/CompactFlash interface is accessed via Area 6 of SH7709A. Area 6 of SH7709A as well as PTG7 must be set as follows:

Area 6	Access method	PCMCIA
	Bus width	16bit
	Wait number	2 wait insertion
	Idle cycle	2 idle cycle insertion
	Address-OE#/WE# assert delay	1.5 cycle delay
	OE#/WE# negate-address delay	3.5 cycle delay
PTG7	Pin function	Other function IOIS16#

5.12.3 Timing

The timing of the PCMCIA/CompactFlash interface is shown in Figure 5-23 and Figure 5-24.

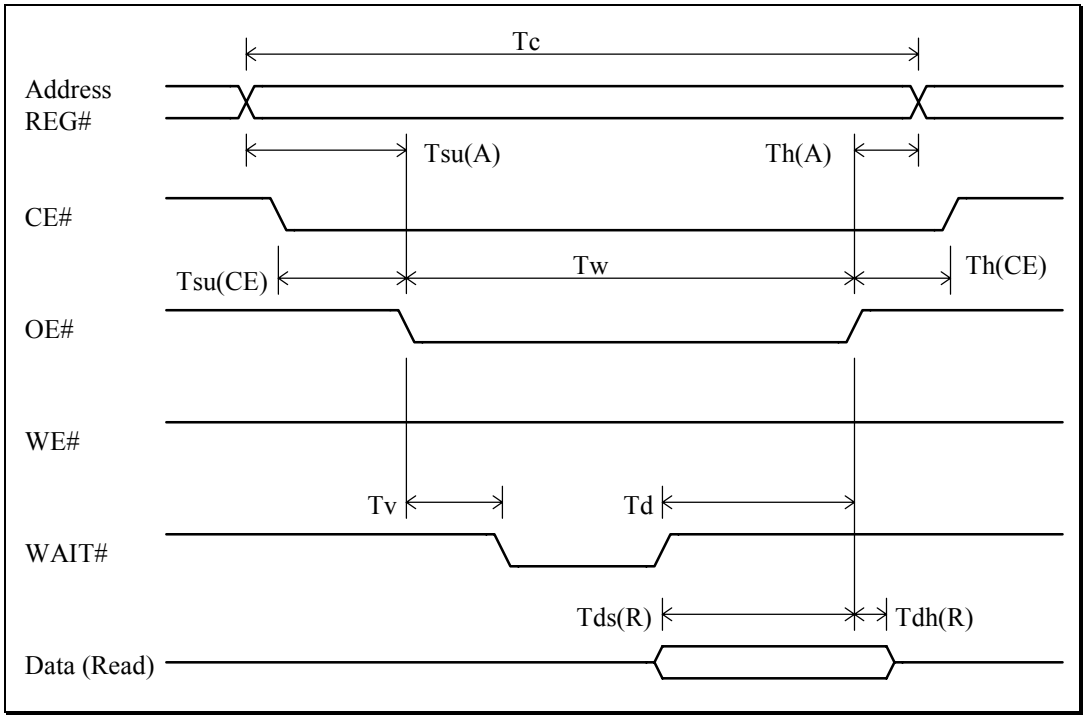


Figure 5-23 PCMCIA Memory Read Timing

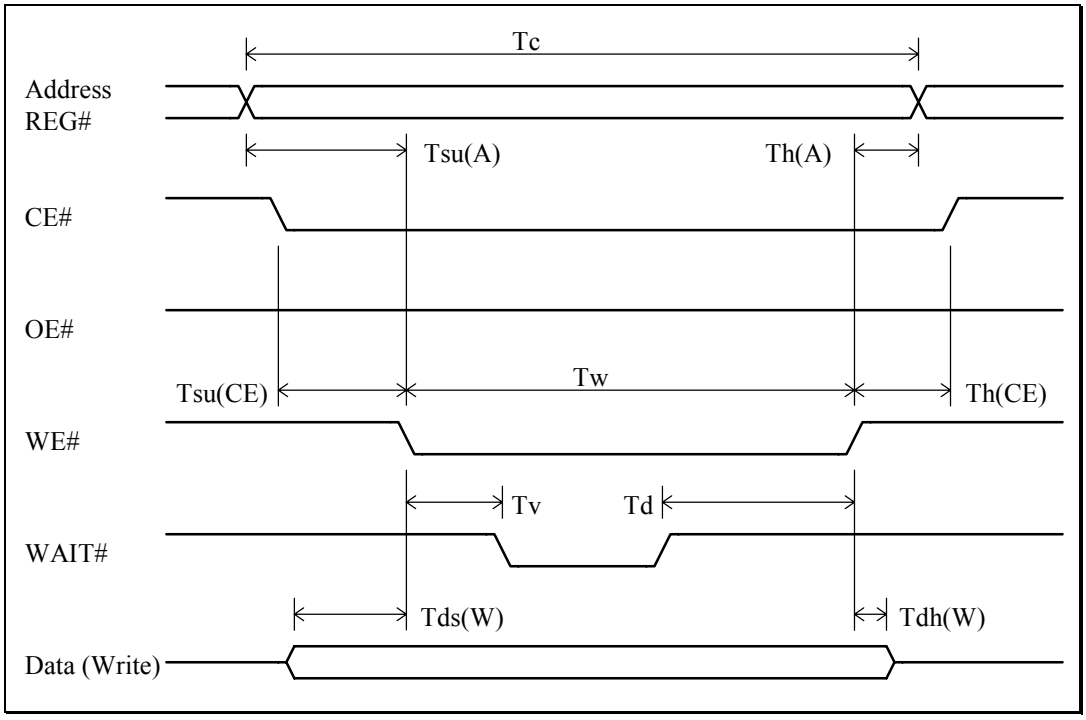


Figure 5-24 PCMCIA Memory Write Timing

Table 5-4 PCMCIA Memory Read/Write Timing

Parameter	Symbol	min.	typ.	max.	unit
Cycle Time	Tc	17			CKIO
Address Setup Time	Tsu(A)		6		CKIO
CE# Setup Time	Tsu(CE)		6		CKIO
Address Hold Time	Th(A)		3		CKIO
CE# Hold Time	Th(CE)		3		CKIO
OE#/WE# Pulse Width	Tw		8		CKIO
WAIT# Valid from OE#/WE#	Tv			4	CKIO
OE#/WE# Hold Time from WAIT# Inactive	Td	4			CKIO
Data Setup Time (Read)	Tds(R)	0.5			CKIO
Data Hold Time (Read)	Tdh(R)	0			CKIO
Data Setup Time (Write)	Tds(W)		6		CKIO
Data Hold Time (Write)	Tdh(W)		3		CKIO

5.12.4 Slot Power On/Off Signals

The relationship between each bit of the Power Control Register and the power control signals is indicated in Table 5-5. However, if the Auto Power bit is "1", when either the CD1# pin or CD2# pin becomes HIGH, the following is true regardless of the register settings: VPPPGM = LOW, VPPVCC = LOW, VCC5# = HIGH, and VCC3# = HIGH.

Table 5-5 PCMCIA Power Control

Register settings				Power control signals			
VCC3.3V	VCCPower	VPPPower1	VPPPower0	VPPPGM	VPPVCC	VCC5#	VCC3#
x	0	x	x	L	L	H	H
0	1	0	0	L	L	L	H
1	1	0	0	L	L	H	L
0	1	0	1	L	H	L	H
1	1	0	1	L	H	H	L
0	1	1	0	H	L	L	H
1	1	1	0	H	L	H	L
0	1	1	1	L	L	L	H
1	1	1	1	L	L	H	L

The following indicates the condition for each of the power control signals to become active.

$$power\_on = VccPower \times \left(\overline{AutoPower} + \left(\overline{CD1\#} \times \overline{CD2\#} \right) \right)$$

$$VPPVCC = power\_on \times VppPower0 \times \overline{VppPower1}$$

$$VPPPGM = power\_on \times \overline{VppPower0} \times VppPower1$$

$$VCC5\# = \overline{power\_on} + Vcc3.3V$$

$$VCC3\# = \overline{power\_on} + \overline{Vcc3.3V}$$

The conditions for turning the control signals for the slot (CE1#, CE2#, OE#, WE#, IORD#, IOWR#, REG#, and RESET) to high impedance are listed in the following formula:

$$card\_in = \overline{CD1\#} \times \overline{CD2\#}$$

$$enable = card\_in \times power\_on \times CardEnable$$

When enable is "1", the control signal is driven; when it becomes "0", the control signal goes into high impedance.

When this happens, the following is true: ADRENA# = HIGH and DATAENA# = HIGH.

5.12.5 Slot Signals at Power-Off

When no card is inserted in the slot or power of the slot is turned off, the signals to the slot are as follows:

Output signals (CE1#, CE2#, OE#, WE#, IORD#, IOWR#, REG#, and RESET):

Because these signals are driven by the power of the slot, when the power is turned off they cannot be driven.

Input signals (RDY_IREQ#, WAIT#, WP_IOIS16#, BVD1_STSCHG#, and BVD2_SPKR):

These signals are masked inside the CARD-E09A to become HIGH. The internal pull-up resistance is separated.

Input signals (CD1#, CD2#, AVS1, and AVS2):

These signals continue to function even when the power of the slot is turned off.

5.12.6 Slot Power-On/Off Timing

Figure 5-25 indicates the timing of the power on/off of the slot. To follow the PCMCIA/JEIDA standards, the power on/off must be controlled in the following way.

-- Power-On --

① When a card is inserted (CD1# and CD2# pins both become LOW), the interrupt becomes active.
② Turn on the power of the slot.
③ After approximately 101 msec of the power on, turn the signal of the slot to become active.
At this moment, the card reset must be active. (Before this, CardReset# must be set to "0".)
④ After 10 usec, turn the reset to become inactive.
⑤ Access to the slot can begin 20 msec after the reset becomes inactive.

-- Power-Off --

① After 1 usec when access to the slot is finished, turn the signal to the slot to high impedance.
② After the signal to the slot is turned to high impedance (min. 0 sec), turn off the power of the slot.

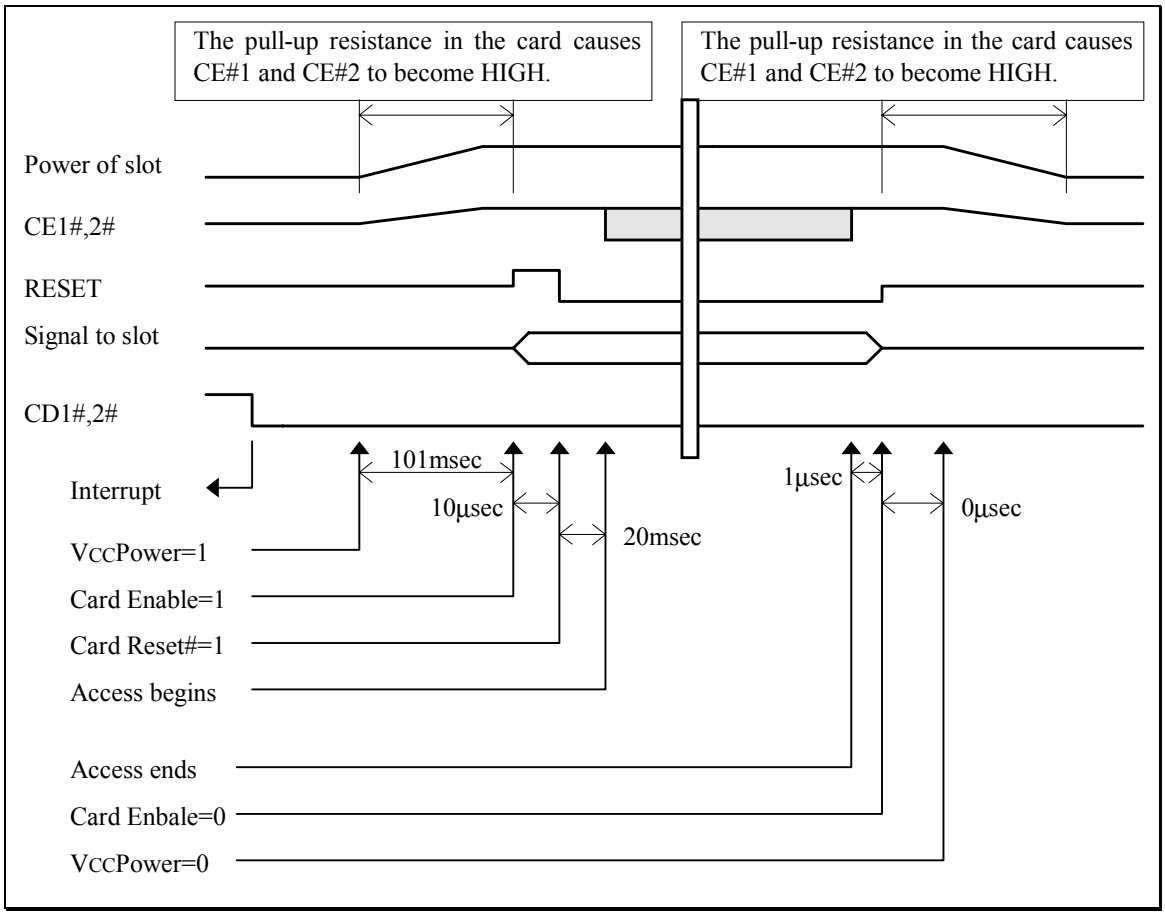


Figure 5-25 PCMCIA Power-On/Off Timing

5.12.7 Slot Auto Power-On/Off Timing

When Auto Power is set to "1", depending on the detection result of the card, the power of the slot is controlled automatically. However, it controls only the power's on/off operation but not its timing. The power on/off timing must be controlled from the software, as shown in Figure 5-26 PCMCIA Power-On/Off Timing.

Figure 5-27 shows the Auto Power-On timing. When the card is inserted (both CD1# and CD2# pins become LOW), the interrupt becomes active and at the same time the power of the slot is turned on. Except for power-on, all other operations must be handled by the software.

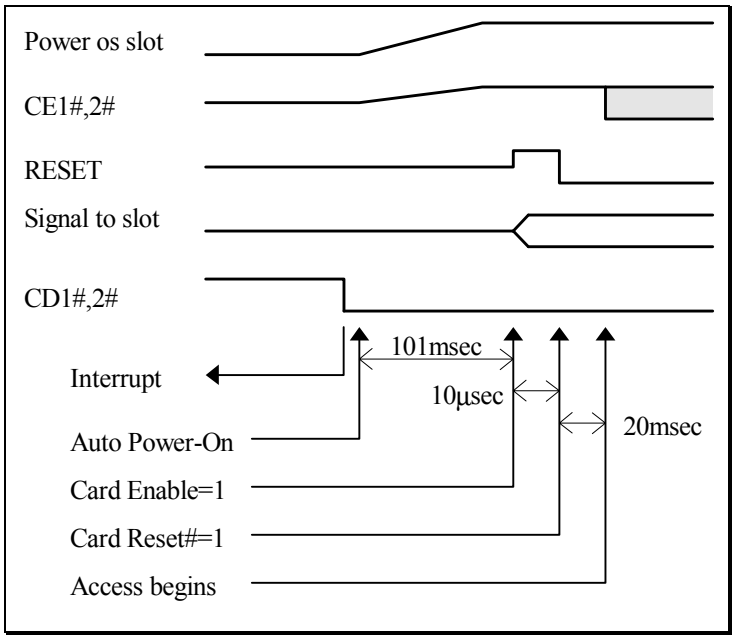


Figure 5-26 PCMCIA Auto Power-On Timing

Figure 5-27 shows the Auto Power-Off timing when the card is removed. When the card is removed (either the CD1# or CD2# pin becomes HIGH), the interrupt becomes active and at the same time the PCMCIA signals change as follows:

- Signal to the signal goes into high impedance.
- All power on/off signals are off.
- ADRENA# becomes HIGH and DATAENA# also becomes HIGH.

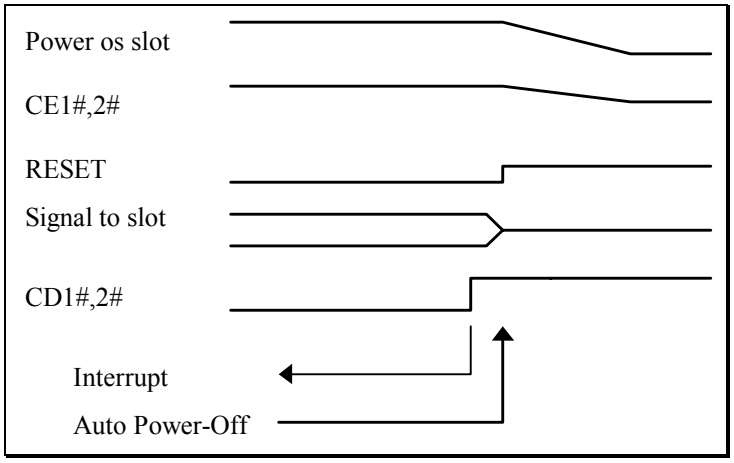


Figure 5-27 PCMCIA Auto Power-Off Timing

Subsequently, when the card is inserted, the power becomes on. At this moment signals to the card must go into high impedance. To do so, Card Enable must be preset to "0".

5.12.8 Interrupt

Only when set at the I/O mode the RDY_IREQ# of the PCMCIA/CompactFlash interface functions as the interrupt signal. The IREQ# and state change interrupt of the three channels become SH7709A interrupt according to IRQ0. Cause of the interrupt can be determined by Interrupt Status Registers 1 and 2. The IREQ# input is output directly to IRQ0. Because SH7709A is set as "IRQ0 Interrupt Detection at LOW Level", the interrupt from the card must also be the level interrupt.

5.12.9 Connection example

Figure 5-28 shows a PCMCIA connection example. In this example, the address and data are connected to the buffer so as to enable live wire insertion/removal of the card. DATAENA# is used to control the gate of the data buffer, and RD/WR# to control its direction. For control of the gate of the address buffer, ADRENA# can be used.

Be sure to supply power of the PCMCIA Slot A (VCC) to SLOT_A_VCC of CARD-E09A, and power of the PCMCIA Slot B (VCC) to SLOT_B_VCC.

Table 5-6 shows the power control signal as well as its relationship with the power voltage of the slot.

Table 5-6 PCMCIA Power Control

VPPPGM	VPPVCC	VCC5#	VCC3#	VCC (SLOT_VCC)	VPP
L	L	H	H	0V	0V
L	L	L	H	5V	0V
L	L	H	L	3.3V	0V
L	H	L	H	5V	5V
L	H	H	L	3.3V	3.3V
H	L	L	H	5V	12V
H	L	H	L	3.3V	12V
L	L	L	H	5V	0V
L	L	H	L	3.3V	0V

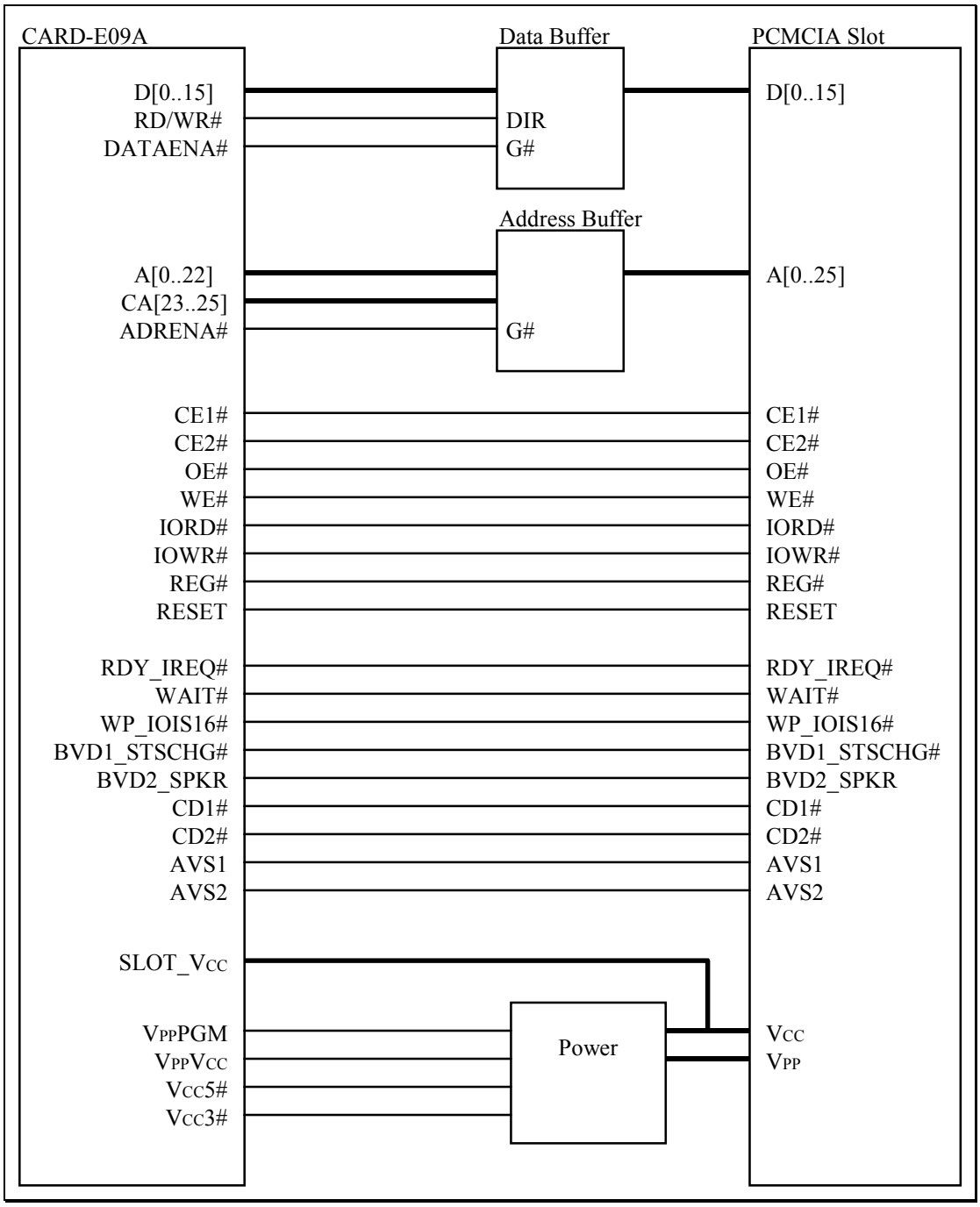


Figure 5-28 PCMCIA Connection Example

5.12.10 CompactFlash

The CARD-E09A provides a connector for CompactFlash cards. A CompactFlash card can be used simply by inserting it into the connector.

The VCC of the CARD-E09A provides the power to the CompactFlash card. For this reason, VCC must meet the rating requirements of CompactFlash cards. Also, as the CARD-E09A does not control the power of the CompactFlash interface, inserting or removing a CompactFlash card can only be performed when the power of the CARD-E09A is turned off.

5.13 ISA Interface

5.13.1 Overview

The CARD-E09A supports ISA interface to allow for easy use of controller, etc. on the ISA bus. The Companion Chip generates ISA interface signals from the control signal output from SH7709A. The ISA interface supports the following functions:

- Read/write of 8- or 16-bit memory devices
- Read/write of 8- or 16-bit I/O devices
- Insertion of hardware wait cycle based on IOCHRDY
- Interrupt

The following ISA bus functions are not supported:

- External bus master cycle
- Refresh cycle
- DMA (CARD-E09A and ISA bus differ in how their DMA functions)

5.13.2 Signals

The CARD-E09A does not have all of the ISA bus signals. The ISA interface signals are listed as follows:

RESETDRV	Initializes devices on the ISA bus interface.
A[0..21], CA[22..23]	Addresses of memory and I/O devices
D[0..15]	Data bus between memory and I/O devices and SH7709A
SBHE#	Indicates the upper 8 bits on the data bus is valid.
MEMR#	This signal permits memory device to drive data on the bus.
MEMW#	This signal instructs the memory device to take in data on the bus.
IOR#	This signal permits the I/O device to drive data on the bus.
IOW#	This signal instructs the I/O device to take in data on the bus.
MEMCS16#	This is an input signal to determines whether SH7709A can perform the 16-bit memory transmission.
IOCS16#	This is an input signal to determines whether SH7709A can perform the 16-bit I/O transmission.
IOCHRDY	If the I/O device as well as memory on the ISA interface need to stretch the bus cycle, this can be accomplished by setting this signal to LOW as soon as a valid address and command is detected.
IRQ[1..4]	This signal requests for interrupt from the device on the ISA bus interface.
ISADATAENA#	This signal controls the gate of a buffer if the buffer is placed at the data bus between the CARD-E09A and the device on the ISA bus interface,
RD/WR#	This signal controls the direction of a data bus buffer if it is placed.

The following signals are not supported:

SMEMR#, SMEMW#, AEN, DRQ, DACK#, TC, REFRESH#, MASTER#, SCLK, OSC, IOCHCK#, WS0#, BALE

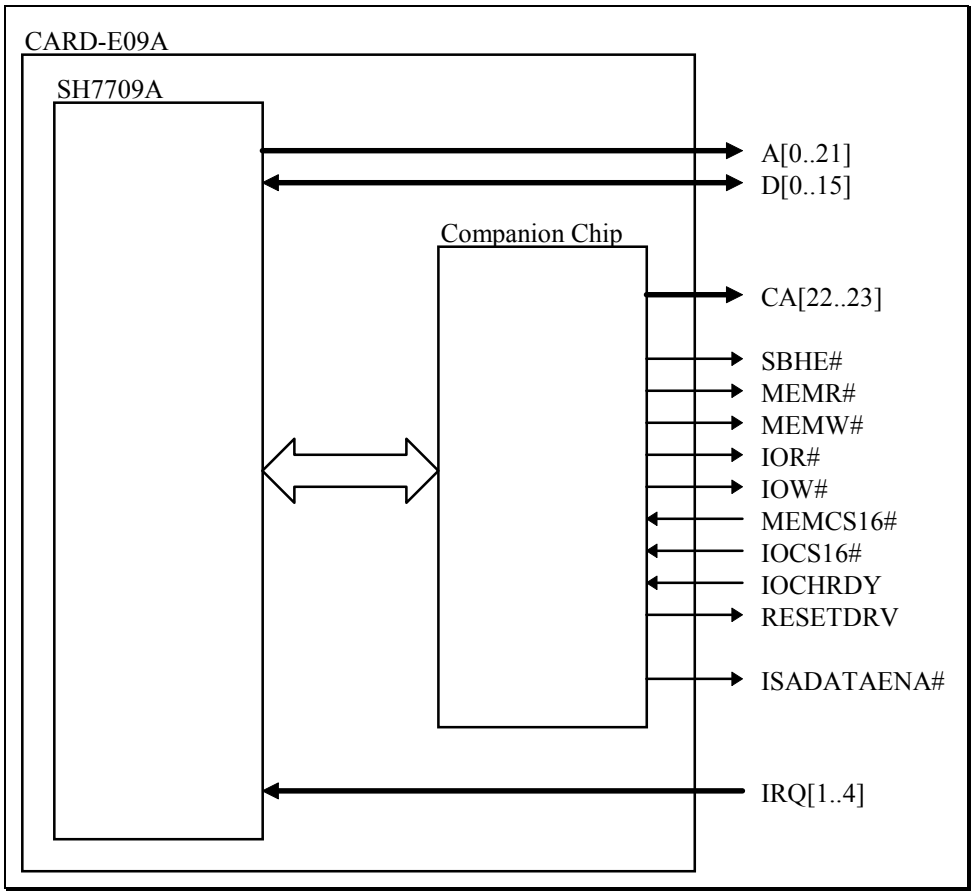


Figure 5-29 ISA Bus Interface Diagram

5.13.3 ISA interface memory map

While memory space and I/O space exist on the ISA bus, SH7709A contains only the memory space. Because of this difference, the 4 MB from 1B800000h to 1BBFFFFFh of SH7709A is mapped to the memory space of the ISA interface; and the 4 MB from 1BC00000h to 1BFFFFFFh is mapped to the I/O space. Because the ISA bus space is 16 MB, the address's upper two bits is specified by the ISA Address Register (Figure 5-30).

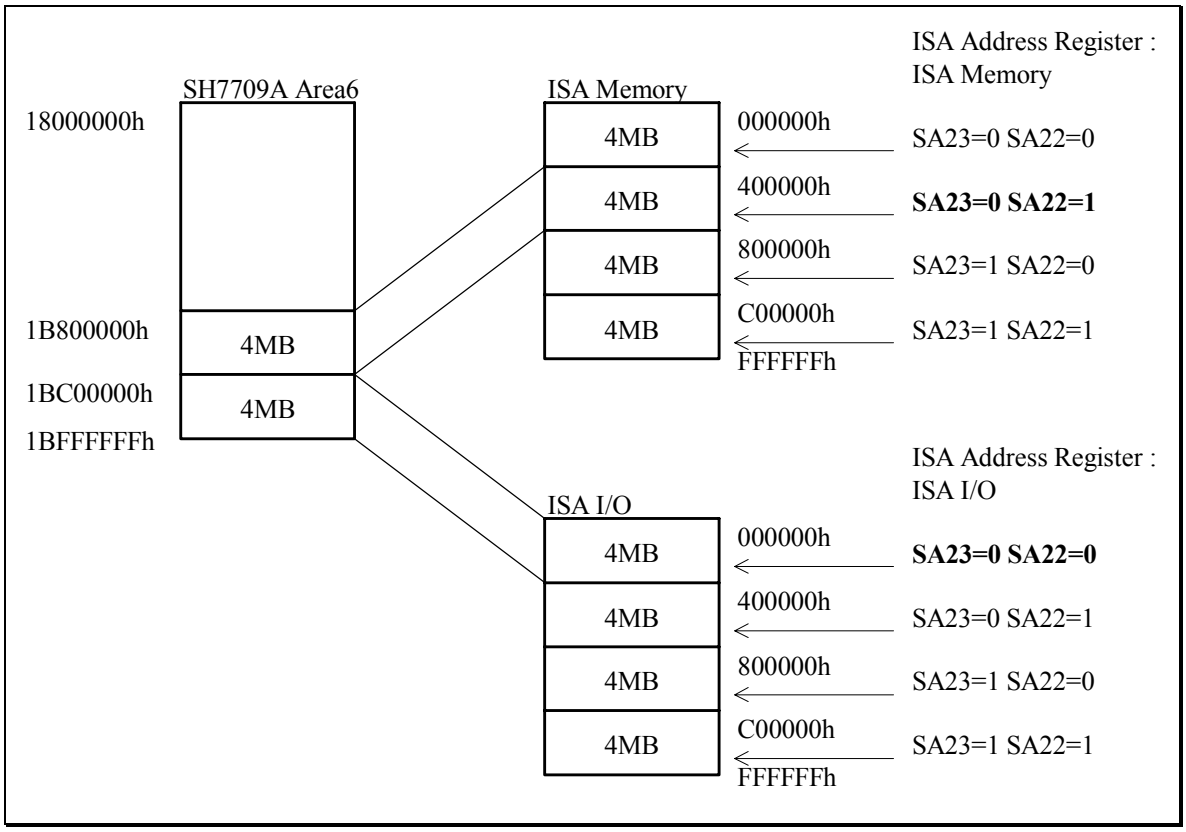


Figure 5-30 ISA Bus Memory Map

For example, when the ISA Address Register's ISA Memory SA23 is set to "0" and the ISA Memory SA22 to "1" and then 1B800000h is accessed, this means accessing the memory address 400000h of the ISA interface. When the ISA Address Register's ISA I/O SA23 is set to "0" and the ISA I/O SA23 to "0" and then 1BC003F0h is accessed, this means accessing the I/O address 0003FFh of the ISA interface. While the I/O space of the ISA bus is 64 KB, the I/O space of the ISA interface for the CARD-E09A is same as the memory space at 16 MB.

5.13.4 Registers

The ISA Address Register is shown as follows.

ISA Address Register

Address = 11000780h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ISA Bus Interface Enable		ISA I/O SA23	ISA I/O SA22			ISA Memory SA23	ISA Memory SA22

bit	Name	R/W	Description
1,0	ISA Memory SA23,22	R/W	These bits specify the upper 2 bits of the ISA Memory space's address.
3,2			
5,4	ISA I/O SA23,22	R/W	These bits specify the upper 2 bits of the ISA I/O space's address.
6			
7	ISA Bus Interface Enable	R/W	This bit enables or disables the ISA Bus Interface, as follows: 0 : ISA Bus Interface Disable 1 : ISA Bus Interface Enable

While the ISA interface is accessed via area 6 of SH7709A, to maintain compatibility area 6 and PTG7 of SH7709A must be set as follows:

Area 6	Access method	PCMCIA
	Bus width	16bit
	Wait number	2 wait insertion
	Idle cycle	2 idle cycle insertion
	Address -OE#/WE# asserted delay	1.5 cycle delay
	OE#/WE# negate address delay	3.5 cycle delay
PTG7	Pin function	Other functionIOIS16#

5.13.5 Timing

The ISA interface timing is shown in Figure 5-31 and Figure 5-32.

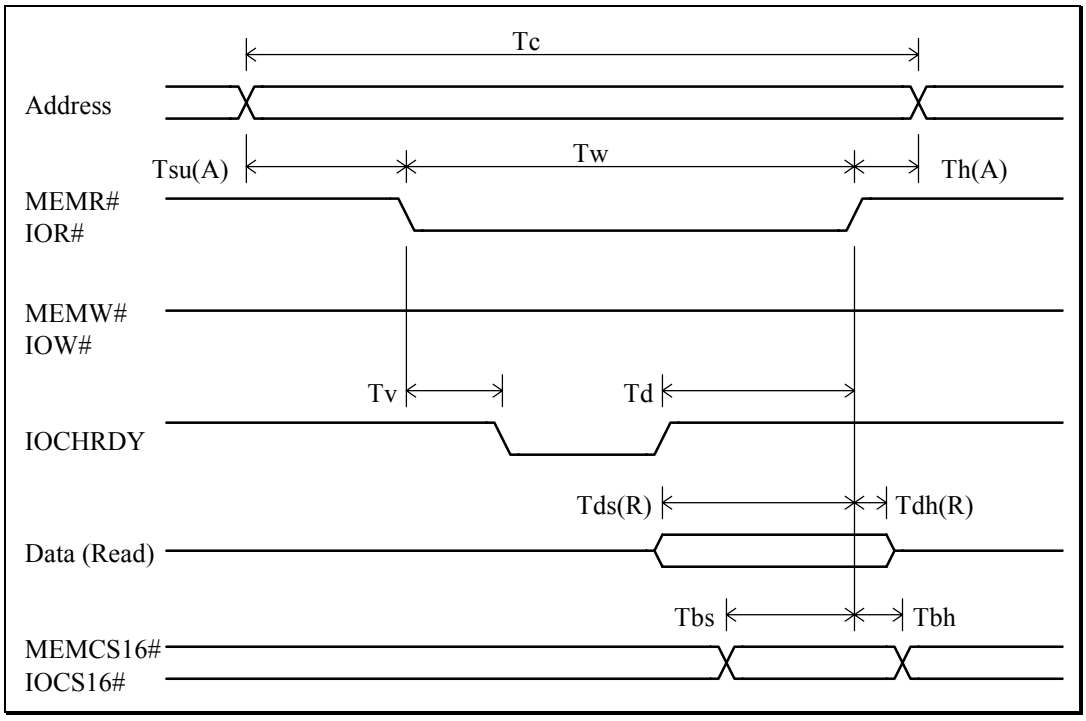


Figure 5-31 ISA Read Timing

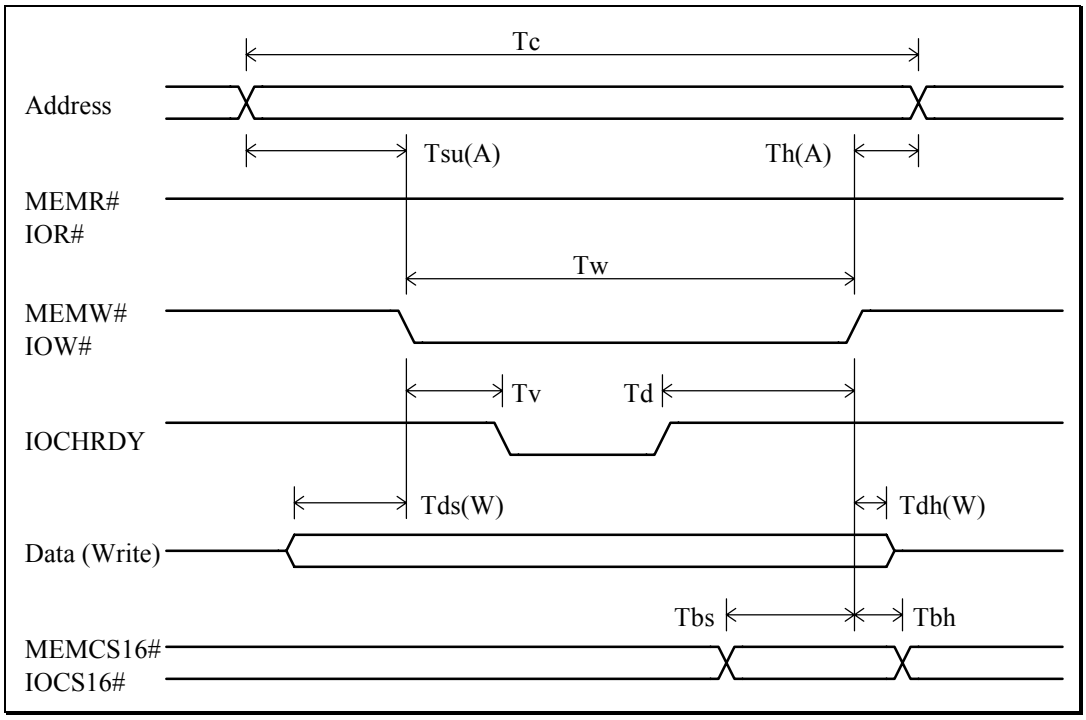


Figure 5-32 ISA Write Timing

Table 5-7 ISA Read/Write Timing

Parameter	Symbol	min.	typ.	max.	unit
Cycle Time	Tc	17			CKIO
Address Setup Time	Tsu(A)		6		CKIO
Address Hold Time	Th(A)		3		CKIO
Command Pulse Width	Tw		8		CKIO
IOCHRDY Valid from Command	Tv			4	CKIO
Command Hold Time from IOCHRDY Active	Td	4			CKIO
Data Setup Time (Read)	Tds(R)	0.5			CKIO
Data Hold Time (Read)	Tdh(R)	0			CKIO
Data Setup Time (Write)	Tds(W)		6		CKIO
Data Hold Time (Write)	Tdh(W)		3		CKIO
MEMCS16#/IOCS16# Setup Time	Tbs		2		CKIO
MEMCS16#/IOCS16# Hold Time	Tbh		0		CKIO

For detailed information on each of the parameters, see the "AC characteristics" section.

5.13.6 Connection example

Figure 5-33 shows a memory device connection example.

While there are two types of ISA bus addresses, LA[17:23] and SA[0..19], the CARD-E09A does not distinguish them. For the address of the memory device, connect each bit compatible with CA[22..23] and [0..21]. Because the CARD-E09A does not have BALE and REFRESH#, be sure to pull up these signals of the memory device. MEMCS16# and IOCHRDY require pull-up resistance.

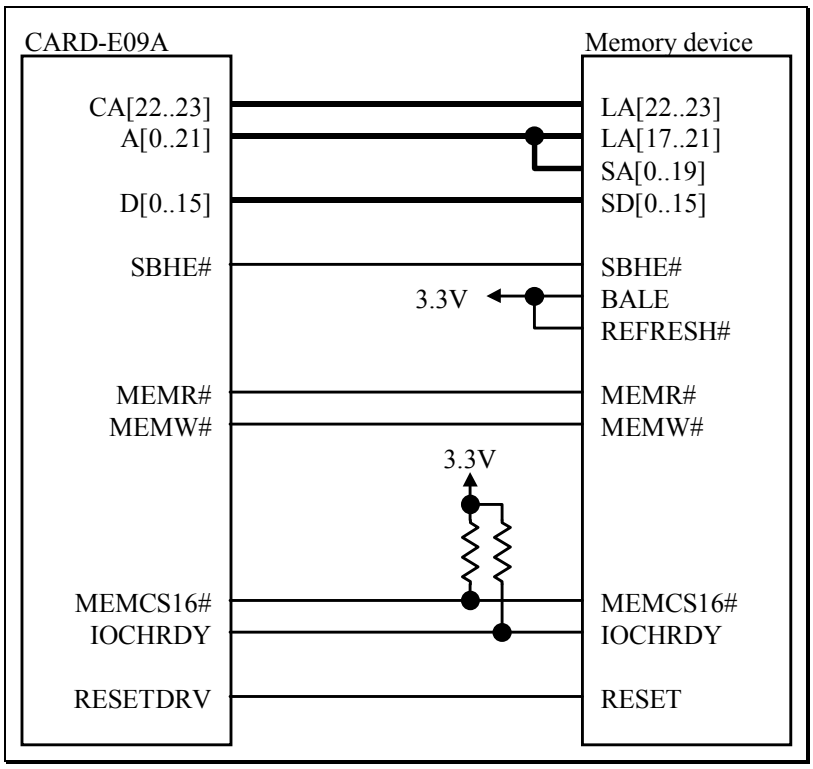


Figure 5-33 Memory Device Connection Example

Since SMEMR# and SMEMW# do not exist in the CARD-E09A, if they are required they must be generated outside the CARD-E09A. A circuitry example is shown in Figure 5-34.

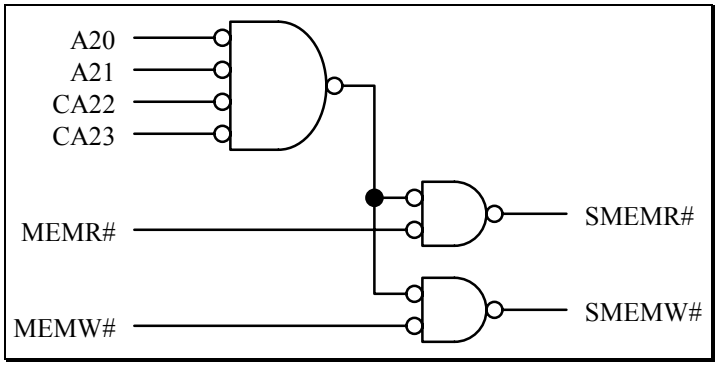


Figure 5-34 SMEMR# & SMEMW# Generation Example

Figure 5-35 shows an I/O device connection example. Since AENI does not exist in the CARD-E09A, be sure to apply pull-down at the I/O device. IOCS16# and IOCHRDY require pull-up resistance. The IRQ output of the I/O device can be input to IRQ[1..4] of the CARD-E09A.

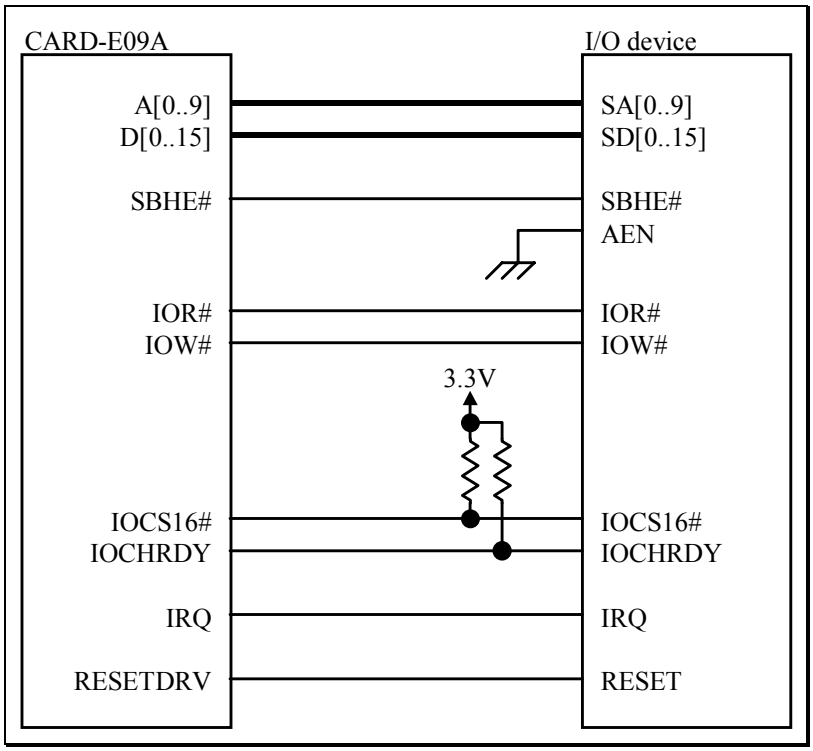


Figure 5-35 I/O Device Connection Example

The above connection example shows use of a 3.3V operating voltage of the device on the ISA interface. To operate at 5V, a buffer must be added in order to convert level of the data bus and IRQ. Because MEMCS16#, IOCS16# and IOCHRDY use the 5V trelant input, this requires only a pull-up operation to 5V; there is no need to add a buffer.

If a buffer is placed on the data bus to enable 5V operation or to remove the problem of insufficient drive power, ISADATAENA# can be used to control the gate of the buffer, and RD/WR# to control its direction.

5.14 CRT/LCD Interface

The CARD-E09A comes with the LCD controller SED1355 which has a CRT interface built in. For detailed information of this interface, refer to the SED1355 manual.

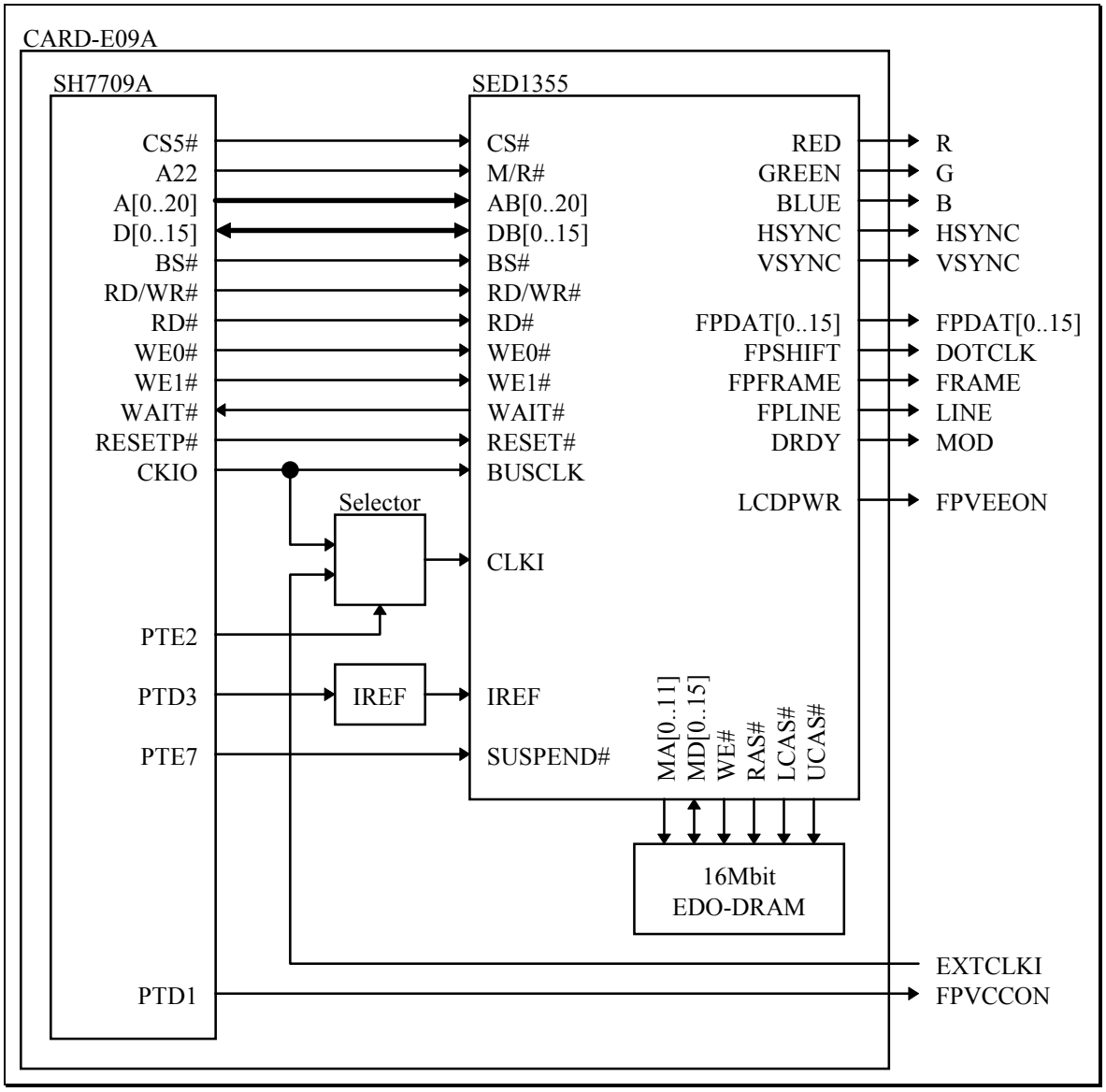


Figure 5-36 CRT/LCD Interface System Diagram

SED1355 is mapped to area 5 of SH7709A

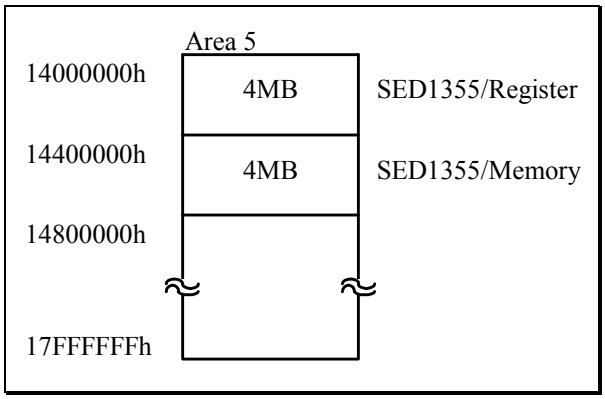


Figure 5-37 SH7709A Memory Map (SED1355)

The CARD-E09A makes use of several ports of SH7709A to control SED1355 and CRT/LCD interface.

Table 5-8 SH7709A Port Assignment

Port	Control
PTE7	This port controls the SUSPEND# pin of SED1355. When PTE7 is turned to LOW, SED1355 enters into the hardware-based suspend mode. During a reset operation, the pull-up resistance turns this port to HIGH.
PTD3	This port controls the fixed current circuitry of the CRT interface. When PTE7 is turned to HIGH, the fixed current circuitry is turned off. During the low power consumption mode (such as standby) or when the CRT interface is not used, be sure to set this port to HIGH. During a reset operation, the pull-up resistance turns this port to HIGH.
PTD1	This port controls the logic power of LCD. During a reset operation, the pull-up resistance turns this port to HIGH.
PTE2	This port selects the CLKI clock of SED1355. When PTE2 is HIGH, CLKI has CKIO input. When PTE2 is LOW, CLKI has EXTCLKI input.

5.15 AD/DA

SH7709A contains a 8-channel A/D converter and a 2-channel D/A converter. On the CARD-E09A, the AN4, AN5, DA0, A/D2 channel of DA1, and D/A2 channel are directly connected to the connectors. For detailed information and operation on the A/D converter and the D/A converter, refer to the SH7709A manual.

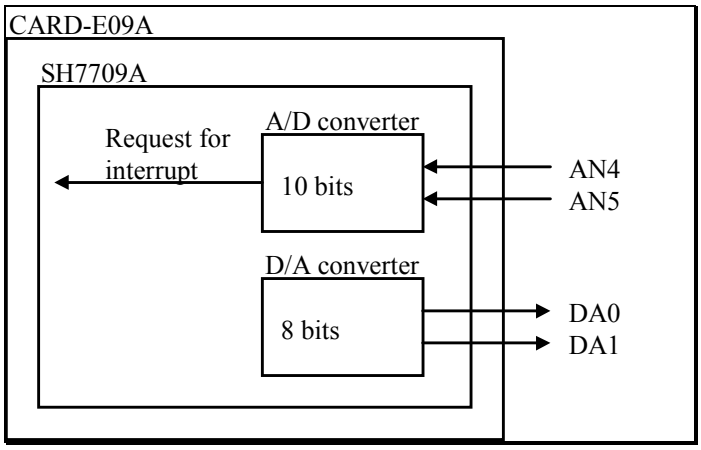


Figure 5-38 AD/DA Block Diagram

To prevent unusual voltage (such as excessive power surge) to damage the analog input pins (AN4,5), be sure to connect a protection circuitry such as the one shown in Figure 5-39.

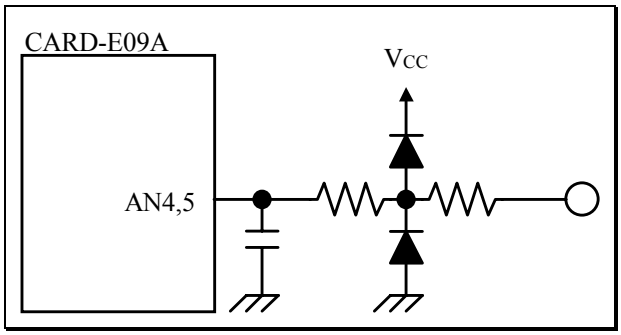


Figure 5-39 Analog Input Pin Protection Circuitry Example

5.16 Port

While SH7709A contains many I/O ports, the CARD-E09A can use the ports for generic input/ouput as shown in Figure 5-40. All of these ports allow for input (pull-up resistance can be turned on or off) or output. During a reset operation to return to the initial state, the pull-up resistance is turned on (as input). Also, these ports also function as SH7709A's port interrupt request input.

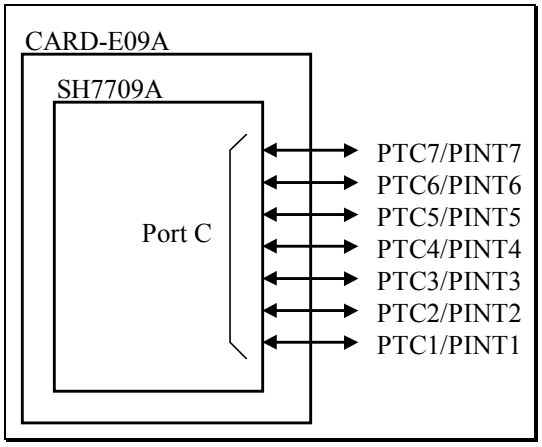
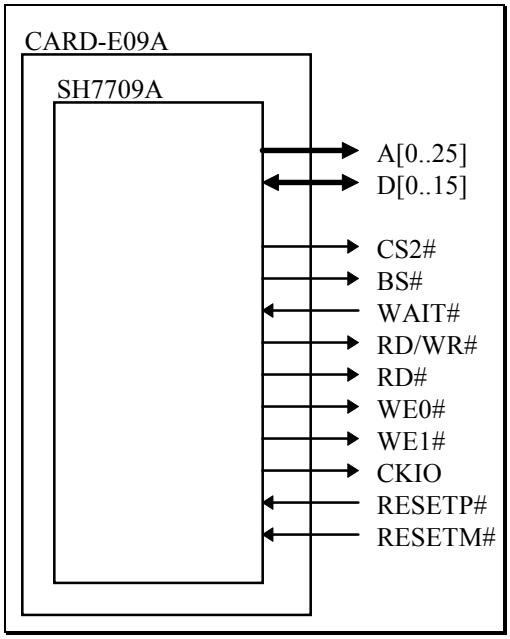


Figure 5-40 Port Diagram

5.17 SH7709A Bus

On the CARD-E09A, because the following signals are directly output to the connector from SH7709A, area 2 of SH7709 can be used outside of it.



A[0..25]	Address output
D[0..15]	Data input/output
CS2#	Area 2 chip select signal
BS#	Bus cycle start signal
WAIT#	Wait state request signal
RD/WR#	Data input/output direction signal
RD#	Read strobe signal
WE0#	Write strobe signal for D[0..7]
WE1#	Write strobe signal for D[8..15]
CKIO	Clock output
RESETP#	Power-on reset request
RESETM#	Manual reset request

Figure 5-41 SH7709A Bus Diagram

When area 2 is used externally, the memory that can be connected is normal memory such as SRAM and ROM; the data bus is 8- or 16-bit at Little Endian.
Functions that can be set at SH7709A (such as wait number) are reflected as they are.
For detailed information on timing, etc., refer to the SH7709A manual.

WAIT#

The external circuitry can insert the wait state by turning WAIT# to become active. WAIT# is also used inside the CARD-E09A, and wired door with WAIT# from the connector. For this reason, outside the CARD-E09A it must be driven at open-drain. However, because signal raise at usual open-drain is slow, timing check becomes difficult. In this situation, driving WAIT#, as shown in Figure 5-42, can be a solution. In this example, the software wait (wait inserted by registers of SH7709A) inserts two waits by using the three-wait, WAIT# input. The external device does not drive WAIT# when CS2# is inactive.(① in the figure). When CS2# becomes active, drive WAIT# to become HIGH or LOW. (② in the figure). And, set WAIT# to LOW at the fourth Tw raised edge so that "L" sampling is performed (③ in the figure). Next, to end the cycle, set WAIT# to HIGH at T2's raised edge so that "H" sampling is performed (④ in the figure). Finally, when CS2# becomes inactive, stop the WAIT# drive (⑤ in the figure). Wait# is pulled up inside the CARD-E09A. Because WAIT# is input into SH7709A as it is, be sure to use it as the signal which has secured the setup and holdtime of CKIO.

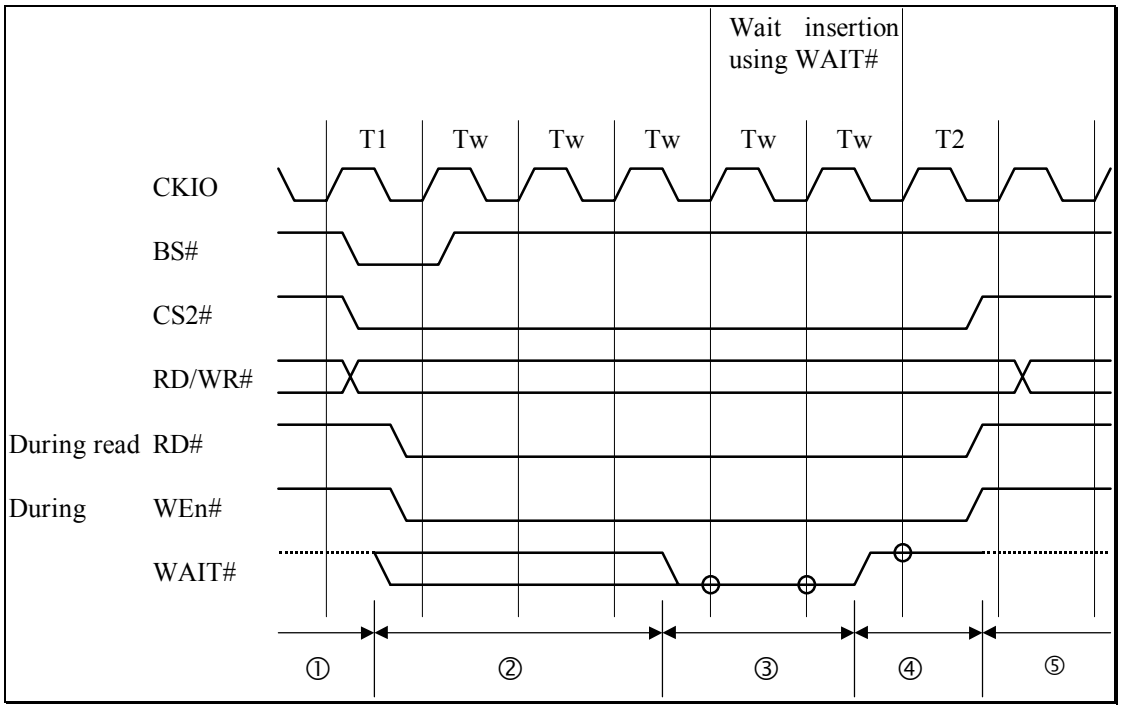


Figure 5-42 WAIT# Example

5.18 Baud Rate Generator

The Companion Chip built into the CARD-E09A use the Baud Rate Generator (BRG) to generate UART (Serial 3 and 4) and 8254 clocks through CKIO.

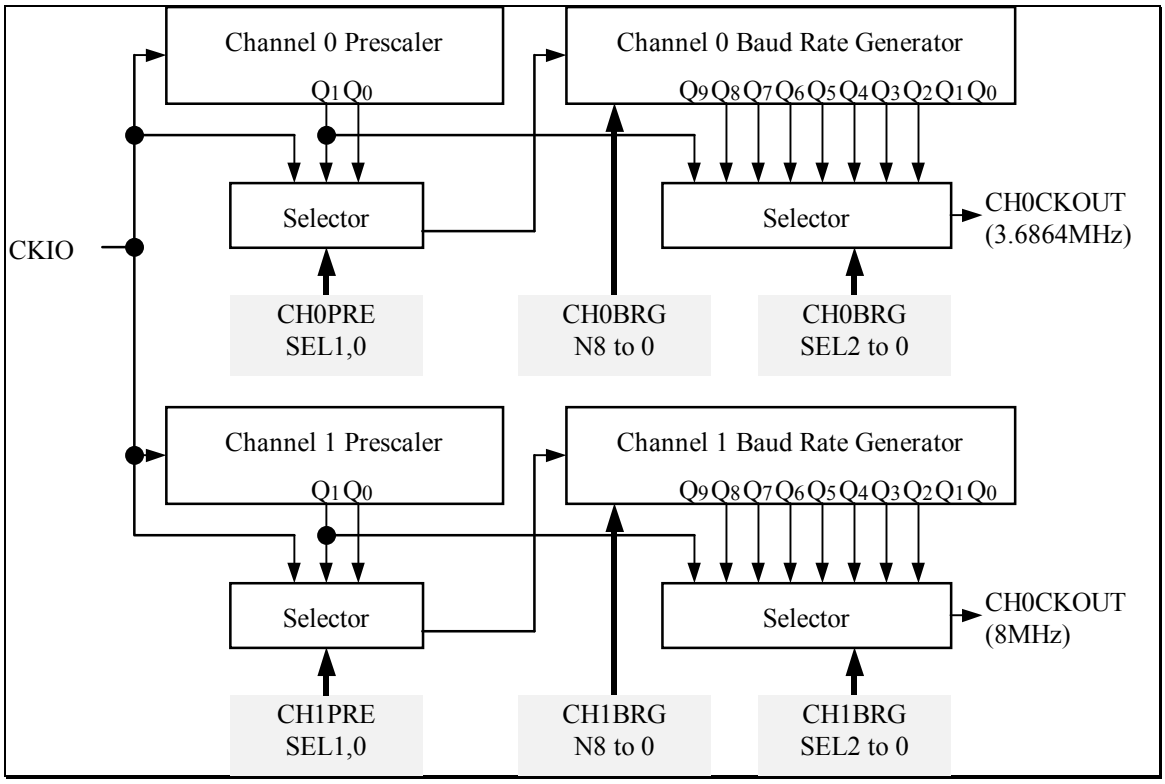


Figure 5-43 BRG Block Diagram (1)

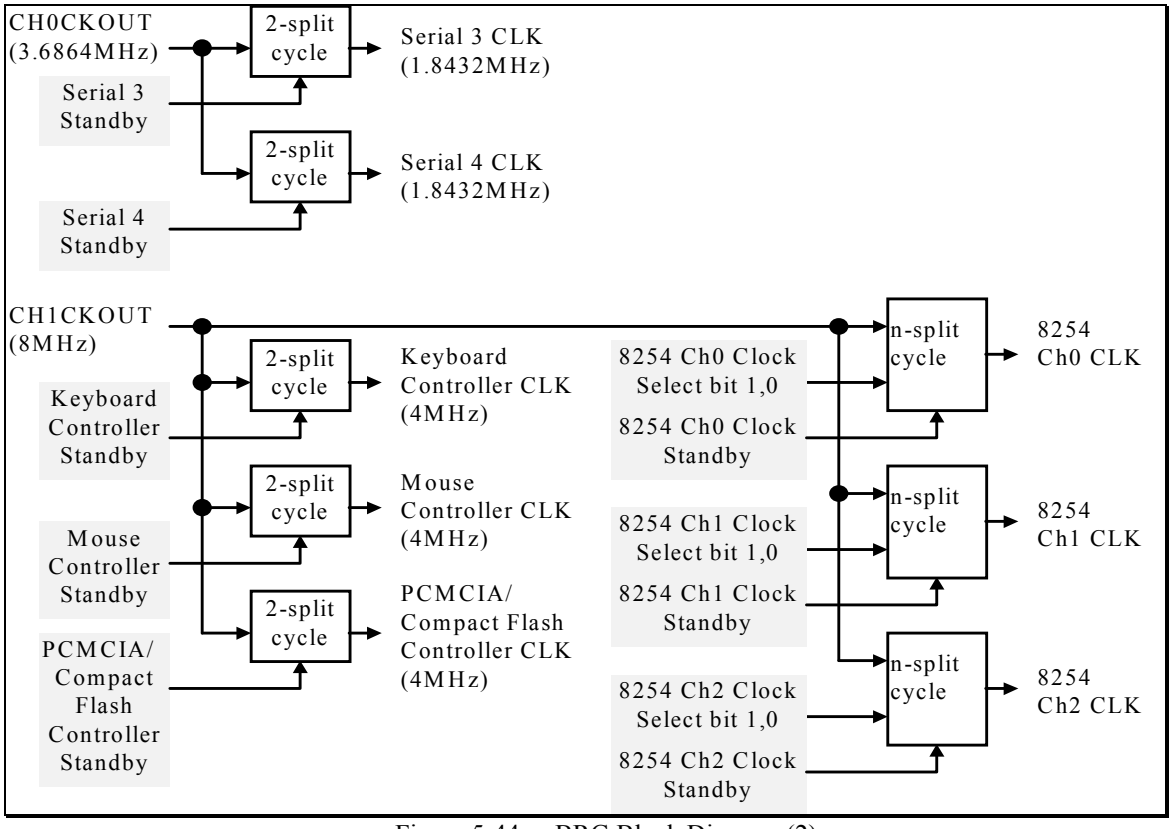


Figure 5-44 BRG Block Diagram (2)

5.18.1 Registers

The following registers can be used at the BRG to set the output frequency.

CH0BRG Control Register 0

Address = 11000800h
Reset = FFh

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CH0BRG N7	CH0BRG N6	CH0BRG N5	CH0BRG N4	CH0BRG N3	CH0BRG N2	CH0BRG N1	CH0BRG N0

bit	Name	R/W	Description
7-0	CH0BRGN7-0	R/W	These bits set the split cycle ratio of the channel 0 baud rate generator. The split cycle ratio is set up using the 9 bits from CH0BRGN8 to CH0BRGN0, but 8 out of the 9 bits are set using these registers. Be sure to set the output signal CH0CKOUT of the channel 0 baud rate generator to 3.6864 MHz. At the Companion Chip, the signal CH0CKOUT with 2-split cycle becomes the base clock of Serial 3 and 4. The initial value of this register is "FFh".

CH0BRG Control Register 1

Address = 11000802h
Reset = 01h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	CH0BRG SEL2	CH0BRG SEL1	CH0BRG SEL0	CH0PRE SEL1	CH0PRE SEL0		CH0BRG N8

bit	Name	R/W	Description
0	CH0BRGN8	R/W	This bit sets the uppermost bit of the split cycle ratio of the channel 0 baud rate generator. Its initial value is "1".
1			
3,2	CH0PRESEL1,0	R/W	These bits set the split cycle ratio of the channel 0 pre-scaler. CH0PRESEL1,0 0,0 : 1/1 0,1 : 1/2 1,0 : 1/4 1,1 : Stops clock at CH0BRG.
6,5,4	CH0BRGSEL2,1,0	R/W	These bits select the clock output capture position of the channel 0 baud rate generator. The split cycle ratio of pre-scaler, the split cycle ratio of the baud rate generator, and this capture position together determine the frequency of CHOCKOUT. CH0BRGSEL2,1,0 CH0BRGSEL2,1,0 0,0,0 : CH0BRGQ6 0,0,1 : CH0BRGQ5 0,1,0 : CH0BRGQ4 0,1,1 : CH0BRGQ3 1,0,0 : CH0BRGQ2 1,0,1 : CH0PREQ1(2-split cycle of CKIO) 1,1,0 : CH0BRGQ8 1,1,1 : CH0BRGQ7
7			

CH0 Test Control Register

Address = 11000804h
Reset = 00h

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

CH0 Test Status Register 0

Address = 11000806h
Reset = Not fixed

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

CH0 Test Status Register 1

Address = 11000806h
Reset = Not fixed

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

CH1BRG Control Register 0

Address = 11000808h
Reset = FFh

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CH1BRG N7	CH1BRG N6	CH1BRG N5	CH1BRG N4	CH1BRG N3	CH1BRG N2	CH1BRG N1	CH1BRG N0

bit	Name	R/W	Description
7-0	CH1BRGN7-0	R/W	These bits set the split cycle ratio of the channel 1 baud rate generator. The split cycle ratio is set up using the 9 bits from CH10BRGN to CH10BRGN0, but 8 out of the 9 bits are set using these registers. Be sure to set the output signal CH1CKOUT of the channel 1 baud rate generator to 8 MHz. At the Companion Chip, the CH1CKOUT signal with 2-split cycle becomes the base clock of the keyboard/mouse controller.

CH1BRG Control Register 1

Address = 1100080Ah
Reset = 01h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	CH1BRG SEL2	CH1BRG SEL1	CH1BRG SEL0	CH1PRE SEL1	CH1PRE SEL0		CH1BRG N8

bit	Name	R/W	Description
0	CH1BRGN8	R/W	This bit sets the uppermost bit of the split cycle ratio of the channel 1 baud rate generator. Its initial value is "1".
1			
3,2	CH1PRESEL1,0	R/W	These bits set the split cycle ratio of the channel 1 pre-scaler. CH1PRESEL1,0 0,0 : 1/1 0,1 : 1/2 1,0 : 1/4 1,1 : Stops clock at CH1BRG.

bit	Name	R/W	Description
6,5,4	CH1BRGSEL2,1,0	R/W	These bits select the clock output capture position of the channel 1 baud rate generator. The split cycle ratio of pre-scaler, the split cycle ratio of the baud rate generator, and this capture position together determine the frequency of CH1CKOUT. CH1BRGSEL2,1,0 CH1BRGSEL2,1,0 0,0,0 : CH1BRGQ6 0,0,1 : CH1BRGQ5 0,1,0 : CH1BRGQ4 0,1,1 : CH1BRGQ3 1,0,0 : CH1BRGQ2 1,0,1 : CH1PREQ1(2-split cycle of CKIO) 1,1,0 : CH1BRGQ8 1,1,1 : CH1BRGQ7
7			

CH1 Test Control Register

Address = 1100080Ch
Reset = 00h

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

CH1 Test Status Register 0

Address = 1100080Eh
Reset = Not fixed

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

CH1 Test Status Register 1

Address = 1100080Eh
Reset = Not fixed

This register is used for testing the Companion Chip. During normal operation, this register has no meaning.

Power Management Register

Address = 11000700h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8254 Ch2 Clock Standby	8254 Ch1 Clock Standby	8254 Ch0 Clock Standby	PCMCIA/ Compact -Flash Interface Standby	Mouse Controller Standby	Keyboard Controller Standby	Serial 4 Standby	Serial 3 Standby

bit	Name	R/W	Description
0	Serial 3 Standby	R/W	This bit stops the clock of Serial 3.
1	Serial 4 Standby	R/W	This bit stops the clock of Serial 4.
2	Keyboard Controller Standby	R/W	This bit stops the clock of the keyboard controller.
3	Mouse Controller Standby	R/W	This bit stops the clock of the mouse controller.
4	PCMCIA/CompactFlash Interface Standby	R/W	This bit stops the clock of the PCMCIA/CompactFlash controller.

bit	Name	R/W	Description
5	8254 Ch0 Clock Standby	R/W	This bit stops the clock of 8254 Ch0.
6	8254 Ch1 Clock Standby	R/W	This bit stops the clock of 8254 Ch1.
7	8254 Ch2 Clock Standby	R/W	This bit stops the clock of 8254 Ch2.

8254 Control Register

Address = 11000702h
Reset = 00h

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		8254 Ch2 Clock Select bit 1	8254 Ch2 Clock Select bit 0	8254 Ch1 Clock Select bit 1	8254 Ch1 Clock Select bit 0	8254 Ch0 Clock Select bit 1	8254 Ch0 Clock Select bit 0

bit	Name	R/W	Description
1,0	8254 Ch0 Clock Select bit 1,0	R/W	These bits specify the 8254 Ch0 clock speed. bit1 bit0 0 0 : 62.5KHz 0 1 : 250KHz 1 0 : 1MHz 1 1 : 4MHz
3,2	8254 Ch1 Clock Select bit 1,0	R/W	These bits specify the 8254 Ch1 clock speed. bit1 bit0 0 0 : 62.5KHz 0 1 : 250KHz 1 0 : 1MHz 1 1 : 4MHz
5,4	8254 Ch2 Clock Select bit 1,0	R/W	These bits specify the 8254 Ch2 clock speed. bit1 bit0 0 0 : 61.0Hz 0 1 : 976.6Hz 1 0 : 15.6KHz 1 1 : 250KHz
7, 6			

Test Register

Address = 11000704h
Reset = 00h

This register is used for testing the Companion Chip. During normal operation, set it to "00".

5.18.2 Setting the output frequency

The BRG output frequency is determined by the following formula:

$$CHxCKOUT = CKIO \times \frac{1}{X} \times \frac{512}{512 + Y} \times \frac{1}{Z}$$

Note) If BRGSEL2-0 = 1,0,1, CHxCKOUT = CKIO/2.

In the formula, X is determined by the CHxPRESEL1,0 bits of CHxBRG Control Register 1.

X	PRE SEL1	PRE SEL0
1	0	0
2	0	1
4	1	0

In the formula, Y is determined by the CHxBRGN8-0 bits of CHxBRG Control Register 1,0.

Y	BRG N8	BRG N7	BRG N6	BRG N5	BRG N4	BRG N3	BRG N2	BRG N1	BRG N0
1	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	1
3	0	0	0	0	0	0	0	1	0
4	0	0	0	0	0	0	0	1	1
5	0	0	0	0	0	0	1	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
508	1	1	1	1	1	1	0	1	1
509	1	1	1	1	1	1	1	0	0
510	1	1	1	1	1	1	1	0	1
511	1	1	1	1	1	1	1	1	0
512	1	1	1	1	1	1	1	1	1

In the formula, Z is determined by the CHxBRGSEL2-0 bits of CHxBRG Control Register 1.

Z	BRG SEL2	BRG SEL1	BRG SEL0
8	0	0	0
16	0	0	1
32	0	1	0
64	0	1	1
128	1	0	0
2	1	1	0
4	1	1	1

Table 5-9 shows an example on how to set up the registers for CKIO.

Table 5-9 BRG Register Value

		CH0 : CH0CKOUT 3.6864MHz				CH1 : CH1CKOUT 8MHz			
CKIO (MHz)		40	33.32	33.2	28.63	40	33.32	33.2	28.63
Output frequency (MHz)		3.68876	3.68941	3.68889	3.68758	8	8.33	8.3	8.18182
Margin of error		0.06%	0.08%	0.07%	0.03%	0.00%	4.13%	3.75%	2.27%
PRE	SEL1	0	0	0	0	0	0	0	0
	SEL0	0	0	0	0	0	0	0	0
BRG	(N9)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	N8	0	0	0	1	0	1	1	1
	N7	1	0	0	1	0	1	1	0
	N6	0	1	0	1	1	1	1	1
	N5	1	0	1	1	1	1	1	1
	N4	1	0	1	0	1	1	1	1
	N3	0	0	1	0	1	1	1	1
	N2	1	0	1	0	1	1	1	1
	N1	0	0	1	0	1	1	1	1
	N0	1	1	1	1	1	1	1	1
BRG	SEL2	0	0	0	1	1	1	1	1
	SEL1	0	0	0	1	1	1	1	1
	SEL0	0	0	0	1	1	0	0	0
CH0BRG Control Register 0		B5h	41h	3Fh	E1h	-	-	-	-
CH0BRG Control Register 1		00h	00h	00h	71h	-	-	-	-
CH1BRG Control Register 0		-	-	-	-	7Fh	FFh	FFh	7Fh
CH1BRG Control Register 1		-	-	-	-	70h	61h	61h	61h

6 ENVIRONMENTAL CHARACTERISTICS

6.1 Temperature

Operating temperature	Ta = 0 to 60°C	
Storage temperature	Ta = -20 to 85°C	(no condensation)

6.2 Humidity

Storage humidity	0 to 90%	(no condensation)

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute maximum rating

Item		Rating	Unit	Note
Electrical voltage	V_{CORE}	-0.3 to 2.5	V	
	V_{CC}	-0.3 to 4.0	V	(Note1)
	SLOT_A_V_{CC}	-0.3 to 7.0	V	
	SLOT_B_V_{CC}	-0.3 to 7.0	V	
	V_{BK}	-0.3 to 7.0	V	
Input voltage	V_I	-0.3 to V_{CC}+0.3	V	
		-0.3 to 7.5V	V	(Note2)
		-0.3 to SLOT_A_V_{CC}+0.5	V	Power Line is the pin of SLOT_A_V_{CC}.
		-0.3 to SLOT_B_V_{CC}+0.5	V	Power Line is the pin of SLOT_B_V_{CC}.

(Note1) This absolute maximum rating does not include a CompactFlash card.
(Note2) KBCLK, KBDATA, MSCLK, MSDATA, STROBE#, AFD#, INIT#, SLCTIN#, SLCT, PE, ERROR, ACK#, BUSY, LPTD[0..7], IOCHRDY, IOCS16#, MEMCS16#

7.2 Recommended operating condition

Item		min.	typ.	max.	Unit	Note
Electrical voltage	V_{CORE}	1.8	1. 9	2.0	V	
	V_{CC}	3.15	3.3	3.45	V	(Note3)
	SLOT_A_V_{CC}	3.15	3.3	3.45	V	Power can be turned off.
		4.5	5.0	5.5		(Note4)
	SLOT_B_V_{CC}	3.15	3.3	3.45	V	Power can be turned off.
		4.5	5.0	5.5		(Note4)
	V_{BK}	3.15	3.3	3.45	V	While operating (same as V_{CC})
		2.0		3.6	V	During backup

(Note3) This recommended operating condition does not include a CompactFlash card.
(Note4) When SLOT_A_V_{CC} or SLOT_B_V_{CC} is not off, set as:
SLOT_A_V_{CC} ≥ V_{CC}
SLOT_B_V_{CC} ≥ V_{CC}

7.3 Current Consumption

Measurement condition
- OS : Windows CE
- Display : CRT = 640 × 480, 256 colors
  LCD = Off
- CompactFlash : Not include
- PCMCIA Slot : Slot-A = ATA
  Slot-B = ATA
- Temperature : Ta = 25°C

SCE8700C01 (133MHz. 16MB SDRAM)

Item		min.	typ.	max.	Unit	Note
Current Consumption	I_{VCORE}		200	350	mA	Operating V_{CORE}=1.9V
			0.5	2.0	mA	Standby V_{CORE}=1.9V
	I_{VCC}		150	300	mA	Operating V_{CC}=3.3V
			1.1	3.3	mA	Standby V_{CC}=3.3V
	$I_{SLOT\_A\_VCC}$			300	µA	Operating SLOT_A_V_{CC}=5.0V
	$I_{SLOT\_B\_VCC}$			300	µA	Operating SLOT_B_V_{CC}=5.0V
	I_{VBK}			30	µA	When RTC-4543 is accessed V_{BK}=V_{CC}
				3	µA	When RTC-4543 is not accessed V_{BK}=V_{CC}
			1	3	µA	Backup V_{BK}=3.0V

SCE8700C02 (133MHz. 32MB SDRAM)

Item		min.	typ.	max.	Unit	Note
Current Consumption	I_{VCORE}		200	350	mA	Operating V_{CORE}=1.9V
			0.5	2.0	mA	Standby V_{CORE}=1.9V
	I_{VCC}		170	350	mA	Operating V_{CC}=3.3V
			1.7	4.5	mA	Standby V_{CC}=3.3V
	$I_{SLOT\_A\_VCC}$			300	µA	Operating SLOT_A_V_{CC}=5.0V
	$I_{SLOT\_B\_VCC}$			300	µA	Operating SLOT_B_V_{CC}=5.0V
	I_{VBK}			30	µA	When RTC-4543 is accessed V_{BK}=V_{CC}
				3	µA	When RTC-4543 is not accessed V_{BK}=V_{CC}
			1	3	µA	Backup V_{BK}=3.0V

7.4 Pin characteristics

Pull-up resistance

Pin	Group	Name	Type	Power Line	Termination (3.3v/5v)
1	Power	GND	Power	-	-
2	Slot_B	BCD1#	I	VCC	100KPU
3		BCE1#	Tri	SLOT_B_VCC	-
4		BCE2#	Tri	SLOT_B_ VCC	-
5		BOE#	Tri	SLOT_B_ VCC	-
6		SLOT_B_ VCC	Power	-	-
7		BVS1	I	VCC	100KPU
8		BIORD#	Tri	SLOT_B_ VCC	-
9		BIOWR#	Tri	SLOT_B_ VCC	-
10		BWE#	Tri	SLOT_B_ VCC	-
11		BRDY_IRQ#	I	SLOT_B_ VCC	100K/60KPU
12		BVS2	I	VCC	100KPU
13		BRESET	Tri	SLOT_B_ VCC	-
14		BWAIT#	I	SLOT_B_ VCC	100K/60KPU
15	Power	VCC	Power	-	-
16	Slot_B	BREG#	Tri	SLOT_B_ VCC	-
17		BBVD2_SPKR	I	SLOT_B_ VCC	100K/60KPU
18		BBVD1_STSCHG#	I	SLOT_B_ VCC	100K/60KPU
19		BWP_IOIS16#	I	SLOT_B_ VCC	100K/60KPU
20	Power	GND	Power	-	-
21	Slot_B	BCD2#	I	VCC	100KPU
22		BADRENA#	O	VCC	-
23		BDATAENA#	O	VCC	-
24		BVPPPGM	O	VCC	-
25		BVPP VCC	O	VCC	-
26		B VCC5#	O	VCC	-
27		BVCC3#	O	VCC	-
28	KB/MS	KBCLK	I/OD	VCC	External
29		KBDATA	I/OD	VCC	External
30		MSCLK	I/OD	VCC	External
31		MSDATA	I/OD	VCC	External
32	ISA	RESETDRV	O	VCC	-
33		IOCHRDY	I	VCC	External
34		IOW#	O	VCC	-
35		IOR#	O	VCC	-
36		MEMCS16#	I	VCC	External
37		SBHE#	O	VCC	-
38		IOCS16#	I	VCC	External
39		MEMR#	O	VCC	-
40		MEMW#	O	VCC	-
41	Power	GND	Power	-	-
42	ISA	ISADATAENA#	O	VCC	-
43	Serial 4	RI4#	I	VCC	50KPU
44		DTR4#	O	VCC	-
45	Power	VCORE	Power	-	-
46		VCORE	Power	-	-
47	Serial 4	CTS4#	I	VCC	50KPU
48		TXD4	O	VCC	-
49		RTS4#	O	VCC	-
50		RXD4	I	VCC	50KPU
51		DSR4#	I	VCC	50KPU
52		DCD4#	I	VCC	50KPU
53	Serial 3	RI3#	I	VCC	50KPU
54		DTR3#	O	VCC	-
55		CTS3#	I	VCC	50KPU
56		TXD3	O	VCC	-
57		RTS3#	O	VCC	-
58		RXD3	I	VCC	50KPU

Pin	Group	Name	Type	Power Line	Termination (3.3v/5v)
59	Serial 3	DSR3#	I	VCC	50KPU
60		DCD3#	I	VCC	50KPU
61	Power	GND	Power	-	-
62	SH-Bus	CKIO	O	VCC	-
63	Timer	TCLK	I	VCC	100KPU
64	SH-Bus	RESETP#	I	VCC	-
65		RESETM#	I	VCC	-
66		WAIT#	I	VCC	4.7KPU
67		CS2#	O	VCC	-
68		CS0#	O	VCC	-
69		RD/WR#	O	VCC	-
70		WE1#	O	VCC	-
71		WE0#	O	VCC	-
72		RD#	O	VCC	-
73		BS#	O	VCC	-
74		A25	O	VCC	HOLD
75		A24	O	VCC	HOLD
76		A23	O	VCC	HOLD
77	Power	VCC	Power	-	-
78	SH-Bus	A22	O	VCC	HOLD
79		A21	O	VCC	-
80		A20	O	VCC	-
81		A19	O	VCC	-
82	Power	GND	Power	-	-
83	SH-Bus	A18	O	VCC	-
84		A17	O	VCC	-
85		A16	O	VCC	-
86		A15	O	VCC	-
87		A14	O	VCC	-
88		A13	O	VCC	-
89		A12	O	VCC	-
90		A11	O	VCC	Hold
91		A10	O	VCC	Hold
92		A9	O	VCC	Hold
93		A8	O	VCC	Hold
94		A7	O	VCC	Hold
95		A6	O	VCC	Hold
96		A5	O	VCC	Hold
97		A4	O	VCC	Hold
98		A3	O	VCC	Hold
99		A2	O	VCC	Hold
100		A1	O	VCC	Hold
101	Power	GND	Power	-	-
102	SH-Bus	A0	O	VCC	Hold
103		D15	I/O	VCC	100KPU
104		D14	I/O	VCC	100KPU
105		D13	I/O	VCC	100KPU
106	Power	VCC	Power	-	-
107	SH-Bus	D12	I/O	VCC	100KPU
108		D11	I/O	VCC	100KPU
109		D10	I/O	VCC	100KPU
110		D9	I/O	VCC	100KPU
111		D8	I/O	VCC	100KPU
112		D7	I/O	VCC	HOLD
113		D6	I/O	VCC	HOLD
114		D5	I/O	VCC	HOLD
115		D4	I/O	VCC	HOLD
116		D3	I/O	VCC	HOLD
117		D2	I/O	VCC	HOLD
118		D1	I/O	VCC	HOLD
119		D0	I/O	VCC	HOLD

Pin	Group	Name	Type	Power Line	Termination (3.3v/5v)
120	Power	GND	Power	-	-
121		GND	Power	-	-
122	Slot_A	ACD1#	I	VCC	100KPU
123		ACE1#	Tri	SLOT_A_VCC	-
124		ACE2#	Tri	SLOT_A_VCC	-
125		AOE#	Tri	SLOT_A_VCC	-
126		SLOT_A_VCC	Power	-	-
127		AVS1	I	VCC	100KPU
128		AIORD#	Tri	SLOT_A_VCC	-
129		AIOWR#	Tri	SLOT_A_ VCC	-
130	SH-Bus	AWE#	Tri	SLOT_A_ VCC	-
131		ARDY_IRQ#	I	SLOT_A_ VCC	100K/60KPU
132		AVS2	I	VCC	100KPU
133		ARESET	Tri	SLOT_A_ VCC	-
134		AWAIT#	I	SLOT_A_ VCC	100K/60KPU
135	Power	VCC	Power	-	-
136	Slot_A	AREG#	Tri	SLOT_A_ VCC	-
137		ABVD2_SPKR	I	SLOT_A_ VCC	100K/60KPU
138		ABVD1_STSCHG#	I	SLOT_A_ VCC	100K/60KPU
139		AWP_IOIS16#	I	SLOT_A_ VCC	100K/60KPU
140	Power	GND	Power	-	-
141	Slot_A	ACD2#	I	VCC	100KPU
142		AADRENA#	O	VCC	-
143		ADATAENA#	O	VCC	-
144		AVPPPGM	O	VCC	-
145		AVPPVCC	O	VCC	-
146		AVCC5#	O	VCC	-
147		AVCC3#	O	VCC	-
148	PCMCIA	CA25	O	VCC	-
149		CA24	O	VCC	-
150	PCMCIA/ISA	CA23	O	VCC	-
151	Parallel	SLCT	I	VCC	External
152		PE	I	VCC	External
153		BUSY	I	VCC	External
154		ACK#	I	VCC	External
155		LPTD7	I/OD	VCC	External
156		LPTD6	I/OD	VCC	External
157		LPTD5	I/OD	VCC	External
158		LPTD4	I/OD	VCC	External
159		LPTD3	I/OD	VCC	External
160		SLCTIN#	I/OD	VCC	External
161	Power	GND	Power	-	-
162	Parallel	LPTD2	I/OD	VCC	External
163		INIT#	I/OD	VCC	External
164		LPTD1	I/OD	VCC	External
165	Power	VCORE	Power	-	-
166		VBK	Power	-	-
167	Parallel	ERROR#	I	VCC	External
168		LPTD0	I/OD	VCC	External
169		AFD#	I/OD	VCC	External
170		STROBE#	I/OD	VCC	External
171	PM	STANDBY#	O	VCC	-
172	Flash ROM	ROMDIS#	I	VCC	50KPU
173		RESERVE	-	-	-
174	Video	EXTCLKI	I	VCC	100KPU
175		RESERVE	-	-	-
176	ISA	CA22	O	VCC	-
177	Serial 0	TXD0	O	VCC	-
178		SCK0	O	VCC	-
179		RXD0	I	VCC	100KPU
180		AN4	I	VCC	-
181	Power	GND	Power	-	-

Pin	Group	Name	Type	Power Line	Termination (3.3v/5v)
182	AD/DA	AN5	I	VCC	-
183		DA1	O	VCC	-
184		DA0	O	VCC	-
185	Serial 1/Irda	TXD1	O	VCC	-
186		RXD1	I	VCC	100KPU
187	Serial 2	TXD2	O	VCC	-
188		RXD2	I	VCC	100KPU
189		RTS2#	O	VCC	-
190		CTS2#	I	VCC	100KPU
191	PM	PWOFF#	O	VCC	-
192		SRBTN#	I	VCC	60KPU
193	Video	FPVCCON	O	VCC	-
194	Port	PTC7/PINT7	I/O	VCC	60KPU
195		PTC6/PINT6	I/O	VCC	60KPU
196		PTC5/PINT5	I/O	VCC	60KPU
197	Power	VCC	Power	-	-
198	Port	PTC4/PINT4	I/O	VCC	60KPU
199		PTC3/PINT3	I/O	VCC	60KPU
200		PTC2/PINT2	I/O	VCC	60KPU
201		PTC1/PINT1	I/O	VCC	60KPU
202	Power	GND	Power	-	-
203	DMA	DACK0#	O	VCC	-
204		DREQ0#	I	VCC	100KPU
205		DACK1#	O	VCC	-
206		DREQ1#	I	VCC	100KPU
207	Interrupt	NMI	I	VCC	100KPU
208		IRQ1	I	VCC	60KPU
209		IRQ2	I	VCC	60KPU
210		IRQ3	I	VCC	60KPU
211		IRQ4	I	VCC	60KPU
212	Video	VSYNC	O	VCC	-
213		HSYNC	O	VCC	-
214		B	O	VCC	150PD
215		G	O	VCC	150PD
216		R	O	VCC	150PD
217		FPDAT15	O	VCC	-
218		FPDAT14	O	VCC	-
219		FPDAT13	O	VCC	-
220		FPDAT12	O	VCC	-
221	Power	GND	Power	-	-
222	Video	FPDAT11	O	VCC	-
223		FPDAT10	O	VCC	-
224		FPDAT9	O	VCC	-
225		FPDAT8	O	VCC	-
226	Power	VCC	Power	-	-
227	Video	FPDAT7	O	VCC	-
228		FPDAT6	O	VCC	-
229		FPDAT5	O	VCC	-
230		FPDAT4	O	VCC	-
231		FPDAT3	O	VCC	-
232		FPDAT2	O	VCC	-
233		FPDAT1	O	VCC	-
234		FPDAT0	O	VCC	-
235		DOTCLK	O	VCC	-
236		MOD	O	VCC	-
237		FPVEEON	O	VCC	-
238		LINE	O	VCC	-
239		FRAME	O	VCC	-
240	Power	GND	Power	-	-

Pull-up resistance (CompactFlash connector)

Pin	Group	Name	Type	Power Line	Termination
1	CompactFlash	GND	Power	-	-
2		D3	I/O	VCC	Hold
3		D4	I/O	VCC	Hold
4		D5	I/O	VCC	Hold
5		D6	I/O	VCC	Hold
6		D7	I/O	VCC	Hold
7		CCE1#	O	VCC	-
8		A10	O	VCC	-
9		COE#	O	VCC	-
10		A9	O	VCC	-
11		A8	O	VCC	-
12		A7	O	VCC	-
13		VCC	Power	-	-
14		A6	O	VCC	-
15		A5	O	VCC	-
16		A4	O	VCC	-
17		A3	O	VCC	-
18		A2	O	VCC	-
19		A1	O	VCC	-
20		A0	O	VCC	-
21		D0	I/O	VCC	Hold
22		D1	I/O	VCC	Hold
23		D2	I/O	VCC	Hold
24		CWP_IOIS16#	I	VCC	100KPU
25		RESERVE	-	-	-
26		RESERVE	-	-	-
27		D11	I/O	VCC	100KPU
28		D12	I/O	VCC	100KPU
29		D13	I/O	VCC	100KPU
30		D14	I/O	VCC	100KPU
31		D17	I/O	VCC	100KPU
32		CCE2#	O	VCC	-
33		RESERVE	-	-	-
34		CIORD#	O	VCC	-
35		CIOWR#	O	VCC	-
36		CWE#	O	VCC	-
37		CRDY_IREQ#	I	VCC	100KPU
38		VCC	Power	-	-
39		RESERVE	-	-	-
40		RESERVE	-	-	-
41		RESET	O	VCC	-
42		CWAIT#	I	VCC	100KPU
43		RESERVE	-	-	-
44		CREG#	O	VCC	-
45		RESERVE	-	-	-
46		CBVD1_STSCHG#	I	VCC	100KPU
47		D8	I/O	VCC	100KPU
48		D9	I/O	VCC	100KPU
49		D10	I/O	VCC	100KPU
50		GND	Power	-	-

Output voltage

Pin	Group	Name	Type	Power Line	Drive (3.3v/5v) [mA]		Output voltage (3.3v/5v) [V]	
					IOL	IOH	VOL(max)	VOH (min)
1	Power	GND	Power	-	-	-	-	-
2	Slot_B	BCD1#	I	VCC	-	-	-	-
3		BCE1#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
4		BCE2#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
5		BOE#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC 0.4
6		SLOT_B_VCC	Power	-	-	-	-	-
7		BVS1	I	VCC	-	-	-	-
8		BIORD#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
9		BIOWR#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
10		BWE#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
11		BRDY_IRQ#	I	SLOT_B_VCC	-	-	-	-
12		BVS2	I	VCC	-	-	-	-
13		BRESET	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
14		BWAIT#	I	SLOT_B_VCC	-	-	-	-
15	Power	VCC	Power	-	-	-	-	-
16	Slot_B	BREG#	Tri	SLOT_B_VCC	2/3	-2/-3	0.4/0.4	SLOT_B_VCC -0.4
17		BBVD2_SPKR	I	SLOT_B_VCC	-	-	-	-
18		BBVD1_STSCHG#	I	SLOT_B_VCC	-	-	-	-
19		BWP_IOIS16#	I	SLOT_B_VCC	-	-	-	-
20	Power	GND	Power	-	-	-	-	-
21	Slot_B	BCD2#	I	VCC	-	-	-	-
22		BADRENA#	O	VCC	2	-2	0.4	VCC-0.4
23		BDATAENA#	O	VCC	2	-2	0.4	VCC-0.4
24		BVPPPGM	O	VCC	6	-6	0.4	VCC-0.4
25		BVPPVCC	O	VCC	6	-6	0.4	VCC-0.4
26		BVCC5#	O	VCC	6	-6	0.4	VCC-0.4
27		BVCC3#	O	VCC	6	-6	0.4	VCC-0.4
28	KB/MS	KBCLK	I/OD	VCC	12	-	0.4	-
29		KBDATA	I/OD	VCC	12	-	0.4	-
30		MSCLK	I/OD	VCC	12	-	0.4	-
31		MSDATA	I/OD	VCC	12	-	0.4	-
32	ISA	RESETDRV	O	VCC	6	-6	0.4	VCC-0.4
33		IOCHRDY	I	VCC	-	-	-	-
34		IOW#	O	VCC	6	-6	0.4	VCC-0.4
35		IOR#	O	VCC	6	-6	0.4	VCC-0.4
36		MEMCS16#	I	VCC	-	-	-	-
37		SBHE#	O	VCC	6	-6	0.4	VCC-0.4
38		IOCS16#	I	VCC	-	-	-	-
39		MEMR#	O	VCC	6	-6	0.4	VCC-0.4
40		MEMW#	O	VCC	6	-6	0.4	VCC-0.4
41	Power	GND	Power	-	-	-	-	-
42	ISA	ISADATAENA#	O	VCC	2	-2	0.4	VCC-0.4
43	Serial 4	RI4#	I	VCC	-	-	-	-
44		DTR4#	O	VCC	2	-2	0.4	VCC-0.4
45	Power	VCORE	Power	-	-	-	-	-
46		VCORE	Power	-	-	-	-	-
47	Serial 4	CTS4#	I	VCC	-	-	-	-
48		TXD4	O	VCC	2	-2	0.4	VCC-0.4
49		RTS4#	O	VCC	2	-2	0.4	VCC-0.4
50		RXD4	I	VCC	-	-	-	-
51		DSR4#	I	VCC	-	-	-	-
52		DCD4#	I	VCC	-	-	-	-
53	Serial 3	RI3#	I	VCC	-	-	-	-
54		DTR3#	O	VCC	2	-2	0.4	VCC-0.4
55		CTS3#	I	VCC	-	-	-	-
56		TXD3	O	VCC	2	-2	0.4	VCC-0.4
57		RTS3#	O	VCC	2	-2	0.4	VCC-0.4
58		RXD3	I	VCC	-	-	-	-

Pin	Group	Name	Type	Power Line	Drive (3.3v/5v) [mA]		Output voltage (3.3v/5v) [V]	
					I_{OL}	I_{OH}	V_{OL}(max)	V_{OH} (min)
59	Serial 3	DSR3#	I	VCC	-	-	-	-
60		DCD3#	I	VCC	-	-	-	-
61	Power	GND	Power	-	-	-	-	-
62	SH-Bus	CKIO	O	VCC	1.6	-0.2	0.55	2.4
63	Timer	TCLK	I	VCC	-	-	-	-
64	SH-Bus	RESETP#	I	VCC	-	-	-	-
65		RESETM#	I	VCC	-	-	-	-
66		WAIT#	I	VCC	-	-	-	-
67		CS2#	O	VCC	1.6	-0.2	0.55	2.4
68		CS0#	O	VCC	1.6	-0.2	0.55	2.4
69		RD/WR#	O	VCC	1.6	-0.2	0.55	2.4
70		WE1#	O	VCC	1.6	-0.2	0.55	2.4
71		WE0#	O	VCC	1.6	-0.2	0.55	2.4
72		RD#	O	VCC	1.6	-0.2	0.55	2.4
73		BS#	O	VCC	1.6	-0.2	0.55	2.4
74		A25	O	VCC	1.6	-0.2	0.55	2.4
75		A24	O	VCC	1.6	-0.2	0.55	2.4
76		A23	O	VCC	1.6	-0.2	0.55	2.4
77	Power	VCC	Power	-	-	-	-	-
78	SH-Bus	A22	O	VCC	1.6	-0.2	0.55	2.4
79		A21	O	VCC	1.6	-0.2	0.55	2.4
80		A20	O	VCC	1.6	-0.2	0.55	2.4
81		A19	O	VCC	1.6	-0.2	0.55	2.4
82	Power	GND	Power	-	-	-	-	-
83	SH-Bus	A18	O	VCC	1.6	-0.2	0.55	2.4
84		A17	O	VCC	1.6	-0.2	0.55	2.4
85		A16	O	VCC	1.6	-0.2	0.55	2.4
86		A15	O	VCC	1.6	-0.2	0.55	2.4
87		A14	O	VCC	1.6	-0.2	0.55	2.4
88		A13	O	VCC	1.6	-0.2	0.55	2.4
89		A12	O	VCC	1.6	-0.2	0.55	2.4
90		A11	O	VCC	1.6	-0.2	0.55	2.4
91		A10	O	VCC	1.6	-0.2	0.55	2.4
92		A9	O	VCC	1.6	-0.2	0.55	2.4
93		A8	O	VCC	1.6	-0.2	0.55	2.4
94		A7	O	VCC	1.6	-0.2	0.55	2.4
95		A6	O	VCC	1.6	-0.2	0.55	2.4
96		A5	O	VCC	1.6	-0.2	0.55	2.4
97		A4	O	VCC	1.6	-0.2	0.55	2.4
98		A3	O	VCC	1.6	-0.2	0.55	2.4
99		A2	O	VCC	1.6	-0.2	0.55	2.4
100		A1	O	VCC	1.6	-0.2	0.55	2.4
101	Power	GND	Power	-	-	-	-	-
102	SH-Bus	A0	O	VCC	1.6	-0.2	0.55	2.4
103		D15	I/O	VCC	1.6	-0.2	0.55	2.4
104		D14	I/O	VCC	1.6	-0.2	0.55	2.4
105		D13	I/O	VCC	1.6	-0.2	0.55	2.4
106	Power	VCC	Power	-	-	-	-	-
107	SH-Bus	D12	I/O	VCC	1.6	-0.2	0.55	2.4
108		D11	I/O	VCC	1.6	-0.2	0.55	2.4
109		D10	I/O	VCC	1.6	-0.2	0.55	2.4
110		D9	I/O	VCC	1.6	-0.2	0.55	2.4
111		D8	I/O	VCC	1.6	-0.2	0.55	2.4
112		D7	I/O	VCC	1.6	-0.2	0.55	2.4
113		D6	I/O	VCC	1.6	-0.2	0.55	2.4
114		D5	I/O	VCC	1.6	-0.2	0.55	2.4
115		D4	I/O	VCC	1.6	-0.2	0.55	2.4
116		D3	I/O	VCC	1.6	-0.2	0.55	2.4
117		D2	I/O	VCC	1.6	-0.2	0.55	2.4

Pin	Group	Name	Type	Power Line	Drive (3.3v/5v) [mA]		Output voltage (3.3v/5v) [V]	
					IOL	IOH	VOL(max)	VOH (min)
118	SH-Bus	D1	I/O	VCC	1.6	-0.2	0.55	2.4
119		D0	I/O	VCC	1.6	-0.2	0.55	2.4
120	Power	GND	Power	-	-	-	-	-
121		GND	Power	-	-	-	-	-
122	Slot_A	ACD1#	I	VCC	-	-	-	-
123		ACE1#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
124		ACE2#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
125		AOE#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
126		SLOT_A_VCC	Power	-	-	-	-	-
127		AVS1	I	VCC	-	-	-	-
128		AIORD#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
129		AIOWR#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
130		AWE#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
131		ARDY_IRQ#	I	SLOT_A_VCC	-	-	-	-
132		AVS2	I	VCC	-	-	-	-
133		ARESET	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
134		AWAIT#	I	SLOT_A_VCC	-	-	-	-
135	Power	VCC	Power	-	-	-	-	-
136	Slot_A	AREG#	Tri	SLOT_A_VCC	2/3	-2/-3	0.4/0.4	SLOT_A_VCC-0.4
137		ABVD2_SPKR	I	SLOT_A_VCC	-	-	-	-
138		ABVD1_STSCHG#	I	SLOT_A_VCC	-	-	-	-
139		AWP_IOIS16#	I	SLOT_A_VCC	-	-	-	-
140	Power	GND	Power	-	-	-	-	-
141	Slot_A	ACD2#	I	VCC	-	-	-	-
142		AADRENA#	O	VCC	2	-2	0.4	VCC-0.4
143		ADATAENA#	O	VCC	2	-2	0.4	VCC-0.4
144		AVPPPGM	O	VCC	6	-6	0.4	VCC-0.4
145		AVPPVCC	O	VCC	6	-6	0.4	VCC-0.4
146		AVCC5#	O	VCC	6	-6	0.4	VCC-0.4
147		AVCC3#	O	VCC	6	-6	0.4	VCC-0.4
148	PCMCIA	CA25	O	VCC	6	-6	0.4	VCC-0.4
149		CA24	O	VCC	6	-6	0.4	VCC-0.4
150	PCMCIA/ISA	CA23	O	VCC	6	-6	0.4	VCC-0.4
151	Parallel	SLCT	I	VCC	-	-	-	-
152		PE	I	VCC	-	-	-	-
153		BUSY	I	VCC	-	-	-	-
154		ACK#	I	VCC	-	-	-	-
155		LPTD7	I/OD	VCC	6	-	0.4	-
156		LPTD6	I/OD	VCC	6	-	0.4	-
157		LPTD5	I/OD	VCC	6	-	0.4	-
158		LPTD4	I/OD	VCC	6	-	0.4	-
159		LPTD3	I/OD	VCC	6	-	0.4	-
160		SLCTIN#	I/OD	VCC	12	-	0.4	-
161	Power	GND	Power	-	-	-	-	-
162	Parallel	LPTD2	I/OD	VCC	6	-	0.4	-
163		INIT#	I/OD	VCC	12	-	0.4	-
164		LPTD1	I/OD	VCC	6	-	0.4	-
165	Power	VCORE	Power	-	-	-	-	-
166		VBK	Power	-	-	-	-	-
167	Parallel	ERROR#	I	VCC	-	-	-	-
168		LPTD0	I/OD	VCC	6	-	0.4	-
169		AFD#	I/OD	VCC	12	-	0.4	-
170		STROBE#	I/OD	VCC	12	-	0.4	-
171	PM	STANDBY#	O	VCC	6	-6	0.4	VCC-0.4
172	Flash ROM	ROMDIS#	I	VCC	-	-	-	-
173		RESERVE	-	-	-	-	-	-
174	Video	EXTCLKI	I	VCC	-	-	-	-
175		RESERVE	-	-	-	-	-	-
176	ISA	CA22	O	VCC	6	-6	0.4	VCC-0.4

Pin	Group	Name	Type	Power Line	Drive (3.3v/5v) [mA]		Output voltage (3.3v/5v) [V]	
					IOL	IOH	VOL(max)	VOH (min)
177	Serial 0	TXD0	O	VCC	1.6	-0.2	0.55	2.4
178		SCK0	O	VCC	1.6	-0.2	0.55	2.4
179		RXD0	I	VCC	-	-	-	-
180		AN4	I	VCC	-	-	-	-
181	Power	GND	Power	-	-	-	-	-
182	AD/DA	AN5	I	VCC	-	-	-	-
183		DA1	O	VCC	-	-	-	-
184		DA0	O	VCC	-	-	-	-
185	Serial 1/Irda	TXD1	O	VCC	1.6	-0.2	0.55	2.4
186		RXD1	I	VCC	-	-	-	-
187	Serial 2	TXD2	O	VCC	1.6	-0.2	0.55	2.4
188		RXD2	I	VCC	-	-	-	-
189		RTS2#	O	VCC	1.6	-0.2	0.55	2.4
190		CTS2#	I	VCC	-	-	-	-
191	PM	PWOFF#	O	VCC	1.6	-0.2	0.55	2.4
192		SRBTN#	I	VCC	-	-	-	-
193	Video	FPVCCON	O	VCC	1.6	-0.2	0.55	2.4
194	Port	PTC7/PINT7	I/O	VCC	1.6	-0.2	0.55	2.4
195		PTC6/PINT6	I/O	VCC	1.6	-0.2	0.55	2.4
196		PTC5/PINT5	I/O	VCC	1.6	-0.2	0.55	2.4
197	Power	VCC	Power	-	-	-	-	-
198	Port	PTC4/PINT4	I/O	VCC	1.6	-0.2	0.55	2.4
199		PTC3/PINT3	I/O	VCC	1.6	-0.2	0.55	2.4
200		PTC2/PINT2	I/O	VCC	1.6	-0.2	0.55	2.4
201		PTC1/PINT1	I/O	VCC	1.6	-0.2	0.55	2.4
202	Power	GND	Power	-	-	-	-	-
203	DMA	DACK0#	O	VCC	1.6	-0.2	0.55	2.4
204		DREQ0#	I	VCC	-	-	-	-
205		DACK1#	O	VCC	1.6	-0.2	0.55	2.4
206		DREQ1#	I	VCC	-	-	-	-
207	Interrupt	NMI	I	VCC	-	-	-	-
208		IRQ1	I	VCC	-	-	-	-
209		IRQ2	I	VCC	-	-	-	-
210		IRQ3	I	VCC	-	-	-	-
211		IRQ4	I	VCC	-	-	-	-
212	Video	VSYNC	O	VCC	6	-6	0.3	VCC-0.3
213		HSYNC	O	VCC	6	-6	0.3	VCC-0.3
214		B	O	VCC	-	-	-	-
215		G	O	VCC	-	-	-	-
216		R	O	VCC	-	-	-	-
217		FPDAT15	O	VCC	6	-6	0.3	VCC-0.3
218		FPDAT14	O	VCC	6	-6	0.3	VCC-0.3
219		FPDAT13	O	VCC	6	-6	0.3	VCC-0.3
220		FPDAT12	O	VCC	6	-6	0.3	VCC-0.3
221	Power	GND	Power	-	-	-	-	-
222	Video	FPDAT11	O	VCC	6	-6	0.3	VCC-0.3
223		FPDAT10	O	VCC	6	-6	0.3	VCC-0.3
224		FPDAT9	O	VCC	6	-6	0.3	VCC-0.3
225		FPDAT8	O	VCC	6	-6	0.3	VCC-0.3
226	Power	VCC	Power	-	-	-	-	-
227	Video	FPDAT7	O	VCC	6	-6	0.3	VCC-0.3
228		FPDAT6	O	VCC	6	-6	0.3	VCC-0.3
229		FPDAT5	O	VCC	6	-6	0.3	VCC-0.3
230		FPDAT4	O	VCC	6	-6	0.3	VCC-0.3
231		FPDAT3	O	VCC	6	-6	0.3	VCC-0.3
232		FPDAT2	O	VCC	6	-6	0.3	VCC-0.3
233		FPDAT1	O	VCC	6	-6	0.3	VCC-0.3
234		FPDAT0	O	VCC	6	-6	0.3	VCC-0.3
235		DOTCLK	O	VCC	6	-6	0.3	VCC-0.3
236		MOD	O	VCC	6	-6	0.3	VCC-0.3

Pin	Group	Name	Type	Power Line	Drive (3.3v/5v) [mA]		Output voltage (3.3v/5v) [V]	
					I_{OL}	I_{OH}	V_{OL}(max)	V_{OH} (min)
237	Video	FPVEEON	O	VCC	2	-2	0.3	VCC-0.3
238		LINE	O	VCC	6	-6	0.3	VCC-0.3
239		FRAME	O	VCC	6	-6	0.3	VCC-0.3
240	Power	GND	Power	-	-	-	-	-

Output voltage (CompactFlash connector)

Pin	Group	Name	Type	Power Line	Drive [mA]		Output voltage [V]	
					I_{OL}	I_{OH}	V_{OL} (max)	V_{OH}(min)
1	CompactFlash	GND	Power	-	-	-	-	-
2		D3	I/O	VCC	1.6	-0.2	0.55	2.4
3		D4	I/O	VCC	1.6	-0.2	0.55	2.4
4		D5	I/O	VCC	1.6	-0.2	0.55	2.4
5		D6	I/O	VCC	1.6	-0.2	0.55	2.4
6		D7	I/O	VCC	1.6	-0.2	0.55	2.4
7		CCE1#	O	VCC	2	-2	0.4	VCC-0.4
8		A10	O	VCC	1.6	-0.2	0.55	2.4
9		COE#	O	VCC	2	-2	0.4	VCC-0.4
10		A9	O	VCC	1.6	-0.2	0.55	2.4
11		A8	O	VCC	1.6	-0.2	0.55	2.4
12		A7	O	VCC	1.6	-0.2	0.55	2.4
13		VCC	Power	-	-	-	-	-
14		A6	O	VCC	1.6	-0.2	0.55	2.4
15		A5	O	VCC	1.6	-0.2	0.55	2.4
16		A4	O	VCC	1.6	-0.2	0.55	2.4
17		A3	O	VCC	1.6	-0.2	0.55	2.4
18		A2	O	VCC	1.6	-0.2	0.55	2.4
19		A1	O	VCC	1.6	-0.2	0.55	2.4
20		A0	O	VCC	1.6	-0.2	0.55	2.4
21		D0	I/O	VCC	1.6	-0.2	0.55	2.4
22		D1	I/O	VCC	1.6	-0.2	0.55	2.4
23		D2	I/O	VCC	1.6	-0.2	0.55	2.4
24		CWP_IOIS16#	I	VCC	-	-	-	-
25		RESERVE	-	-	-	-	-	-
26		RESERVE	-	-	-	-	-	-
27		D11	I/O	VCC	1.6	-0.2	0.55	2.4
28		D12	I/O	VCC	1.6	-0.2	0.55	2.4
29		D13	I/O	VCC	1.6	-0.2	0.55	2.4
30		D14	I/O	VCC	1.6	-0.2	0.55	2.4
31		D17	I/O	VCC	1.6	-0.2	0.55	2.4
32		CCE2#	O	VCC	2	-2	0.4	VCC-0.4
33		RESERVE	-	-	-	-	-	-
34		CIORD#	O	VCC	2	-2	0.4	VCC-0.4
35		CIOWR#	O	VCC	2	-2	0.4	VCC-0.4
36		CWE#	O	VCC	2	-2	0.4	VCC-0.4
37		CRDY_IREQ#	I	VCC	-	-	-	-
38		VCC	Power	-	-	-	-	-
39		RESERVE	-	-	-	-	-	-
40		RESERVE	-	-	-	-	-	-
41		RESET	O	VCC	2	-2	0.4	VCC-0.4
42		CWAIT#	I	VCC	-	-	-	-
43		RESERVE	-	-	-	-	-	-
44		CREG#	O	VCC	2	-2	0.4	VCC-0.4
45		RESERVE	-	-	-	-	-	-
46		CBVD1_STSCHG#	I	VCC	-	-	-	-
47		D8	I/O	VCC	1.6	-0.2	0.55	2.4
48		D9	I/O	VCC	1.6	-0.2	0.55	2.4
49		D10	I/O	VCC	1.6	-0.2	0.55	2.4
50		GND	Power	-	-	-	-	-

Input voltage

Pin	Group	Name	Type	Power Line	Input low (3.3v/5v) level voltage [V]		Input high (3.3v/5v) level voltage [V]	
					VIL (min)	VIL (max)	VIH (min)	VIH (max)
1	Power	GND	Power	-	-	-	-	-
2	Slot_B	BCD1#	I	VCC	GND	0.6	2.4	VCC
3		BCE1#	Tri	SLOT_B_VCC	-	-	-	-
4		BCE2#	Tri	SLOT_B_VCC	-	-	-	-
5		BOE#	Tri	SLOT_B_VCC	-	-	-	-
6		SLOT_B_VCC	Power	-	-	-	-	-
7		BVS1	I	VCC	GND	0.6	2.4	VCC
8		BIORD#	Tri	SLOT_B_VCC	-	-	-	-
9		BIOWR#	Tri	SLOT_B_VCC	-	-	-	-
10		BWE#	Tri	SLOT_B_VCC	-	-	-	-
11		BRDY_IRQ#	I	SLOT_B_VCC	GND	0.8/0.8	2.0/2.0	SLOT_B_VCC
12		BVS2	I	VCC	GND	0.6	2.4	VCC
13		BRESET	Tri	SLOT_B_VCC	-	-	-	-
14		BWAIT#	I	SLOT_B_VCC	GND	0.8/0.8	2.0/2.0	SLOT_B_VCC
15	Power	VCC	Power	-	-	-	-	-
16	Slot_B	BREG#	Tri	SLOT_B_VCC	-	-	-	-
17		BBVD2_SPKR	I	SLOT_B_VCC	GND	0.8/0.8	2.0/2.0	SLOT_B_VCC
18		BBVD1_STSCHG#	I	SLOT_B_VCC	GND	0.8/0.8	2.0/2.0	SLOT_B_VCC
19		BWP_IOIS16#	I	SLOT_B_VCC	GND	0.8/0.8	2.0/2.0	SLOT_B_VCC
20	Power	GND	Power	-	-	-	-	-
21	Slot_B	BCD2#	I	VCC	GND	0.6	2.4	VCC
22		BADRENA#	O	VCC	-	-	-	-
23		BDATAENA#	O	VCC	-	-	-	-
24		BVPPPGM	O	VCC	-	-	-	-
25		BVPPVCC	O	VCC	-	-	-	-
26		BVCC5#	O	VCC	-	-	-	-
27		BVCC3#	O	VCC	-	-	-	-
28	KB/MS	KBCLK	I/OD	VCC	GND	0.8	2.0	5.5
29		KBDATA	I/OD	VCC	GND	0.8	2.0	5.5
30		MSCLK	I/OD	VCC	GND	0.8	2.0	5.5
31		MSDATA	I/OD	VCC	GND	0.8	2.0	5.5
32	ISA	RESETDRV	O	VCC	-	-	-	-
33		IOCHRDY	I	VCC	GND	0.8	2.0	5.5
34		IOW#	O	VCC	-	-	-	-
35		IOR#	O	VCC	-	-	-	-
36		MEMCS16#	I	VCC	GND	0.8	2.0	5.5
37		SBHE#	O	VCC	-	-	-	-
38		IOCS16#	I	VCC	GND	0.8	2.0	5.5
39		MEMR#	O	VCC	-	-	-	-
40		MEMW#	O	VCC	-	-	-	-
41	Power	GND	Power	-	-	-	-	-
42	ISA	ISADATAENA#	O	VCC	-	-	-	-
43	Serial 4	RI4#	I	VCC	GND	0.8	2.0	VCC
44		DTR4#	O	VCC	-	-	-	-
45	Power	VCORE	Power	-	-	-	-	-
46		VCORE	Power	-	-	-	-	-
47	Serial 4	CTS4#	I	VCC	GND	0.8	2.0	VCC
48		TXD4	O	VCC	-	-	-	-
49		RTS4#	O	VCC	-	-	-	-
50		RXD4	I	VCC	GND	0.8	2.0	VCC
51		DSR4#	I	VCC	GND	0.8	2.0	VCC
52		DCD4#	I	VCC	GND	0.8	2.0	VCC
53	Serial 3	RI3#	I	VCC	GND	0.8	2.0	VCC
54		DTR3#	O	VCC	-	-	-	-
55		CTS3#	I	VCC	GND	0.8	2.0	VCC
56		TXD3	O	VCC	-	-	-	-
57		RTS3#	O	VCC	-	-	-	-
58		RXD3	I	VCC	GND	0.8	2.0	VCC
59		DSR3#	I	VCC	GND	0.8	2.0	VCC

Pin	Group	Name	Type	Power Line	Input low (3.3v/5v) level voltage [V]		Input high (3.3v/5v) level voltage [V]	
					VIL (min)	VIL (max)	VIH (min)	VIH (max)
60	Serial 3	DCD3#	I	VCC	GND	0.8	2.0	VCC
61	Power	GND	Power	-	-	-	-	-
62	SH-Bus	CKIO	O	VCC	-	-	-	-
63	Timer	TCLK	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
64	SH-Bus	RESETP# (2)	I	VCC	-0.3	VCC x 0.2	VCCx0.9	VCC+0.3
65		RESETM#	I	VCC	-0.3	VCC x 0.2	VCCx0.9	VCC+0.3
66		WAIT#	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
67		CS2#	O	VCC	-	-	-	-
68		CS0#	O	VCC	-	-	-	-
69		RD/WR#	O	VCC	-	-	-	-
70		WE1#	O	VCC	-	-	-	-
71		WE0#	O	VCC	-	-	-	-
72		RD#	O	VCC	-	-	-	-
73		BS#	O	VCC	-	-	-	-
74		A25	O	VCC	-	-	-	-
75		A24	O	VCC	-	-	-	-
76		A23	O	VCC	-	-	-	-
77	Power	VCC	Power	-	-	-	-	-
78	SH-Bus	A22	O	VCC	-	-	-	-
79		A21	O	VCC	-	-	-	-
80		A20	O	VCC	-	-	-	-
81		A19	O	VCC	-	-	-	-
82	Power	GND	Power	-	-	-	-	-
83	SH-Bus	A18	O	VCC	-	-	-	-
84		A17	O	VCC	-	-	-	-
85		A16	O	VCC	-	-	-	-
86		A15	O	VCC	-	-	-	-
87		A14	O	VCC	-	-	-	-
88		A13	O	VCC	-	-	-	-
89		A12	O	VCC	-	-	-	-
90		A11	O	VCC	-	-	-	-
91		A10	O	VCC	-	-	-	-
92		A9	O	VCC	-	-	-	-
93		A8	O	VCC	-	-	-	-
94		A7	O	VCC	-	-	-	-
95		A6	O	VCC	-	-	-	-
96		A5	O	VCC	-	-	-	-
97		A4	O	VCC	-	-	-	-
98		A3	O	VCC	-	-	-	-
99		A2	O	VCC	-	-	-	-
100		A1	O	VCC	-	-	-	-
101	Power	GND	Power	-	-	-	-	-
102	SH-Bus	A0	O	VCC	-	-	-	-
103		D15	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
104		D14	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
105		D13	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
106	Power	VCC	Power	-	-		-	-
107	SH-Bus	D12	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
108		D11	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
109		D10	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
110		D9	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
111		D8	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
112		D7	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
113		D6	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
114		D5	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
115		D4	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
116		D3	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
117		D2	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
118		D1	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3

Pin	Group	Name	Type	Power Line	Input low (3.3v/5v) level voltage [V]		Input high (3.3v/5v) level voltage [V]	
					VIL (min)	VIL (max)	VIH (min)	VIH (max)
119	SH-Bus	D0	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
120	Power	GND	Power	-	-	-	-	-
121		GND	Power	-	-	-	-	-
122	Slot_A	ACD1#	I	VCC	GND	0.6	2.4	VCC
123		ACE1#	Tri	SLOT_A_VCC	-	-	-	-
124		ACE2#	Tri	SLOT_A_VCC	-	-	-	-
125		AOE#	Tri	SLOT_A_VCC	-	-	-	-
126		SLOT_A_VCC	Power	-	-	-	-	-
127		AVS1	I	VCC	GND	0.6	2.4	VCC
128		AIORD#	Tri	SLOT_A_VCC	-	-	-	-
129		AIOWR#	Tri	SLOT_A_VCC	-	-	-	-
130		AWE#	Tri	SLOT_A_VCC	-	-	-	-
131		ARDY_IRQ#	I	SLOT_A_VCC	GND	0.8/0.8	2.0/2.0	SLOT_A_VCC
132		AVS2	I	VCC	GND	0.6	2.4	VCC
133		ARESET	Tri	SLOT_A_VCC	-	-	-	-
134		AWAIT#	I	SLOT_A_VCC	GND	0.8/0.8	2.0/2.0	SLOT_A_VCC
135	Power	VCC	Power	-	-	-	-	-
136	Slot_A	AREG#	Tri	SLOT_A_VCC	-	-	-	-
137		ABVD2_SPKR	I	SLOT_A_VCC	GND	0.8/0.8	2.0/2.0	SLOT_A_VCC
138		ABVD1_STSCHG#	I	SLOT_A_VCC	GND	0.8/0.8	2.0/2.0	SLOT_A_VCC
139		AWP_IOIS16#	I	SLOT_A_VCC	GND	0.8/0.8	2.0/2.0	SLOT_A_VCC
140	Power	GND	Power	-	-	-	-	-
141	Slot_A	ACD2#	I	VCC	GND	0.6	2.4	VCC
142		AADRENA#	O	VCC	-	-	-	-
143		ADATAENA#	O	VCC	-	-	-	-
144		AVPPPGM	O	VCC	-	-	-	-
145		AVPPVCC	O	VCC	-	-	-	-
146		AVCC5#	O	VCC	-	-	-	-
147		AVCC3#	O	VCC	-	-	-	-
148	PCMCIA	CA25	O	VCC	-	-	-	-
149		CA24	O	VCC	-	-	-	-
150	PCMCIA/ISA	CA23	O	VCC	-	-	-	-
151	Parallel	SLCT	I	VCC	GND	0.8	2.0	5.5
152		PE	I	VCC	GND	0.8	2.0	5.5
153		BUSY	I	VCC	GND	0.8	2.0	5.5
154		ACK#	I	VCC	GND	0.8	2.0	5.5
155		LPTD7	I/OD	VCC	GND	0.8	2.0	5.5
156		LPTD6	I/OD	VCC	GND	0.8	2.0	5.5
157		LPTD5	I/OD	VCC	GND	0.8	2.0	5.5
158		LPTD4	I/OD	VCC	GND	0.8	2.0	5.5
159		LPTD3	I/OD	VCC	GND	0.8	2.0	5.5
160		SLCTIN#	I/OD	VCC	GND	0.8	2.0	5.5
161	Power	GND	Power	-	-	-	-	-
162	Parallel	LPTD2	I/OD	VCC	GND	0.8	2.0	5.5
163		INIT#	I/OD	VCC	GND	0.8	2.0	5.5
164		LPTD1	I/OD	VCC	GND	0.8	2.0	5.5
165	Power	VCORE	Power	-	-	-	-	-
166		VBK	Power	-	-	-	-	-
167	Parallel	ERROR#	I	VCC	GND	0.8	2.0	5.5
168		LPTD0	I/OD	VCC	GND	0.8	2.0	5.5
169		AFD#	I/OD	VCC	GND	0.8	2.0	5.5
170		STROBE#	I/OD	VCC	GND	0.8	2.0	5.5
171	PM	STANDBY#	O	VCC	-	-	-	-
172	Flash ROM	ROMDIS#	I	VCC	GND	0.8	2.0	VCC
173		RESERVE	-	-	-	-	-	-
174	Video	EXTCLKI	I	VCC	GND	VCC x 0.3	VCC x 0.7	5.5
175		RESERVE	-	-	-	-	-	-
176	ISA	CA22	O	VCC	-	-	-	-
177	Serial 0	TXD0	O	VCC	-	-	-	-

Pin	Group	Name	Type	Power Line	Input low (3.3v/5v) level voltage [V]		Input high (3.3v/5v) level voltage [V]	
					VIL (min)	VIL (max)	VIH (min)	VIH (max)
178	Serial 0	SCK0	O	VCC	-	-	-	-
179		RXD0	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
180		AN4	I	VCC	-	-	-	-
181	Power	GND	Power	-	-	-	-	-
182	AD/DA	AN5	I	VCC	-	-	-	-
183		DA1	O	VCC	-	-	-	-
184		DA0	O	VCC	-	-	-	-
185	Serial 1/Irda	TXD1	O	VCC	-	-	-	-
186		RXD1	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
187	Serial 2	TXD2	O	VCC	-	-	-	-
188		RXD2	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
189		RTS2#	O	VCC	-	-	-	-
190		CTS2#	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
191	PM	PWOFF#	O	VCC	-	-	-	-
192		SRBTN#	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
193	Video	FPVCCON	O	VCC	-	-	-	-
194	Port	PTC7/PINT7	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
195		PTC6/PINT6	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
196		PTC5/PINT5	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
197	Power	VCC	Power	-	-	-	-	-
198	Port	PTC4/PINT4	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
199		PTC3/PINT3	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
200		PTC2/PINT2	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
201		PTC1/PINT1	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
202	Power	GND	Power	-	-	-	-	-
203	DMA	DACK0#	O	VCC	-	-	-	-
204		DREQ0#	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
205		DACK1#	O	VCC	-	-	-	-
206		DREQ1#	I	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
207	Interrupt	NMI	I	VCC	-0.3	VCC x 0.1	VCCx0.9	VCC+0.3
208		IRQ1	I	VCC	-0.3	0.5	VCC-0.5	VCC+0.3
209		IRQ2	I	VCC	-0.3	0.5	VCC-0.5	VCC+0.3
210		IRQ3	I	VCC	-0.3	0.5	VCC-0.5	VCC+0.3
211		IRQ4	I	VCC	-0.3	0.5	VCC-0.5	VCC+0.3
212	Video	VSYNC	O	VCC	-	-	-	-
213		HSYNC	O	VCC	-	-	-	-
214		B	O	VCC	-	-	-	-
215		G	O	VCC	-	-	-	-
216		R	O	VCC	-	-	-	-
217		FPDAT15	O	VCC	-	-	-	-
218		FPDAT14	O	VCC	-	-	-	-
219		FPDAT13	O	VCC	-	-	-	-
220		FPDAT12	O	VCC	-	-	-	-
221	Power	GND	Power	-	-	-	-	-
222	Video	FPDAT11	O	VCC	-	-	-	-
223		FPDAT10	O	VCC	-	-	-	-
224		FPDAT9	O	VCC	-	-	-	-
225		FPDAT8	O	VCC	-	-	-	-
226	Power	VCC	Power	-	-	-	-	-
227	Video	FPDAT7	O	VCC	-	-	-	-
228		FPDAT6	O	VCC	-	-	-	-
229		FPDAT5	O	VCC	-	-	-	-
230		FPDAT4	O	VCC	-	-	-	-
231		FPDAT3	O	VCC	-	-	-	-
232		FPDAT2	O	VCC	-	-	-	-
233		FPDAT1	O	VCC	-	-	-	-
234		FPDAT0	O	VCC	-	-	-	-
235		DOTCLK	O	VCC	-	-	-	-
236		MOD	O	VCC	-	-	-	-
237		FPVEEON	O	VCC	-	-	-	-
238		LINE	O	VCC	-	-	-	-
239		FRAME	O	VCC	-	-	-	-
240	Power	GND	Power	-	-	-	-	-

(Note2) During RTC backup, be sure not to let RESETP# exceed 0.5V (V_{BK}=2.0V).

Input voltage (CompactFlash connector)

Pin	Group	Name	Type	Power Line	Input low level voltage [V]		Input high level voltage [V]	
					VIL (min)	VIL (max)	VIH (min)	VIH (max)
1	CompactFlash	GND	Power	-	-	-	-	-
2		D3	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
3		D4	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
4		D5	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
5		D6	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
6		D7	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
7		CCE1#	O	VCC	-	-	-	-
8		A10	O	VCC	-	-	-	-
9		COE#	O	VCC	-	-	-	-
10		A9	O	VCC	-	-	-	-
11		A8	O	VCC	-	-	-	-
12		A7	O	VCC	-	-	-	-
13		VCC	Power	-	-	-	-	-
14		A6	O	VCC	-	-	-	-
15		A5	O	VCC	-	-	-	-
16		A4	O	VCC	-	-	-	-
17		A3	O	VCC	-	-	-	-
18		A2	O	VCC	-	-	-	-
19		A1	O	VCC	-	-	-	-
20		A0	O	VCC	-	-	-	-
21		D0	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
22		D1	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
23		D2	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
24		CWP_IOIS16#	I	VCC	GND	0.8	2.0	VCC
25		RESERVE	-	-	-	-	-	-
26		RESERVE	-	-	-	-	-	-
27		D11	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
28		D12	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
29		D13	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
30		D14	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
31		D17	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
32		CCE2#	O	VCC	-	-	-	-
33		RESERVE	-	-	-	-	-	-
34		CIORD#	O	VCC	-	-	-	-
35		CIOWR#	O	VCC	-	-	-	-
36		CWE#	O	VCC	-	-	-	-
37		CRDY_IREQ#	I	VCC	GND	0.8	2.0	VCC
38		VCC	Power	-	-	-	-	-
39		RESERVE	-	-	-	-	-	-
40		RESERVE	-	-	-	-	-	-
41		RESET	O	VCC	-	-	-	-
42		CWAIT#	I	VCC	GND	0.8	2.0	VCC
43		RESERVE	-	-	-	-	-	-
44		CREG#	O	VCC	-	-	-	-
45		RESERVE	-	-	-	-	-	-
46		CBVD1_STSCHG#	I	VCC	GND	0.8	2.0	VCC
47		D8	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
48		D9	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
49		D10	I/O	VCC	-0.3	VCC x 0.2	2.0	VCC+0.3
50		GND	Power	-	-	-	-	-

8 AC CHARACTERISTICS

Clock Timing

Table 8-1 CKIO A.C Specification

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=30pF

Item	Symbol	min.	max.	Unit	note
CKIO Frequency			33.3	MHz	
CKIO Cycle Time	t_{01}	30		nsec	
CKIO High Pulse Width	t_{02}	8		nsec	
CKIO Low Pulse Width	t_{03}	8		nsec	
CKIO Fall Time	t_{04}		6	nsec	
CKIO Rise Time	t_{05}		6	nsec	

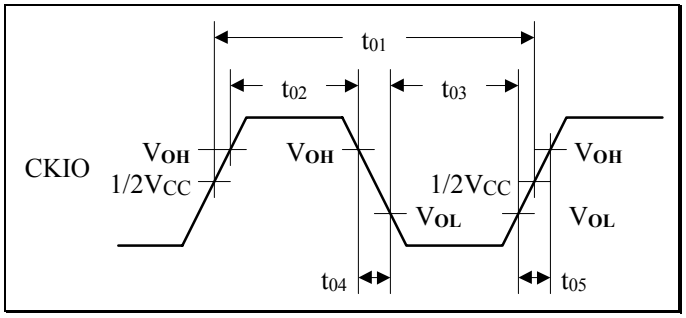


Figure 8-1 CKIO Timing

Table 8-2 EXTCLKI A.C Specification

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=30pF

Item	Symbol	min.	max.	Unit	note
EXTCLKI Frequency			33	MHz	
EXTCLKI Cycle Time	t_{06}	30.3		nsec	
EXTCLKI High Pulse Width	t_{07}	13.5		nsec	
EXTCLKI Low Pulse Width	t_{08}	13.5		nsec	
EXTCLKI Fall Time	t_{09}		10	nsec	
EXTCLKI Rise Time	t_{10}		10	nsec	

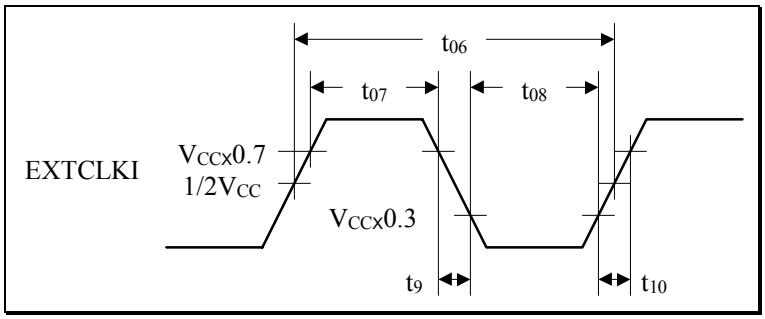


Figure 8-2 EXTCLKI Timing

SH-Bus Timing

Table 8-3 H-Bus A.C Specification

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=50pF (excluding CS2#)

Item	Symbol	min.	max.	Unit	note
Address Delay Time	t_{101}	1	13	nsec	
BS# Delay Time	t_{102}		12	nsec	
CS2# Delay Time 1	t_{103}	1	12	nsec	30pF
CS2# Delay Time 2	t_{104}	1	12	nsec	30pF
Address Hold Time	t_{105}	10		nsec	
RD/WR# Hold Time	t_{106}	0		nsec	
RD/WR# Delay Time	t_{107}	1	12	nsec	
RD# Delay Time	t_{108}		12	nsec	
Read Data Setup Time	t_{109}	12		nsec	
Read Data Hold Time	t_{110}	0		nsec	
WE# Delay Time	t_{111}		12	nsec	
Write Data Delay Time	t_{112}		12	nsec	
Write Data Hold Time	t_{113}	2		nsec	
WAIT# Setup Time	t_{114}	10		nsec	
WAIT# Hold Time	t_{115}	0		nsec	

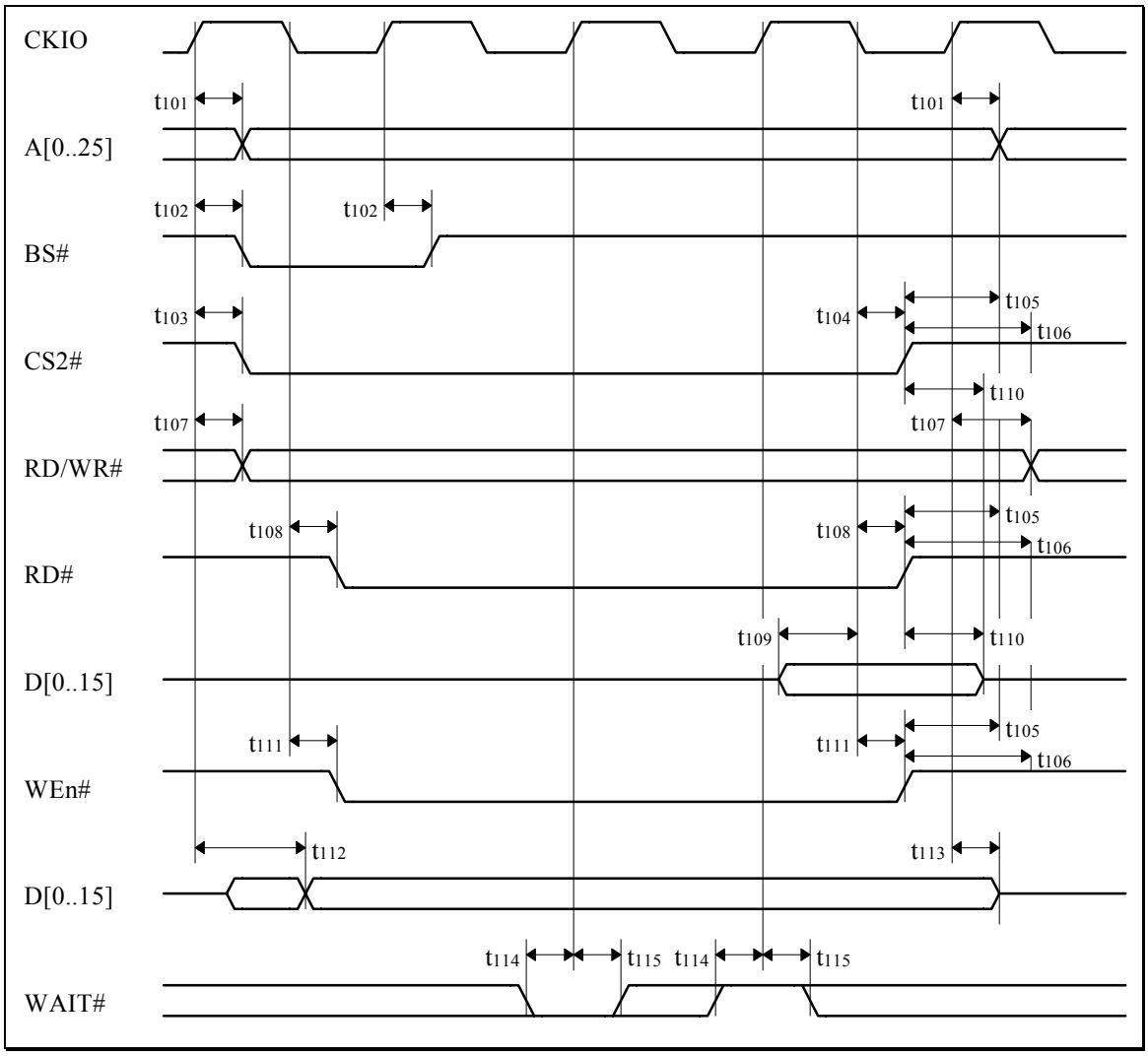


Figure 8-3 SH-Bus Timing

ISA Interface Timing

Table 8-4 ISA Interface A.C Specification

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=50pF

Item	Symbol	min.	max.	Unit	note
Address Setup Time	t_{201}	150		nsec	
Address Hold Time	t_{202}	75		nsec	
Command Pulse Width	t_{203}	220		nsec	
Read Data Setup Time	t_{204}	50		nsec	
Read Data Hold Time	t_{205}	0		nsec	
Write Data Setup Time	t_{206}	100		nsec	
Write Data Hold Time	t_{207}	75		nsec	
MEMCS16#, IOCS16# Setup Time	t_{208}	95		nsec	
MEMCS16#, IOCS16# Hold Time	t_{209}	0		nsec	
IOCHRDY Delay Time from Command	t_{210}		90	nsec	
IOCHRDY Active to Command Inactive Time	t_{211}	100		nsec	
IOCHRDY Hold Time	t_{212}	0		nsec	
ISADATAENA# Setup Time	t_{213}	70		nsec	
ISADATAENA# Hold Time	t_{214}	40		nsec	

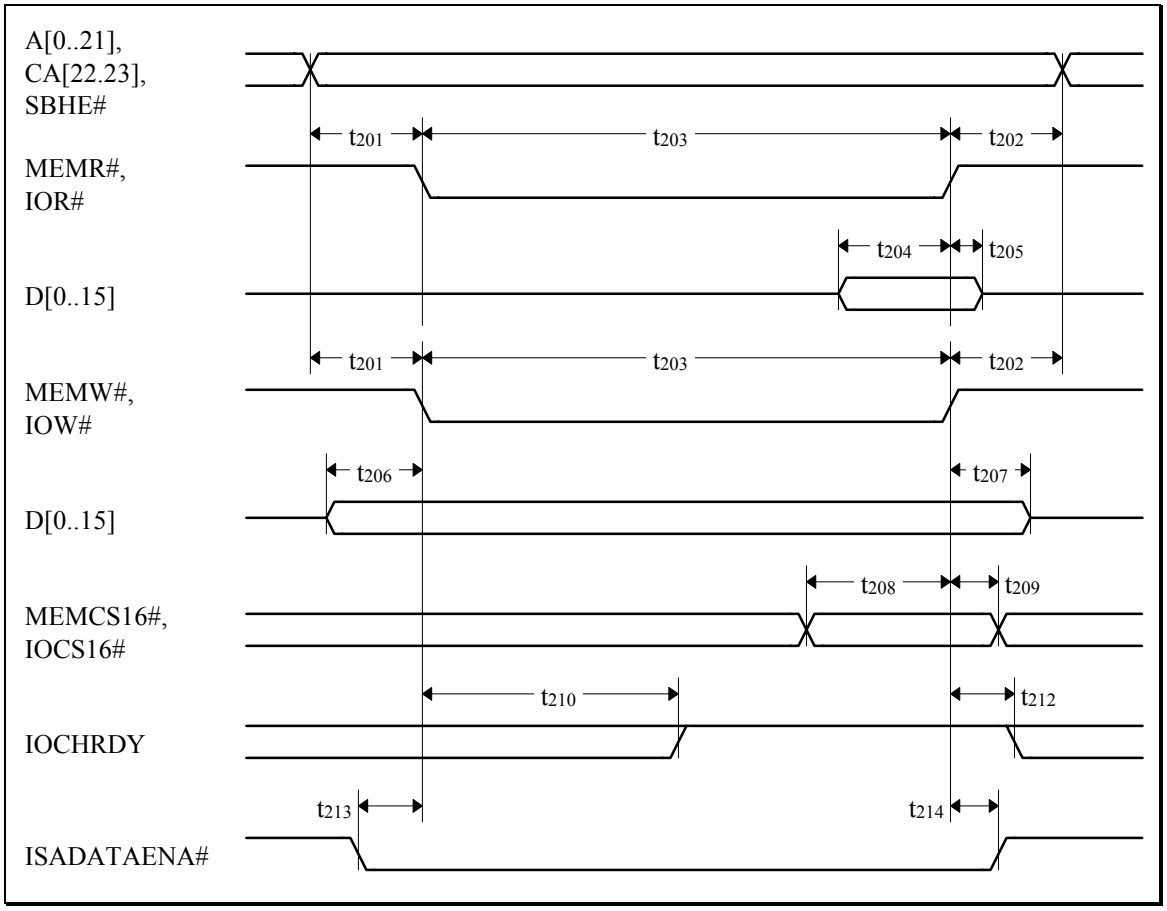


Figure 8-4 ISA Interface Timing (IOCHRDY Asserted)

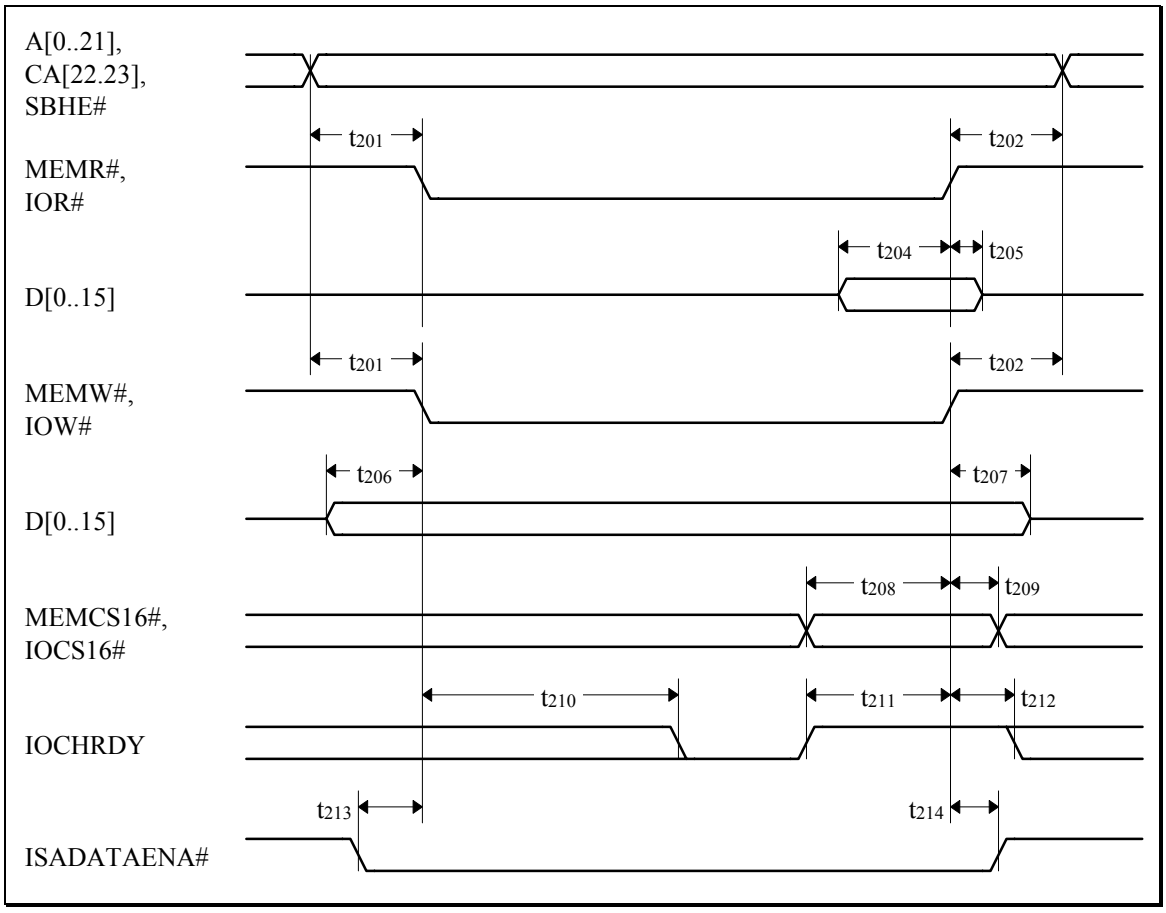


Figure 8-5 ISA Interface Timing (IOCHRDY Deasserted)

PCMCIA Timing (Memory)

Table 8-5 PCMCIA A.C Specification (Memory)

V_{CC}=3.3±0.15V, SLOT_A,B_V_{CC}=5V±10% or 3.3±0.15V, Ta=0 to 60°C, CL=50pF

Item	Symbol	min.	max.	Unit	note
Address Setup Time	t_{301}	150		nsec	
Address Hold Time	t_{302}	75		nsec	
OE#, WE# Pulse Width	t_{303}	220		nsec	
Read Data Setup Time	t_{304}	50		nsec	
Read Data Hold Time	t_{305}	0		nsec	
Write Data Setup Time	t_{306}	100		nsec	
Write Data Hold Time	t_{307}	75		nsec	
WAIT# Delay Time from OE#, WE#	t_{310}		90	nsec	
WAIT# Inactive to OE#, WE# Inactive Time	t_{311}	100		nsec	
WAIT# Hold Time	t_{312}	0		nsec	
DATAENA# Setup Time	t_{313}	70		nsec	
DATAENA# Hold Time	t_{314}	40		nsec	

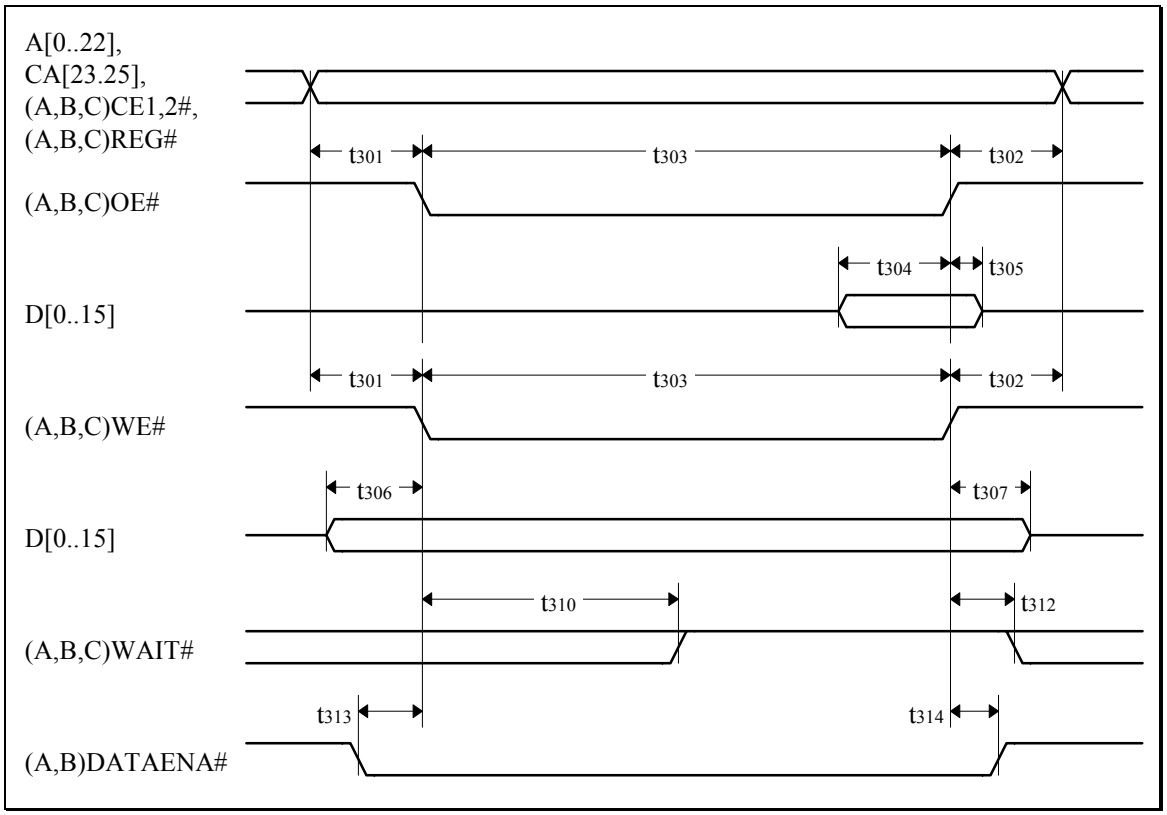


Figure 8-6 PCMCIA Memory Timing (WAIT# Deasserted)

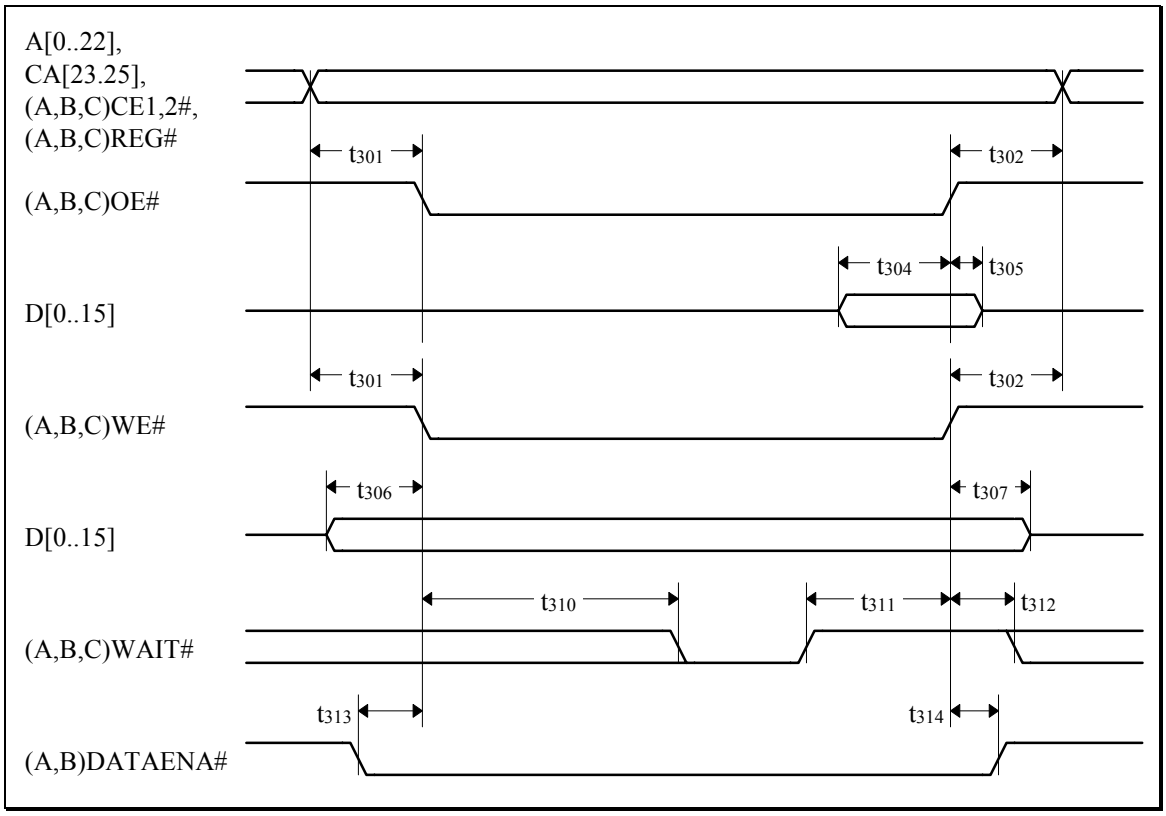


Figure 8-7 PCMCIA Memory Timing (WAIT# Asserted)

PCMCIA Timing (I/O)

Table 8-6 PCMCIA A.C Specification (I/O)

V_{CC}=3.3±0.15V, SLOT_A,B_V_{CC}=5V±10% or 3.3±0.15V, Ta=0 to 60°C, CL=50pF

Item	Symbol	min.	max.	Unit	note
Address Setup Time	t_{401}	150		nsec	
Address Hold Time	t_{402}	75		nsec	
IORD#, IOWR# Pulse Width	t_{403}	220		nsec	
Read Data Setup Time	t_{404}	50		nsec	
Read Data Hold Time	t_{405}	0		nsec	
Write Data Setup Time	t_{406}	100		nsec	
Write Data Hold Time	t_{407}	75		nsec	
IOIS16# Setup Time	t_{408}	95		nsec	
IOIS16# Hold Time	t_{409}	0		nsec	
WAIT# Delay Time from IORD#, IOWR#	t_{410}		90	nsec	
WAIT# Inactive to IORD#, IOWR# Inactive Time	t_{411}	100		nsec	
WAIT# Hold Time	t_{412}	0		nsec	
DATAENA# Setup Time	t_{413}	70		nsec	
DATAENA# Hold Time	t_{414}	40		nsec	

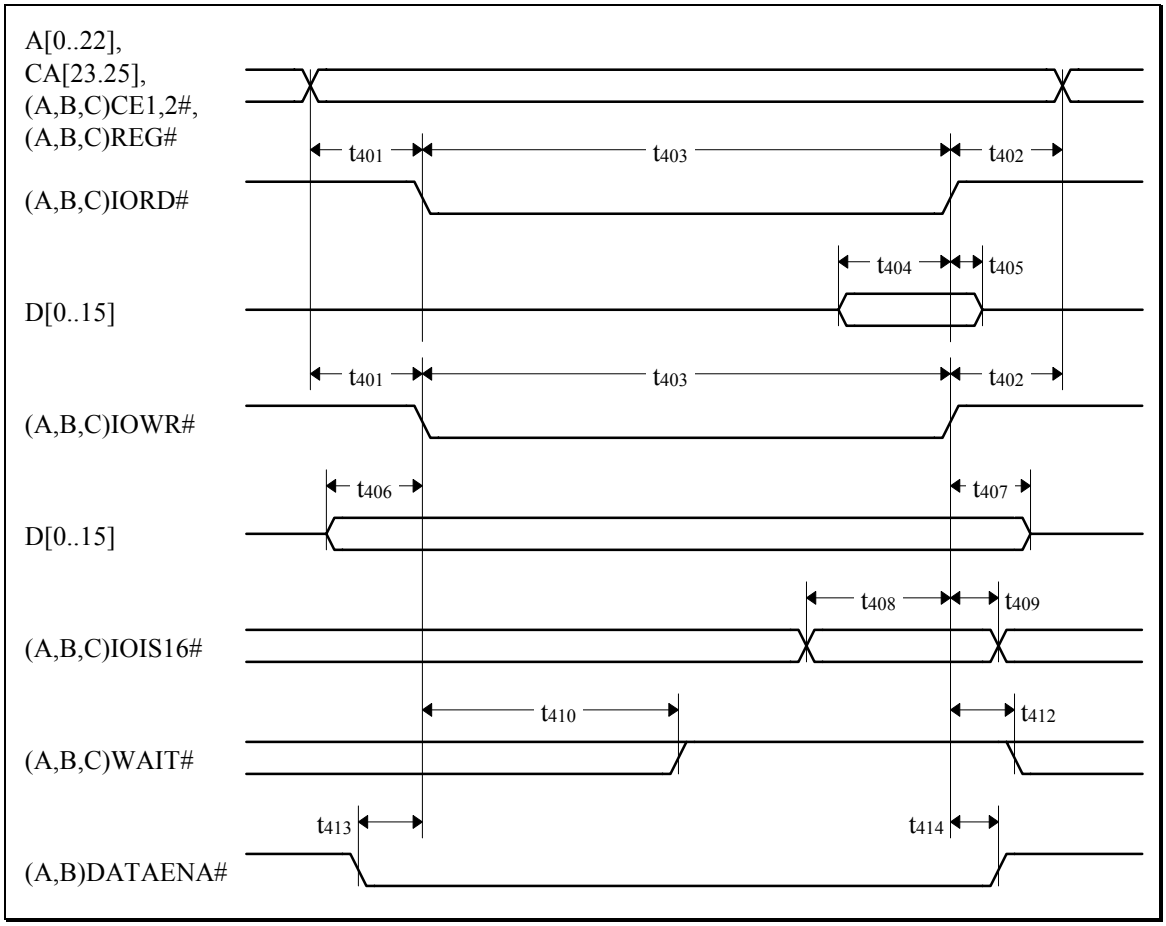


Figure 8-8 PCMCIA I/O Timing (WAIT# Deasserted)

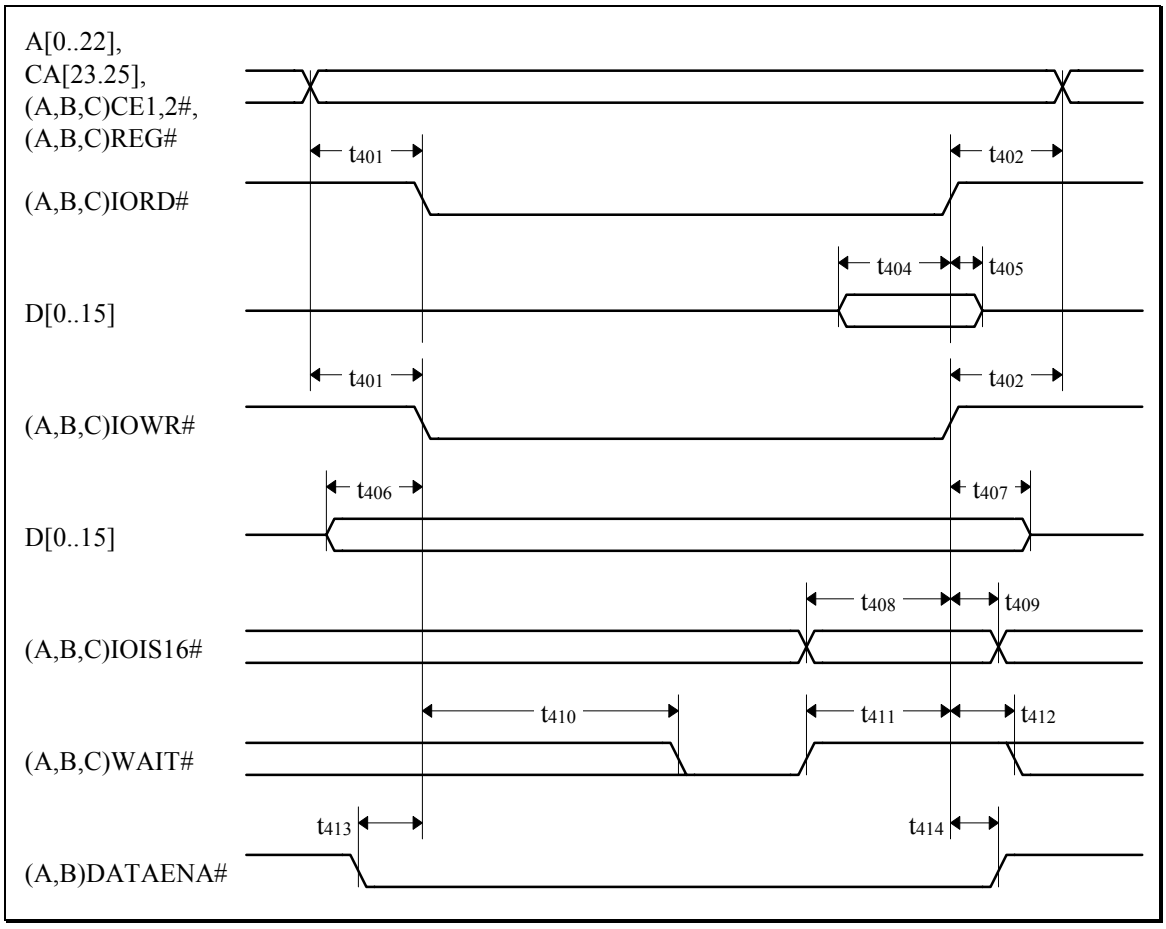


Figure 8-9 PCMCIA I/O Timing (WAIT# Asserted)

EPP Timing

Table 8-7 EPP A.C Specification

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=50pF

Item	Symbol	min.	max.	Unit	note
AFD#, SLCTIN# Pulse Width	$t_{501(a)}$	730		nsec	
AFD#, SLCTIN#, STROBE# Pulse Width	$t_{501(b)}$	640		nsec	
Read Data Setup Time	t_{502}	50		nsec	
Read Data Hold Time	t_{503}	0		nsec	
Write Data Setup Time	t_{504}	15		nsec	
Write Data Hold Time	t_{505}	70		nsec	
BUSY Delay Time from AFD#, SLCTIN#	t_{506}		300	nsec	
BUSY Inactive to AFD#, SLCTIN# Inactive Time	$t_{507(a)}$	200		nsec	
BUSY Inactive to AFD#, SLCTIN# Inactive Time	$t_{507(b)}$	110		nsec	
BUSY Hold Time	t_{508}	0		nsec	

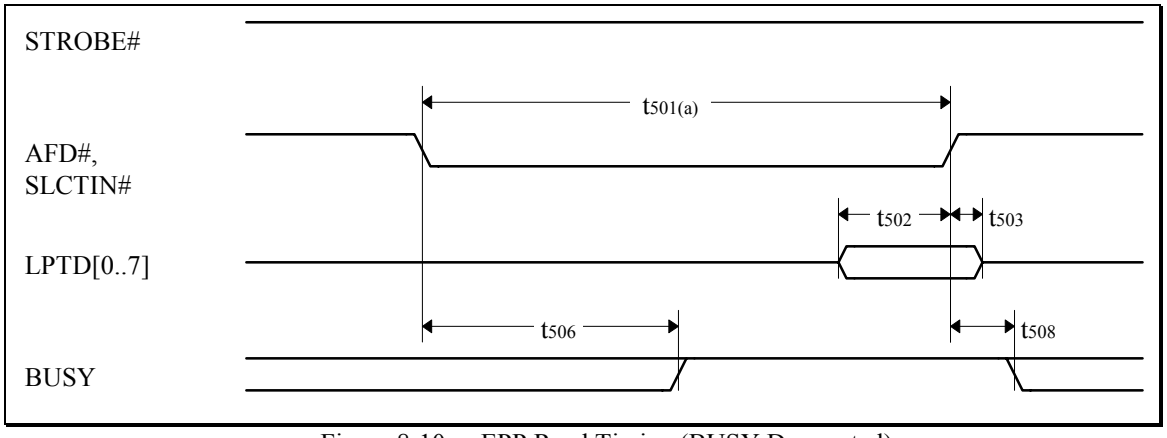


Figure 8-10 EPP Read Timing (BUSY Deasserted)

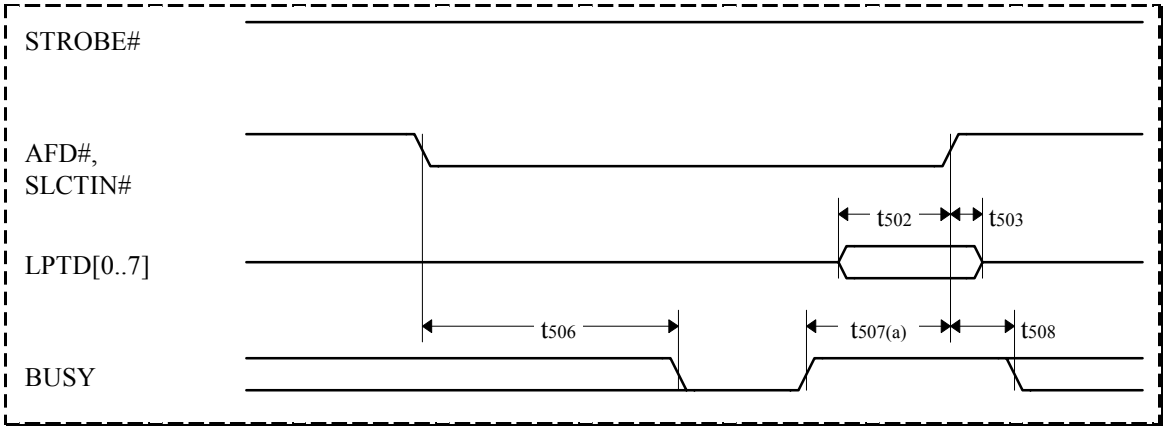


Figure 8-11 EPP Read Timing (BUSY Asserted)

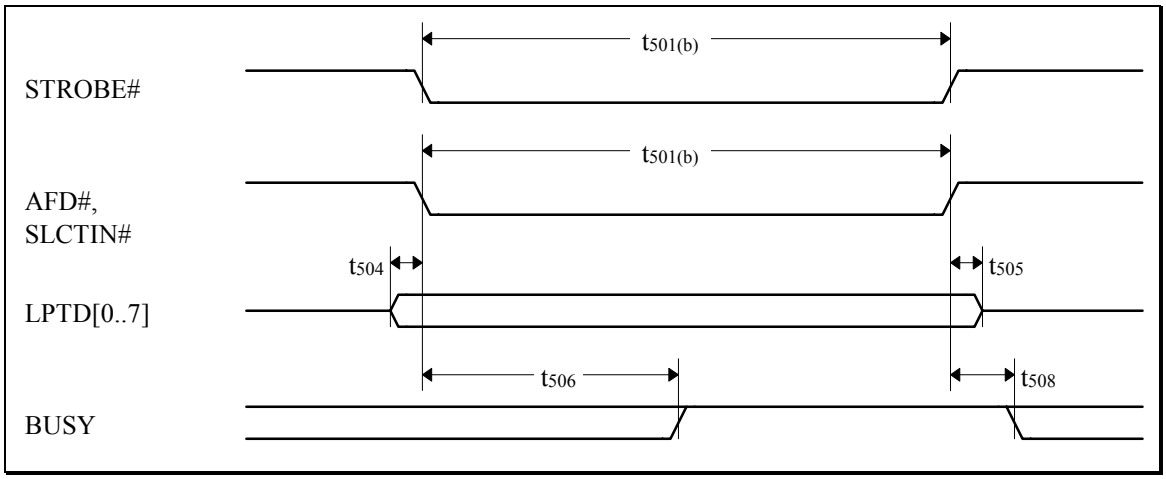


Figure 8-12 EPP Write Timing (BUSY Deasserted)

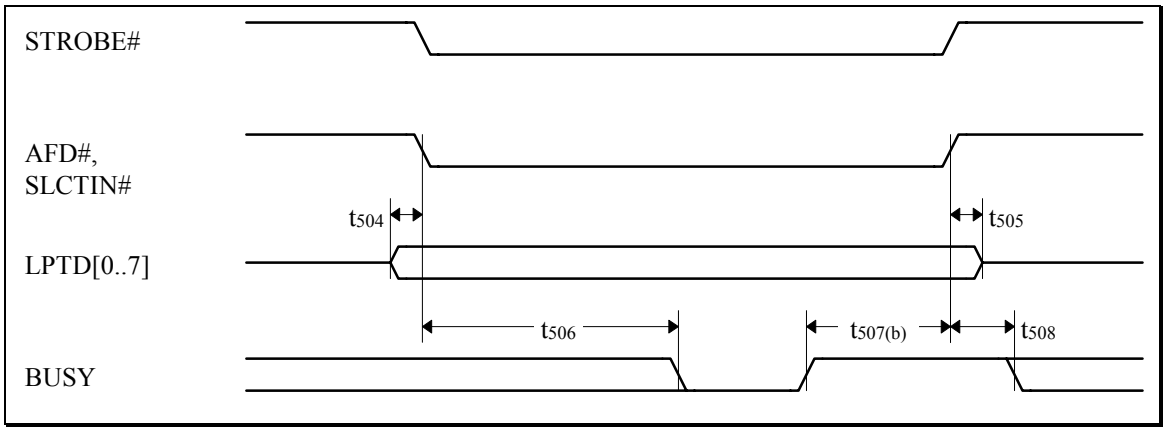


Figure 8-13 EPP Write Timing (BUSY Asserted)

Keyboard/Mouse Timing

Table 8-8 Keyboard/Mouse Interface A.C Characteristics

V_{CC}=3.3±0.15V, Ta=0 to 60°C, CL=50pF

Parameter	Symbol	min.	typ.	max.	unit	note
Clock Low Time	t_{601}	30		50	µsec	
Clock High Time	t_{602}	30		50	µsec	
Receiving Data Setup Time	t_{603}	5			µsec	
Receiving Data Hold Time	t_{604}	5			µsec	
Clock Line Inactive Time	t_{605}		96		µsec	
Start Bit Active Delay	t_{606}		48		µsec	
Sending Data Delay Time	t_{607}			5	µsec	

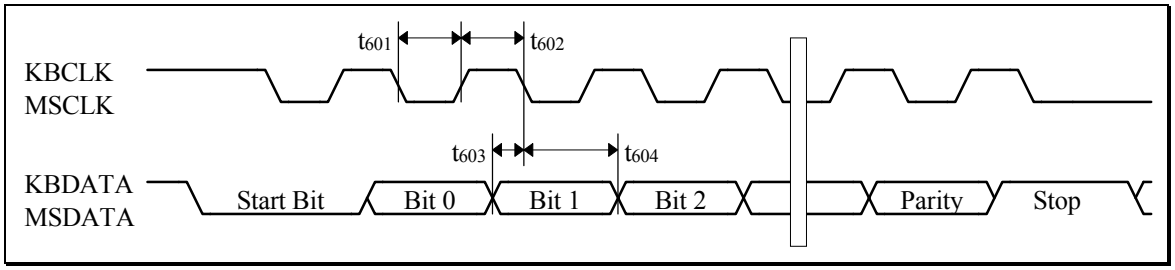


Figure 8-14 Keyboard/Mouse Receiving Data Timing

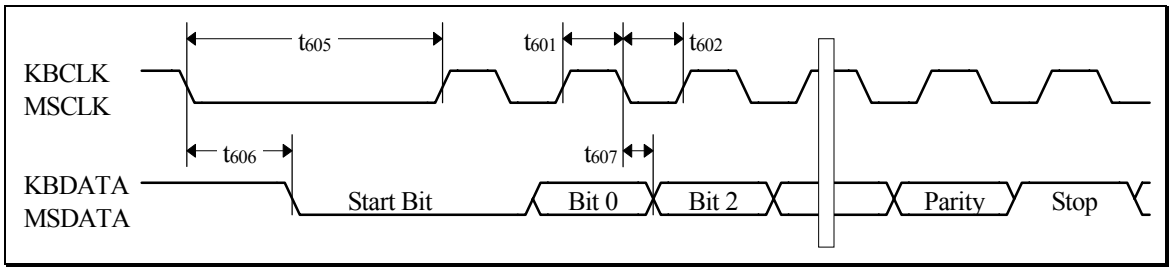


Figure 8-15 Keyboard/Mouse Sending Data Timing

Power On/Off Timing

Table 8-9 Power On/Off A.C Specification

Item	Symbol	min.	max.	Unit	note
RESETP# Turn Off Delay from 1.8V of V_{CORE} and 3.15V of VCC	t_{701}	50		msec	
RESETP# Active Setup Time to 1.8V of V_{CORE} and 3.15V of VCC	t_{702}	0		msec	

Always set as follows: $V_{CC} \geq V_{CORE}$.

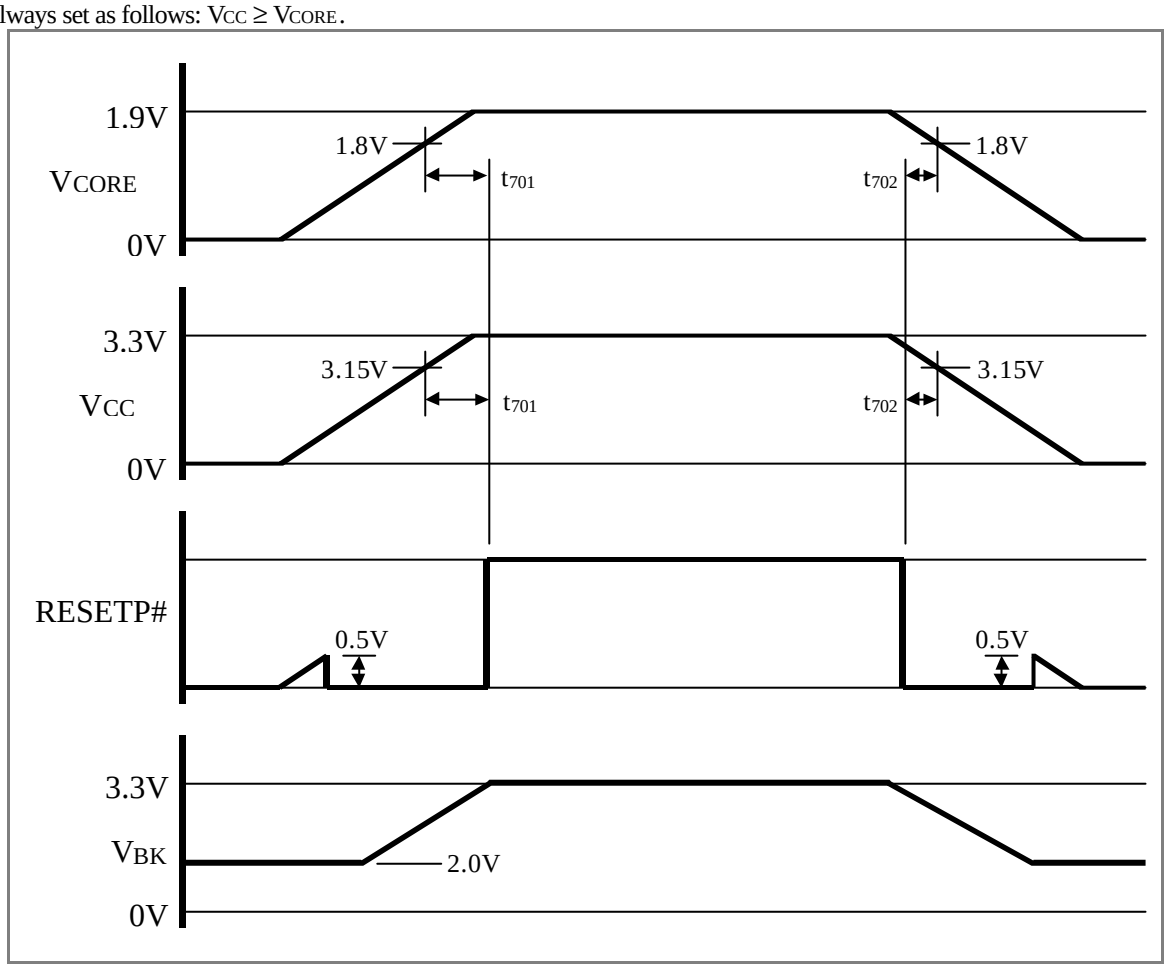


Figure 8-16 Power On/Off Timing

9 CAUTIONS ON HANDLING

- When using the CARD-E09A, make sure it operates within the guaranteed ranges in maximum rating, operating voltage, as well as other conditions.

- The ratings in these specifications do not include CompactFlash.
  Be sure the system meet the rating requirement of CompactFlash.

- The CARD-E09A contains a lot of CMOS devices. Because strong static electricity may damage CMOS devices, be sure to provide mechanism to prevent static electricity during transportation and assembly work.

- If excessive external noise is allowed at the power source or the input/output pins, this may cause incorrect operation or even malfunction. To ensure stable operation, be sure to place a filter capacity near the power connector of the CARD-E09A. Also, avoid placing near the CARD-E09A devices generating high noise level.

- If the CARD-E09A is used without anything connected to its input pin, this may cause incorrect operation induced by unstable voltage and noise. For unused pins where there is input other than signal of pull-up resistance inside the CARD-E09A or if the pins are bi-directional, use either pull-up or pull-down resistance to fix the input.

- When power is supplied, the initial state of the CARD-E09A is not fixed. To make sure the CARD-E09A is definitely operating, reset the CARD-E09A using RESETP# right after power is supplied.

In pursuit of "Saving" Technology, Epson electronic devices. Our lineup of semiconductors, liquid crystal displays and quartz devices assists in creating the products of our customers' dreams.
Epson IS energy savings.

EPSON International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone : +1-310-955-5300 Fax : +1-310-955-5400

SALES OFFICES
West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone : +1-408-922-0200 Fax : +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone : +1-815-455-7630 Fax : +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone : +1-781-246-3600 Fax : +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone : +1-877-EEA-0020 Fax : +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone : +49- (0) 89-14005-0 Fax : +49- (0) 89-14005-110

- GERMANY -
SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone : +49- (0) 2171-5045-0 Fax : +49- (0) 2171-5045-10

- UNITED KINGDOM -
UK BRANCH OFFICE
Unit 2.4 Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone : +44- (0) 1344-381700 Fax : +44- (0) 1344-381701

- FRANCE -
FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone : +33- (0) 1-64862350 Fax : +33- (0) 1-64862355

ASIA

- CHINA -
EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone : 64106655 Fax : 64107319

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone : 21-6485-5552 Fax : 21-6485-0775

- HONG KONG, CHINA -
EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, HONG KONG
Phone : +852-2585-4600 Fax : +852-2827-4346
Telex : 65542 EPSCO HX

- TAIWAN -
EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287,Nanking East Road, Sec. 3
Taipei, TAIWAN
Phone : 02-2717-7360 Fax : 02-2712-9164
Telex : 24444 EPSONTB

HSINCHU OFFICE
13F-3, No.295, Kuang-Fu Road, Sec. 2
HsinChu 300, TAIWAN
Phone : 03-573-9900 Fax : 03-573-9169

- SINGAPORE -
EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone : +65-337-7911 Fax : +65-334-2716

- KOREA -
SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone : 02-784-6027 Fax : 02-767-3677

- JAPAN -

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
Card Products & Marketing Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-7503 Fax: +81-(0)42-587-8423

ED International Marketing Department I
(Europe & U.S.A.)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812 Fax: +81-(0)42-587-5564

ED International Marketing Department II (Asia)
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814 Fax: +81-(0)42-587-5110

CARD-E09A
Hardware Manual

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Devices Information on Epson WWW server
http://www.epson.co.jp/device/

First issue April,1999
Revised February, 2000
Printed in Japan Ⓟ A