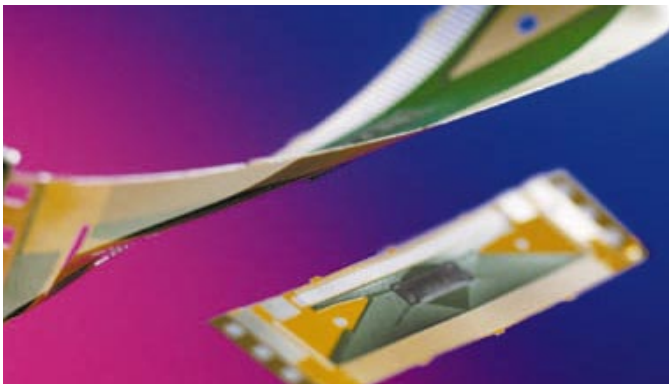
EPSON
NEWSLETTER 2001
4

ASSP

LESS EXTERNAL COMPONENTS

S1D15B10

LCD driver which requires less external components



EPSON has developed the LCD driver S1D15B10 (former SED15BA) on the base of its de facto standard for 1/65 duty LCD drivers, the S1D15605 (former SED1565). The technology used for the S1D15B10 requires only external booster capacitors to take full advantage of the on-chip power supply. There is NO need for external smoothing capacitors, which allows the developer to realize an LCD driver circuit with a minimal amount of external parts. Also the chip is designed as a slim-chip, which makes it even more appealing for COG use, as less glass space is necessary for mounting the LSI.

The MCU interface offers the choice between an 8bit parallel or serial interface. The serial interface can be realized using either 3 or 4 lines. Compared to the parallel I/F, the number of signal lines can be reduced significantly, which is also a relevant design-in criteria for COG assembly.

The on-chip Display Data RAM (DDRAM) display memory allows simultaneous display update and display refresh. The one-to-one correspondence between pixels of the LCD and the on-chip display memory enables easy programming and offers high flexibility for the graphic display.

Memory

STACKED PACKAGE

STACKED CSP

2 or 3 LSIs Integrated in an Ultra Compact Package

Mainly driven from the demands of the mobile equipment market EPSON's product lines of SRAM, VSRAM, ASIC, LCD controller/driver and microcomputer use the ultra compact, thin package CSPs (Chip Scale Packages). In order to further pursue the goal of higher integration, EPSON is now able to offer Stacked CSP which bundles up to three dies in one package. Mass production of the Stacked CSP has already started.

Applicable to various LSIs

The Stacked CSP makes it possible to stack one component die over another, thus building a more compact package which will save space on the final board. Moreover the stacked CSP approach can be used even if the dies are produced by different process technologies. The stacked package technology can be applied upon request to whichever combination is needed (e.g. microcomputer + SRAM, Flash + SRAM + ASIC, etc.).

STRUCTURE FEATURES

Bump Type 2 (or 3) dies (2 of them having same dimensions)	The lower die is connected by a bump*, and the upper die is connected by wire bonding (an eventual third die of smaller size can be placed on top of the first two connected by wire bonding)	Package height: 1.25 mm Typ. (even for a three die stack) Ball pitch: 0.8 mm
Wire Type 2 (or 3) dies (all having different dimensions)	Two or three dies are connected by wire bonding.	Package height: 1.25 mm Typ. Ball pitch: 0.8 mm

***bump:** *Small projection of gold formed on the die's pads. When connecting to the PCB, the chip is turned over, and connection is done using thermo-compression bonding on the wiring part of the PCB.*

EPSON OPENS TWO EUROPEAN DESIGN CENTERS

EPSON has officially inaugurated two new offices to enhance customer support capabilities: a Design Center in Livingston, Scotland and a Branch Office in Barcelona, Spain.
The establishment of EPSON Design Centers in Europe is mainly driven by changes in the mobile communication market. The product cycle of applications in this market is shortening and the demand for additional features is on the increase.
As a result, manufacturers face increasing pressure in their product development. This has lead to semiconductor vendors being called upon to supply not only ICs but also firmware and software. Through the Design Centers EPSON is now able to offer "complete solution"— firmware and hardware design in the mobile communication field.

SCOTLAND DESIGN CENTER

The Scotland Design Center (ESDC) focus on "energy saving DSP", whereby algorithms are carefully optimised to consume the least possible power, and hence to extend battery life (increasingly critical in mobile terminals, such as cellphones and MP-3 players).
The developments of ESDC are typically at the leading-edge of system-on-chip technology. ESDC provides complete end-to-end support for DSP-based products. In close collaboration with BDC, ESDC can provide complete component and system solutions to customers, using EPSON's original low-power CMOS technologies. Typical DSP firmware applications currently under development include AMR (Adaptive Multi-Rate speech coding for 2G and 3G mobile systems, Channel coding (error correction) incorporating the Viterbi Processor, and MP-3 stereo audio decoding.

BARCELONA BRANCH OFFICE

The Barcelona Branch Office (BDC) will function mainly as a Design Center for embedded semiconductor products in mobile equipment, offering standard services such as synthesis, place & route, netlist validation, ATPG, Scan Insertion, writing of VHDL code, etc. for simple Gate Arrays (ranging from 1K gates in 1 µm up to 2,5 MGates in 0.25 µm) or Standard Cells. Moreover it will focus on sophisticated services for System-On-Chip: development of analogue cells, mixed-signal simulations, pre-evaluation of viability (technical and commercial) for mixed-signal designs, development of debug platforms, firmware and hardware integration, etc. EPSON focus specifically on Analogue design, one of the most required services in System-On-Chip projects.

OVERVIEW	ESDC	BDC
Address	Integration House, Alba Campus, Livingston, EH54 7HH, Scotland	Edificio Prima Sant Cugat, Avda. Alcalde Barrils num. 64-68 E-08190 Sant Cugat del Vallès, SPAIN Phone: +34-93-544 24 90, Fax: +34-93-544 24 91
Floor space:	Approx. 420 m^2	Approx. 450 m^2
Start of full-fledged operations	May 7, 2001	January 1, 2001
Representative	Mitsuharu Kodaira	Narcis Avellana
Employees	**13** (including 10 engineers) as of May 2001; to be increased to 30 employees (including 25 engineers) during fiscal 2001 (April 2001–March 2002)	**8** (6 EPSON and 2 EPSON-CNM) as of May 2001; to be increased
Operations	1. Development of DSP firmware for speech and audio applications and support for firmware development by clients (For example, an AMR [Adaptive Multi Rate] Speech CODEC is currently under development and is scheduled to be completed by June 2001.) 2. Integrated planning of systems-on-a-chip, from planning, marketing, and setting the specifications for CMOS LSI products to their development, evaluation, and customer support	1. General ASIC services, for example Synthesis, FPGA to ASIC conversion, support on writing VHDL code, etc. 2. System On Chip integration and development of debugging environments 3. IP development and support, especially on analogue
Target applications	Speech and audio applications to be used on mobile information terminals equipped with wireless interfaces	Mobile communications

Note: *The firmware is a mixture of hardware and software. One of the most important technologies for the firmware development is a 'partitioning' between hardware and software to optimise performance and to lower the power consumption. The firmware is implemented into an LSI for a wide variety of applications including portable audio equipment and personal digital assistants.*

EPSON'S COST SAVING ALTERNATIVE TO FPGAs

EPSON's Gate Arrays offer a lot more than just a state of the art technology. There are multiple reasons to consider using Gate Arrays, including commercial advantages. Through the EPSON Design Center in Barcelona, we are able to provide full design support and offer a complete conversion service of FPGAs.

ADVANTAGES OF USING GATE ARRAYS AND CONVERTING FPGAS

Reduction of the unit price

FPGAs need to be configurated and programmed by the customer often using internal RAM-cells, Anti-Fuse, PROM or EEPROM technologies combined with additional structures and interconnect wiring to program the device. This leads to an increased die size and results in a higher unit price. As Gate Arrays are hard-wired and therefore already "configurated" in the factory, the die can be much smaller.

Reduction of the total cost by increasing the reliability

FPGA technologies using RAM-cells for configuration need an external boot device (e.g. ROM, PROM) to drive it, otherwise the FPGA will loose its configuration after power down. Gate Arrays do not need a boot device: reducing the number of additonal devices – allowing the reduction in size of the PCB itself. Fewer devices means higher reliability and minimises the number of manufacturing partners required. In any case the FPGA must be programmed, which influences the entire production costs. With Gate Arrays the customer gets a completed and tested product, facilitating immediate use without requiring add. programming actions.

Reduction of power consumption

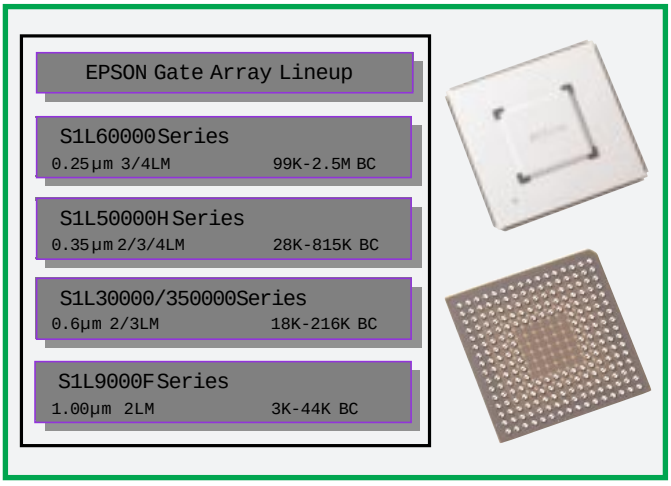
Especially when operating at higher frequencies applications sensitive to power consumption will benefit in using an ASIC in preference of FPGA.

Availability of high gate counts

EPSON's Gate Arrays offer densities of up to 2.5 Million Gates (standard equipped with 2 input power NAND gates), which makes it easy to combine several logic chips into one device, and add additional functions or SRAM blocks.

Flexibility through wide choice of packages

As there is no fixed pin assignment with Gate Arrays, the customer can design the layout of his PCB due to his needs or even make pin-to-pin compatible devices. The pins for programming the FPGA are not needed with Gate Arrays and may be left blank or used for other functions.



Reliability and Security

EPSON's Gate Arrays are produced in two of our own factories in Japan. Therefore the customer can be sure to get products with a continuous high level of quality over a long period. Furthermore it is almost impossible to copy the internal circuitry of a Gate Array chip without mask or design data compared to programmable logic devices, if the programmable logic device is connected to an external configuration PROM or EEPROM.

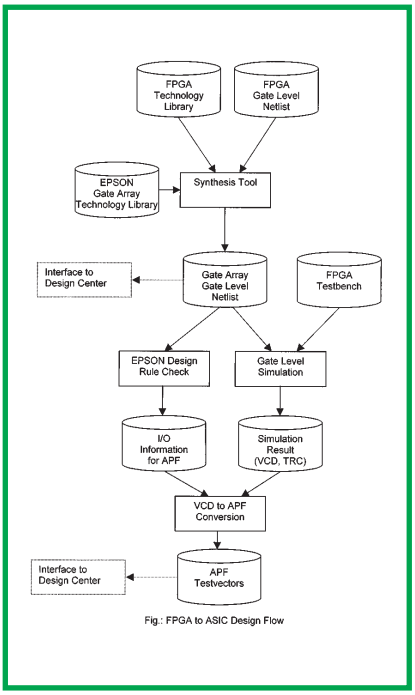


Fig.: FPGA to ASIC Design Flow

EPSON offers

EPSON supports all major HDL tools for the Gate Array design on Workstations and PCs as well as our own schematic editor. The customer will be provided with a complete design kit on CD-ROM and has direct support from EPSON's Design Center in Barcelona during design.
Furthermore EPSON can offer the complete service of converting FPGAs.
EPSON provides fast sample delivery and mass production in order to reduce time-to-market. Engineering Samples (tested like MP products) can be produced within 3 weeks, Mass Production times of 8 weeks are possible. Due to the low NRE-cost (Non Recurring Engineering) for Gate Arrays compared to other mask based ASIC technologies, the commercial break-even-point of FPGAs may be reached with business volumes of as low as 5-10K pcs/year. EPSON is already supporting projects of this size.
The commercial advantage typically increases with the quantity and the gate count of the device.

EPSON's Gate Arrays can be combined with a wide variety of packages and as a highlight it can be delivered in die form.

Personalisation of the package

EPSON supports personalised ASIC packages with customized part numbers and customer logo printed on the chip.

EPSON Oscillators in 5x7

One standard — more than 5x7 applications

As leader on the crystal oscillator (XO) market, EPSON has to offer a wide range of solutions in a 5x7 mm² package. This package size is currently becoming the industry standard and therefore also became a common platform for the wide range of dedicated oscillators EPSON has to offer. Besides just catching up with the current trend towards ceramic packages, EPSON created a highly price competitive 5x7 plastic mold SMD package, that is of course fully size and land pattern compatible to the ceramic version. This latter package type is coded by the suffix JF in the product name and is also used for the SG-645. The suffix CA indicates a 5x7 ceramic package, which is also used in the SG-7xx series.

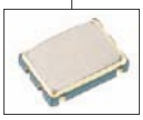
Fast Delivery

The SG-8002 series is a lineup of programmable PLL-based oscillators.

SG-8002JF & SG-8002CA 1 - 125MHz
Programmable (OTP)
3.3V or 5V
+/-50x10 $^{-6}$ (-20 to +70°C)
+/-100x10 $^{-6}$ (-40 to +85°C)
Minimum leadtime:
Samples – max. 5 days!
Mass Production – 4 weeks

Standard

The SG-710 and SG-720 are non-PLL oscillators ideal for standard applications.



SG-720 & SG-710 1.8 – 80MHz
+/-50x10 $^{-6}$ (-10 to +70°C)
+/-100x10 $^{-6}$ (-40 to +85°C)
Supply: 3.3V or 5V

Low Frequency

SG-3030JF can provide a stable 32.768KHz clock with a fan-out of 3 (15pF).

SG-3030JF 32.768kHz
fast startup: max. 3s
5+/-23x10 $^{-6}$ (+25°C)
Supply: 1.5 - 5V (output level controllable)

High Stability - PXO

The HG-2050CA and HG-2150CA are advanced products for situations, where high stability is needed.

HG-2050CA 2 - 70MHz
Stability: +/-25x10 $^{-6}$ (-20 to +70°C)
+/-50x10 $^{-6}$ (-40 to +85°C)
Supply: 3.3V or 5V
HG-2150CA 1 - 80MHz
Stability: +/-15x10 $^{-6}$ (-20 to +70°C)
+/-25x10 $^{-6}$ (-40 to +85°C)
Supply: 3.3V or 5V

Lowest Jitter

The EG-series is a new lineup of SAW based oscillators, delivering the lowest jitter to the industry.

EG-2001CA 106.25-166MHz; Accum. jitter: 4 ps max.
Output: LV-TTL (3.3V)
EG-2002 62.5-180MHz; Accum. jitter: 4 ps max.
Output: LV-TTL (3.3V)
EG-2101 62.5 - 400MHz; Accum. jitter: 4 ps max.
Output: D-PECL (3.3V)

Pullability – VCXO

These two VCXOs are for applications like xDSL, SONET/SDH or PDX.
VG-4231CA 16 - 41MHz
Stability: +/-35x10 $^{-6}$ (-20 to +70°C); +/-50x10 $^{-6}$ (-40 to +85°C)
Pull Range: +/- 130x10 $^{-6}$
Supply: 3.3V or 5V
VG-1201CA 1 - 80MHz
Stability: +/-20x10 $^{-6}$ (-20 to +70°C); +/-35x10 $^{-6}$ (-40 to +85°C)
Pull Range: +/-100x10 $^{-6}$ min (<41MHz); +/-75x10 $^{-6}$ min (≥41MHz)
Supply: 3.3V or 5V

Versatility

For higher frequencies, the SG-645**W and the SG-710**W are available (W = jitter optimised PLL Osc.).

SG-645W** 32.0001 - 135MHz
+/- 50x10 $^{-6}$ (-20 to +70°C)
+/-100x10 $^{-6}$ (-40 to +85°C)
Supply: 3.3V or 5V
SG-710W** 66.6667 - 135MHz
+/-50x10 $^{-6}$ (-20 to +70°C)
+/-100x10 $^{-6}$ (-40 to +85°C)
Supply: 3.3V or 5V

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