

SRM2AV213LLBT₈

2M-bit Static RAM

Preliminary
**Super Low Voltage
 Operation
 Products**

- Super Low Voltage Operation and Low Current Consumption
- Access Time 85ns (2.4V)
- 131,072 Words x 16-bit Asynchronous
- Wide Temperature Range

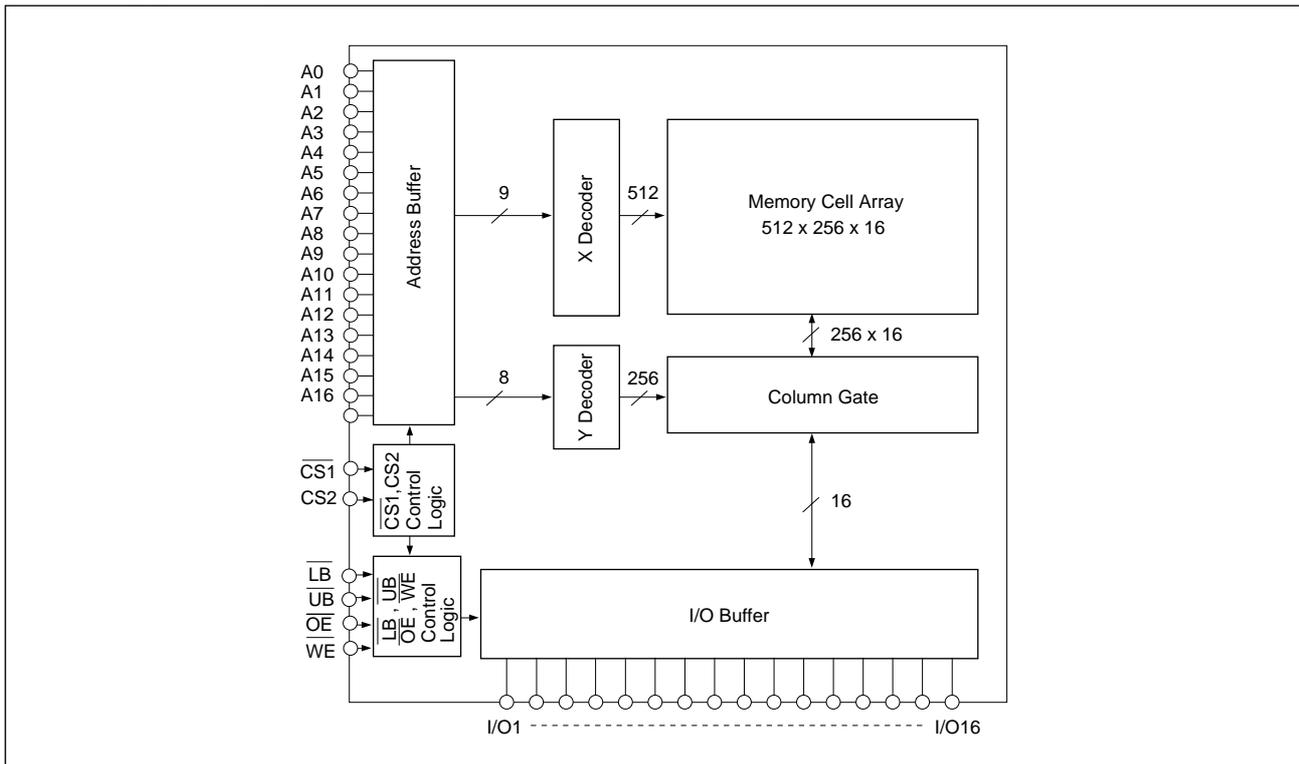
DESCRIPTION

The SRM2AV213LLBT₈ is a 131,072 words x 16-bit asynchronous, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock and no refreshing circuit. It is possible to control the data width by the data byte control. 3-state output allows easy expansion of memory capacity. The temperature range of the SRM2AV213LLBT₈ is from -40 to 85°C, and it is suitable for the industrial products.

FEATURES

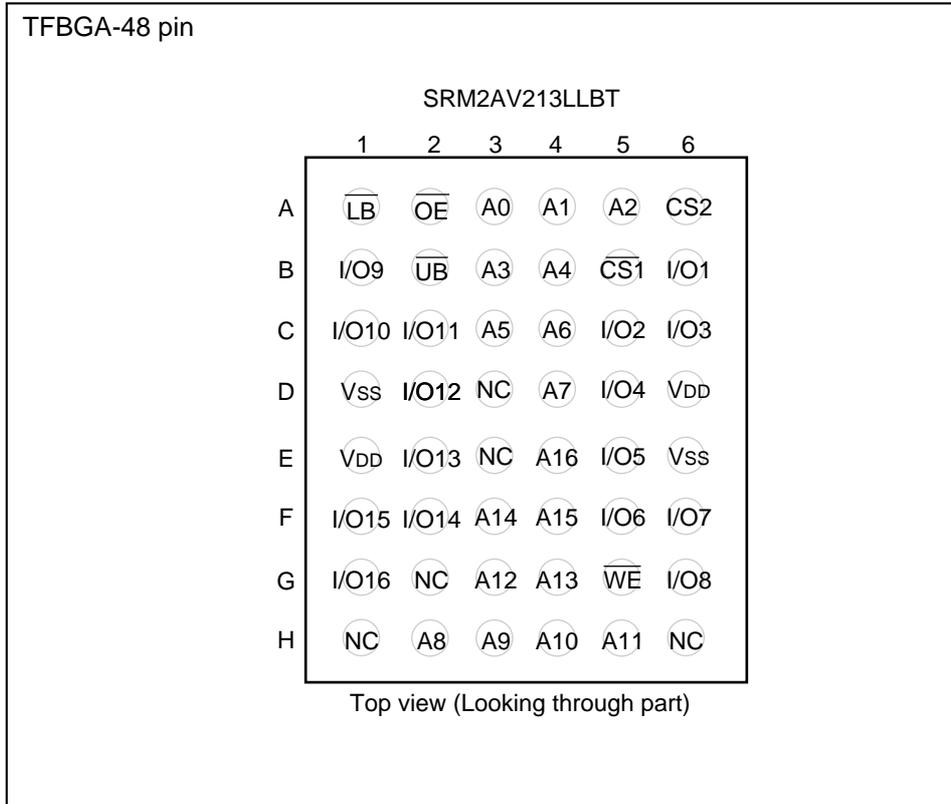
- Fast Access time 85ns (2.4V)
- Low supply current LL Version
- Completely static No clock required
- Supply voltage 2.4V to 3.3V
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM2AV213LLBT TFBGA-48 pin (Tape CSP)

BLOCK DIAGRAM



SRM2AV213LLBT₈

■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A16	Address Input
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{CS1}}$	Chip Select1
CS2	Chip Select2
$\overline{\text{LB}}$	LOWER Byte Enable
$\overline{\text{UB}}$	UPPER Byte Enable
I/O1 to 16	Data I/O
V _{DD}	Power Supply (2.4V to 3.3V)
V _{SS}	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	- 0.5 to 4.0	V
Input voltage	V _I	- 0.5* to V _{DD} + 0.3	V
Input/Output voltage	V _{I/O}	- 0.5* to V _{DD} + 0.3	V
Power dissipation	P _D	0.5	W
Operating temperature	T _{opr}	- 40 to 85	°C
Storage temperature	T _{stg}	- 65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	-

* V_I, V_{I/O} (Min.) = -2.0V (when pulse width is less than 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85 °C)

Parameter	Symbol	V _{DD} = 2.4 to 3.3V			V _{DD} = 2.7 to 3.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{DD}	2.4	3.0	3.3	2.7	3.0	3.3	V
	V _{SS}	0.0	0.0	0.0	0.0	0.0	0.0	V
Input voltage	V _{IH}	0.75V _{DD}	-	V _{DD} +0.3	2.0	-	V _{DD} +0.3	V
	V _{IL}	- 0.3*	-	0.3	- 0.3*	-	0.6	V

* if pulse width is less than 50ns it is - 2.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{SS}=0V, Ta = -40 to 85 °C)

Parameter	Symbol	Conditions	V _{DD} = 2.4 to 3.3V			Unit	
			Min.	Typ. *1	Max.		
Input leakage current	I _{LI}	V _I = 0 to V _{DD}	-1.0	-	1.0	μA	
Output leakage current	I _{LO}	LB and UB = V _{IH} or CS1 = V _{IH} or CS2 = V _{IL} or WE=V _{IL} or OE = V _{IH} , V _{I/O} = 0 to V _{DD}	-1.0	-	1.0	μA	
High level output voltage	V _{OH}	I _{OH}	-0.5mA -100μA	2.0 V _{DD} -0.2	- -	- -	V
Low level output voltage	V _{OL}	I _{OL}	1.0mA 100μA	- -	- -	0.4 0.2	V
Standby supply current	I _{DDS}	CS1 = V _{IH} or CS2= V _{IL}	-	-	1.0	mA	
	I _{DDS1}	CS1 = CS2 ≥ V _{DD} - 0.2V or CS2 ≤ 0.2V Ta ≤ 25°C, V _{DD} ≤ 3.0V	LL LL	- 0.5	15 1.0	μA	
Average operating current	I _{DDA}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA, t _{cy} = Min.	-	25	35	mA	
	I _{DDA1}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA, t _{cy} = 1μs	-	4.0	6.0	mA	
Operating Supply Current	I _{DDO}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA	-	4.0	6.0	mA	

*1 : Typical values are measured at Ta = 25°C and V_{DD} = 3.0V

● Terminal Capacitance

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C _{ADD}	V _{ADD} = 0V	-	-	8	pF
Input Capacitance	C _I	V _I = 0V	-	-	8	pF
I/O Capacitance	C _{I/O}	V _{I/O} = 0V	-	-	10	pF

Note : This parameter is made by the inspection data of sample, not of all products

SRM2AV213LLBT8

● AC Electrical Characteristics

○ Read Cycle

(V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions	SRM2AV213LLBT8		Unit
			2.4 to 3.3V		
			Min.	Max.	
Read cycle time	t _{RC}	1	85	–	ns
Address access time	t _{ACC}	1	–	85	ns
$\overline{\text{CS}}1$ access time	t _{ACS1}	1	–	85	ns
CS2 access time	t _{ACS2}	1	–	85	ns
$\overline{\text{OE}}$ access time	t _{OE}	1	–	45	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ access time	t _{AB}	1	–	45	ns
$\overline{\text{CS}}1$ output set time	t _{CLZ1}	2	5	–	ns
CS2 output set time	t _{CLZ2}	2	5	–	ns
$\overline{\text{CS}}1$ output floating	t _{CHZ1}	2	–	30	ns
CS2 output floating	t _{CHZ2}	2	–	30	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ output set time	t _{BLZ}	2	0	–	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ output floating	t _{BHZ}	2	–	30	ns
$\overline{\text{OE}}$ output set time	t _{OLZ}	2	0	–	ns
$\overline{\text{OE}}$ output floating	t _{OHZ}	2	–	30	ns
Output hold time	t _{OH}	1	5	–	ns

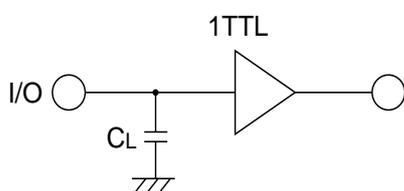
○ Write Cycle

(V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions	SRM2AV213LLBT8		Unit
			2.4 to 3.3V		
			Min.	Max.	
Write cycle time	t _{WC}	1	85	–	ns
Chip select time ($\overline{\text{CS}}1$)	t _{CW1}	1	70	–	ns
Chip select time (CS2)	t _{CW2}	1	70	–	ns
Address enable time	t _{AW}	1	70	–	ns
Address setup time	t _{AS}	1	0	–	ns
Write pulse width	t _{WP}	1	60	–	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ select time	t _{BW}	1	70	–	ns
Address hold time	t _{WR}	1	0	–	ns
Data setup time	t _{DW}	1	35	–	ns
Data hold time	t _{DH}	1	0	–	ns
$\overline{\text{WE}}$ output floating	t _{WHZ}	2	–	35	ns
$\overline{\text{WE}}$ output set time	t _{OW}	2	5	–	ns

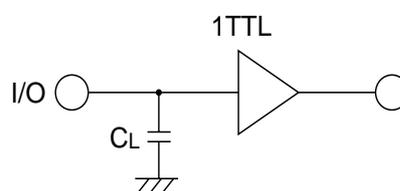
*1 Test Conditions

1. Input pulse level : 0.3V to 0.8V_{DD}(2.4V to 3.3V)
2. tr = tr = 5ns
3. Input and output timing reference levels : 1/2V_{DD}(2.4V to 3.3V)
4. Output load : CL = 50pF (Includes Jig Capacitance)

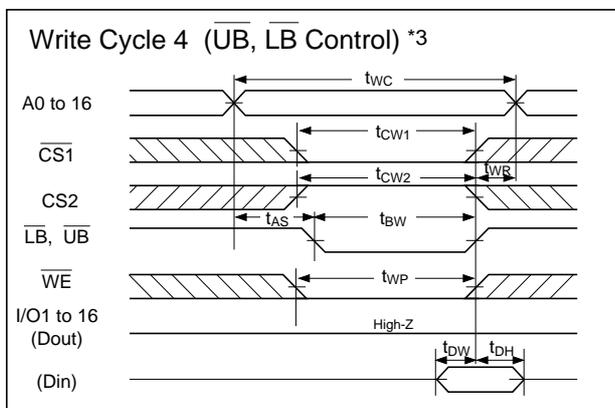
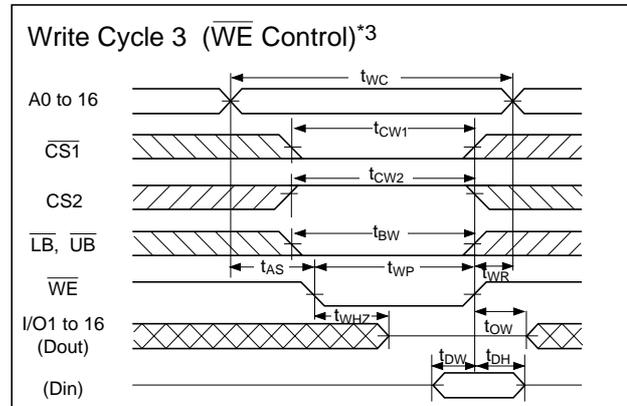
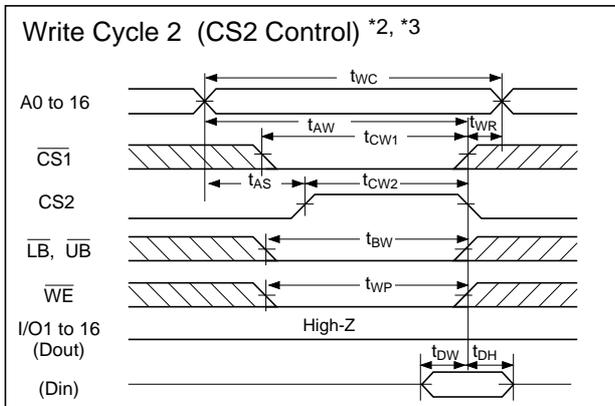
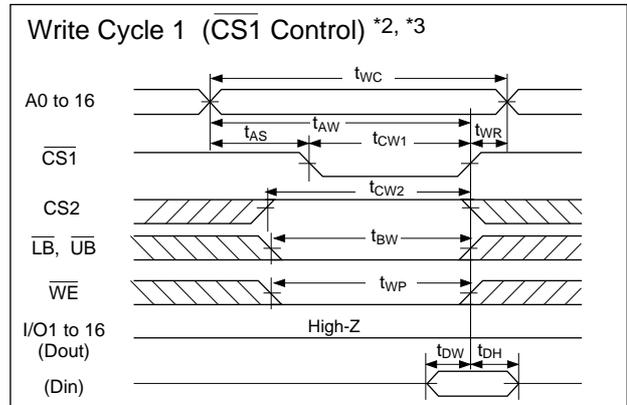
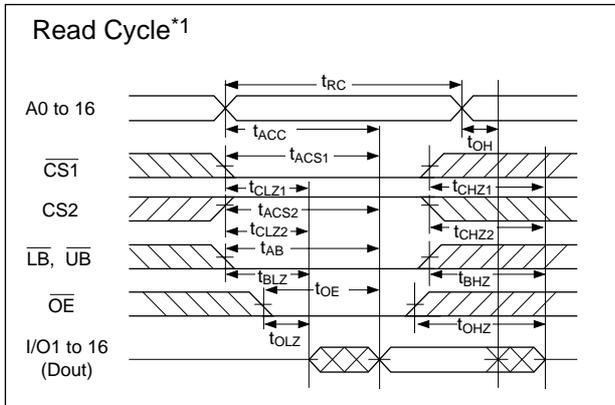


*2 Test Conditions

1. Input pulse level : 0.3V to 0.8V_{DD}(2.4V to 3.3V)
2. tr = tr = 5ns
3. Input timing reference levels : 1/2V_{DD}(2.4V to 3.3V)
4. Output timing reference levels : ±200mV (The level changed from stable output voltage level)
5. Output load : CL = 5pF (Includes Jig Capacitance)



● Timing Chart



Note : *1 During read cycle time, \overline{WE} is to be "High" level.

*2 In write cycle time that is controlled by $\overline{CS1}$ or $\overline{CS2}$, output buffer is to be "Hi-Z" state even if \overline{OE} is "Low" level.

*3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

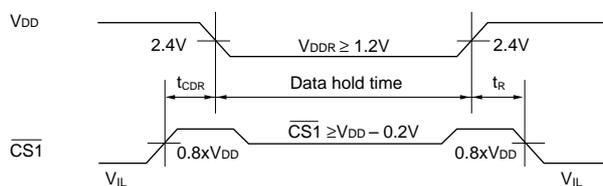
($V_{SS} = 0V$, $T_a = -40$ to $85^\circ C$)

Parameter	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Data retention supply voltage	V_{DDR}		1.2	–	3.3	V
Data retention current	I_{DDR}	$V_{DDR} = 2.5V$ $\overline{CS1} = \overline{CS2} \geq V_{DD} - 0.2V$ or $\overline{CS2} \leq 0.2V$	–	0.4	13	μA
Data hold time	t_{CDR}		0	–	–	ns
Operation recovery time	t_R		5	–	–	ms

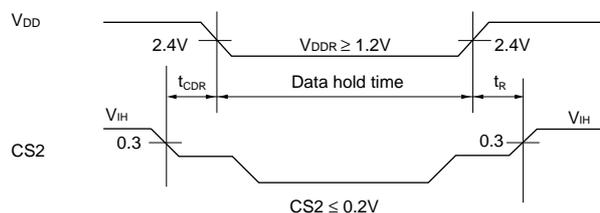
* : Reference data at $T_a = 25^\circ C$

SRM2AV213LLBT8

Data retention timing (CS1 Control)



Data retention timing (CS2 Control)



FUNCTIONS

Truth Table

$\overline{CS1}$	CS2	\overline{LB}	\overline{UB}	\overline{OE}	\overline{WE}	I/O1 to 8	I/O9 to 16	MODE	I_{DD}
H	X	X	X	X	X	High-Z	High-Z	Not Selected	I_{DDs}, I_{DDs1}
X	L	X	X	X	X	High-Z	High-Z	Not Selected	I_{DDs}, I_{DDs1}
L	H	X	X	H	H	High-Z	High-Z	Output disable	I_{DDA}, I_{DDA1}
L	H	H	H	X	X	High-Z	High-Z	Output disable	I_{DDA}, I_{DDA1}
L	H	L	H	X	L	Data In	High-Z	Lower Byte Write	I_{DDA}, I_{DDA1}
L	H	H	L	X	L	High-Z	Data In	Upper Byte Write	I_{DDA}, I_{DDA1}
L	H	L	L	X	L	Data In	Data In	All Byte Write	I_{DDA}, I_{DDA1}
L	H	L	H	L	H	DataOut	High-Z	Lower Byte Read	I_{DDA}, I_{DDA1}
L	H	H	L	L	H	High-Z	DataOut	Upper Byte Read	I_{DDA}, I_{DDA1}
L	H	L	L	L	H	Data Out	Data Out	All Byte Read	I_{DDA}, I_{DDA1}

X : High or Low

Reading data

It is possible to control the data width by \overline{LB} and \overline{UB} pins.

(1) Reading data from lower byte

Data is able to be read when the address is set while holding $\overline{CS1}$ = "Low", CS2 = "High", \overline{OE} = "Low", \overline{LB} = "Low", and \overline{WE} = "High".

(2) Reading data from upper byte

Data is able to be read when the address is set while holding $\overline{CS1}$ = "Low", CS2 = "High", \overline{OE} = "Low", \overline{UB} = "Low", and \overline{WE} = "High".

(3) Reading data from both bytes

Data is able to be read when the address is set while holding $\overline{CS1}$ = "Low", CS2 = "High", \overline{OE} = "Low", \overline{UB} = "Low", \overline{LB} = "Low", and \overline{WE} = "High".

Since I/O pins are in "Hi-Z" state when \overline{OE} = "High", the data bus line can be used for any other objective, then access time is apparently able to be cut down.

● Writing data

(1) Writing data into lower byte

There are the following four ways of writing data into memory.

- i) Hold $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, $\overline{UB} = \text{"High"}$, and $\overline{LB} = \text{"Low"}$, set address and give "Low" pulse to $\overline{CS1}$.
- ii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{WE} = \text{"Low"}$, $\overline{UB} = \text{"High"}$, and $\overline{LB} = \text{"Low"}$, set address and give "High" pulse to $\overline{CS2}$.
- iii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{UB} = \text{"High"}$, and $\overline{LB} = \text{"Low"}$, set address and give "Low" pulse to \overline{WE} .
- ix) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, and $\overline{UB} = \text{"High"}$, set address and give "Low" pulse to \overline{LB} .

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, \overline{WE} and $\overline{LB} = \text{"Low"}$.

(2) Writing data into upper byte

There are the following four ways of writing data into the memory.

- i) Hold $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, $\overline{LB} = \text{"High"}$, and $\overline{UB} = \text{"Low"}$, set address and give "Low" pulse to $\overline{CS1}$.
- ii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{WE} = \text{"Low"}$, $\overline{LB} = \text{"High"}$, and $\overline{UB} = \text{"Low"}$, set address and give "High" pulse to $\overline{CS2}$.
- iii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{LB} = \text{"High"}$, and $\overline{UB} = \text{"Low"}$, set address and give "Low" pulse to \overline{WE} .
- ix) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, and $\overline{LB} = \text{"High"}$, set address and give "Low" pulse to \overline{UB} .

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, \overline{WE} and $\overline{UB} = \text{"Low"}$.

(3) Writing data into both bytes

There are the following four ways of writing data into the memory.

- i) Hold $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, \overline{LB} and $\overline{UB} = \text{"Low"}$, set address and give "Low" pulse to $\overline{CS1}$.
- ii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{WE} = \text{"Low"}$, \overline{LB} and $\overline{UB} = \text{"Low"}$, set address and give "High" pulse to $\overline{CS2}$.
- iii) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, \overline{LB} and $\overline{UB} = \text{"Low"}$, set address and give "Low" pulse to \overline{WE} .
- ix) Hold $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, set address and give "Low" pulse to \overline{LB} and \overline{UB} .

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS1} = \text{"Low"}$, $\overline{CS2} = \text{"High"}$, $\overline{WE} = \text{"Low"}$, \overline{UB} and $\overline{LB} = \text{"Low"}$.

As DATA I/O pins are in "Hi-Z" when $\overline{CS1} = \text{"High"}$, $\overline{CS2} = \text{"Low"}$, $\overline{OE} = \text{"High"}$, or \overline{LB} and $\overline{UB} = \text{"High"}$, the contention on the data bus can be avoided. But while I/O pins are in the output state, the data that is opposite to the output data should not be given.

● Standby mode

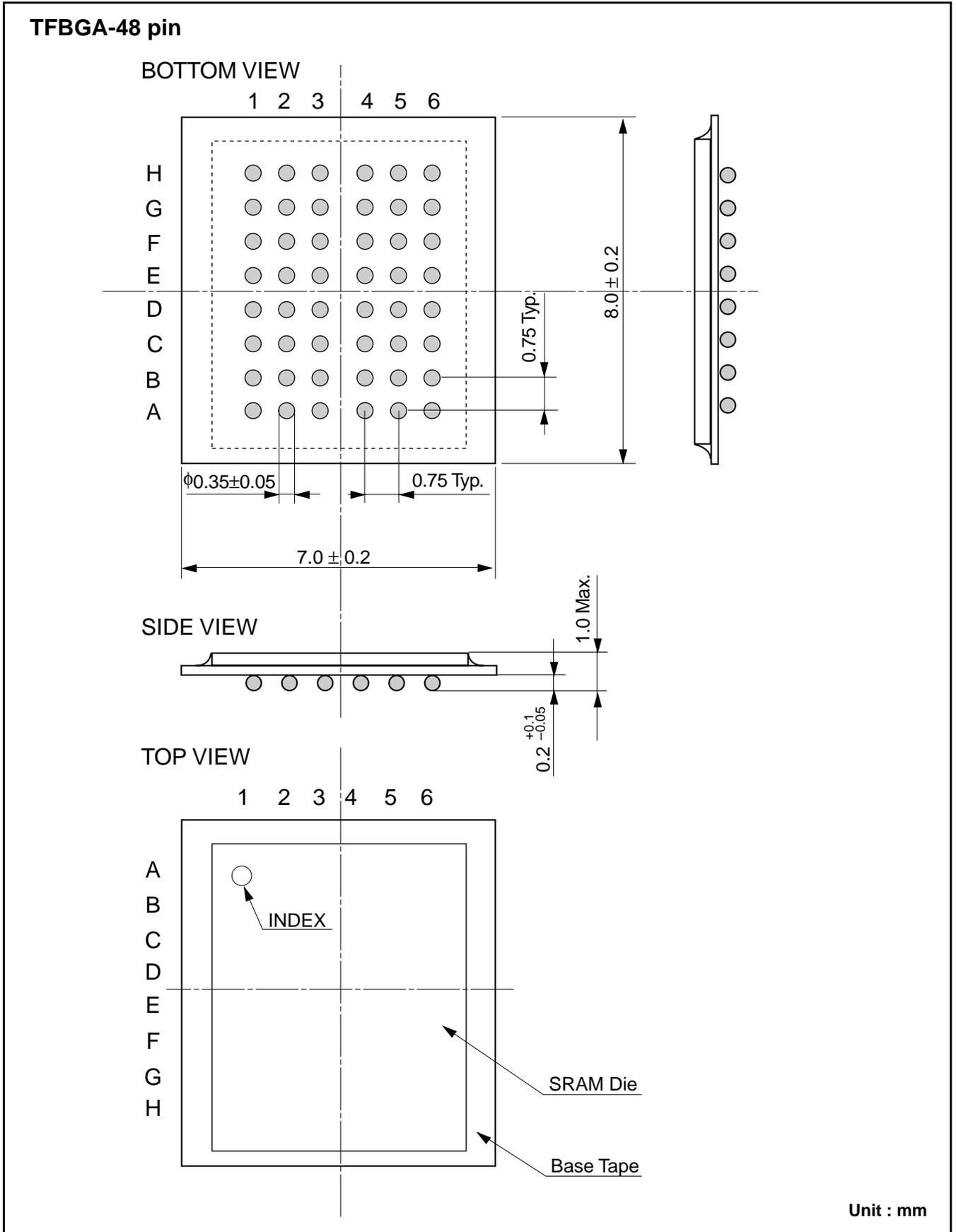
When $\overline{CS1}$ is "High" or $\overline{CS2}$ is "Low" the chip is in the standby mode (only retaining data operation). In this case data I/O pins are Hi-Z, and all inputs of addresses, \overline{WE} , \overline{OE} , \overline{UB} , \overline{LB} , and data are inhibited. When $\overline{CS1} = \overline{CS2} \geq V_{DD} - 0.2V$ or $\overline{CS2} \leq 0.2V$, there is almost no current flow except through the high resistance parts of the memory.

● Data retention at low voltage

In case of the data retention in the standby mode, the power supply can be gone down till the specified voltage. But it is impossible to write or read in this mode.

SRM2AV213LLBT8

PACKAGE DIMENSIONS



■ CHARACTERISTICS CURVES

Under Measurement

SRM2AV213LLBT8

NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 1999 All right reserved.

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : +81-(0)42-587-5812 FAX : +81-(0)42-587-5564

ED International Marketing Department II (Asia)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone : +81-(0)42-587-5814 FAX : +81-(0)42-587-5110

■ EPSON Electronic Devices Website

<http://www.epson.co.jp/device/>



Revised November, 1999
Printed in Japan ①
Rev.1.0