

SRM2AV400LLBT₈

4M-bit Static RAM

Preliminary



- Super Low Voltage Operation and Low Current Consumption
- Access Time 85ns (2.4V)
- 524,288 Words x 8-bit Asynchronous
- Wide Temperature Range

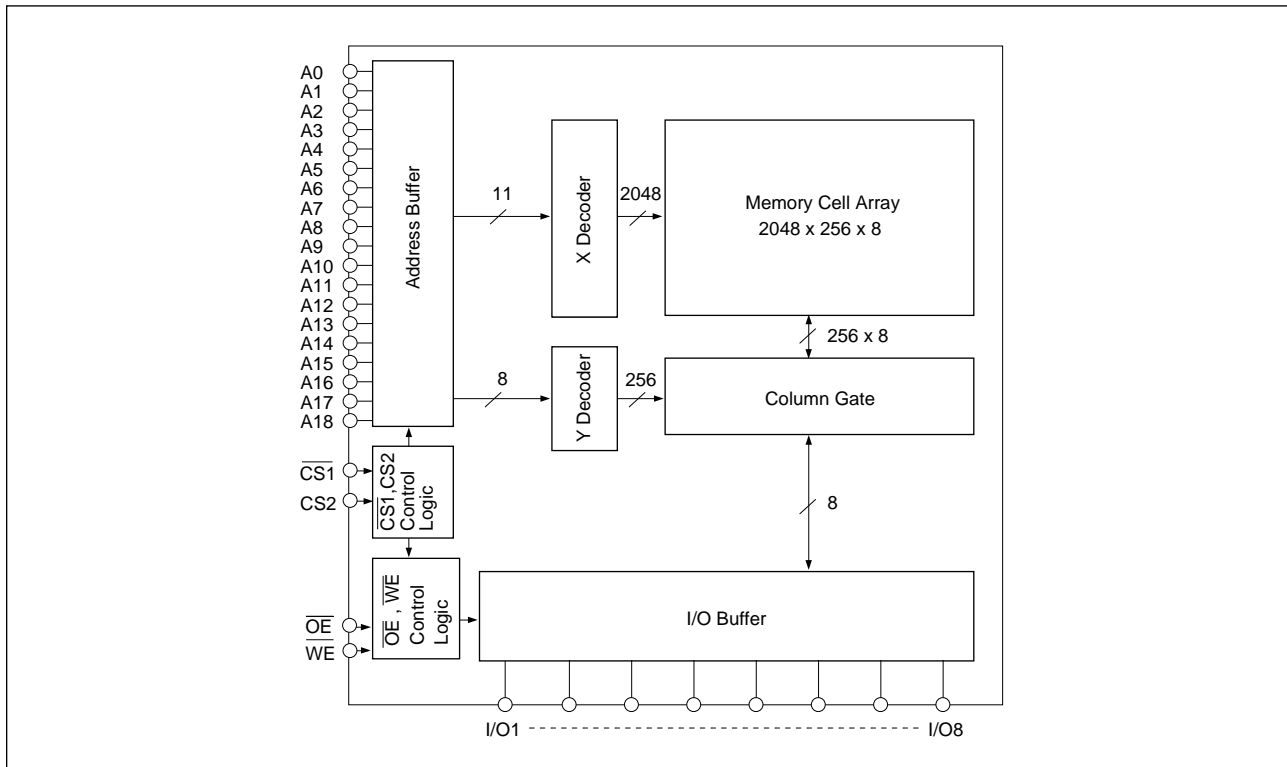
DESCRIPTION

The SRM2AV400LLBT₈ is a 524,288 words x 8-bit asynchronous, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock and no refreshing circuit. 3-state output allows easy expansion of memory capacity. The temperature range of the SRM2AV400LLBT₈ is from -40 to 85°C, and it is suitable for the industrial products.

FEATURES

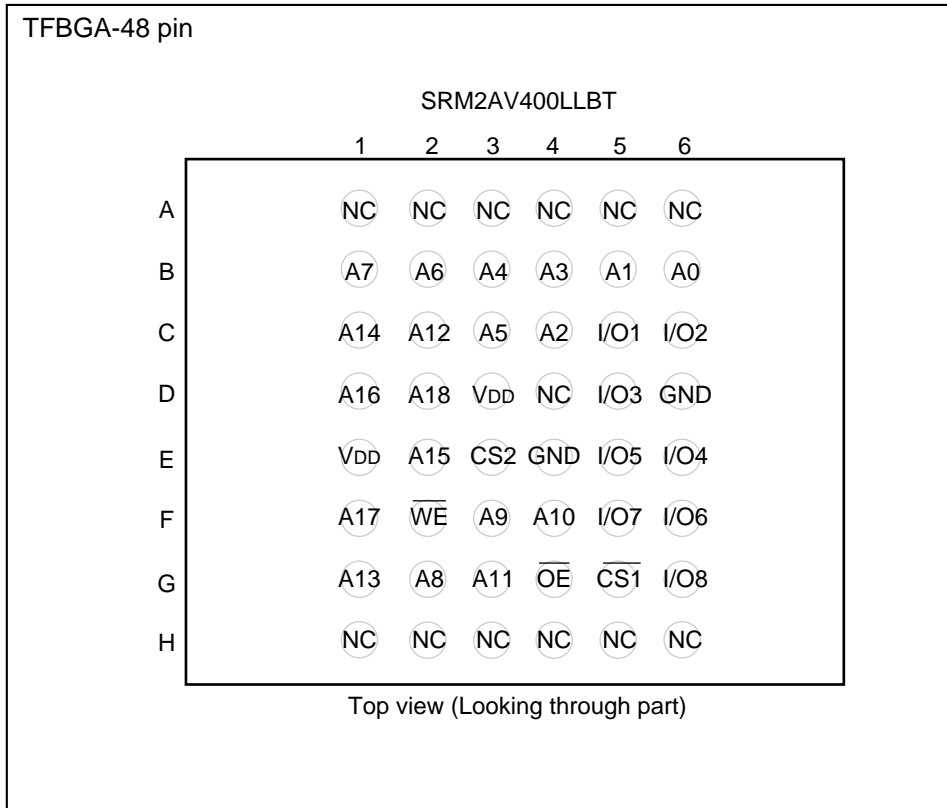
- Fast Access time 85ns (2.4V)
- Low supply current LL Version
- Completely static No clock required
- Supply voltage 2.4V to 3.3V
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM2AV400LLBT TFBGA-48 pin (Tape CSP)

BLOCK DIAGRAM



SRM2AV400LLBT₈

■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A18	Address Input
\overline{WE}	Write Enable
\overline{OE}	Output Enable
$\overline{CS1}$	Chip Select1
CS2	Chip Select2
I/O1 to 8	Data I/O
VDD	Power Supply (2.4V to 3.3V)
VSS	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	- 0.5 to 4.0	V
Input voltage	V _I	- 0.5 * to V _{DD} + 0.3	V
Input/Output voltage	V _{I/O}	- 0.5 * to V _{DD} + 0.3	V
Power dissipation	P _D	0.5	W
Operating temperature	T _{opr}	- 40 to 85	°C
Storage temperature	T _{stg}	- 65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	-

* V_I, V_{I/O} (Min.) = -2.0V (when pulse width is less than 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(T_a = -40 to 85 °C)

Parameter	Symbol	V _{DD} = 2.4 to 3.3V			V _{DD} = 2.7 to 3.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{DD}	2.4	3.0	3.3	2.7	3.0	3.3	V
	V _{SS}	0.0	0.0	0.0	0.0	0.0	0.0	V
Input voltage	V _{IH}	0.75V _{DD}	-	V _{DD} +0.3	2.0	-	V _{DD} +0.3	V
	V _{IL}	- 0.3*	-	0.3	- 0.3*	-	0.6	V

* if pulse width is less than 50ns it is - 2.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{SS} = 0V, T_a = -40 to 85 °C)

Parameter	Symbol	Conditions	V _{DD} = 2.4 to 3.3V			Unit	
			Min.	Typ. *1	Max.		
Input leakage current	I _{LI}	V _I = 0 to V _{DD}	-1.0	-	1.0	μA	
Output leakage current	I _{LO}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{I/O} = 0 to V _{DD}	-1.0	-	1.0	μA	
High level output voltage	V _{OH}	I _{OH}	-0.5mA	2.0	-	-	V
			-100μA	V _{DD} -0.2	-	-	V
Low level output voltage	V _{OL}	I _{OL}	1.0mA	-	-	0.4	V
			100μA	-	-	0.2	V
Standby supply current	I _{DDS}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$	-	-	1.0	mA	
	I _{DDS1}	$\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$ T _a ≤ 25°C, V _{DD} ≤ 3.0V	-	-	15	μA	
Average operating current	I _{DDA}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA, t _{cyc} = Min.	-	25	35	mA	
	I _{DDA1}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA, t _{cyc} = 1μs	-	4.0	6.0	mA	
Operating Supply Current	I _{DDO}	V _I = V _{IL} or V _{IH} I _{I/O} = 0mA	-	4.0	6.0	mA	

*1 : Typical values are measured at T_a = 25°C and V_{DD} = 3.0V

● Terminal Capacitance

(T_a = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C _{ADD}	V _{ADD} = 0V	-	-	8	pF
Input Capacitance	C _I	V _I = 0V	-	-	8	pF
I/O Capacitance	C _{I/O}	V _{I/O} = 0V	-	-	10	pF

Note : This parameter is made by the inspection data of sample, not of all products

SRM2AV400LLBT₈

● AC Electrical Characteristics

○ Read Cycle

(V_{SS} = 0V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions	SRM2AV400LLBT ₈		Unit
			2.4 to 3.0V		
			Min.	Max.	
Read cycle time	t _{RC}	1	85	–	ns
Address access time	t _{ACC}	1	–	85	ns
CS1 access time	t _{ACS1}	1	–	85	ns
CS2 access time	t _{ACS2}	1	–	85	ns
OE access time	t _{OE}	1	–	45	ns
CS1 output set time	t _{CLZ1}	2	5	–	ns
CS2 output set time	t _{CLZ2}	2	5	–	ns
CS1 output floating	t _{CHZ1}	2	–	30	ns
CS2 output floating	t _{CHZ2}	2	–	30	ns
OE output set time	t _{OLZ}	2	0	–	ns
OE output floating	t _{OHZ}	2	–	30	ns
Output hold time	t _{OH}	1	5	–	ns

○ Write Cycle

(V_{SS} = 0V, Ta = -40 to 85°C)

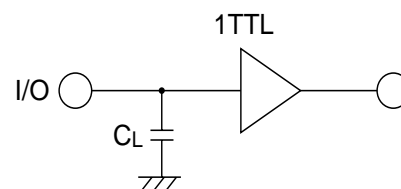
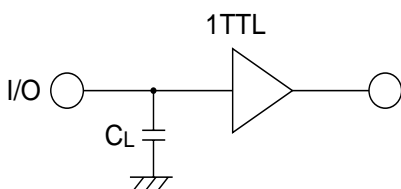
Parameter	Symbol	Test Conditions	SRM2AV400LLBT ₈		Unit
			2.4 to 3.3V		
			Min.	Max.	
Write cycle time	t _{WC}	1	85	–	ns
Chip select time (CS1)	t _{CW1}	1	70	–	ns
Chip select time (CS2)	t _{CW2}	1	70	–	ns
Address enable time	t _{AW}	1	70	–	ns
Address setup time	t _{AS}	1	0	–	ns
Write pulse width	t _{WP}	1	60	–	ns
Address hold time	t _{WR}	1	0	–	ns
Data setup time	t _{DW}	1	35	–	ns
Data hold time	t _{DH}	1	0	–	ns
WE output floating	t _{WHZ}	2	–	35	ns
WE output set time	t _{OW}	2	5	–	ns

*1 Test Conditions

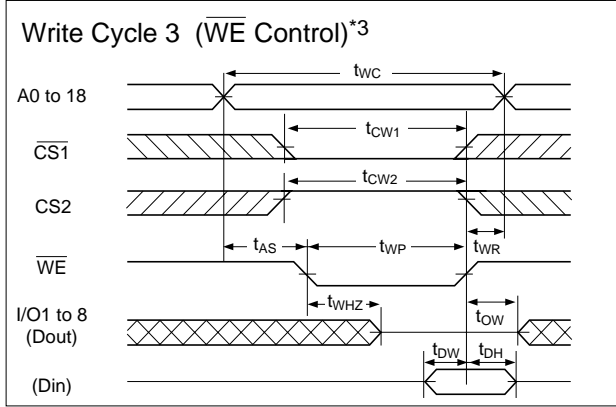
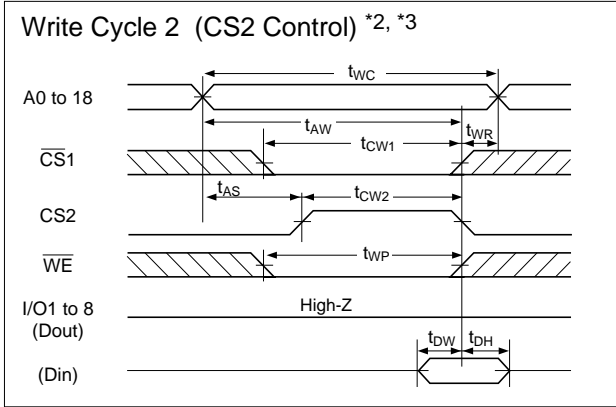
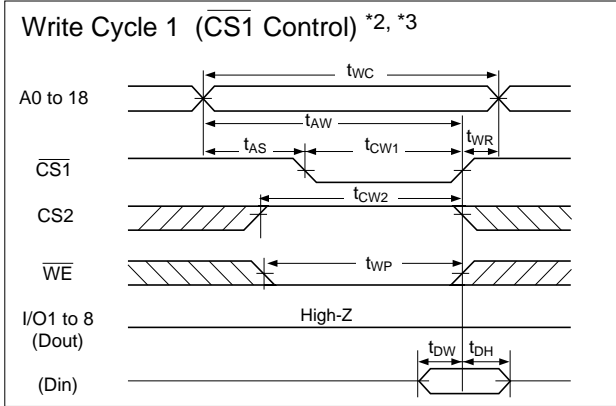
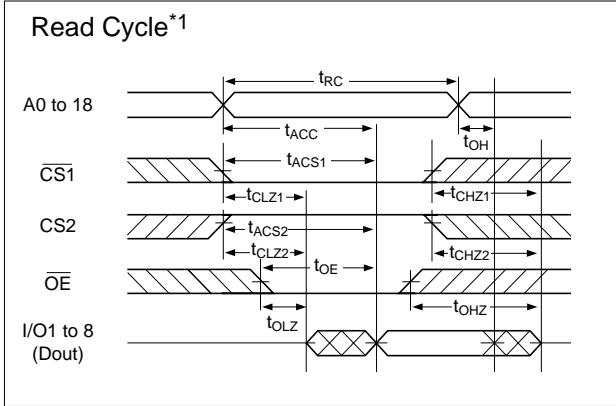
1. Input pulse level : 0.3V to 0.8V_{DD}(2.4V to 3.3V)
2. t_r = t_f = 5ns
3. Input and output timing reference levels : 1/2V_{DD}(2.4V to 3.3V)
4. Output load : C_L = 50pF (Includes Jig Capacitance)

*2 Test Conditions

1. Input pulse level : 0.3V to 0.8V_{DD}(2.4V to 3.3V)
2. t_r = t_f = 5ns
3. Input timing reference levels : 1/2V_{DD}(2.4V to 3.3V)
4. Output timing reference levels : ±200mV (The level changed from stable output voltage level)
5. Output load : C_L = 5pF (Includes Jig Capacitance)



● Timing Chart



- Note :
- *1 During read cycle time, \overline{WE} is to be "High" level.
 - *2 In write cycle time that is controlled by CS1 or CS2, output buffer is to be "Hi-Z" state even if \overline{OE} is "Low" level.
 - *3 When output buffer is in output state, be careful that do not input the opposite signals to the output data.

● DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

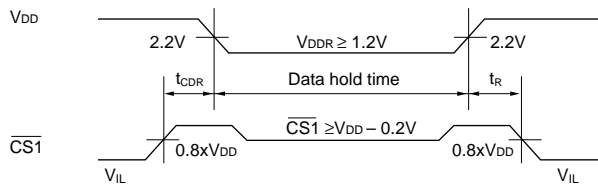
($V_{SS} = 0V, T_a = -40 \text{ to } 85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Data retention supply voltage	V_{DDR}		1.2	—	3.3	V
Data retention current	I_{DDR}	$V_{DDR} = 2.5V$ $\overline{CS1} = \overline{CS2} \geq V_{DD} - 0.2V$ or $\overline{CS2} \leq 0.2V$	—	0.4	13	μA
Data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		5	—	—	ms

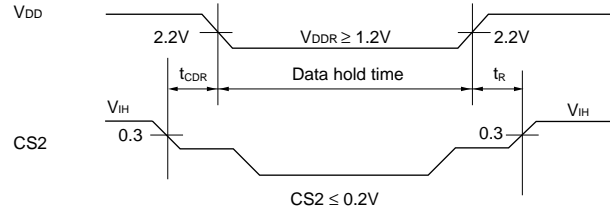
* : Reference data at $T_a = 25^\circ\text{C}$

SRM2AV400LLBT8

Data retention timing (CS1 Control)



Data retention timing (CS2 Control)



FUNCTIONS

Truth Table

CS1	CS2	OE	WE	I/O1 to 8	MODE	IDD
H	X	X	X	High-Z	Not Selected	IDDS, IDDS1
X	L	X	X	High-Z	Not Selected	IDDS, IDDS1
L	H	H	H	High-Z	Output disable	IDDA, IDDA1
L	H	X	L	Data In	Byte Write	IDDA, IDDA1
L	H	L	H	Data Out	Byte Read	IDDA, IDDA1

X : High or Low

Reading data

(1) Reading data from byte

Data is able to be read when the address is set while holding CS1 = "Low", CS2 = "High", OE = "Low", and WE = "High".

Since I/O pins are in "Hi-Z" state when OE = "High", the data bus line can be used for any other objective, then access time is apparently able to be cut down.

Writing data

(1) Writing data into byte

There are the following three ways of writing data into the memory.

- Hold CS2 = "High", WE = "Low", set address and give "Low" pulse to CS1.
- Hold CS1 = "Low", WE = "Low", set address and give "High" pulse to CS2.
- Hold CS1 = "Low", CS2 = "High", set address and give "Low" pulse to WE.

Anyway, data on I/O pins are latched up into the memory cell during CS1 = "Low", CS2 = "High", and WE = "Low". As DATA I/O pins are in "Hi-Z" when CS1 = "High", CS2 = "Low", or OE = "High", the contention on the data bus can be avoided. But while I/O pins are in the output state, the data that is opposite to the output data should not be given.

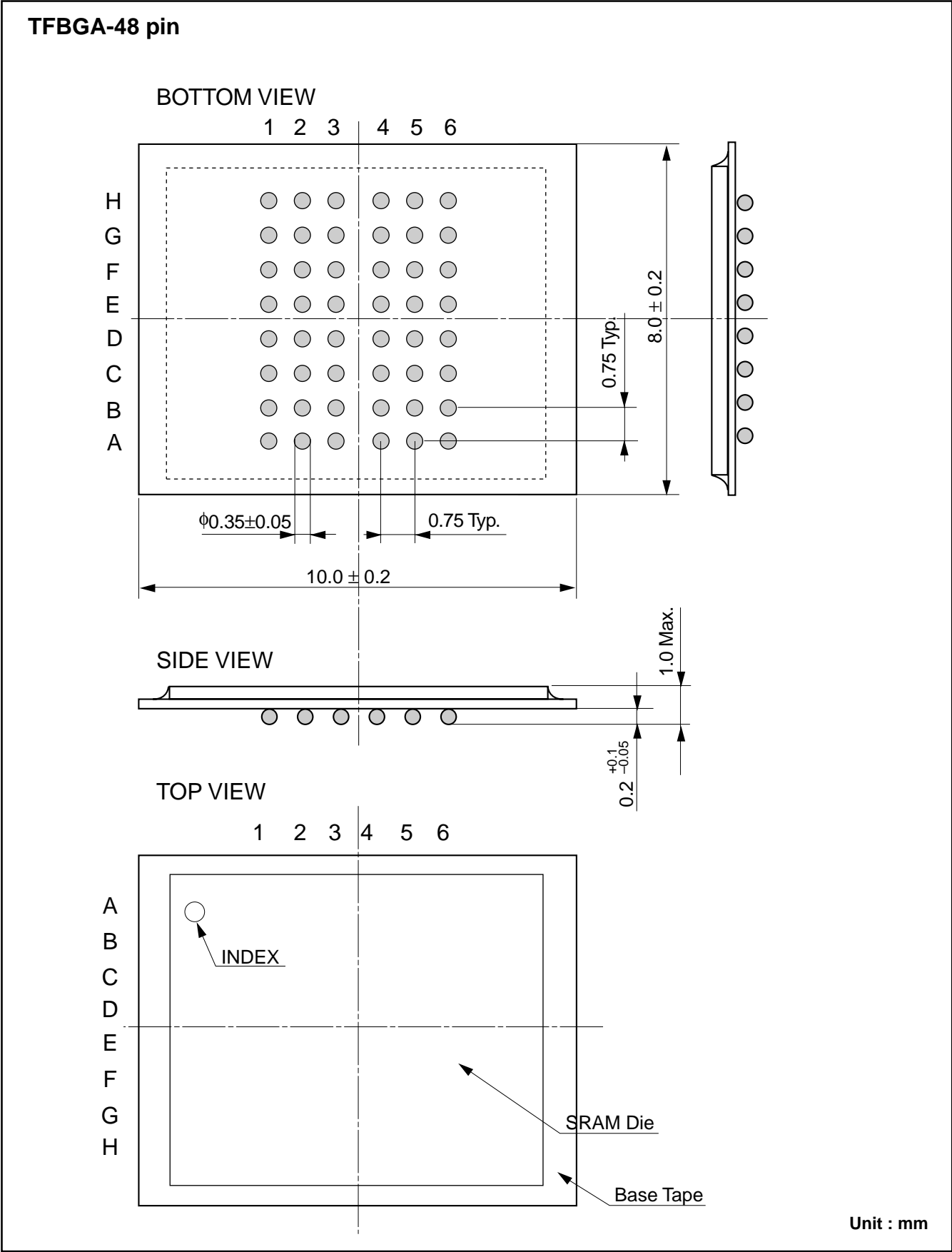
Standby mode

When CS1 is "High" or CS2 is "Low" the chip is in the standby mode (only retaining data operation). In this case data I/O pins are Hi-Z, and all inputs of addresses, WE, OE, and data are inhibited. When CS1 = CS2 ≥ VDD - 0.2V or CS2 ≤ 0.2V, there is almost no current flow except through the high resistance parts of the memory.

Data retention at low voltage

In case of the data retention in the standby mode, the power supply can be gone down till the specified voltage. But it is impossible to write or read in this mode.

■ PACKAGE DIMENSIONS



■ **CHARACTERISTICS CURVES**

Under Measurement

SRM2AV400LLBT8

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Revised November, 1999
Printed in Japan ①

Rev.1.0