M253-60

EPSON

Application Manual

Real Time Clock Module

RTC-4543

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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Our Lineup of semiconductors, Liquid crystal displays and quartz devices assists in creating the products of our customers' dreams.
Epson IS energy savings.

CONTENTS

32-kHz Output Serial RTC Module

RTC-4543

- Built-in crystal permits operation without requiring adjustment
- Built-in time counters (seconds, minutes, hours) and calendar counters (days, days of the week, months, years)
- Operating voltage range: 2.5V to 5.5V
- Supply voltage detection voltage: 1.7 ±0.3V
- Low current consumption: 1.0 μA/2.0V (Max.)
- Automatic processing for leap years
- Output selectable between 32.768 kHz/1 Hz

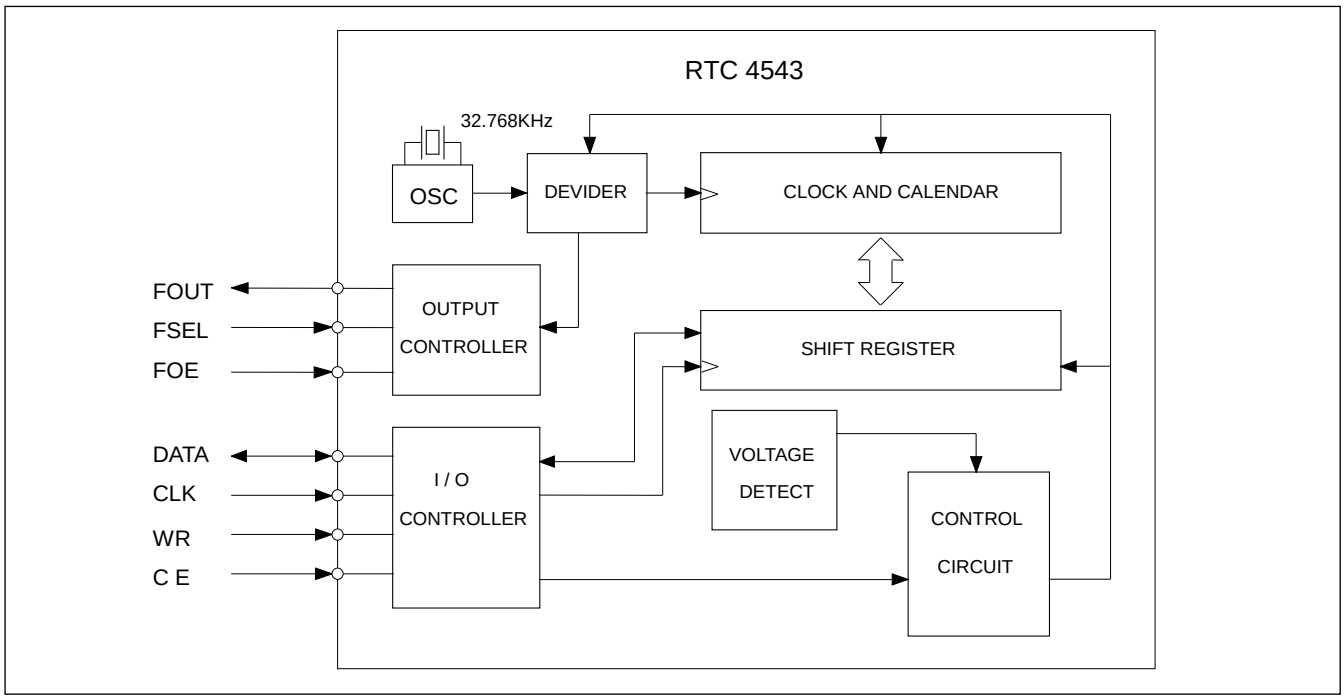
■ Overview

This module is a real-time clock with a serial interface and a built-in crystal resonator. This module is also equipped with clock and calendar circuits, an automatic leap year compensation function, and a supply voltage detection function.

In addition, this module has a 32.768 kHz/1 Hz selectable output function for hardware control that is independent of the RTC circuit.

This module is available in a compact SOP 14-pin package (RTC-4543SA) and a thin SOP 18-pin package (RTC-4543SB).

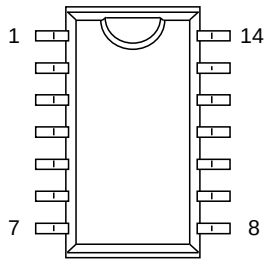
■ Block diagram



■ Pin Connections

RTC - 4543SA

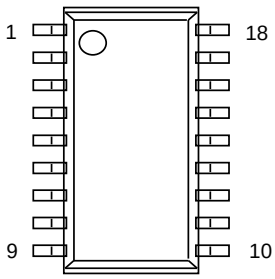
1	GND	14	FOUT
2	N.C	13	N.C
3	CE	12	N.C
4	FSEL	11	DATA
5	WR	10	CLK
6	FOE	9	V_{DD}
7	N.C	8	N.C



SOP - 14pin

RTC - 4543SB

1	N.C	18	N.C
2	N.C	17	N.C
3	N.C	16	N.C
4	N.C	15	N.C
5	FOE	14	V_{DD}
6	WR	13	N.C
7	FSEL	12	CLK
8	CE	11	DATA
9	GND	10	FOUT



SOP - 18pin

■ Pin Functions

Signal	Pin No. SOP-14pin (SOP-18pin)	I/O	Function
GND	1 (9)		Connects to negative (-) side (ground) of the power supply.
CE	3 (8)	Input	Chip enable input pin. When high, the chip is enabled. When low, the DATA pin goes to high impedance and the CLK, DATA, and WR pins are not able to accept input. In addition, when low, the TM bit is cleared.
FSEL	4 (7)	Input	Selects the frequency that is output from the FOUT pin. High: 1 Hz Low: 32.768 kHz
WR	5 (6)	Input	DATA pin input/output switching pin. High: Data input (when writing the RTC) Low: Data output (when reading the RTC)
FOE	6 (5)	Input	When high, the frequency selected by the FSEL pin is output from the FOUT pin. When low, the FOUT pin goes to high impedance.
V_{DD}	9 (14)		Connects to the positive (+) side of the power supply.
CLK	10 (12)	Input	Serial clock input pin. Data is gotten at the rising edge during a write, and data is output at the rising edge during a read.
DATA	11 (11)	Bi-directio-nal	Input/output pin that is used for writing and reading data.
FOUT	14 (10)	Output	Outputs the frequency selected by the FSEL pin. 1 Hz output is synchronized with the internal one-second signal. This output is not affected by the CE pin.
N.C.	2,7,8,12,13 (1,2,3,4,13, 15,16,17,18)		Although these pins are not connected internally, they should always be left open in order to obtain the most stable oscillation possible.

● Always connect a passthrough capacitor of at least 0.1 μF as close as possible between VDD and GND.

■ Electrical Characteristics

1. Absolute Maximum Ratings

Item	Symbol	Conditions	MIN.	MAX.	Unit
Supply voltage	VDD	Ta=25°C	-0.3	7.0	V
Input voltage	VI		GND - 0.3	V_{DD}+0.3	V
Output voltage	VO		GND - 0.3	V_{DD}+0.3	V
Storage temperature	TSTG	—	-55	+125	°C

2. Operating Condition

Item	Symbol	Conditions	MIN.	MAX.	Unit
Operating supply voltage	V_{DD}	—	2.5	5.5	V
Date Holding voltage	VCLK	—	1.4	5.5	V
Operating temperature	TOPR	—	-40	+85	°C

3. Frequency Characteristics

Item	Symbol	Conditions	MAX.	Unit
Frequency tolerance	∆f/fO	Ta=25°C, V_{DD}=5.0V	5 ± 23 *	ppm
Frequency temperature characteristics	top	-10 to +70°C, 25°C ref.	+ 10 / - 120	ppm
Frequency voltage characteristics	f/V	Ta=25°C, V_{DD}=2.0 ~ 5.5V	± 2	ppm/V
Oscillation start time	t_{STA}	Ta=25°C, V_{DD}=2.5V	3	sec
Aging	fa	Ta = 25°C, V_{DD} = 5 V, first year	± 5	ppm

* Monthly deviation: Approx. 1 min.

4. DC Characteristics

Unless specified otherwise: V_{DD} = 5 V ± 10%, Ta = -40 to +85°C

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Current consumption (1)	$I_{DD}1$	V_{DD}=5.0V	CE=L , FOE=L FSEL=H		1.5	3.0	µA
Current consumption (2)	$I_{DD}2$	V_{DD}=3.0V			1.0	2.0	µA
Current consumption (3)	$I_{DD}3$	V_{DD}=2.0V			0.5	1.0	µA
Current consumption (4)	$I_{DD}4$	V_{DD}=5.0V	CE=L , FOE=H FSEL=L No load on the FOUT pin		4.0	10.0	µA
Current consumption (5)	$I_{DD}5$	V_{DD}=3.0V			2.5	6.5	µA
Current consumption (6)	$I_{DD}6$	V_{DD}=2.0V			1.5	4.0	µA
Input voltage	V_{IH}	WR,DATA,CE,CLK, FOE,FSEL pins		0.8 VDD			V
	V_{IL}	WR,CE,CLK,FOE,FSEL pins V_{IN} = V_{DD} or GND				0.2 V_{DD}	V
Input off/leak current	I_{OFF}					0.5	µA
Output voltage	$V_{OH(1)}$	V_{DD}=5.0V	IOH=-1.0mA DATA , FOUT pins	4.5			V
	$V_{OH(2)}$	V_{DD}=3.0V		2.0			V
	$V_{OL(1)}$	V_{DD}=5.0V	IOH= 1.0mA				V
	$V_{OL(2)}$	V_{DD}=3.0V	DATA , FOUT pins				V
Output load condition (fanout)	N / CL	FOUT pin		2 LSTTL / 30pF MAX.			
Output leak current	I_{OZH}	V_{OUT}=5.5V	DATA , FOUT pins	-1.0		1.0	µA
	I_{OZL}	V_{OUT}=0V	DATA , FOUT pins	-1.0		1.0	µA
Supply voltage detection voltage	V_{DT}	—		1.4	1.7	2.0	V

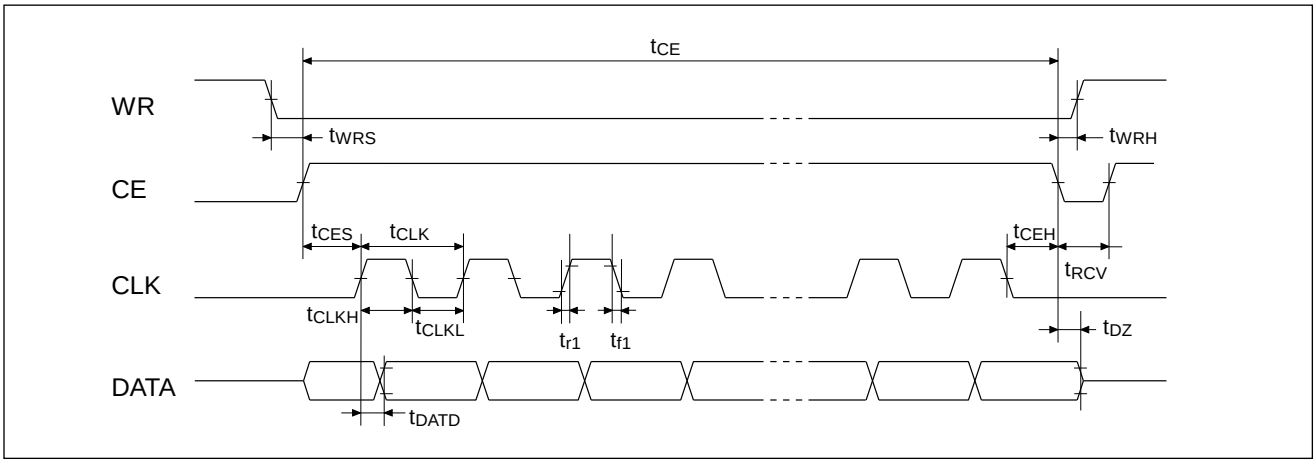
5. AC Characteristics

Unless specified otherwise: Ta = -40 to +85°C, CL = 50 pF

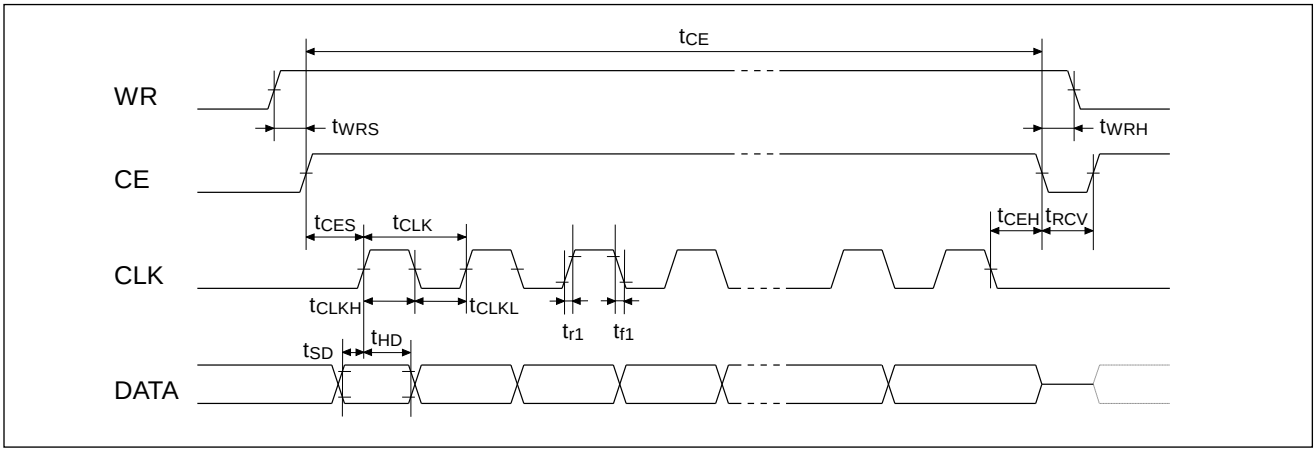
Item	Symbol	V_{DD}=5V±10%		V_{DD}=3V±10%		Unit
		MIN.	MAX.	MIN.	MAX.	
CLK clock cycle	t_{CLK}	0.75	7800	1.5	7800	µS
CLK low pulse width	t_{CLKL}	0.375	3900	0.75	3900	µS
CLK high pulse width	t_{CLKH}	0.375	3900	0.75	3900	µS
CE setup time	t_{CES}	0.375	3900	0.75	3900	µS
CE hold time	t_{CEH}	0.375		0.75		µS
CE enable time	t_{CE}		0.9		0.9	Sec
Write data setup time	t_{SD}	0.1		0.2		µS
Write data hold time	t_{HD}	0.1		0.1		µS
WR setup time	t_{WRS}	100		100		nS
WR hold time	t_{WRH}	100		100		nS
DATA output delay time	t_{DATD}		0.2		0.4	µS
DATA output floating time	t_{DZ}		0.1		0.2	µS
Clock input rise time	t_{r1}		50		100	nS
Clock input fall time	t_{f1}		50		100	nS
FOUT rise time (CL = 30 pF)	t_{r2}		100		200	nS
FOUT fall time (CL = 30 pF)	t_{f2}		100		200	nS
Disable time (CL = 30 pF)	t_{XZ}		100		200	nS
Enable time (CL = 30 pF)	t_{ZX}		100		200	nS
FOUT duty ratio (CL = 30 pF)	Duty	40	60	40	60	%
Wait time	t_{RCV}	0.95		1.9		µS

6. Timing Charts

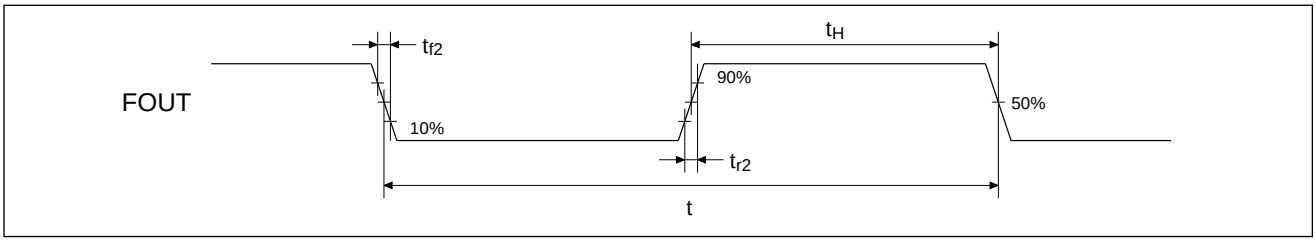
(1) Data read



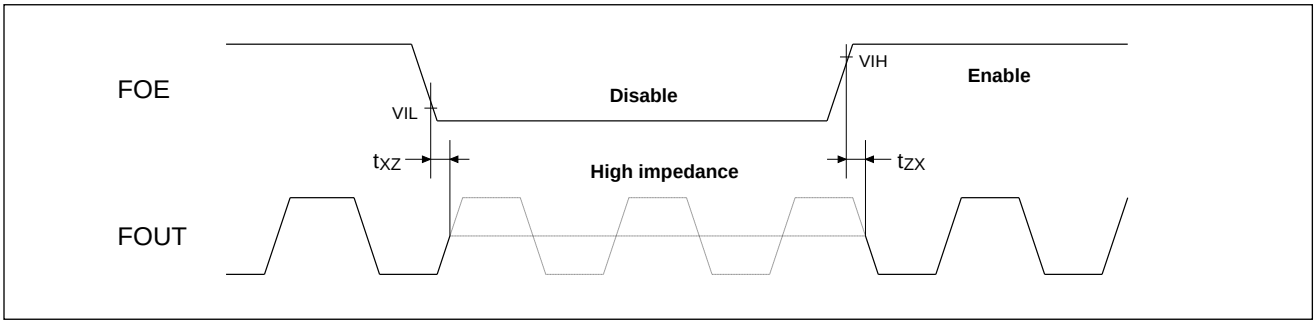
(2) Data write



(3) FOUT output



(4) Disable/enable



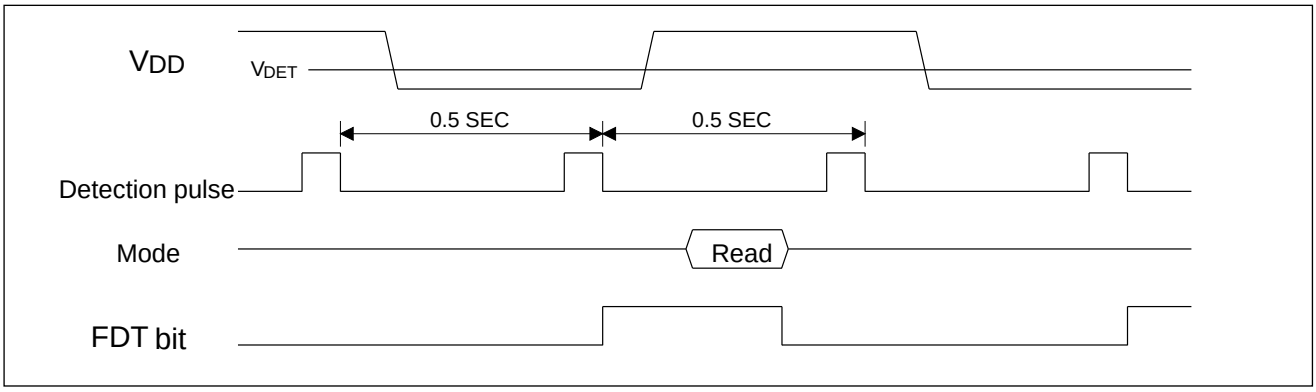
■ Timer Data Organization

- The counter data is BCD code.
- The timer automatically adjusts for different month lengths and for leap year.
- The time is indicated in 24-hour format.
- Writes and reads are both performed on an LSB-first basis.

	MSB							LSB
Seconds (0 to 59)	FDT	s40	s20	s10	s8	s4	s2	s1
Minutes (0 to 59)	*	mi40	mi20	mi10	mi8	mi4	mi2	mi1
Hour (0 to 23)	*	*	h20	h10	h8	h4	h2	h1
Day of the week (1 to 7)					*	w4	w2	w1
Day (1 to 31)	*	*	d20	d10	d8	d4	d2	d1
Month (1 to 12)	TM	*	*	mo10	mo8	mo4	mo2	mo1
Year (0 to 99)	y80	y40	y20	y10	y8	y4	y2	y1

* bits: Any data may be written to these bits.

- FDT bit: Supply voltage detection bit
  - This bit is set to “1” when voltage of 1.7 ±0.3 V or less is detected between V_{DD} and GND.
  - The FDT bit is cleared if all of the digits up to the year digits are read.
  - Although this bit can be both read and written, normally set this bit to “0”.

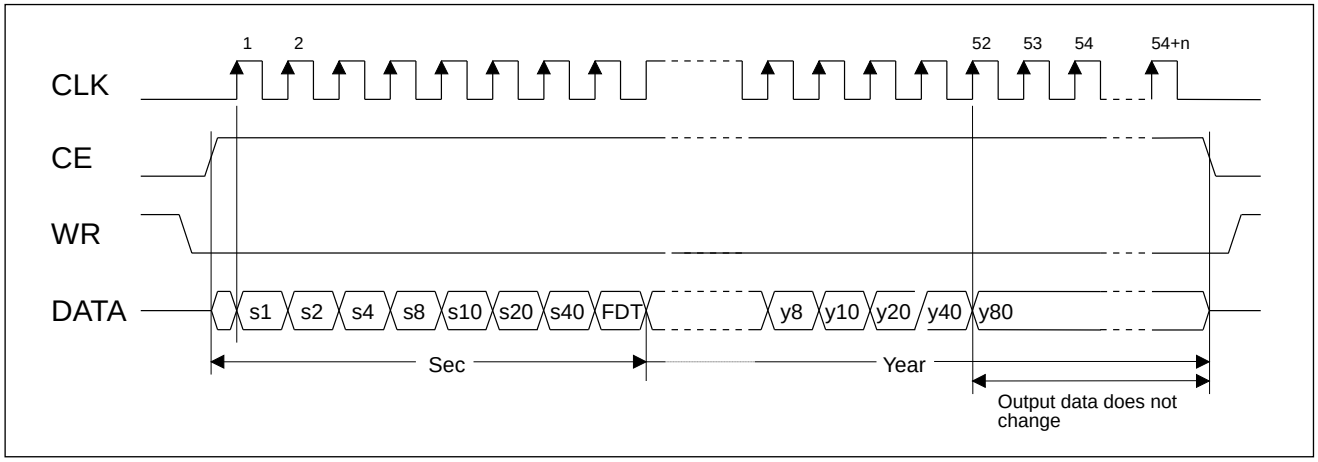


The supply voltage detection circuit monitors the supply voltage once every 0.5 seconds; if the supply voltage is lower than the detection voltage value, the FDT bit is set to “1”.

- TM bit: This is a test bit for SEIKO-EPSON’s use. Always set this bit to “0”.

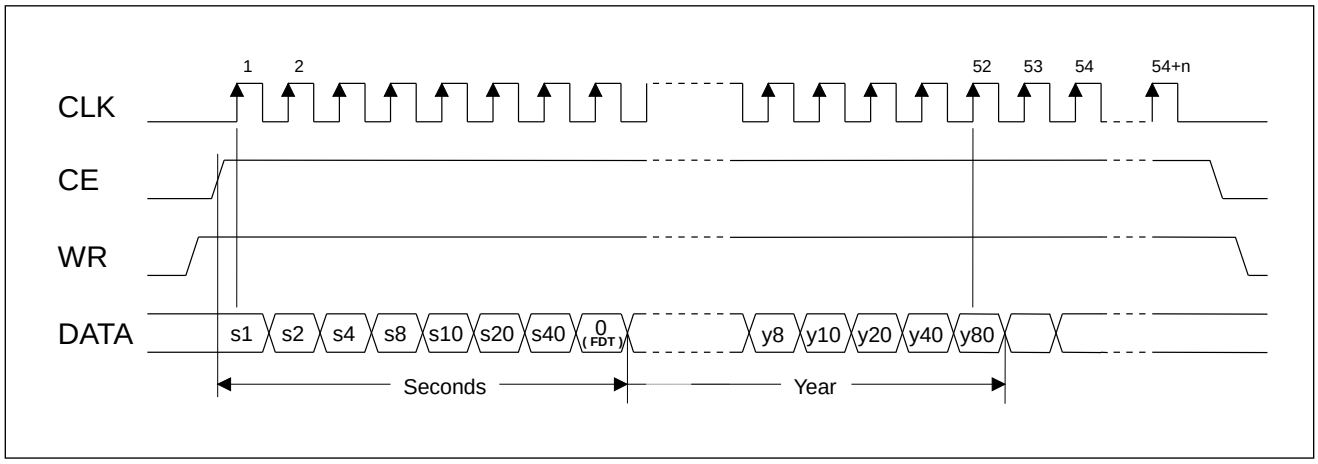
■ Description of Operation

(1) Data reads



1) When the WR pin is low and the CE pin is high, the RTC enters data output mode.
2) At the first rising edge of the CLK signal, the clock and calendar data are loaded into the shift register and the LSB of the seconds digits is output from the DATA pin.
3) The remaining seconds, minutes, hour, day of the week, day, month, and year data is shifted out, in sequence and in synchronization with the rising edge of the CLK signal, so that the data is output from the DATA pin.
   The output data is valid until the rising edge of the 52nd clock pulse; even if more than 52 clock pulses are input, the output data does not change.
4) If data is required in less than 52 clock pulses, that part of the data can be gotten by setting the CE pin low after the necessary number of clock pulses have been output.
   Example: If only the data from “seconds” to “day of the week” is needed:
   After 28 clock pulses, set the CE pin low in order to get the data from “seconds” to “day of the week.”
5) When performing successive data read operations, a wait (t_{RCV}) is necessary after the CE pin is set low.
6) Note that if an update operation (a one-second carry) occurs during a data read operation, the data that is read will have an error of -1 second.
7) Complete data read operations within t_{CE} (max.) = 0.9 seconds, as described earlier.

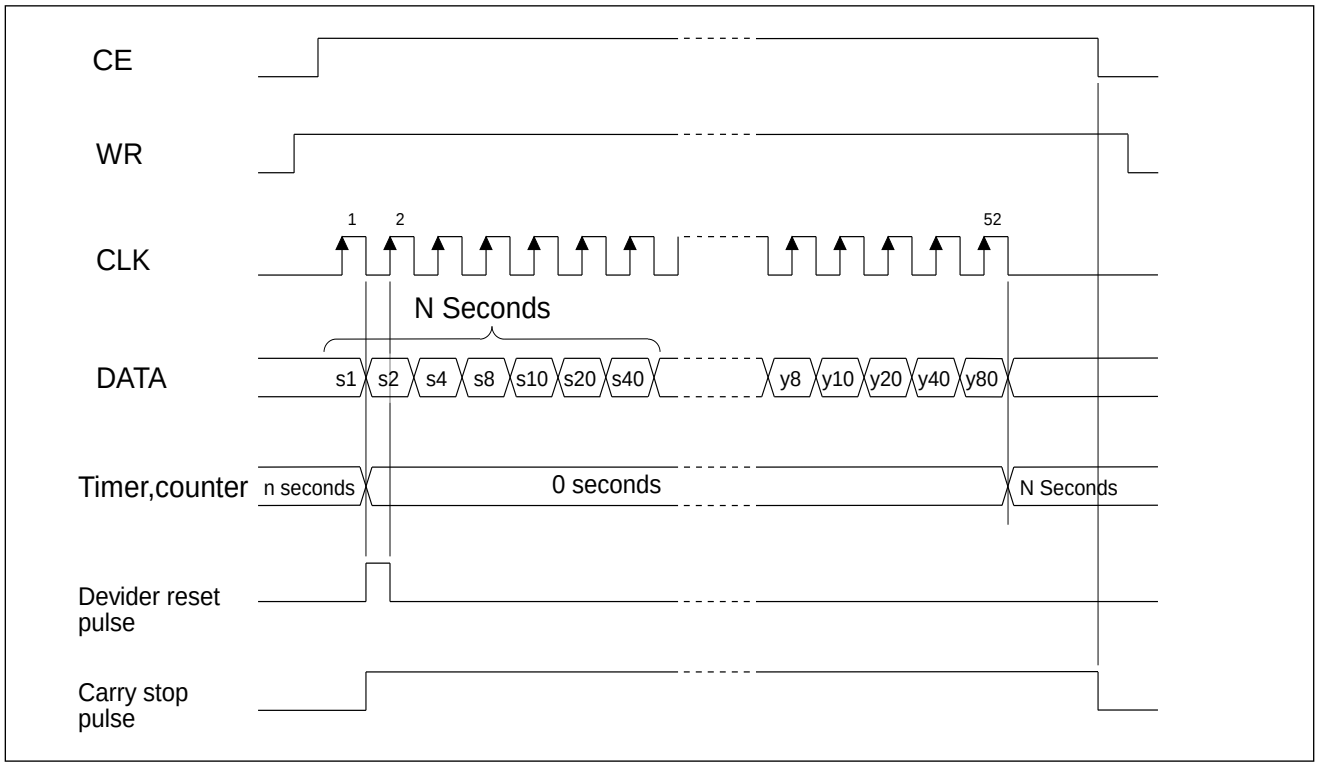
(2) Data writes



1) When the WR pin is high and the CE pin is high, the RTC enters data input mode.
2) In this mode, data is input, in succession and in synchronization with the rising edge of the CLK signal, to the shift register from the DATA pin, starting from the LSB of the seconds digits.
3) The sub-seconds counter is reset between the falling edge of the first clock pulse and the rising edge of the second clock pulse. In addition, carries to the seconds counter are prohibited at the falling edge of the first clock pulse.
4) After the last data is input to the shift register at the rising edge of the 52nd clock pulse, the contents of the shift register are transferred to the timer counter.
5) Note that during a data write operation, 52 bits of data must be input.
   - If the CE pin is set low before 52 bits have been input, the data that was input becomes invalid.
   - If more than 52 bits of data are input, the 53rd and subsequent bits are ignored. (The first 52 bits of data are valid.)
6) Once the CE pin is set low, the prohibition on carries to the seconds counter is lifted.
   Complete data write operations within t_{CE} (max.) = 0.9 seconds, as described earlier.
7) If a data read operation is to be performed immediately after a data write operation, a wait (t_{RCV}) is necessary after the CE pin is set low.

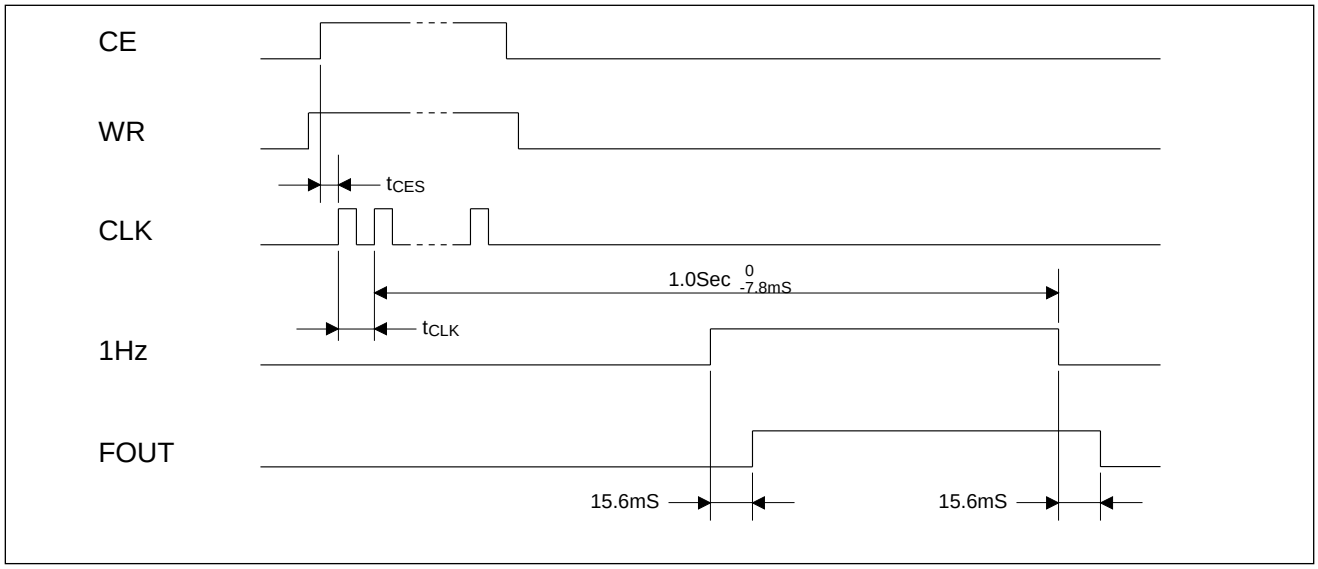
* Misoperation will result if illegal data is written. Therefore, be certain to write legal data.

(3) Data writes (Devider Reset)



After the counter is reset, carries to the seconds digit are halted. After the data write operation, the prohibition on carries to the seconds counter is lifted by setting the CE pin low.
Complete data write operations within t_{CE} (max.) = 0.9 seconds, as described earlier.

(4) FOUT output and 1 Hz carries

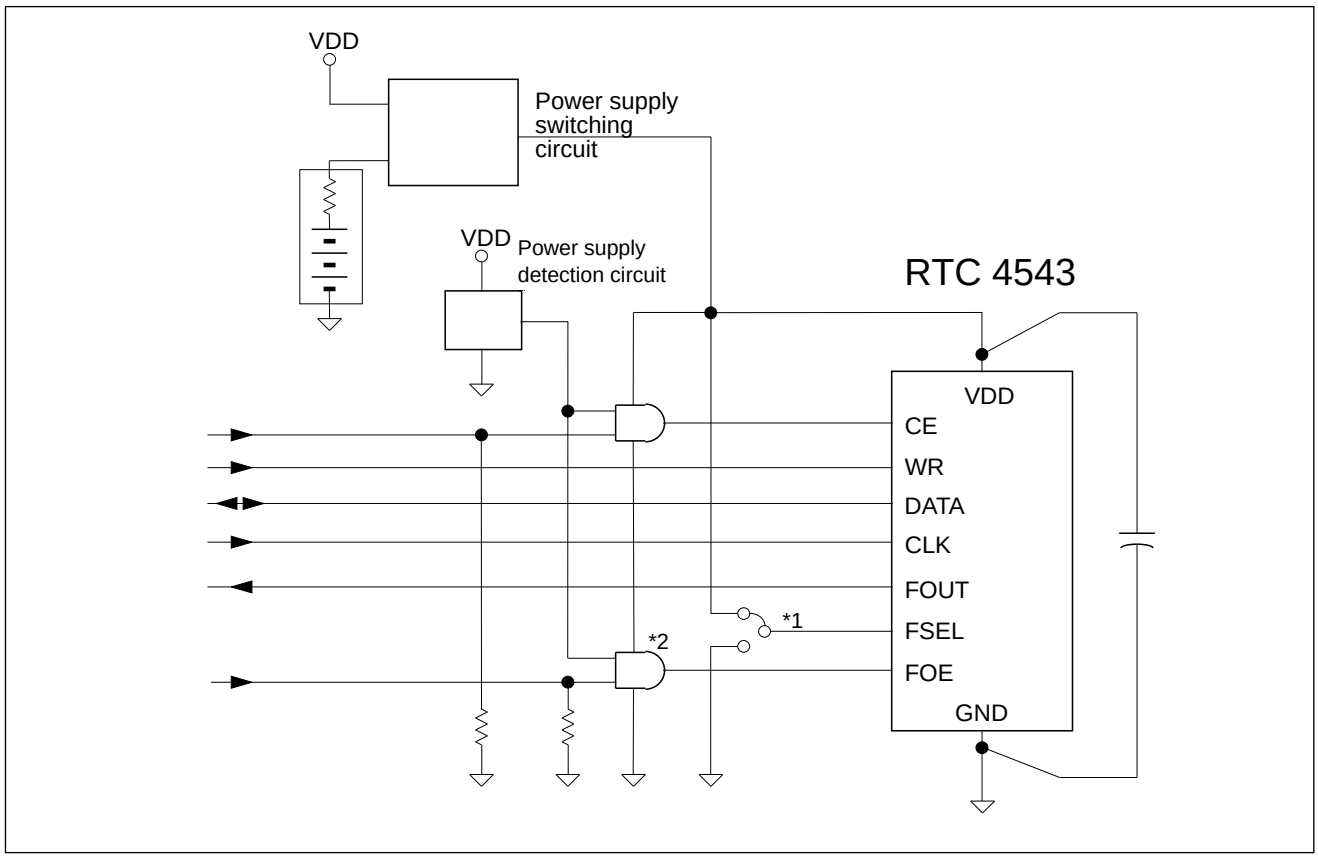


During a data write operation, because a reset is applied to the Devider counter (from the 128 Hz level to the 1 Hz level) after the CE pin goes high during the time between the falling edge of the first clock cycle and the rising edge of the second clock cycle, the length of the first 1 Hz cycle after the data write operation is Subsequent cycles are output at 1.0-second intervals.

The 1-Hz signal that is output on FOUT is the internal 1-Hz signal with a 15.6-ms shift applied.

■ Examples of External Circuits

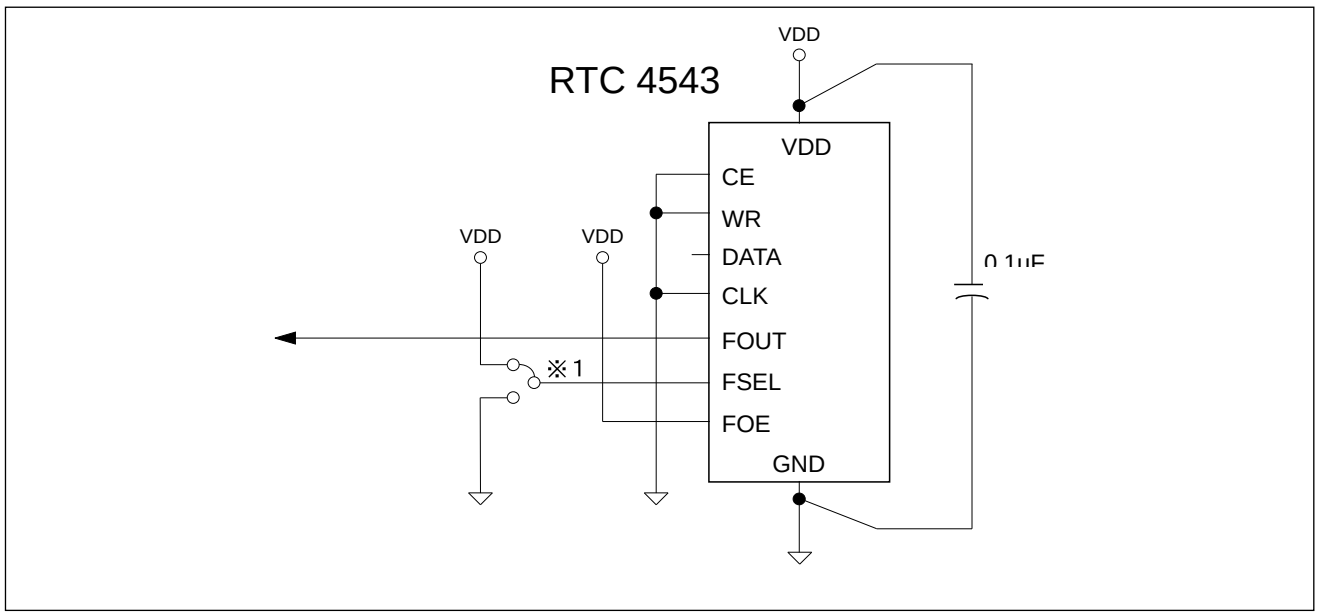
● Example 1. When used as an RTC + clock source



*1: FOUT output frequency setting (High: 1 Hz; low: 32.768 KHz)

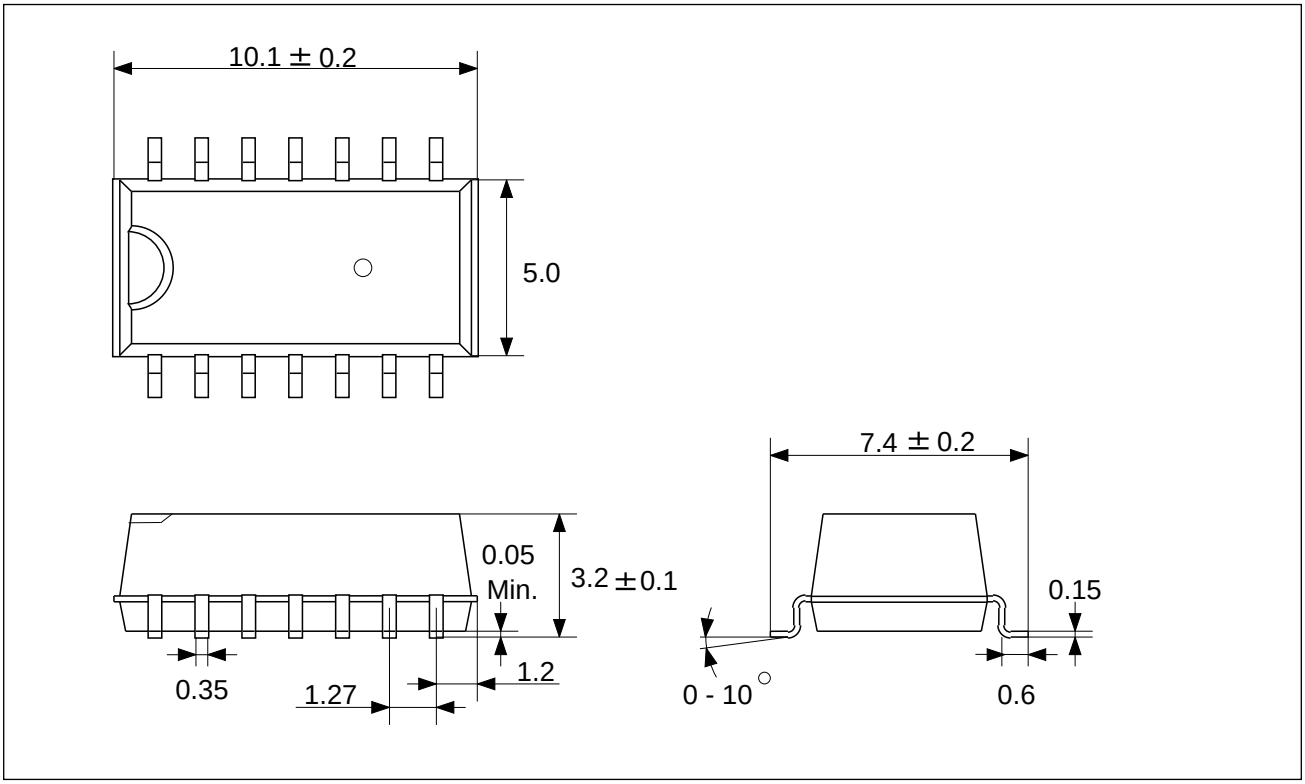
*2: Prohibits FOUT output during back up, reducing current consumption.

● Example 2. When used as a clock source (oscillator)

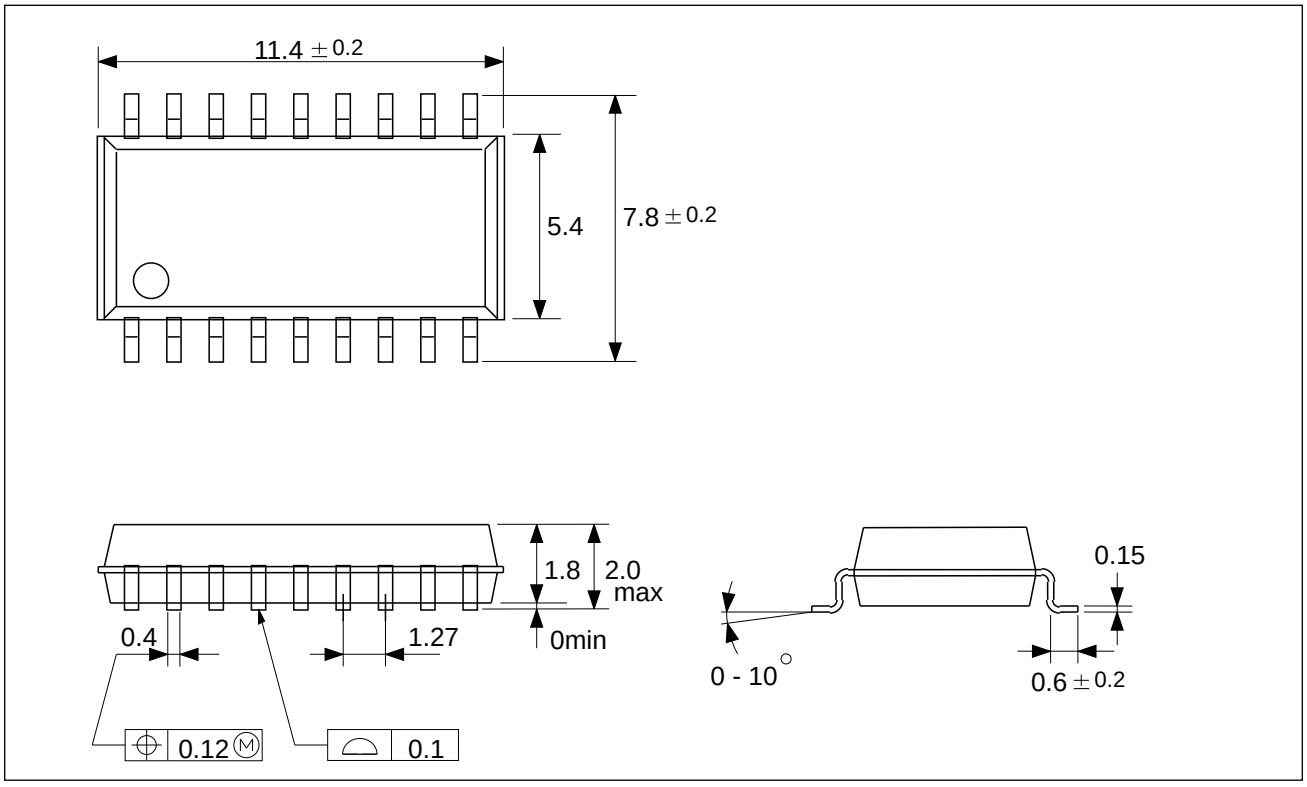


■ External Dimensions

● RTC-4543SA (SOP 14-pin)

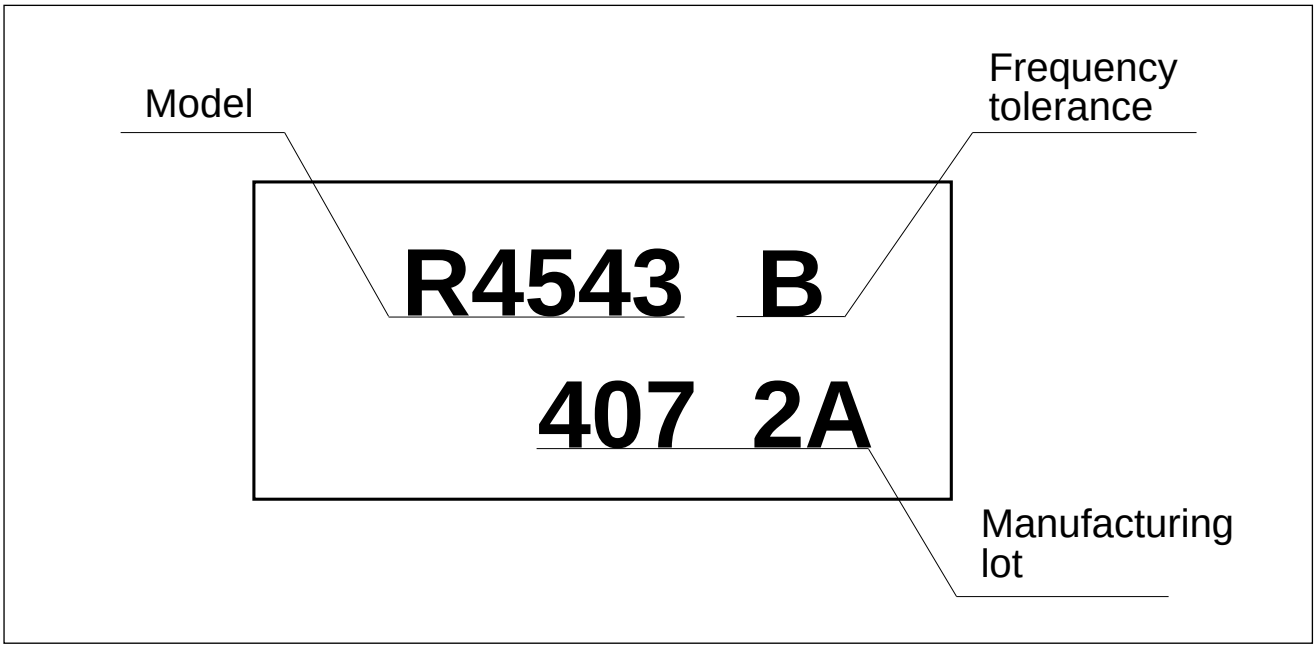


● RTC-4543SB (SOP 18-pin)

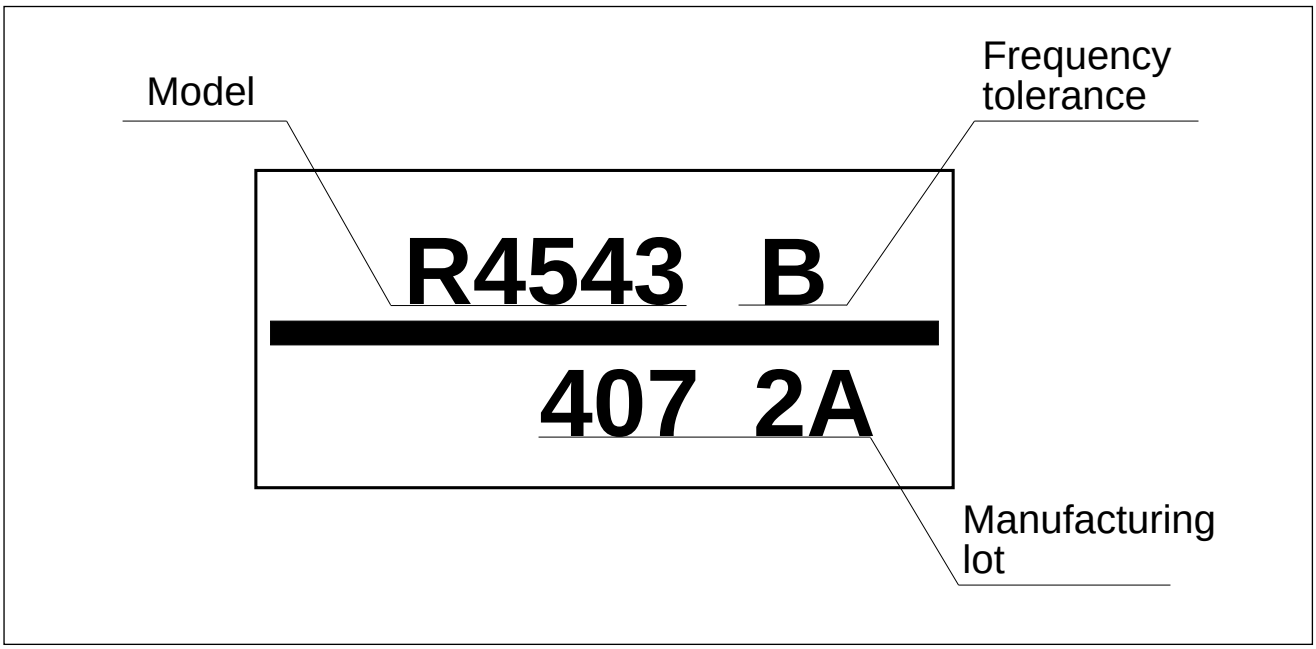


■ Layout of Package Markings

● **RTC-4543SA (SOP 14-pin)**



● **RTC-4543SB (SOP 18-pin)**



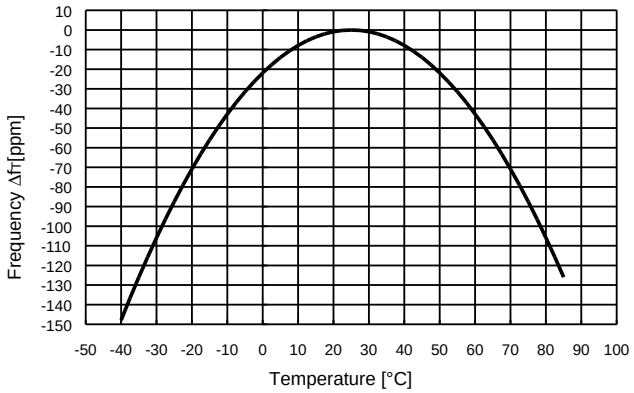
Note: The markings and their positions as pictured above are only approximations. These illustrations do not define the details of the style, size, and position of the characters marked on the packages.

■ Reference Data

(1) Example of Frequency-Temperature Characteristics

θ_T = 25°C

α= -0.035ppm/(C2(TYP.) TYP.



Determining the frequency stability (clock accuracy)

1. The frequency-temperature characteristics can be approximated by the following equation:
   $\Delta fT(ppm)=\alpha(\theta T-\theta x)^2$

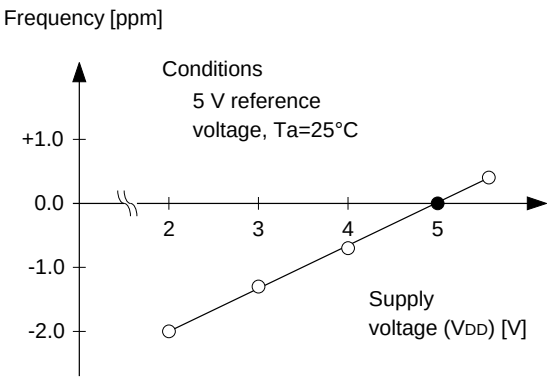
Δfr(ppm):	Frequency deviation at any given temperature
α(ppm/°C^2):	Second-order temperature (-0.035 ±0.005 ppm/°C^2)
θ_T(°C):	Highest temperature (25°C±5°C)
θ_X(°C):	Any given temperature

2. In order to determine the clock accuracy, add in the frequency tolerance and the voltage characteristics.
   $\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta fv$

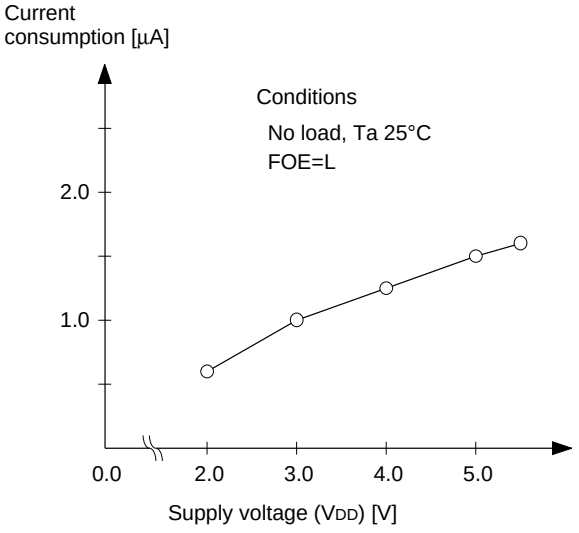
$\Delta f/f$(ppm):	Clock accuracy at any given temperature and voltage (frequency stability)
$\Delta f/f_0$(ppm):	Frequency accuracy
Δf_T(ppm):	Frequency deviation at any given temperature
Δf_V(ppm):	Frequency deviation at any given voltage

3. Determining the daily error
   Daily error =$\Delta f/f$ x 10^{-6} x 86400 (seconds)
   With error of 11.574 ppm, the error of the clock is about one second per day.

(2) Example of Frequency-Voltage Characteristics



(3) Example of Current Consumption-Voltage Characteristics



Note: This data shows values obtained from a sample lot. For rated values, please see the specifications on page 3.

■ Notes on Use

(1) Notes on handling

In order to attain low power consumption, this module incorporates a CMOS IC. Therefore, the following points should be kept in mind when using this module.

1. Static electricity

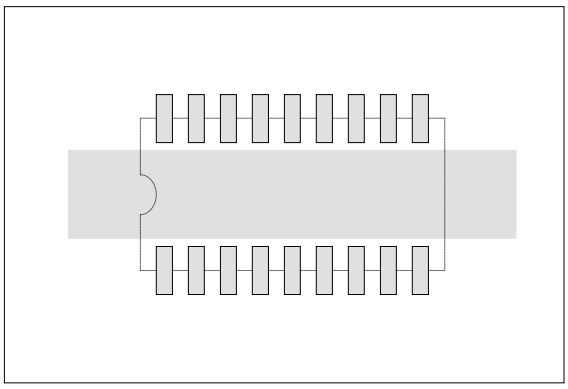
While this module does have built-in circuitry designed to protect it against damage from electrostatic discharge, the module could still be damaged by an extremely large electrostatic discharge. Therefore, packing materials and shipping containers should be made of conductive materials.

Furthermore, soldering equipment, test circuits, etc., that do not have high-voltage leakage, and ground such equipment when working with it.

2. Electronic noise

If excessive external noise is applied to the power supply and I/O pins, the module may operate incorrectly or may even be damaged as a result of the latch-up phenomenon.

In order to assure stable operation, connect a passthrough capacitor (ceramic is recommended) of at least 0.1 μF located as closely as possible to the power supply pins on this module (between V_{DD} and GND). Furthermore, do not place a device that generates high noise levels near this module.



3. Electric potential of I/O pins

Because having the electric potential of the input pins at an intermediate level contributes to increased power consumption, reduced noise margin, and degradation of the device, keep the electric potential as close as possible to the electric potential of V_{DD} or GND.

4. Treatment of unused input pins

Because the input impedance of the input pins is extremely high and using the module with these pins open can result in undefined electric potential and misoperation due to noise, unused input pins must always be connected to a pull-up or pull-down resistor.

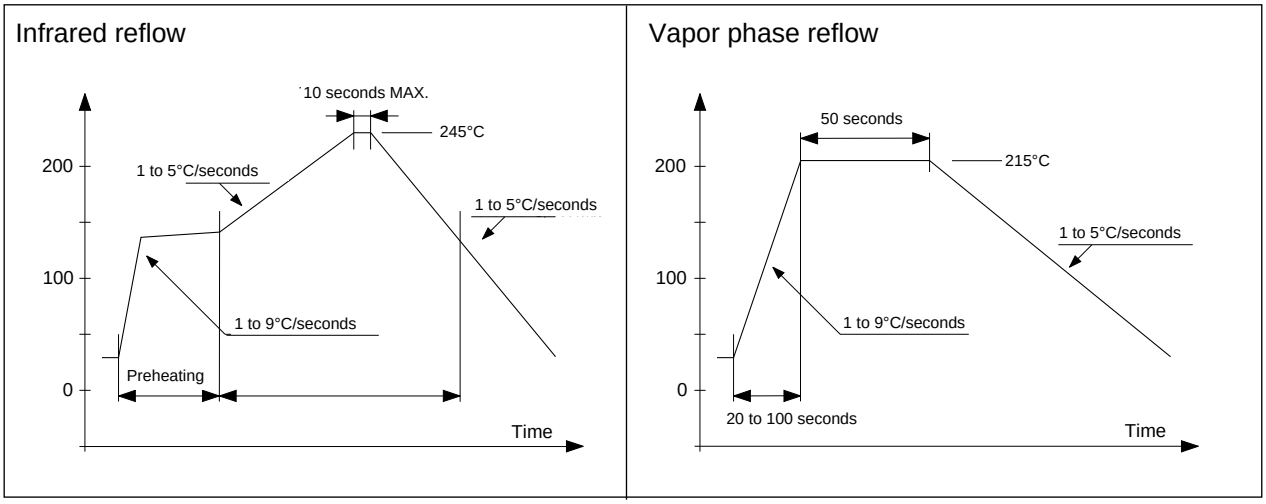
(2) Notes on mounting

1. Soldering temperature conditions

If the internal temperature of the package exceeds 260°C, the characteristics of the crystal resonator may deteriorate and the package may be damaged. Therefore, before using this module, be sure to confirm what temperatures it will be exposed to during the mounting process. If the mounting temperature conditions are ever changed, the suitability of those temperature conditions for this package must be confirmed again.

Soldering conditions: Up to 260°C for up to 10 seconds, twice, or up to 230°C for up to 3 minutes.

Example of SMD product Soldering Conditions



2. Mounters

While this module can be used with general-purpose mounters, be sure to confirm the force of impact that the module will be subjected to during mounting, since certain machines or conditions can result in damage to the internal crystal resonator. If the mounting conditions are ever changed, the suitability of those conditions for this package must be confirmed again.

3. Ultrasonic cleaning

nder certain conditions, ultrasonic cleaning can damage the crystal resonator. Because we cannot specify the conditions under which you perform ultrasonic cleaning (including the type of cleaner, the power level, the duration, the condition of the inside of the chamber, etc.), SEIKO-EPSON does not warrant this product against ultrasonic cleaning.

4. Mounting orientation

If this module is mounted backwards, it may be damaged. Always confirm the orientation of the module before mounting it.

5. Leakage between pins

f power is supplied to this module while it is dirty or while condensation is present, leakage between pins may result. Be sure that the module is clean and dry before supplying power to it.

EPSON

Application Manual

RTC-4543

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