M263-60

EPSON

Application Manual

Real Time Clock Module

RTC-4563

SEIKO EPSON CORPORATION

CONTENTS

Serial RTC Module with alarm and timer functions

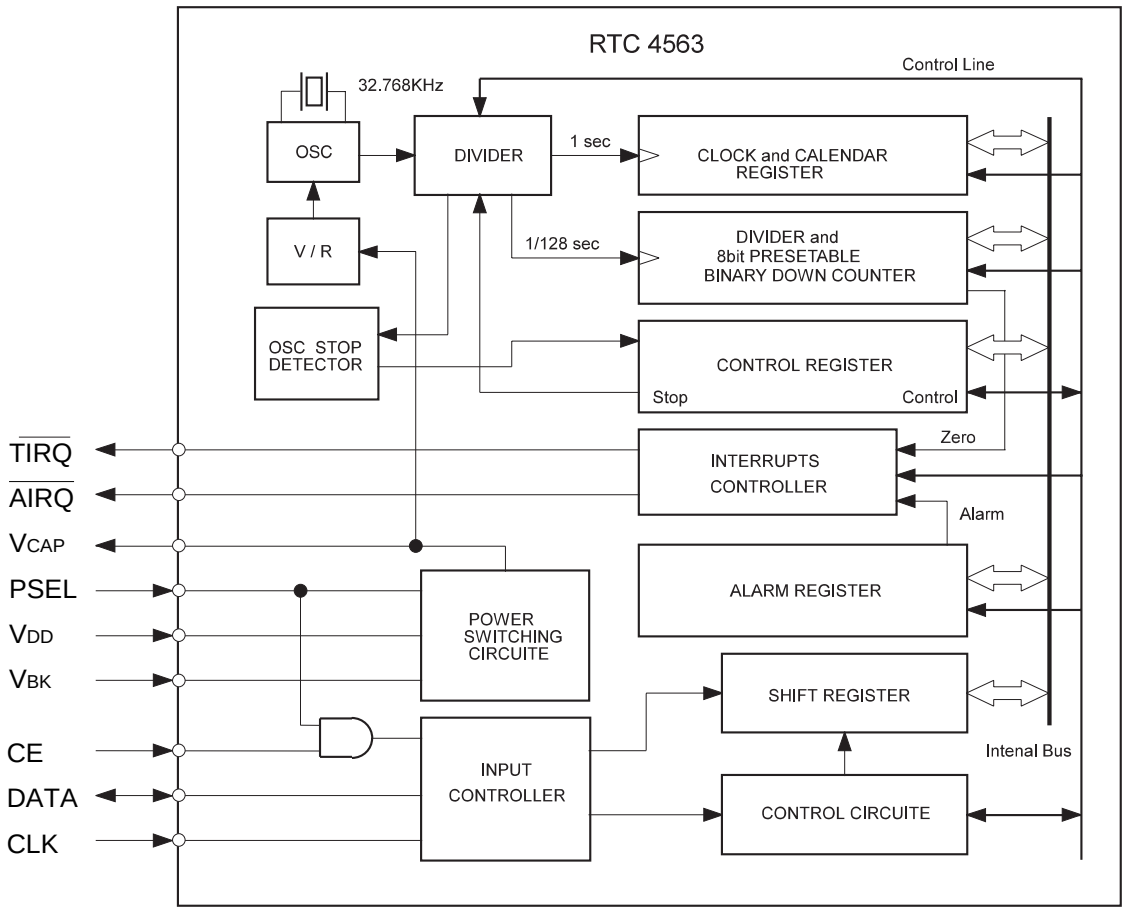
RTC-4563

- Built-in frequency adjusted 32.768KHz crystal oscillator
- Serial interface that can be controlled through three signal lines
- Day, hour, and minute alarm interrupt functions
- Interval timer interrupt function that can be set with an interval ranging from 1/128th of a second to 255 hours
- Dual dedicated interrupt outputs for software maskable alarms and for timers
- Power supply switching function
- Functions that detect termination of serial communications due to an error, halting of crystal oscillation, and when the time is being updated
- Automatic leap year compensation function (western and Japanese calendars)
- Daylight savings time switchover support function
- Wide interface voltage range, from 2.5 to 5.5V
- Wide timing voltage range, from 2.0 to 5.5V
- Low current consumption : 0.9µ A/3V (typ.)
- Small SOP package suited for high-density mounting

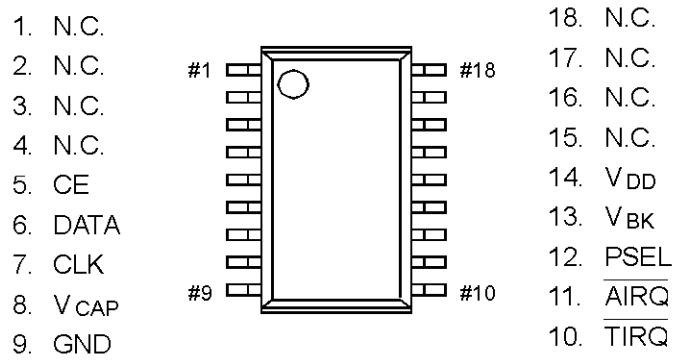
■ Overview

This module is a serial interface-type real-time clock with a crystal oscillator on chip. This module includes clock and calendar circuitry (from seconds to years) with automatic leap year compensation, power supply switching circuitry, alarms, and timer interrupt functions, as well as functions that detect when oscillation is halted, the time is being updated, or when communications terminated due to an abnormality. The serial interface permits control through three signal lines, keeping the number of ports required on the system side to a minimum. Because the small SOP package can be used in high-density mounting, this module is ideal for portable telephones, hand-held terminals, and other compact electronic equipment.

■ Block diagram



■ Terminal connection



■ Terminal function

Signal name	Pin No.	I/O	Function
CE	5	Input	Chip enable input pin. When high, access to the internal registers is enabled. While low, the DATA pin goes to high impedance. When the CE pin is set low, the fr, TEST, and RESET bits are forcibly cleared to "0". Set this pin low when turning the power on, when the device is not to be accessed, and when using the backup power supply.
DATA	6	Bi-directional	This I/O pin is used to for setting write mode/read mode, for writing an address, and for reading and writing data. This pin functions either as an input pin or an output pin, according to the write mode/read mode setting made in the first 8 bits of input data following the rising edge of the CE input.
CLK	7	Input	Shift clock input pin. In write mode, the data is read from the DATA pin at the rising edge of the CLK signal; in read mode, the data is output from the DATA pin at the rising edge of the CLK signal.
V_{CAP}	8	-	Capacitor connection pin for the internal power supply. Connect a 0.1µF capacitor between V_{CAP} and GND.
GND	9	-	Connect to the negative (ground) line of the power supply.
$\overline{TIRQ}$	10	Output	Open drain interrupt output pin for the interval timer.
$\overline{AIRQ}$	11	Output	Open drain interrupt output pin for alarms.
P_{SEL}	12	Input	Power supply selection input pin. When high, the V_{DD} power supply is used as the internal power supply; when low, the V_{BK} power supply is used as the internal power supply. Access is prohibited when this signal is low. If PSEL is set low while the device is being accessed, the access data is not guaranteed.
V_{BK}	13	Input	Input pin for the backup power supply. When using the backup power supply, internal timekeeping operations are possible between 2.0 and 5.5V.
V_{DD}	14	Input	Connect to the positive line of the power supply. Access is possible between 2.5 and 5.5V.
N.C	1, 2, 3, 4, 15, 16, 17, 18		Although these pins are not connected internally, they should always be left open in order to obtain the most stable oscillation possible.

* Always connect a passthrough capacitor of at least 0.1mF as close as possible between VDD and GND.
* Because this is a CMOS IC, having the electric potential of the input pins at an intermediate level contributes to increased power consumption, and degradation of the device. Keep the electric potential of the input pins as close as possible to the electric potential of V_{DD} or GND.

■ Characteristics

1. Absolute maximum ratings

Item	Symbol	Conditions	Rated values	Unit
Supply voltage (1)	V_{DD}	-	-0.3 to +7.0	V
Supply voltage (2)	VBAT		-0.3 to +7.0	
Input voltage	VIN1	CE,CLK,PSEL	-0.3 to +7.0	
	VIN2	DATA	GND-0.3 to V_{DD} + 0.3	
Output voltage	VOUT1	$\overline{TIRQ}$, $\overline{AIRQ}$	-0.3 to +7.0	
	VOUT2	DATA	GND-0.3 to V_{DD}+0.3	
Storage temperature	TSTG	-	-55 to +125	˚C

2. Operating conditions

Item	Symbol	Conditions	Range	Unit
Supply voltage	V_{DD}	-	2.5 to 5.5	V
Timekeeping supply voltage	VCLK		2.0 to 5.5	
Operating temperature	TOPR		-40 to +85	˚C

3. Oscillation characteristics

Item	Symbol	Conditions	Specifications	Unit
Frequency tolerance	Δf/fo	Ta=25˚C, V_{DD}=3V	5±23	ppm
Oscillation start time	t_{STA}	Ta=25˚C, V_{DD}=2.5V After initial setting of registers	5 (max.)	s
Frequency temperature characteristics		-10 to 70˚C 25°C reference	+10/-120	ppm
Frequency voltage characteristics		Ta=25˚C, V_{DD}=2.0 to 5.5V	±2.0	ppm/V

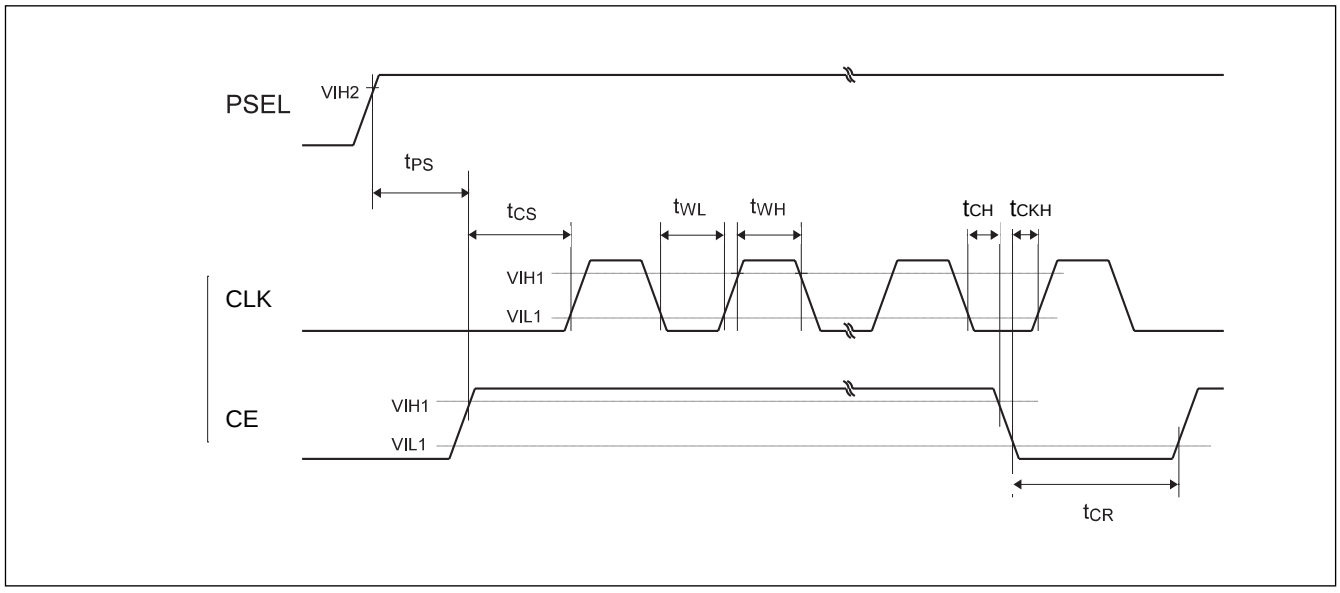
4. DC characteristics

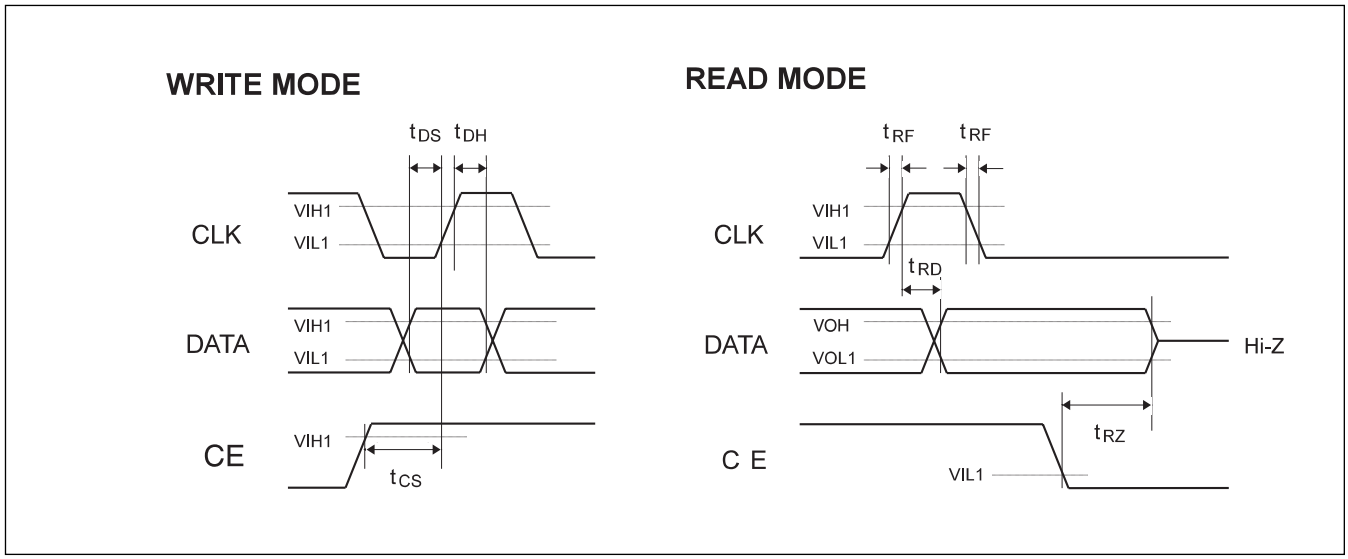
(V_{DD}=2.5 to 5.5V, Ta=-40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	V_{IH1}	-	0.8V_{DD}	-	V_{DD}	V	except for Input pins, PSEL
	V_{IL1}		0		0.2V_{DD}		
Input voltage (2)	V_{IH2}		0.7V_{CAP}		V_{CAP}		PSEL
	V_{IL2}		0		0.3V_{CAP}		
Input leak current (1)	I_{LK1}	VI=V_{DD}/GND	-		1/-1	µA	CE,CLK
Input leak current (2)	I_{LK2}	VI=V_{DD}/GND					DATA
Low output voltage (1)	V_{OL1}	IO=1mA			0.2V_{DD}	V	
High output voltage	V_{OH}	IO=-400mA	0.8V_{DD}		-		
Low output voltage (2)	V_{OL2}	IO=1mA	-		0.2V_{DD}		$\overline{AIRQ}$,$\overline{TIRQ}$
Off leak current	I_{OFLK}	VO=V_{DD}			10	µA	
Current consumption (1)	I_{DD1}	V_{DD}=5V VI:CE=GND, PSEL=V_{DD} DATA, CLK=GND		1.2	1.8		V_{DD}
Current consumption (2)	I_{DD2}	V_{DD}=3V VI:CE=GND,PSEL=V_{DD} DATA, CLK=GND		0.9	1.5		
Current consumption (3)	I_{BK1}	V_{BK}=2V VI:CE=GND,PSEL=GND DATA, CLK=GND		0.8	1.3		V_{BK}

5. AC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK high pulse width	t_{WH}	-	300	-	-	ns
CLK low pulse width	t_{WL}		300			
CE setup time	t_{CS}		150			
CE hold time	t_{CH}		200			
CE recovery time	t_{CR}		300			
CLK hold time	t_{CKH}		20			
Write data setup time	t_{DS}		50			
Write data hold time	t_{DH}		50			
Read data delay time	t_{RD}	CL=50pF	0		250	
Output disable delay time	t_{RZ}	-	-		100	
Input rise/fall time	t_{RF}				20	
PSEL setup time	t_{PS}		12		-	µs





■ Registers

1. Register table

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Read	Write
0	Seconds	f0	40								Yes
1	Minutes	fr	40	20	10	8	4	2	1		
2	Hours	fr	*								
3	Day of the week	fr	6	5	4	3	2	1	0		Bit 7 only: No
4	Day	fr	*	20							
5	Month	fr	*	*							
6	Year	80	40	20	10	8	4	2	1		
7	Minute alarm	AE	40	20							
8	Hour alarm	AE	*	20						Yes	
9	Day of the week alarm	AE	6	5	4	3	2	1	0		
A	Timer count data	128	64	32	16						Yes
B	Timer preset data	128	64	32	16						
C	Daylight savings time day	DAF	*	20	10	8	4	2	1		
D	Daylight savings time month	MAF	*	*	10						
E	Control 1	TV1	TV0	AI/AP	TI/TP	AF	TF	AIE	TIE		
F	Control 2	WF	TEST	STOP	RESET	HOLD	+1	-1	TCSTOP		Bit 7 only: No

1.1 Timekeeping/calendar registers (register 0 to register 6)

- The data in these registers is BCD format. For example, "0101 1001" represents 59 seconds. In addition, the "*" mark in the register table means that the register is readable and writable, and can be used as RAM. Time is kept in the 24-hour format.
- Writing to a bit marked with an asterisk ("*") is permitted; such bits can be used as RAM. When the alarm and timer functions are not used, registers 7 to B can be used as 8-bit memory registers, and registers C and D can be used as 7-bit memory registers. Because register A is a down counter, when using it as RAM, it is necessary to set TCSTOP to "1".
- Year register and leap years

  A leap year is detected by dividing the two BCD digits of the year register by four; if the remainder is zero, the year is a leap year. Therefore, leap years can be automatically determined whether the year is numbered according to the western calendar or the Japanese calendar (year of Heisei).

- Day of the week

  The day of the week register uses 7 bits, from 0 to 6; the meanings of the bits are shown in the table below. Do not set more than one bit to "1" at any one time.

bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

- **fo (OSC flag)**

  This flag indicates that oscillation stopped, and is used to monitor drops in the battery output. "1" indicates that oscillation stopped, and writing a "0" to this bit clears it. However, a "0" cannot be written to this bit while oscillation is still stopped. Although it is possible to write a "1" to this bit, doing so is not recommended.
  This bit is not affected even if other bits (HOLD, STOP, RESET) are "1".

- **fr (READ flag)**

  This flag is set to "0" when the CE input is low, and is set to "1" when a carry into the ones digits of the seconds counter is generated while the CE input is high. This makes it possible to determine if a carry into the seconds counter occurred while the timekeeping registers were being read (while the CE input is high). If fr is "1", it is necessary to read all of the timekeeping registers again.

1.2 Alarm registers (register 7 to register 9)

Alarms can be set for days of the week, hours, and minutes. Bit 7 of each alarm register is an AE bit that can be used to set an hourly alarm or a daily alarm. An alarm can also be set for multiple days of the week. However, when using the day of the week alarm, also set either or both the hour and minute alarms. If the day of the week alarm is set by itself, the alarm may not be output properly.
When the AE bit is "0", the register in question and the timekeeping register is compared; when the AE bit is "1", this indicates "don't care", and the registers are assumed to match, regardless of the data.

1.3 Timer registers (register A and register B)

This is an 8-bit presettable down counter. The timer count register counts down at the specified interval; once the value in the register reaches zero, the data in the preset data register is reloaded into the timer count register which then begins counting down again. These registers can be used as an interval timer with an interval ranging from a minimum of 1/128th of a second to a maximum of 255 hours.

1.4 Daylight savings time month and day registers (register C and register D)

These alarm registers are completely independent of the hour, minute, and day of the week alarms. If the data in the daylight savings time day register matches the day data in the timekeeping registers, the DAF bit is set to "1"; if the data in the daylight saving time month register also matches the month data, the MAF bit is set to "1".

The DAF bit and the MAF bit are set to "1" approximately 31 μs after the registers match. Neither bit can be output to the IRQ pin.

Although these registers can be used as normal month and day alarms, these registers make it an easy matter to set the date on which daylight savings time goes into effect and make the change to daylight savings time when these registers used in conjunction with the +1, -1 bit.

The DAF bit and the MAF bit retain their value until a "0" is written to them. Note, however, that a "0" cannot be written to either of these bits for about 61 [micro]s after they have changed from "0" to "1".

Do not write a "1" to either the DAF bit or the MAF bit.

1.5 Control register 1 (register E)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	TV1	TV0	AI/AP	TI/TP	AF	TF	AIE	TIE

- **TV bit: (Timer countdown interval)**

This bit sets the timer countdown interval.

TV1,TV0	1 , 1	1 , 0	0 , 1	0 , 0
Interval	1 hour	1 min.	1 sec	1/128 sec

TV1,TV0 / Counter setting	1 , 1 (hour)	1 , 0 (min.)	0 , 1 (sec)	0 , 0 (sec)
0	1/128 sec	1/128 sec	1/128 sec	1/128 sec
1	1 hour	1 min.	1 sec	1/128 sec
2	2 hour	2 min.	2 sec	2/128 sec
3	3 hour	3 min.	3 sec	3/128 sec
. . .	. . .	. . .	. . .	. . .
255	255 hour	255 min.	255 sec	255/128 sec

• **AI/AP, TI/TP bits: (Interrupt signal output mode select interrupt/periodic)**

These bits set the alarm signal output mode.

bit	0	1
AI/AP	The alarm interrupt signal is in interrupt mode; when an alarm interrupt is generated, the AIRQ pin is kept low (however, AIE = 1) until a "0" is written to the AF bit.	The alarm interrupt signal is in repeat mode; when an alarm interrupt is generated, the /AIRQ pin immediately goes low (however, AIE = 1) and the AF bit is set to "1". After approximately 3.9ms, the /AIRQ pin goes to high impedance and the AF bit is maintained at "1" until a "0" is written to it.
TI/TP	The timer interrupt signal is in interrupt mode; when a timer interrupt is generated, the TIRQ pin is kept low (however, TIE = 1) until a "0" is written to the TF bit.	The timer interrupt signal is in repeat mode; when a timer interrupt is generated, the /TIRQ pin immediately goes low (however, TIE = 1) and the TF bit is set to "1". After approximately 3.9ms, the /TIRQ pin goes to high impedance and the TF bit is maintained at "1" until a "0" is written to it.*

* If decrementing by TCSTOP is stopped within approximately 3.9 ms after a timer interrupt is generated, the TIRQ pin is kept low (however, TIE = 1) even in repeat mode. In this case, if decrementing by TCSTOP is resumed, the $\overline{\text{TIRQ}}$ pin will go to high impedance within 3.9 ms.

• **AF, TF bits: (Alarm flag, timer flag)**

The AF bit goes to "1" when an alarm is generated, and the TF bit goes to "1" when the timer reaches zero. The data in both bits is retained until a "0" is written to them. It is not possible to write a "1" to either bit.

• **AIE, TIE bits: (Alarm, timer interrupt enable)**

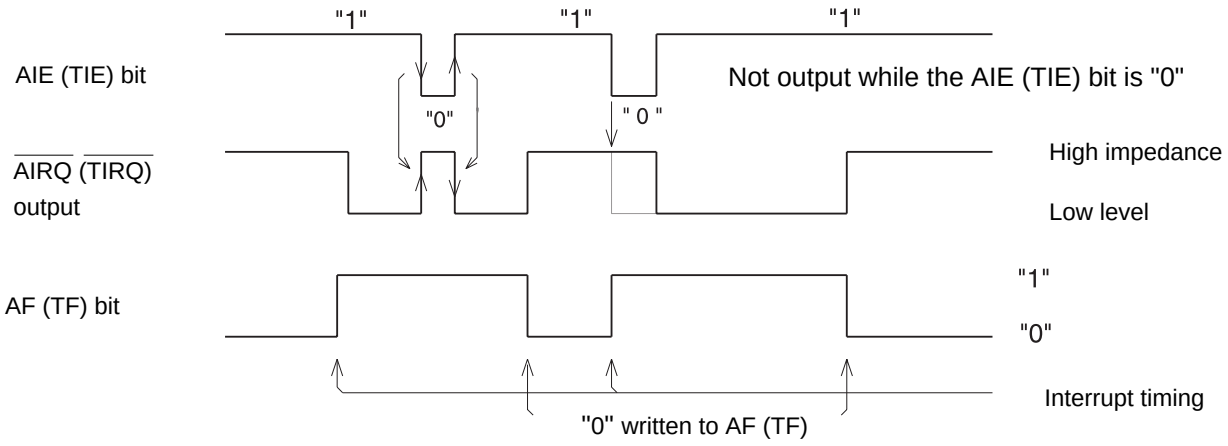
These bits determine whether or not the IRQ pin is driven when an alarm or timer interrupt event occurs. AIE corresponds to the alarm, TIE corresponds to the timer. When the AIE bit is "0", the $\overline{\text{AIRQ}}$ pin goes to high impedance; when the TIE bit is "0", the $\overline{\text{TIRQ}}$ pin goes to high impedance.

1.5.1 AI/AP, TI/TP, AF, TF Bit Operations and $\overline{\text{AIRQ}}$, $\overline{\text{TIRQ}}$ Output

The relationships between the operation of the various alarm- and timer-related bits and IRQ output is described below.

(1) When in interrupt mode (AI/AP or TI/TP = 0)

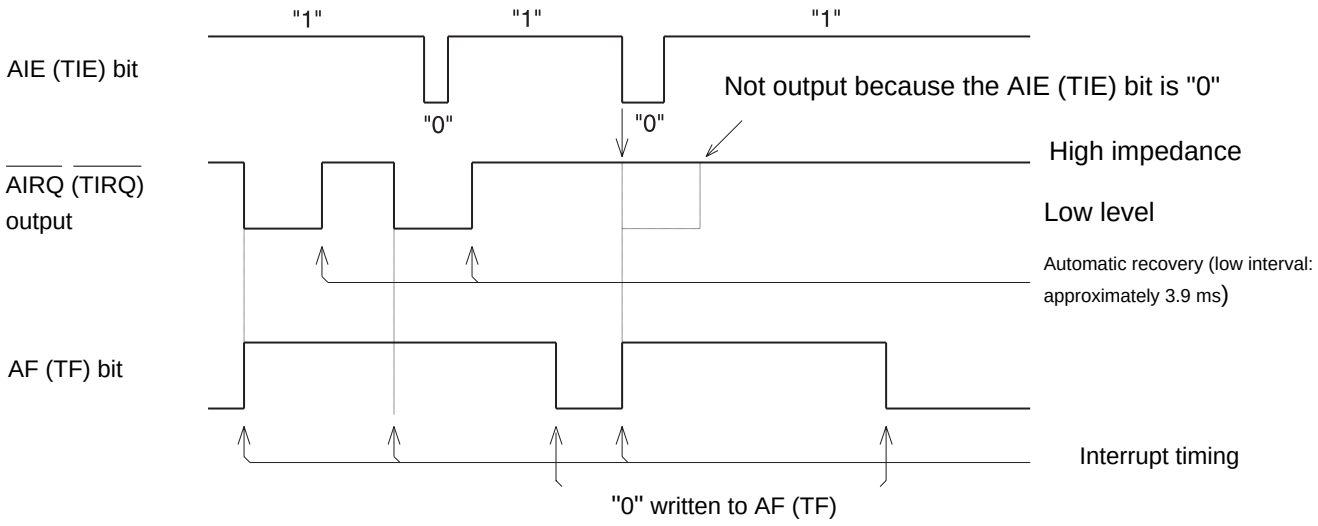
When AIE (TIE) = 1, the status of the AF (TF) interrupt flag is reflected in the IRQ pin; when AIE (TIE) = 0, the IRQ pin goes to high impedance.



(2) When in repeat mode (AI/AP or TI/TP = 1)

1) If AIE (TIE) = 1 when an interrupt is generated, the IRQ pin goes to low output; after approximately 3.9ms, the IRQ pin goes to high impedance, and the AF (TF) bit is maintained at its current level.

2) If AIE (TIE) = 0 when an interrupt is generated, the IRQ pin remains at high impedance; only the AF (TF) bit goes to "1", and then retains that value.



During automatic recovery, if the AF (TF) bit is cleared the AF (TF) bit goes to "0" immediately; the $\overline{\text{AIRQ}}$ ($\overline{\text{TIRQ}}$) output goes low for 3.9 ms, and then subsequently goes to high impedance.

1.6 Control register 2 (register F)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	WF	TEST	STOP	RESET	HOLD	+1	-1	TCSTOP

- **WF bit: (Write fail flag)**

  This bit is set to "1" when a write was not performed as an 8-bit unit; for example, if CE was set high and then set low after only seven CLK pulses. This bit is a read-only bit; it cannot be written. This bit is cleared by performing an ordinary write operation.

  This bit is unaffected, even if other bits (HOLD, STOP, RESET) are "1".

- **TEST bit:** This is a test bit for Seiko-Epson's use.

  Always set this bit to "0". When writing to the other bits in the CF register, be careful not to accidentally write a "1" to this bit. This bit is cleared by setting CE low.

- **STOP bit**

  If this bit is set to "1", timekeeping stops (after 4KHz). If this bit is set back to "0", timekeeping resumes.

- **RESET bit**

  Setting this bit to "1" resets the counter below the seconds counter, stopping timekeeping. If a "1" is written to this bit, it is cleared either by writing a "0" to this bit again with the auto increment function, or by setting CE low.

  The only effect on timekeeping precision is a maximum error 61 μs. This bit is unaffected by the status of other bits.

- **HOLD bit**: This bit stops carries to the ones digit of the seconds counter. Timekeeping continues below the seconds counter, and if there was a carry to the seconds counter while HOLD = 1, compensation (by means of adding one second) is made immediately (within 0 to 122 μs) after HOLD is released.
  This bit is cleared by writing a "0" to it.

- **+1 bit:** This bit advances the time ahead by one hour. If this bit is changed from "0" to "1", the hours register (register 2) is immediately incremented, and the day of the week, day, month, and year data are also updated if necessary. Set this bit to "1" in order to switch to daylight savings time.
  It takes approximately 160 [micro]s for the hours register to be incremented once this bit is set. Because the internal operation of alarm interrupts is not assured during this time interval, set the AIE bit to "0", disabling alarms. In addition, if the time data is read during this interval, the time that is read will not yet have been advanced one hour; avoid reading the data during this interval.
  This bit is cleared by writing a "0" to it. The minutes and seconds data is unaffected by this bit. During initialization after the power has first been turned on, clear this bit to "0".

- **-1 bit**: This bit sets the time back one hour.
  If this bit is changed from "0" to "1", updating of the time in the hours register (register 2) is skipped once, at which point this bit is simultaneously and automatically cleared to "0". To cancel this operation, write a "0" to this bit.
  The minutes and seconds data is unaffected by this bit.

- **TCSTOP bit** (Timer count stop) This bit controls the counting down of the countdown timer.
  When this bit is "1", the timer does not count down. When this bit is "0", the timer data is counted down at the set interval. There is a maximum delay of up to 3.9ms from the time when this bit is set to "0" until the timer starts counting down.

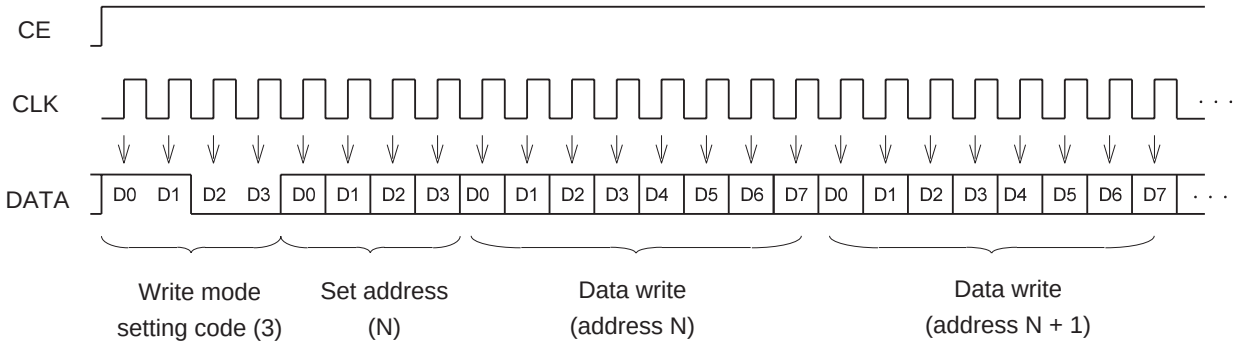
■ Usage

● Functional Overview

The basic sequence for reads and writes is the same: after the CE input goes high, the 4-bit mode is set, the 4-bit address is specified, and then the data is read or written in 8-bit units.
If the input of an 8-bit unit of data is not yet complete when the CE input is set low, the 8-bit data that was being written when the CE input went low is ignored. (Prior data is valid. Also, in these circumstances, the WF bit is set to "1", indicating that the write operation was not completed normally.)
Writes and reads are both LSB first.

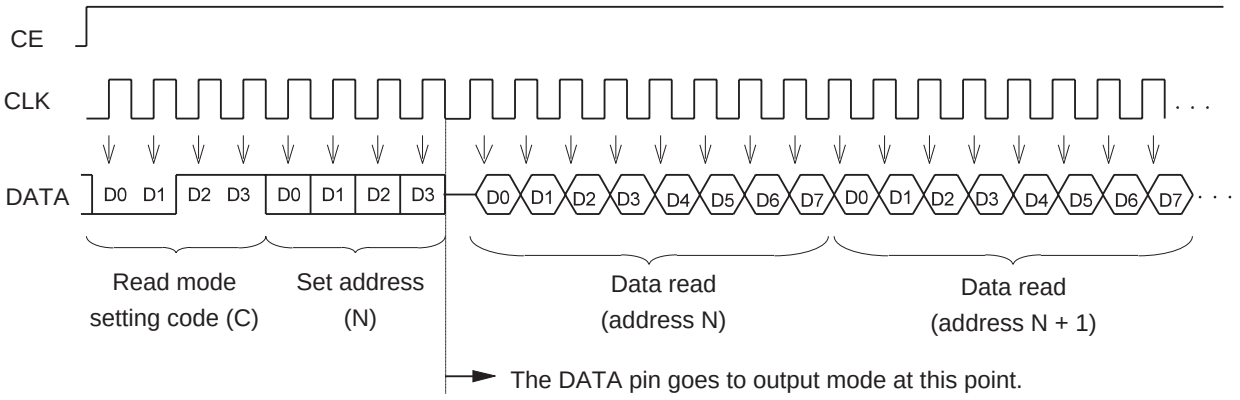
[Writes]

1) After the CE input goes high, set the value of the first four write bits is to "3", indicating write mode, and then set the address to be written in the next four bits.
2) The 8 bits of write data that follow are written to the address that was set; the address is then automatically incremented, and the next 8 bits of data are written to the new address.
3) The automatic address incrementation is cyclic, with address 0 following address F.



[Reads]

1) After the CE input goes high, set the value of the first four write bits to "C", indicating read mode, and then set the address to be written in the next four bits.
2) The 8 bits of data that follow are read from the address that was set; the address is then automatically incremented, and the next 8 bits of data are read from the new address.
3) The automatic address incrementation is cyclic, with address 0 following address F.



If the mode setting code was set to a value other than "C" or "3", the subsequent data is ignored and the DATA pin remains in the input state.

■ Alarm usage

Alarms can be set for days of the week, hours, and minutes. Alarms can be set for more than one day of the week. In order to avoid inadvertent hardware interrupts while setting alarms, it is recommended that the AF bit and AIE bit both be set to "0".
Next, set the alarm data, and then, in order to assure proper initialization of the alarm circuit, clear the AF flag to zero once. Next, set the AIE bit to "1". If hardware interrupts are not to be used at all, set the AIE bit to "0", and monitor the AF bit through software as necessary.

● Examples of usage

1) Outputting an alarm at 55 minutes on the hour, every hour of every day

Write "0" to the AIE bit and a "0" to the AF bit.
Write "1" to the AI/AP bit. (repeat mode)
Write "1" to the AE bit in the days of the week alarm register.
Write "1" to the AE bit in the hours alarm register.
Write "55h" in the minutes alarm register.
Clear the AF bit to "0".
Write "1" to the AIE bit.

2) Outputting an alarm at 6:00 p.m. tomorrow

Write "0" to the AIE bit and a "0" to the AF bit.
Write "0" to the AI/AP bit.
Fetch the current day of the week from register 3, shift the data one bit to the left and write the result in the days of the week alarm register. (Be careful concerning the "fr" bit, and if bit 6 is "1" (Saturday), write "01h" (Sunday).)
Write "18h" in the hours alarm register.
Write "00h" in the minutes alarm register.
Clear the AF bit to "0".
Write "1" to the AIE bit.

3) Outputting an alarm at 9:00 a.m. every day

Write "0" to the AIE bit and a "0" to the AF bit.
Write "1" to the AI/AP bit. (repeat mode)
Write "1" to the AE bit in the days of the week alarm register.
Write "9" in the hours alarm register.
Write "00h" in the minutes alarm register.
Clear the AF bit to "0".
Write "1" to the AIE bit.

4) Outputting an alarm at 6:00 a.m. every day except Saturday and Sunday

Write "0" to the AIE bit and a "0" to the AF bit.
Write "1" to the AI/AP bit. (repeat mode)
Write "3Eh" in days of the week alarm register.
Write "6" in the hours alarm register.
Write "00h" in the minutes alarm register.
Clear the AF bit to "0".
Write "1" to the AIE bit.

■ Timer function usage

The timer is an 8-bit presettable down counter. The timer count register counts down at the preset interval; when the data reaches zero, a timer interrupt is generated, the data in the preset data register is reloaded, and the count down operation resumes. This timer can be used as an interval timer with a minimum interval of 1/128th of a second and a maximum interval of 255 hours. The internal divider circuit is reset when data is written to the preset data register, register B. The internal divider circuit reset is not generated by operations involving the TCSTOP bit and the timer count register. In order to avoid inadvertent hardware interrupts while setting the timer, it is recommended that the TCSTOP bit be set to "1" first to stop the count down operation, and then the TF bit and TIE bit both be set to "0". After the timer has been set, set the TIE bit to "1" and then clear the TCSTOP bit to "0". If hardware interrupts are not to be used at all, set the TIE bit to "0", and monitor the TF bit through software as necessary.

<Note>
When initially setting the timer, first set the TIE bit to "0" to disable timer interrupts, and then set the TCSTOP bit to "1" to stop the timer. Next, write the preset data to register B, and set the timer data in register A. Then set the TIE bit and clear the TCSTOP bit to "0" according to the required timing in order to start the count down operation.
If the count data is written in register A, then the preset data is written in register B, and then the internal divider circuit is reset, the count data in register A may be decremented.

● Examples of usage

1) Using the timer as a 128Hz reference oscillation source

Set the TCSTOP bit in control register 2 to "1" to stop the timer.
Set the TIE bit in control register 1 to "0" to disable timer interrupts.
Set the TV1 and TV0 bits in control register 1 both to "0", and set the TI/TP bit to "1".
Write "1" to the timer preset data register.
Write "1" to the timer count data register.
Clear the TF bit on control register 1 to "0".
Set the TIE bit in control register 1 to "1" to enable timer interrupts.
Clear the TCSTOP bit in control register 2 to "0".
A 128Hz signal is output from the /TIRQ pin. However, the initial duty is unstable because there is a delay of up to 3.9ms after timer start before the signal is output.

2) Using the timer as a 1.5-second interval timer

Set the TCSTOP bit in control register 2 to "1" to stop the timer.
Set the TIE bit in control register 1 to "0" to disable timer interrupts.
Set the TV1 and TV0 bits in control register 1 both to "0", and set the TI/TP bit to "1".
Write "C0h" (192 in decimal) to the timer preset data register. (1/128 = 7.8125ms x 192 = 1.5 seconds)
Write the same value, "C0h" (192 in decimal), to the timer count data register.
Clear the TF bit on control register 1 to "0".
Set the TIE bit in control register 1 to "1" to enable timer interrupts.
Clear the TCSTOP bit in control register 2 to "0".
A signal with a low pulse of 3.9ms is output from the /TIRQ pin every 1.5 seconds. However, there is a delay of up to 3.9ms after timer start before the signal is output.

■ Daylight savings time function

If the daylight savings time function is not used, set both the +1 and -1 bits to "0". Be careful of bit operations involving the +1 bit in particular, because changing the +1 bit from "0" to "1" immediately advances the time by one hour.

● Example of usage

1. Set the date of the transition to daylight savings time in the daylight savings time month and day registers.
2. Confirm that the MAF bit is not set.
3. Monitor the MSB (the MAF bit) of the daylight savings time month register.
4. When the month of the transition arrives, clear the DAF bit in register D. (This is because there is a possibility that the DAF could be set on the matching day of a month prior to the month of the transition.)
5. Confirm that the DAF bit was cleared.
6. Monitor the MSB (the DAF bit) of register D.
7. Once the day of the transition arrives, set the +1 bit at any time.
8. <<Transition made to daylight savings time>>
9. Set the date of the transition back to standard time in the daylight savings time month and day registers.
10. Confirm that the MAF bit is not set.
11. Monitor the MSB (the MAF bit) of the daylight savings time month register.
12. When the month of the transition back to standard time arrives (MAF = 1), clear the DAF bit in register D.
13. Confirm that the DAF bit was cleared.
14. Monitor the MSB (the DAF bit) of register D.
15. Once the day of the transition arrives, set the -1 bit and clear the +1 bit to "0" at any time.
16. The time reverts to standard time within one hour, and the -1 bit is automatically cleared to "0".
17. Return to step 1.

The above operations make it possible to switch to daylight savings time; the current status can be determined as follows:

- **When the +1 and -1 bits are "1" and "0", respectively, daylight savings time is in effect.**
- **When the +1 and -1 bits are "0" and "1", respectively, the transition to standard time will occur within one hour.**
- **When the +1 and -1 bits are "0" and "0", respectively, standard time is in effect.**

When the current month and day registers are compared to the daylight savings time month and day registers and are found to match, the MAF and DAF bits are immediately set to "1", but once the registers no longer match, the previously set flags are not reset automatically. Therefore, if the MAF and DAF bits are cleared before the date changes, they are immediately set again.
In order to avoid having these bits set again, first confirm that the MAF and DAF bits in registers C and D have both been set, and then write "00h" (a nonexistent date) or other data that differs from the current date to each register (registers C and D). Furthermore, once data has been set in registers C and D, be certain to confirm that MAF and DAF have been cleared.

Although the daylight savings time month and day registers can be used as RAM if they are not used for their intended purpose, mask the MSB when reading or writing these registers in order to avoid inadvertently setting the MSB alarm flag. When the +1 bit operation is in progress, set the AIE bit to "0". Once the +1 hour operation has been completed, the AIE bit can be set as desired.

■ Initialization operation when power is applied

Initialize the device according to the following procedure when power is applied.

(1) After power is applied, wait for the start of oscillation and then write the contents of data map 1, starting at address F and using auto incrementation. (Once the data has been written to address E, set CE low.)

(2) Wait a minimum of 122 μs, and then write the contents of data map 2 in the same manner as in step 1.

(3) Once step 2 is completed (CE is low), all of the internal logic will be initialized after approximately 3.9 ms; once this operation is complete, any desired data can be written to all of the registers.

As soon as the internal logic has been initialized, the AF and TF bits are both set to "1".

Note that until this entire initialization operation is completed, the $\overline{\text{AIRQ}}$ and $\overline{\text{TIRQ}}$ outputs are unstable, so exercise caution when using these outputs.

Data map 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	hex
F	Control 2	0	0	0	**1**	0	0	0	**1**	**11h**
0	Seconds	0	0	0	0	0	0	0	0	00h
1	Minutes	0	0	0	0	0	0	0	0	00h
2	Hours	0	0	0	0	0	0	0	0	00h
3	Day of the week	0	0	0	0	0	0	0	0	00h
4	Day	0	0	0	0	0	0	0	0	00h
5	Month	0	0	0	0	0	0	0	0	00h
6	Year	0	0	0	0	0	0	0	0	00h
7	Minute alarm	0	0	0	0	0	0	0	0	00h
8	Hour alarm	0	0	0	0	0	0	0	0	00h
9	Day of the week alarm	0	0	0	0	0	0	0	0	00h
A	Timer count data	0	0	0	0	0	0	0	0	00h
B	Timer preset data	0	0	0	0	0	0	0	0	00h
C	Daylight savings time day	0	0	0	0	0	0	0	0	00h
D	Daylight savings time month	0	0	0	0	0	0	0	0	00h
E	Control 1	0	0	0	0	0	0	0	0	00h

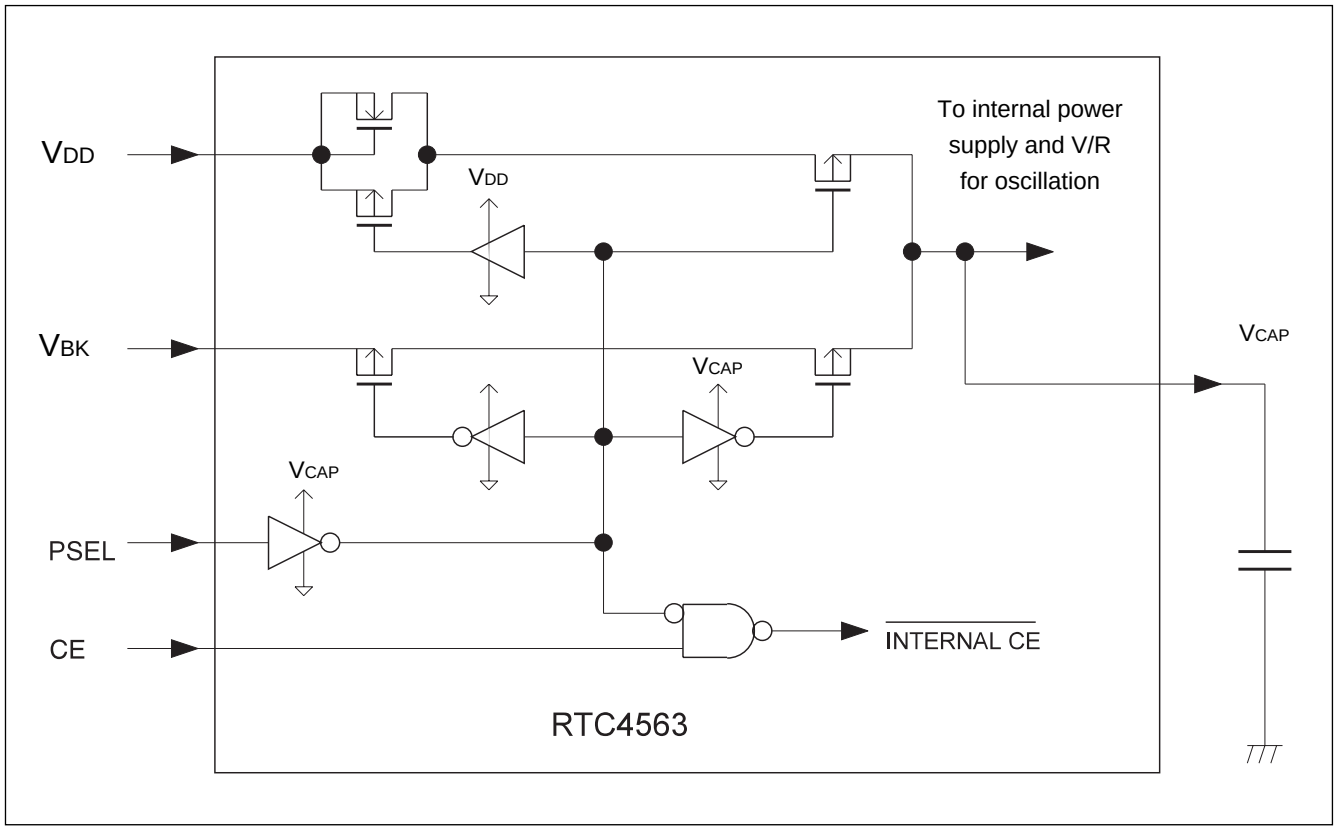
Data map 2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	hex
F	Control 2	0	0	0	**1**	0	0	0	**1**	**11h**
0	Seconds	0	0	0	0	0	0	0	0	00h
1	Minutes	0	0	0	0	0	0	0	0	00h
2	Hours	0	0	0	0	0	0	0	0	00h
3	Day of the week	0	0	0	0	0	0	0	0	00h
4	Day	0	0	0	0	0	0	0	0	00h
5	Month	0	0	0	0	0	0	0	0	00h
6	Year	0	0	0	0	0	0	0	0	00h
7	Minute alarm	0	0	0	0	0	0	0	0	00h
8	Hour alarm	0	0	0	0	0	0	0	0	00h
9	Day of the week alarm	**1**	0	0	0	0	0	0	0	**80h**
A	Timer count data	0	0	0	0	0	0	0	0	00h
B	Timer preset data	0	0	0	0	0	0	0	0	00h
C	Daylight savings time day	0	0	0	0	0	0	0	0	00h
D	Daylight savings time month	0	0	0	0	0	0	0	0	00h
E	Control 1	0	0	0	0	0	0	0	0	00h

■ Power supply switching circuit

The power supply switching circuit selects $V_{CAP} = V_{DD}$ when PSEL = V_{CAP} x 0.7V or more, and selects $V_{CAP} = V_{BK}$ when PSEL = V_{CAP} x 0.3V or less.

When V_{BK} is selected, the clock input and DATA input/output are invalid and access is prohibited.



<Notes>

1) Initial operation

- If $V_{DD} = V_{BK}$ = GND and then only V_{BK} rises, V_{CAP} may be unstable. In this case, once V_{DD} rises, V_{CAP} will stabilize.
- When V_{DD} rises from the $V_{DD} = V_{BK}$ = GND state, the rise should occur at a rate of no more than 20ms/V; if the rise requires more than 20ms/V, the internal voltage regulator might not operate.

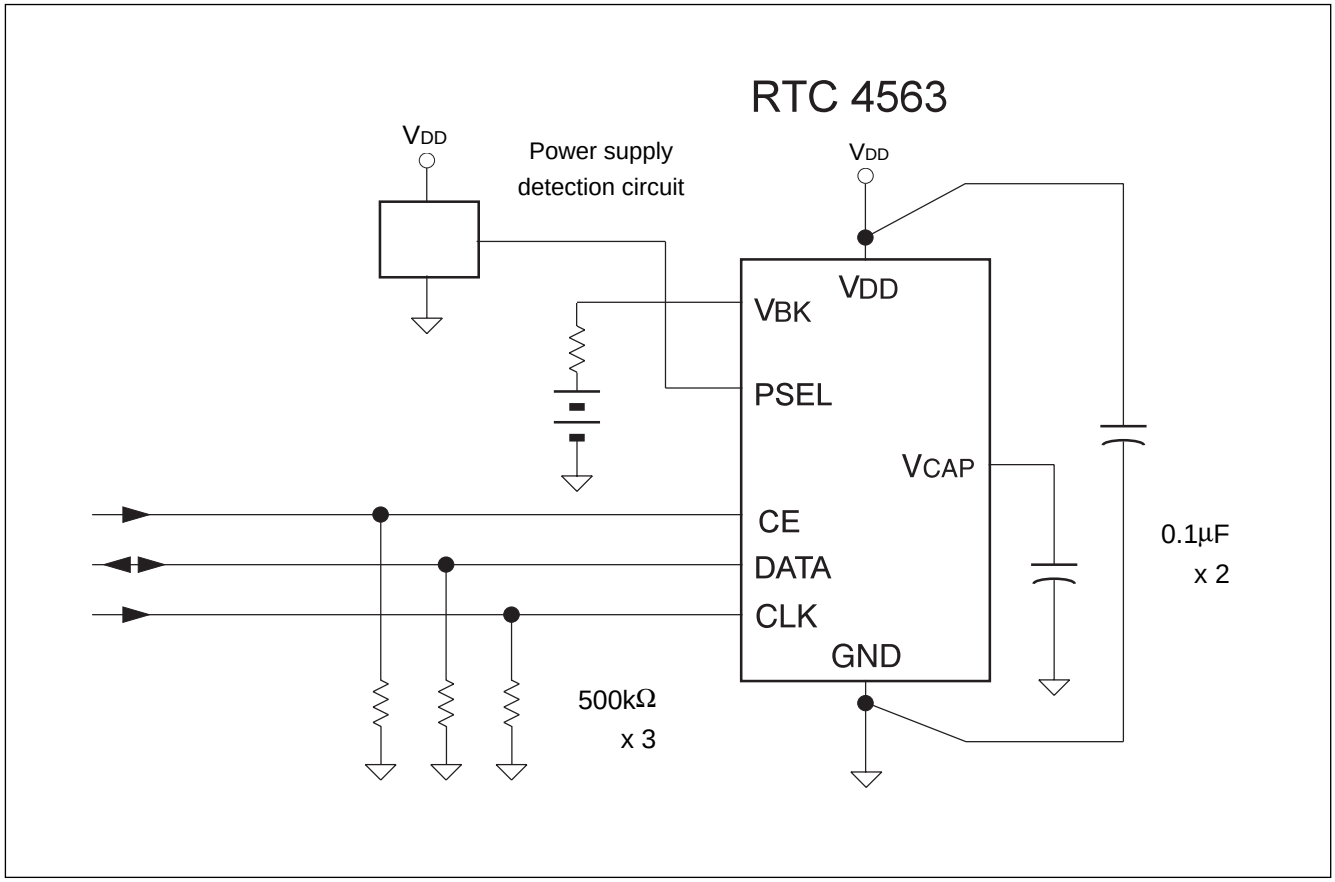
2) Switching operation

- There is a delay of up to 12µs (as a countermeasure against feedback chattering) from the time when PSEL is input until the internal power supply switches.
- When switching from V_{DD} to V_{BK} (PSEL switching), the RTC operating voltage should be 2.5V or more, and for at least 12µs after the switch V_{CAP} should not drop below the minimum timekeeping voltage (2V).
- Note that if V_{CAP} does drop below the minimum timekeeping voltage (2V), oscillation may stop and internal data may be lost.
- If the PSEL rise and fall times are slow, feedback chattering may result. The PSEL rise and fall times should be less than 1 µs.

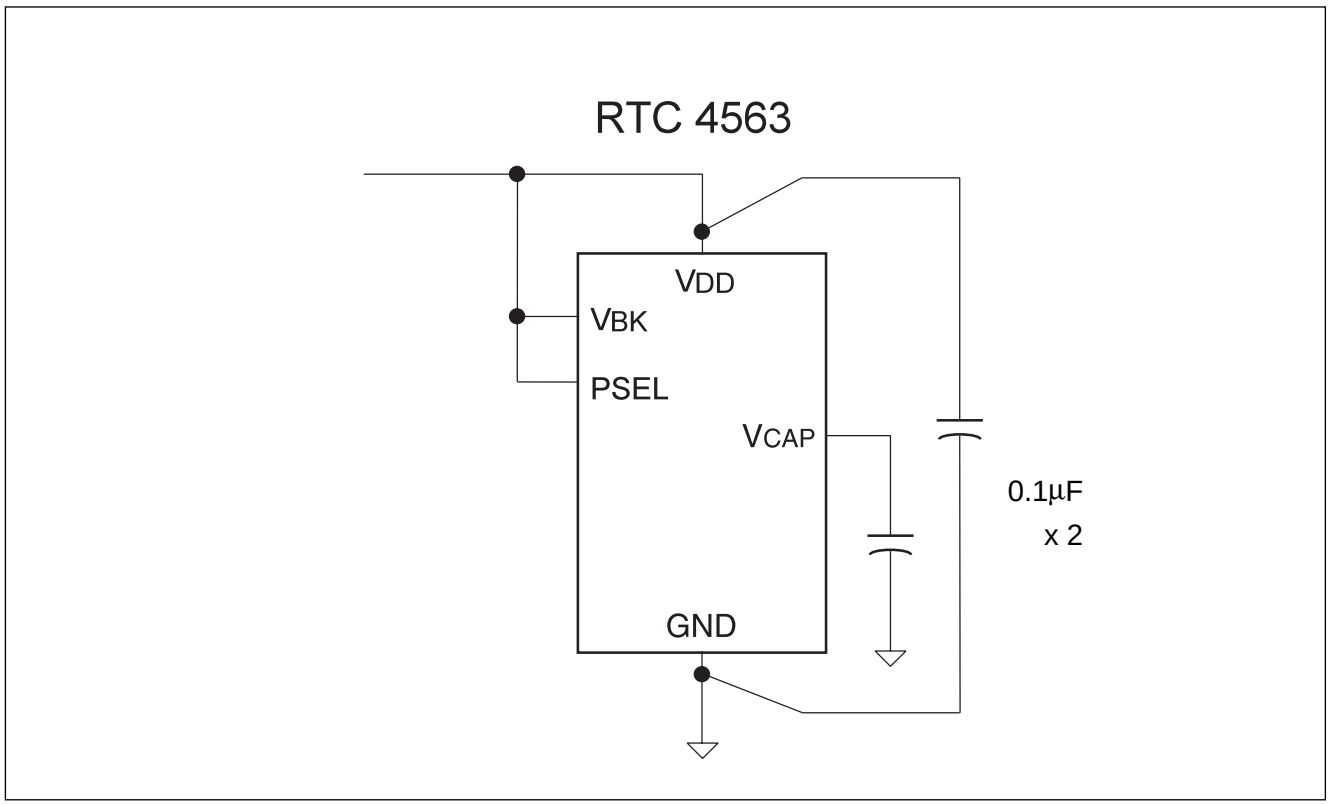
3) Leak current

- When V_{DD} - 1V > V_{BK}, leak current from V_{DD} to V_{BK} will be generated. It is recommended that the difference in electric potential be less than 1V when switching between V_{DD} and V_{BK}.

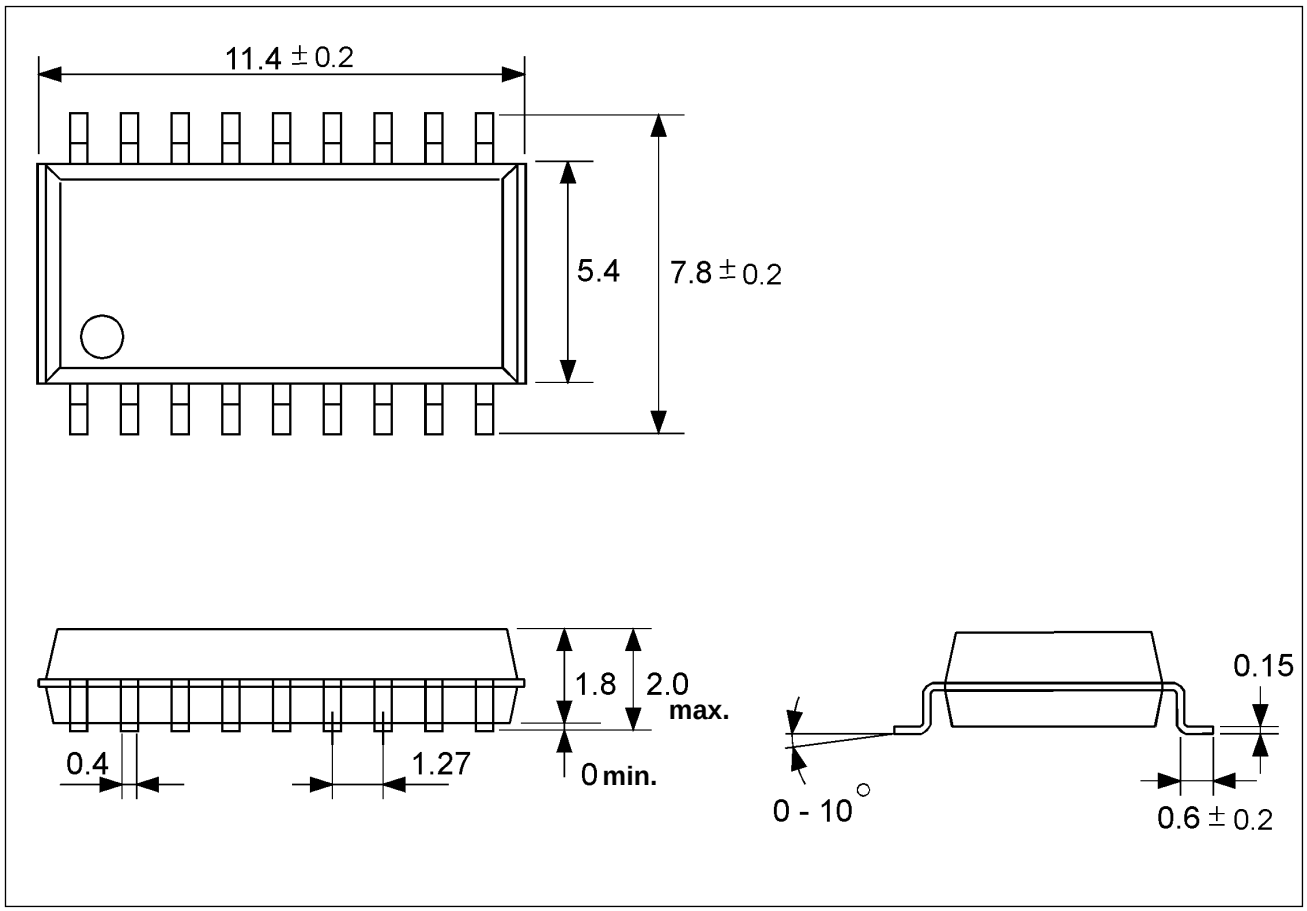
■ Examples of external connections



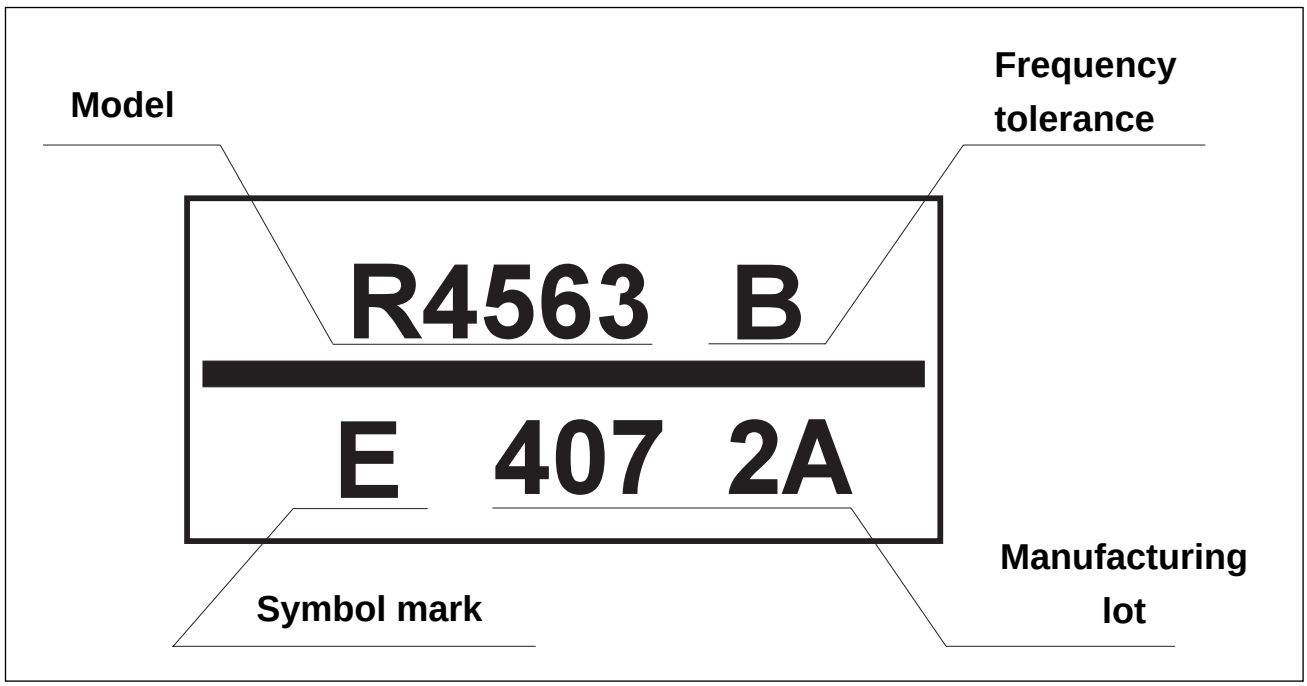
When not using the power supply switching circuit or when switching the power supply externally, connect the V_{DD}, V_{BK} and PSEL pins as shown below.



■ Package outline



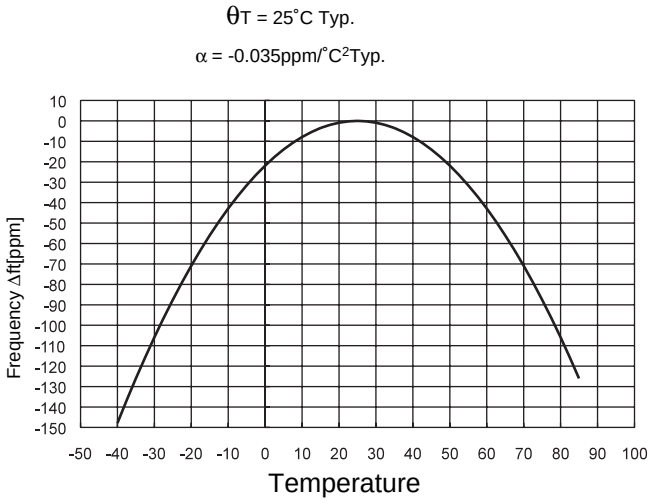
■ Layout of package markings



Note: The markings and their positions as pictured above are only approximations. These illustrations do not define the details of the style, size, and position of the characters marked on the packages.

■ Reference data

(1) Example of frequency-temperature characteristics



Determining the frequency stability (clock accuracy)

1. The frequency-temperature characteristics can be approximated by the following equation:

$\Delta ft(ppm)=\alpha(\theta T-\theta X)^2$

Δf_T(ppm)	:	Frequency deviation at any given temperature
α(ppm/℃^{2})	:	Second-order temperature characteristics (-0.035 ± 0.005 ppm/°C[2])
θ_T(℃)	:	Highest temperature (25°C ± 5°C)
θ_X(℃)	:	Any given temperature

2. In order to determine the clock accuracy, add in the frequency accuracy and the voltage characteristics.

$\Delta f/f(ppm)=\Delta f/fo + \Delta fT + \Delta fv$

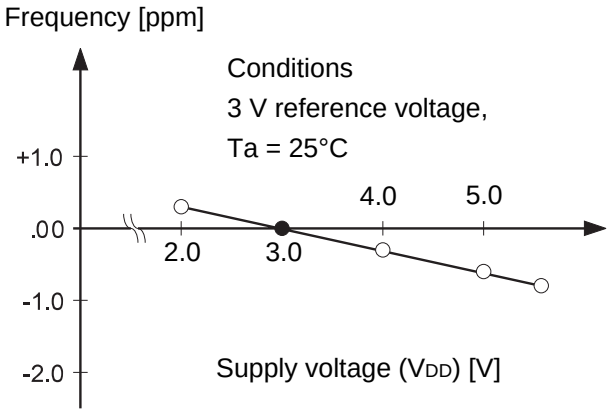
$\Delta f/f$ (ppm)	:	Clock accuracy at any given temperature and voltage (frequency stability)
$\Delta f/f_0$ (ppm)	:	Frequency accuracy)
Δf_T (ppm)	:	Frequency deviation at any given temperature
Δf_v (ppm)	:	Frequency deviation at any given voltage

3. Determining the daily error

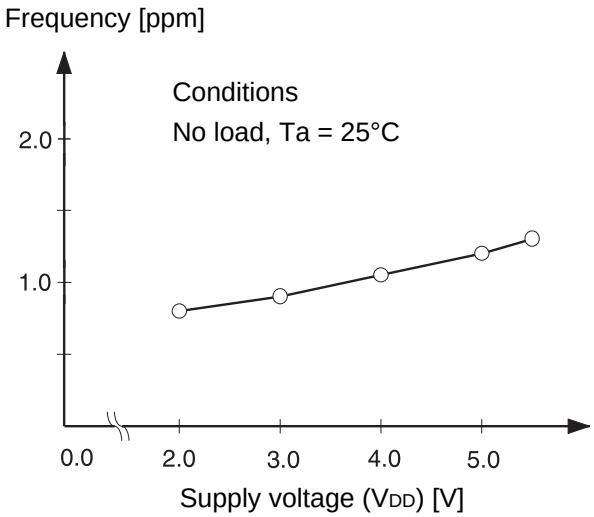
Daily error = $\Delta f/f \times 10^{-6} \times 86400$ (seconds)

With error of 11.574 ppm, the error of the clock is about one second per day.

(2) Example of frequency-voltage characteristics



(3)Example of current consumption-voltage characteristics



■ Notes on use

(1) Notes on handling

In order to attain low power consumption, this module incorporates a CMOS IC. Therefore, the following points should be kept in mind when using this module.

1. Static electricity

While this module does have built-in circuitry designed to protect it against damage from electrostatic discharge, the module could still be damaged by an extremely large electrostatic discharge. Therefore, packing materials and shipping containers should be made of conductive materials.

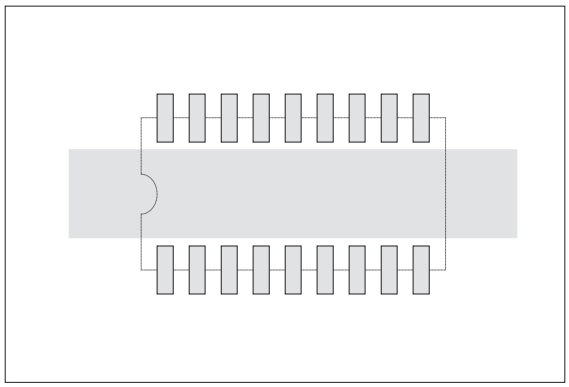
Furthermore, use soldering equipment, test circuits, etc., that do not have high-voltage leakage, and ground such equipment when working with it.

2. Electronic noise

If excessive external noise is applied to the power supply and I/O pins, the module may operate incorrectly or may even be damaged as a result of the latch-up phenomenon.

In order to assure stable operation, connect a passthrough capacitor (ceramic is recommended) of at least 0.1 μF located as closely as possible to the power supply pins on this module (between V_{DD} and GND). Furthermore, do not place a device that generates high noise levels near this module.

Keep signal lines away from the shaded areas shown in the figure at right, and fill the area with a GND pattern, if possible.



3. Electric potential of I/O pins

Because having the electric potential of the input pins at an intermediate level contributes to increased power consumption, reduced noise margin, and degradation of the device, keep the electric potential as close as possible to the electric potential of V_{DD} or GND.

4. Treatment of unused input pins

Because the input impedance of the input pins is extremely high and using the module with these pins open can result in unstable electric potential and misoperation due to noise, unused input pins must always be connected to a pull-up or pull-down resistor.

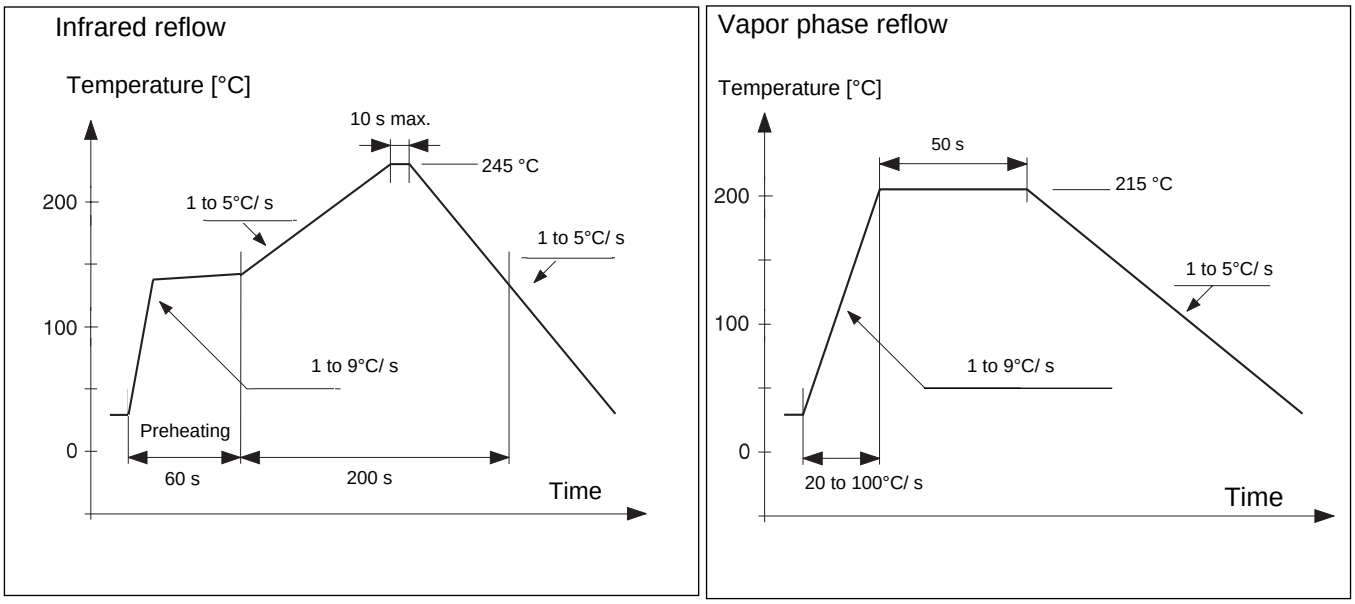
(2) Notes on mounting

1. Soldering temperature conditions

If the internal temperature of the package exceeds 260°C, the characteristics of the crystal resonator may deteriorate and the package may be damaged. Therefore, before using this module, be sure to confirm what temperatures it will be exposed to during the mounting process. If the mounting temperature conditions are ever changed, the suitability of those temperature conditions for this package must be confirmed again.

Soldering conditions: Up to 260°C for up to 10 seconds, twice, or up to 230°C for up to 3 minutes.

Example of SMD Product Soldering Conditions



2. Mounters

While this module can be used with general-purpose mounters, be sure to confirm the force of impact that the module will be subjected to during mounting, since certain machines or conditions can result in damage to the internal crystal resonator. If the mounting conditions are ever changed, the suitability of those conditions for this package must be confirmed again.

3. Ultrasonic cleaning

Under certain conditions, ultrasonic cleaning can damage the crystal resonator. Because we cannot specify the conditions under which you perform ultrasonic cleaning (including the type of cleaner, the power level, the duration, the condition of the inside of the chamber, etc.), Seiko-Epson does not warrant this product against ultrasonic cleaning.

4. Mounting orientation

If this module is mounted backwards, it may be damaged. Always confirm the orientation of the module before mounting it.

5. Leakage between pins

If power is supplied to this module while it is dirty or while condensation is present, leakage between pins may result. Be sure that the module is clean and dry before supplying power to it.

EPSON

Application Manual

RTC-4563

Distributer

SEIKO EPSON CORPORATION

Quartz Dvice Division
8548 Nakaminowa, Minowa-machi, Kamiina-gun, Nagano-ken, 399-46 Japan
Phone: (0265) 79-9149 Fax: (0265) 79-9492

Head Office
3-5, Owa 3-chome, Suwa-shi, Nagano-ken, 392 Japan
Phone: (0266) 52-3131 Fax: (0266) 58-9861