REAL TIME CLOCK MODULE
RTC-63421/63421M/63423
APPLICATION MANUAL

EPSON

INTRODUCTION

1. This Manual is based on materials as of April 1992.
   The contents are subject to change without notice. Please contact us separately for information regarding the product's warranty.
2. In this manual, the compornent and circuit examples other than RTC are designed solely to describe the product and we are not responsible for any problems that may occur as a result of these examples. All behaviors must be verified by you.
3. This manual neither guarantees any rights to the buyer, nor is it a commercial title or license.
4. We have prepared this manual as carefully as possible. If you find it incomplete or unsatisfactory in any respect, we would welcome your comments.

Contents

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■Overview

This module is a real time clock with a builtin crystal resonator. The module can be directly connected to a microprocessor, and has the alarm interrupt and reference signal output in additon to the time and calendar functions.

The module is multi-functional and adjustment-free for time accuracy.

The module is essential for equiptment requiring time management; this includes facsimiles, multi-function telephone sets, personal computers, word processors, or sequencers.

■Features:

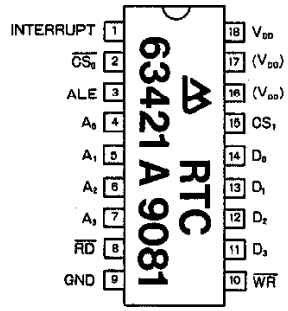
- ○The built-in crystal resonator makes the product streamlined and adjustment-free.
- ○The module can be directly connected to the CPU. (T_{WW}, T_{RD}=120nsec)
- ○The INTEL and MOTOROLA bus systems.
- ○Contains the time (hour, minute, and second) counter and calendar (year, month, day, and day of the week) counter.
- ○Periodic interrupt. (constant periodic output waveform)
- ○Selectable counting range.
- ○Available for setting the collation range of the time registers against the alarm registers.
- ○Not-used bits available for the RAM. (up to 17×4 bits)
- ○30-second correction, and STOP/START and RESET functions.
- ○Data protect function. (backup function)
- ○Decreasing current consumption by using C-MOS devices. (1.8μA Max. at V_{DD}=2V)
- ○Can be mounted under the same soldering conditions as the universal SMD IC.

Module type	Applicable CPU	Package Type
RTC-63421	Intel (80 series) bus systems	DIP 18-pin
RTC-63421M	Motorola (68 series) bus systems	DIP 18-pin
RTC-63423	Motel (80/68 series) bus systems	SOP 24-pin

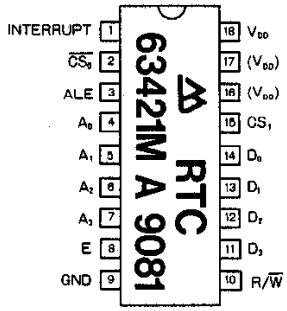
※Pins and functions are compatible with the MSM6542 series.

■Terminal connections

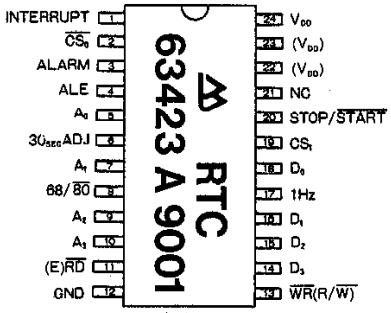
●RTC-63421



●RTC-63421M



●RTC-63423



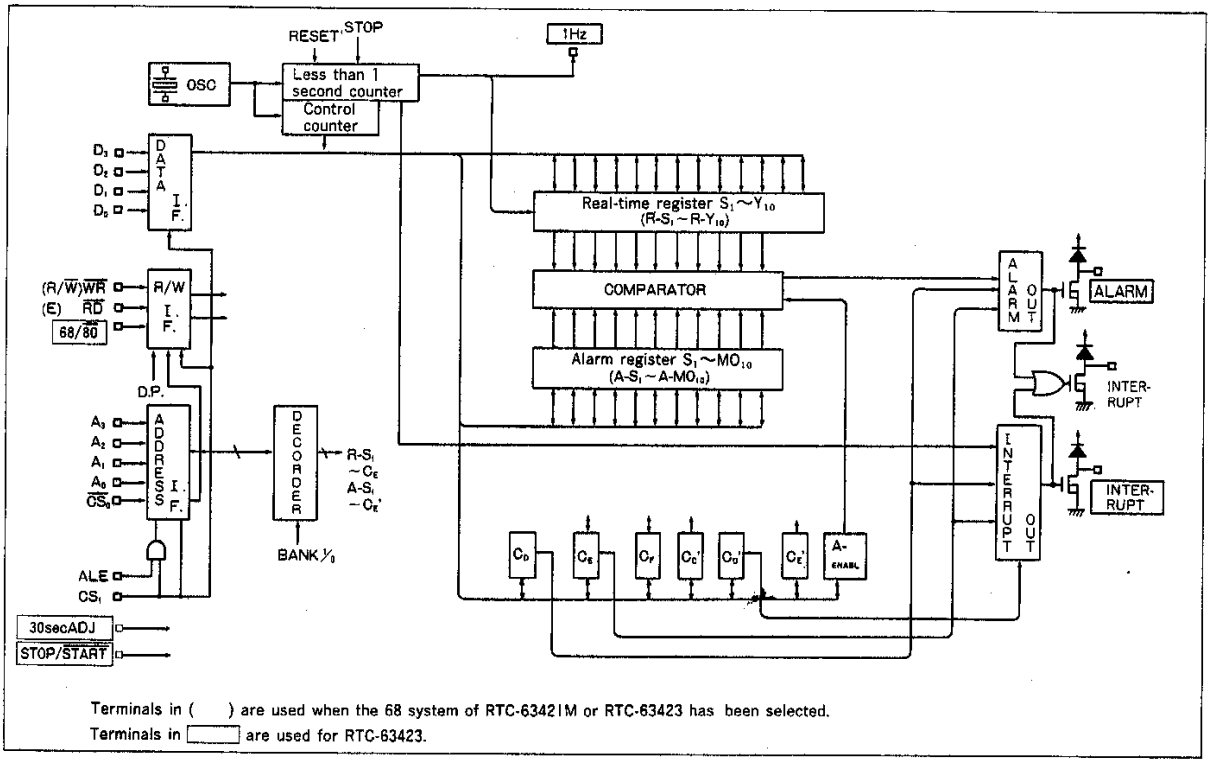
Terminal in ( ) are used when the MOTOROLA bus systems.

Notes:

- (VDD) is at the same electric level as VDD. (VDD) must not be connected externally.
- NC terminal should be GND in order to avoid noise.

RTC-63421/63421M/63423

Block diagram



Terminals in ( ) are used when the 68 system of RTC-63421M or RTC-63423 has been selected.
Terminals in [ ] are used for RTC-63423.

Terminal functions

Terminal symbol (name)	Terminal No. 63421	63421M	63423	Output Input	Function
D_0 to D_3 (Data Bus)	11 to 14	11 to 14	14, 15 16, 18	Bi-direction	Connected to the data bus of the microprocessor to read/write registers.

Common		Series		Series		Mode of D_0 to D_3
CS_1	$\overline{CS_0}$	$\overline{RD}$	$\overline{WR}$	E	R/$\overline{W}$	
H	L	L	H	H	H	Output mode (read mode)
H	L	H	L	H	L	Input mode (write mode)
L	—	Don't Care				High impedance
—	H					

A_0 to A_3 (Address Bus)	4 to 7	4 to 7	5, 7, 9, 10	Input	Connected this terminal to the address bus of the microprocessor. The terminal selects the RTC register (address).
ALE (Address Latch Enable)	3	3	4	Input	Reads in address data and $\overline{CS_0}$.

ALE	Address data and the $\overline{CS_0}$ state.
H	Read into the RTC to set an address.
L	Held in the RTC (Held at the ALE trailing edge).

When the microprocessor has no ALE terminal, use the ALE terminal of the RTC by fixing it to "H".

$\overline{WR}$ (WRITE)	10	—	13	Input	Write data of D_0 to D_3 onto the register specified by the A_0 to A_3 at the leading edge of $\overline{WR}$.
$\overline{RD}$ (READ)	8	—	11	Input	Output data from the register specified by the A_0 to A_3 to D_0 to D_3 during $\overline{RD}$ = L. $\overline{RD}$ and $\overline{WR}$ must not be simultaneously "L".
R/$\overline{W}$ (READ/ WRITE)	—	10	13	Input	Reads and writes data from the specified register in combination with the E terminal below.

R/$\overline{W}$	Mode	Contents
H	READ mode	Output the contents of data from the specified register to D_0~D_3 during E = H.
L	WRITE mode	Write data onto the specified register at the trailing edge of the E.

Terminal symbol (name)	Terminal No. 63421	63421M	63423	Output Input	Function
E (Enable)	—	8	11	Input	Used in combination with the R/$\overline{W}$ terminal above when reading/writing data from/to the register specified by the A_0 to A_3.
$CS_1 \cdot \overline{CS_0}$ (Chip Select)	15, 2	15, 2	19, 2	Output	Only when the CS_1 = H and the $\overline{CS_0}$ = L, the ALE, $\overline{RD}$, and $\overline{WR}$, or the E and R/$\overline{W}$ are valid. For the 80 system, the $\overline{CS_0}$ must operate in conjunction with the ALE (see the item on the ALE). The CS_1 is used to detect the supply voltage. (see the section "Using the CS_1") When the CS_1 is set to "L", the HOLD and RESET bits are automatically reset. (set to "0")
INTERRUPT	1	1	1	Output	This terminal requests interruption of the microprocessor which is N-ch OPEN DRAIN. Module type / Interrupt mode / Description: 63421/63421M — Constant periodic and alarm interrupts — Constant periodic and alarm interrupts are ORed and output. 63423 — Constant periodic interrupt — Alarm interrupt is output from the alarm terminal below. Output is never inhibited by CS_1, $\overline{CS_0}$.
ALARM	—	—	3	Output	This terminal requests interruption of the microprocessor when the alarm has occurred. This terminal is N-ch OPEN DRAIN. Output is never inhibited by CS_1, $\overline{CS_0}$.
1Hz	—	—	17	Output	Outputs pulse of the 50% duty. This terminal can be used to check the clocks accuracy. Output is never inhibited by CS_1, $\overline{CS_0}$. Notes: ① Being the 1-second output of the clock counter, the 1-Hz output is cleared to the "L" level when the Reset and 30-seconds ADJ are executed. The 1-Hz output stops in the level at that time when the STOP is executed. ② Being the C-MOS output, current consumption increases (the battery exhausts) even at stand-by when this output is connected to load.
30 sec ADJ (30 Seconds Adjustment)	—	—	6	Input	Conducts 30-seconds correction through hardware. Correction takes place at the leading edge of "H". Second digit state before correction / Second digit state after correction / Condition: Less than 30 seconds — "00" second without a carry from the one-minute digit. — HD/$\overline{SFT}$ = don't care 30 seconds or more — "00" second with a carry from the one-minute digit.
STOP/$\overline{START}$	—	—	20	Input	Starts or stops counting through the hardware The HD/$\overline{SFT}$ bit can select this terminal or STOP bit of software. STOP/$\overline{START}$ / Counting / Condition: H — Counting up stop at 4096Hz or more. — HD/$\overline{SFT}$ = 1 L — Counting starts. To select the HD/$\overline{SFT}$ bit = 0, connect this terminal to GND.
68/$\overline{80}$	—	—	8	Input	Selects whether the RTC is used for the 68 system or the 80 system. 68/$\overline{80}$ / Applicable CPU / State of Pin 11 and Pin 13: H (V_{DD}) — 68 series — State of Pin 11 = E, State of Pin 13 = R/$\overline{W}$ L (GND) — 80 series — State of Pin 11 = $\overline{RD}$, State of Pin 13 = $\overline{WR}$
V_{DD}	18	18	24		Connect this terminal to the power source. When the power is on, or in the Bus Access mode, supply 5V ± 10%. Supply 2V or more in Battery Backup mode.
GND	9	9	12		Connect this terminal to the ground.
(V_{DD})	16, 17	16, 17	22, 23		This terminal is connected to V_{DD}, inside for EPSON's special design. Keep this terminal open.
NC	—	—	21		This terminal is not connected. Connect this terminal to GND.

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■Characteristics

1. Absolute maximum ratings

Item	Symbol	Condition	Specifications	Unit
Supply voltage	V_{DD}	Ta=25°C	−0.3 to 7.0	V
Input/Output voltage	$V_{I/O}$	Ta=25°C	GND−0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	RTC-63421・RTC-63421M	−55 to +85	°C
		RTC-63423	−55 to +125	
Soldering condition	T_{SOL}	RTC-63421 RTC-63421M	260°C or less within 10 seconds (lead part) (150°C or less for the package)	
		RTC-63423	Twice at 260°C or less within 10 seconds, or once at 230°C or less within 3 minutes.	

2. Operating ranges

Item	Symbol	Condition	Specifications	Unit
Supply voltage	V_{DD}	———	4.5 to 5.5	V
Operating temperature	T_{OPR}	Note 1	−40 to +85	°C
Data hold voltage	V_{DH}	Note 2	2.0 to 6.0	V

Notes: 1. When the 68/$\overline{80}$ terminal of RTC-63423 is in the "H" state, and RTC-63421M,the switching characteristics guarantee temperature is 0-70°C.

Notes: 2. This supply voltage does not assure interface to equipment outside the RTC, but assures the internal clock and RAM data in the RTC.

3. Frequency characteristics and current consumption characteristics

Item	Symbol	Condition		Specifications	Unite
Frequency tolerance	△f/fo	Ta=25°C V_{DD}=5V	63421A/63421MA	+15/− 5 (5±10)	ppm
			63421B/63421MB	+55/−45 (5±50)	
			63423A	+25/−15 (5±20)	
			63423	+55/−45 (5±50)	
Frequency temperature characteristics		−10 to +70°C (Reference at 25°C)		+10/−120	
		−40 to +85°C (Reference at 25°C)		+10/−220	
Aging	fa	V_{DD}=5V, a=25°C, first year		±5MAX.	ppm/year
Shock resistance	S.R.	Drop test of 3 times on a hard board from 75cm height, or 3000G×0.3 msec×1/2 Sin wave×3 Directions.		±10MAX.	ppm
Current consumption	I_{DD1}	CS_1=0V exclude input current	V_{DD}=5V	30MAX.	μA
	I_{DD2}		V_{DD}=2V	1.8MAX.	

※Unless otherwise specified, the characteristic values are standard in the ranges of operating temperature and voltage.

4. Electrical characteristics (DC characteristics)

(V_{DD} = 5V ± 0.5V, Ta = −40 to +85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit	terminal
"H" input voltage	V_{IH1}	———	2.2	——	——	V	STOP/$\overline{\text{START}}$, 68/$\overline{80}$, All inputs except the CS_1
"L" input voltage	V_{IL1}	———	———	——	0.8		
"H" input voltage	V_{IH2}	V_{DD} = 2 to 5.5V	$4/5V_{DD}$	——	——	V	STOP/$\overline{\text{START}}$, 68/$\overline{80}$, CS_1
"L" input voltage	V_{IL2}		——	——	$1/5V_{DD}$		
Input leak current (1)	V_{LK1}	$V_I = V_{DD}/0V$	−1	——	1	μA	Inputs other than D_0 to D_3, STOP/$\overline{\text{START}}$
Input leak current (2)	V_{LK2}		−10	——	10		D_0 to D_3, STOP/$\overline{\text{START}}$
"H" input current	I_{HLK}	$V_{IH} = 0.8V_{DD}$	−100	——	−20	μA	STOP/$\overline{\text{START}}$
"L" input current	I_{LLK}	$V_{IL} = 0.2V_{DD}$	20		100		
"H" output volatage	V_{OH}	$I_{OH} = -400\mu A$	2.4	——	——	V	D_0 to D_3, 1Hz
"L" output voltage	V_{OL1}	$I_{OL} = 2.5mA$	——	——	0.4		
"L" output voltage	V_{OL2}	$I_{OL} = 2.5mA$	——	——	0.4		ALARM, INTERRUPT OPEN DRAIN output
Off leak current	I_{OFFLK}	$V_I = V_{DD}/0V$	——	——	10	μA	
Input capacity (1)	C_{I1}	Input frequency 1MHz	——	3	——	pF	Input other D_0 to D_3
Input capacity (2)	C_{I2}		——	5	——		D_0 to D_3
Oscillation start time	T_{OSC}	$V_{DD} \geq 4.5V$, Ta = 25°C	——	——	1	sec	Measured at INTERRUPT = 1024Hz

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■Switching characteristics (AC characteristics)

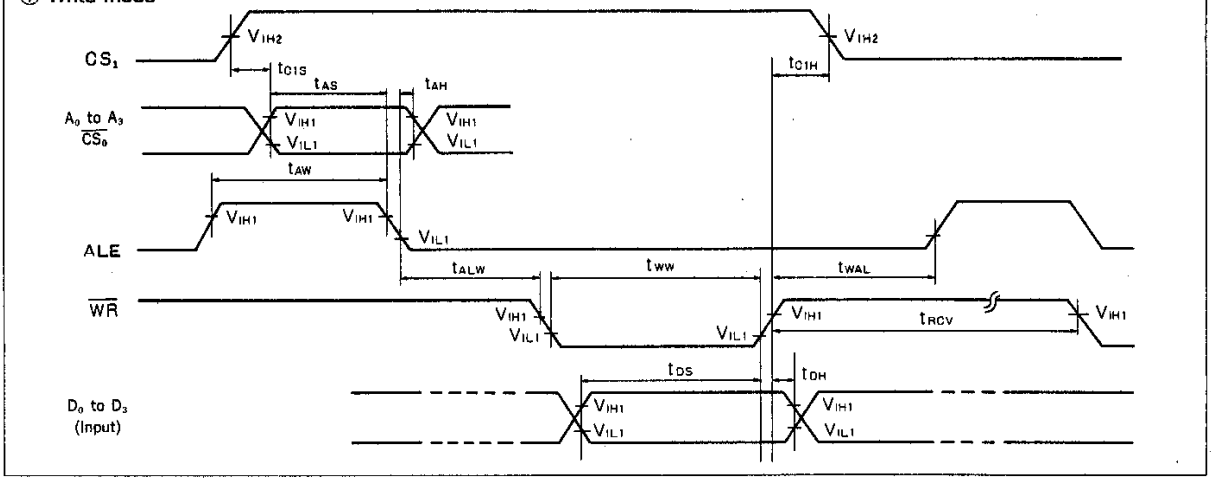
1. The 80 CPU (INTEL bus) system

(I) When the ALE is used

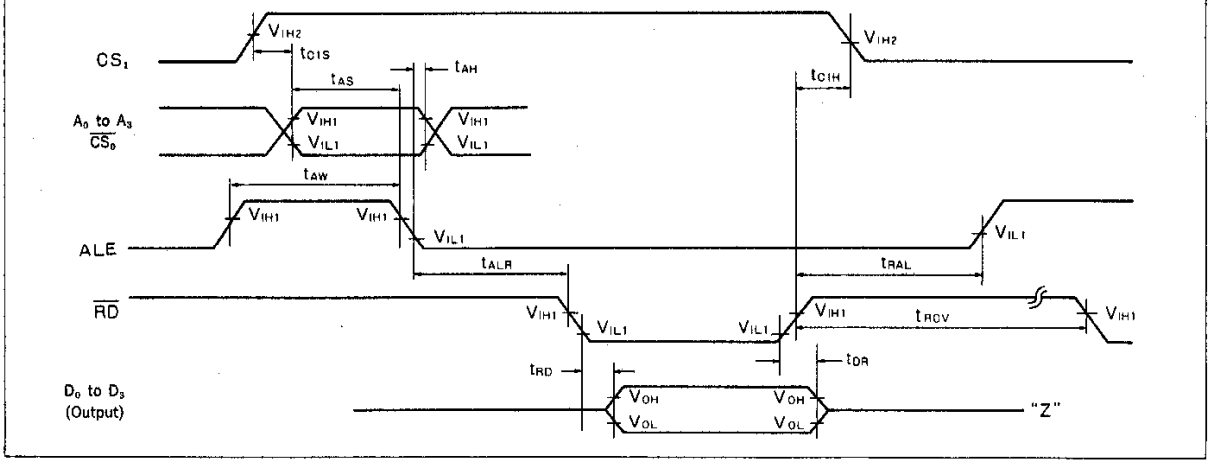
(V_{DD} = 5V ± 0.5V, Ta = −40 to +85°C)

Item	Symbol	Condition	MIN	MAX	Unit
CS_1 Set up Time	t_{C1S}		1000	—	nsec
Address Set up Time	t_{AS}		25	—	
Address HOLD Time	t_{AH}		25	—	
ALE Pulse Width	t_{AW}		40	—	
ALE Before WRITE	t_{ALW}		10	—	
ALE Before READ	t_{ALR}		10	—	
ALE After WRITE	t_{WAL}		20	—	
ALE After READ	t_{RAL}		20	—	
WRITE Pulse Width	t_{WW}		120	—	
$\overline{RD}$ to Data	t_{RD}	CL = 150pF	—	120	
DATA Hold	t_{DR}		10	45	
DATA Set up Time	t_{DS}		100	—	
DATA Hold Time	t_{DH}		10	—	
CS_1 Hold Time	t_{C1H}		1000	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}		100	—	

① Write mode



② Read mode



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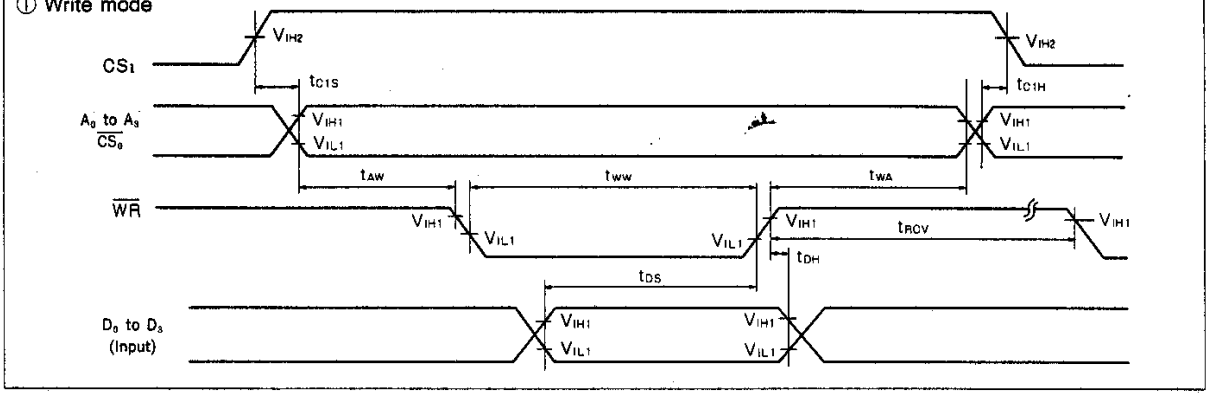
(2) When fixed at ALE = V_{DD}

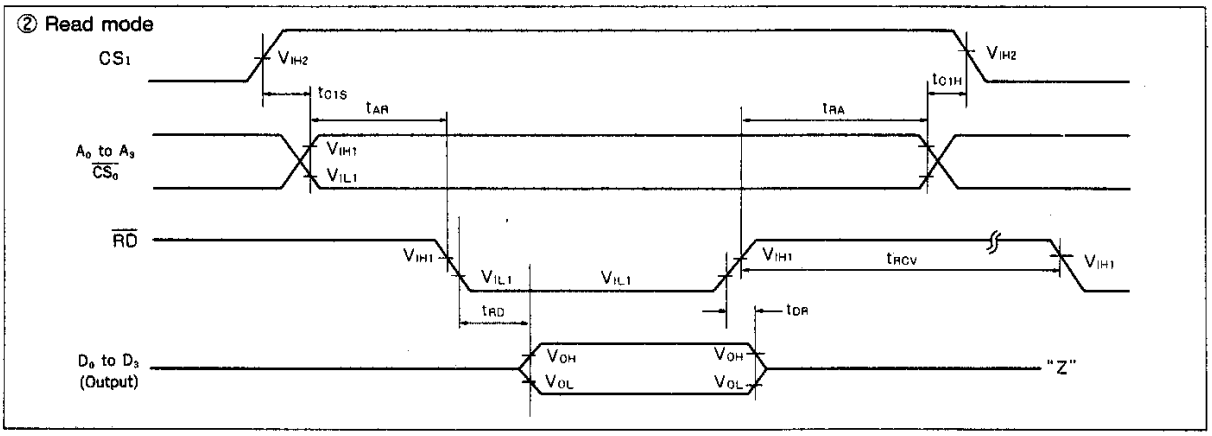
(V_{DD} = 5V ± 0.5V, Ta = −40 to +85°C)

Item	Symbol	Condition	MIN	MAX	Unit
CS_1 Set up Time	t_{C1S}		1000	—	nsec
Address Stable Before WRITE	t_{AW}		20	—	
Address Stable Before READ	t_{AR}		20	—	
Address Stable After WRITE	t_{WA}		10	—	
Address Stable After READ	t_{RA}		20	—	
WRITE Pulse Width	t_{WW}		120	—	
$\overline{RD}$ to Data	t_{RD}	OL = 150pF	—	120	
DATA Hold	t_{DR}		10	45	
DATA Set up Time	t_{DS}		100	—	
DATA Hold Time	t_{DH}		10	—	
CS_1 Hold Time	t_{C1H}		1000	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}		100	—	

① Write mode



② Read mode



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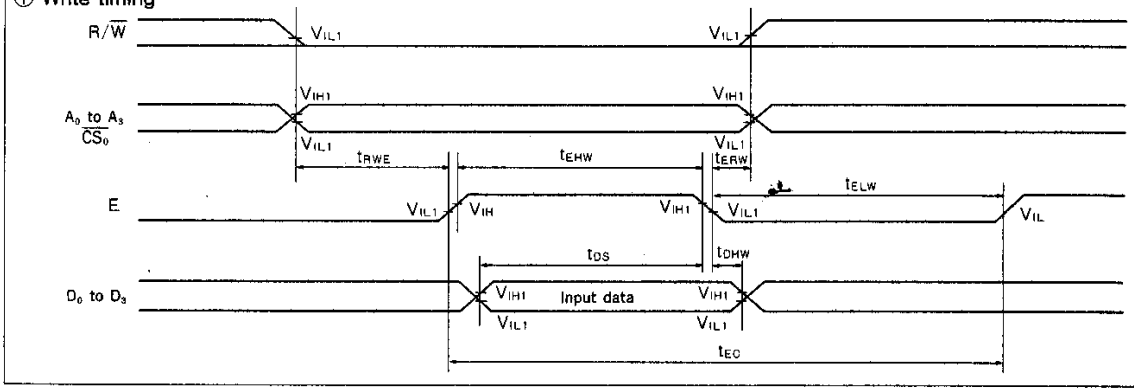
2. The 68 CPU (MOTOROLA bus) system

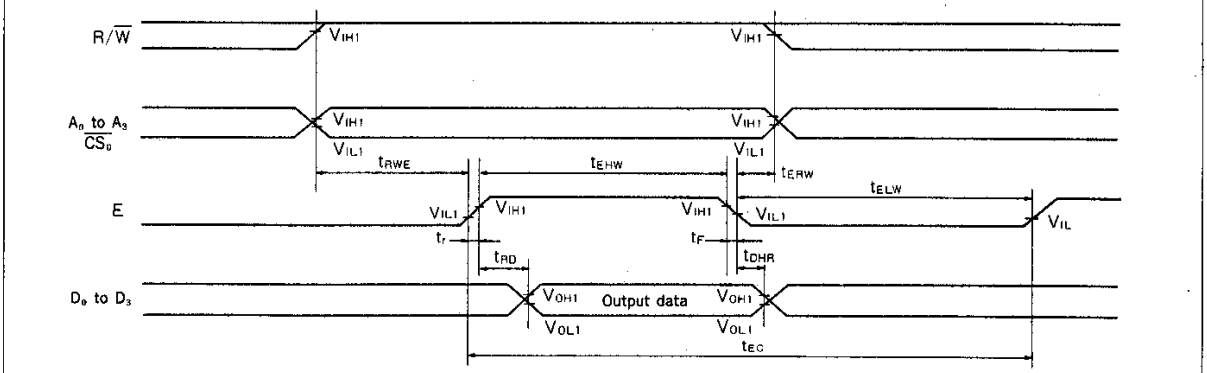
(V_{DD} = 5V ± 0.5V, Ta = 0 to 70°C)

Htem	Symbol	Rating		Unite
		MIN	MAX	
R/$\overline{W}$, Address Set up time	t_{RWE}	100	—	nsec
E "H" Pulse Width	t_{EHW}	220	—	
R/$\overline{W}$, Address Hold Time	t_{ERW}	20	—	
E "L" Pulse Hold Time	t_{ELW}	220	—	
E Cycle Time	t_{EC}	500	—	
WRITE DATA Hold Time	t_{DS}	180	—	
DATA Hold Time	t_{DHW}	20	—	
E to Data (CL = 150pF)	t_{RD}	—	120	
READ Data Hold	t_{DHR}	10	—	

① Write timing



② Read timing



■Registers

1. Register table

Address	A_3	A_2	A_1	A_0	Register symbol	BANK 0 D_3	BANK 0 D_2	BANK 0 D_1	BANK 0 D_0	Real-time register name	Register symbol	BANK 1 D_3	BANK 1 D_2	BANK 1 D_1	BANK 1 D_0	Alarm register name
0	0	0	0	0	R-S_1	r-s_8	r-s_4	r-s_2	r-s_1	1 second digit	A-S_1	a-s_8	a-s_4	a-s_2	a-s_1	1 second digit
1	0	0	0	1	R-S_{10}	*	r-s_{40}	r-s_{20}	r-s_{10}	10 seconds digit	A-S_{10}	*	a-s_{40}	a-s_{20}	a-s_{10}	10 seconds digit
2	0	0	1	0	R-MI_1	r-mi_8	r-mi_4	r-mi_2	r-mi_1	1 minute digit	A-MI_1	a-mi_8	a-mi_4	a-mi_2	a-mi_1	1 minute digit
3	0	0	1	1	R-MI_{10}	*	r-mi_{40}	r-mi_{20}	r-mi_{10}	10 minutes digit	A-MI_{10}	*	a-mi_{40}	a-mi_{20}	a-mi_{10}	10 minutes digit
4	0	1	0	0	R-H_1	r-h_8	r-h_4	r-h_2	r-h_1	1 hour digit	A-H_1	a-h_8	a-h_4	a-h_2	a-h_1	1 hour digit
5	0	1	0	1	R-H_{10}	*	r-PM/$\overline{AM}$	r-h_{20}	r-h_{10}	10 hours digit	A-H_{10}	*	a-PM/$\overline{AM}$	a-h_{20}	a-h_{10}	10 hours digit
6	0	1	1	0	R-D_1	r-d_8	r-d_4	r-d_2	r-d_1	1 day digit	A-D_1	a-d_8	a-d_4	a-d_2	a-d_1	1 day digit
7	0	1	1	1	R-D_{10}	*	*	r-d_{20}	r-d_{10}	10 days digit	A-D_{10}	*	*	a-d_{20}	a-d_{10}	10 days digit
8	1	0	0	0	R-MO_1	r-mo_8	r-mo_4	r-mo_2	r-mo_1	1 month digit	A-MO_1	a-mo_8	a-mo_4	a-mo_2	a-mo_1	1 month digit
9	1	0	0	1	R-MO_{10}	*	*	*	r-mo_{10}	10 months digit	A-MO_{10}	*	*	*	a-mo_{10}	10 months digit
A	1	0	1	0	R-Y_1	r-y_8	r-y_4	r-y_2	r-y_1	1 year digit	A-W	*	a-w_4	a-w_2	a-w_1	Day of week
B	1	0	1	1	R-Y_{10}	r-y_{80}	r-y_{40}	r-y_{20}	r-y_{10}	10 years digit	A-ENB	ae_8	ae_4	ae_2	ae_1	Area Enable register
C	1	1	0	0	R-W	*	r-w_4	r-w_2	r-w_1	Day of week digit	Cc'	*	*	$TEST_2$	$TEST_1$	Test register
D	1	1	0	1	C_D	IT/$\overline{PLS_2}$	IT/$\overline{PLS_1}$	$MASK_2$	$MASK_1$	Control register D	C_D'	*	CY_2	CY_1	CY_0	Control register D'
E	1	1	1	0	C_E	IRQ•$FLAG_0$	RESET	IRQ•$FLAG_2$	IRQ•$FLAG_1$	Control register E	C_E'	HD/$\overline{SFT}$	24/$\overline{12}$	CAL	D.P.	.Control register E'
F	1	1	1	1	C_F	$BANK_1$/$\overline{BANK_0}$	STOP	30 seconds ADJ	READ FLAG	Control register F	C_F'	Same as BANK 0				Control register F'

2. Notice

(1) "H" of the date bus is in positive logic corresponds to "1" in the register.
(2) Do not set data out of range for the clock. Otherwise, a counting error may occur.
(3) When the power is turned on, (before initialization) the state of the bites is undefined. Write the registers to set the values.

3. Real-time/alarm registers

(1) When registers marked with * are used as the real-time register and alarm register, data becomes "0" at the time of read. When they are used as the RAM, read/write are enabled.
The area indicated by [ ] can be set as a RAM area.
(2) Both real-time and alarm registers are in BCD code.
(3) For both real-time and alarm registers, decode the week digit for use.

Example:

Data	0	1	2	3	4	5	6
Day of the week	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

(4) For both r-PM/$\overline{AM}$ and a-PM/$\overline{AM}$ of the real-time and alarm registers, the PM/$\overline{AM}$ bit is for PM at "1" and for AM at "0".
(5) The bits selectable as the RAM are R-D_1 to R-Y_{10} (6×4 bits) and A-S_1 to A-W (11×4 bits) of up to 17×4 bits.

4. Functions of the control register bits

Bit name	Role
$MASK_1$	$MASK_1$ = 1 inhibits the constant periodic interrupt output.
$MASK_2$	$MASK_2$ = 1 inhibits the alarm interrupt output.
IT/$\overline{PLS_1}$	IT/$\overline{PLS_1}$ = 1 enables the constant periodic interrupt mode: IT/$\overline{PLS_1}$ = 0 enables the constant periodic pulse mode.
IT/$\overline{PLS_2}$	IT/$\overline{PLS_2}$ = 1 enables the alarm interrupt mode; IT/$\overline{PLS_2}$ = 0 enables the alarm pulse mode.
IRQ $FLAG_1$	This bit is set to "1" at the constant periodic output timing. This bit is released by reading/writing IRQ $FLAG_1$.
IRQ $FLAG_2$	This bit is set to "1" at the alarm output timing. This bit is released by reading/writing IRQ $FLAG_2$.
RESET	RESET = 1 resets the less than one second counter.
IRQ $FLAG_0$	This bit is set to "1" during the interrupt clear disable period. (for 122μs after the interrupt occurrence timing)
READ FLAG	This bit is used to read the time data; the bit is set to "1" during the carry from the one-second digit.
30 seconds ADJ	When this bit is "1", the 30-seconds correction is enabled.
STOP	STOP = 1 stops counting at 4096Hz or more; STOP = 0 restarts counting.
$BANK_1$/$\overline{BANK_0}$	Setting this bit to "1" selects $BANK_1$; setting this bit to "0" selects $BANK_0$.
$TEST_{1,2}$	This bit is used by Epson to test the system. The user must set this bit to "0".
CY_0 to CY_2	These bits are used to set the pulse mode period.
D.P.	When D.P. = 1, data is protected; to continue reading. keep the bit at "1".
CAL	This bit determines the counting-up rang of the counters; CAL = 1 is for R-S_1 to R-Y_{10} and R-W, and CAL = 0 is for R-S_1 to R-H_{10} and R-W.
24/$\overline{12}$	When 24/$\overline{12}$ = 1, the 24-hour system is selected; when 24/$\overline{12}$ = 0, the 12-hour system is selected.
HD/$\overline{SFT}$	This bit determines whether the STOP/$\overline{START}$ is used together in hardware (HD/$\overline{SFT}$ = 1) or software (HD/$\overline{SFT}$ = 0) (valid only for RTC-63423).

5. Setting the constant periodic output and alarm output modes

(1) Constant periodic output mode

Mode	$MASK_1$	$IT/\overline{PLS_1}$	$IRQ\ FLAG_1$	INTERRUPT terminal	Output timing setting bit
Constant periodic pulse mode	0	0	Set to "1" at the periodic timing	Set to "L" at the periodic timing	CY_0 to CY_2 (1024Hz~10 minutes)
Constant periodic interrupt mode	0	1			
Constant periodic output disable	1	Don't Care	"0"	OPEN	

(2) Alarm output mode

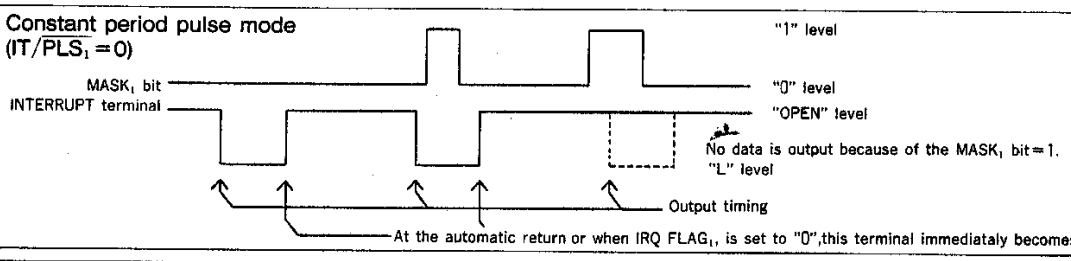
Mode	$MASK_2$	$IT/\overline{PLS_2}$	$IRQ\ FLAG_2$	INTERRUPT terminal $*_1$ or ALARM terminal $*_2$	Output timing setting bit
Alarm pulse mode	0	0	Set to "1" at the alarm timing	Set to "L" at the alarm timing	A-ENB and A-S_1 to A-W
Alarm interrupt mode	0	1			
Alarm output disable	1	Don't Care	"0"	OPEN	

$*_1$···RTC-63421/63421M, $*_2$···RTC-63423

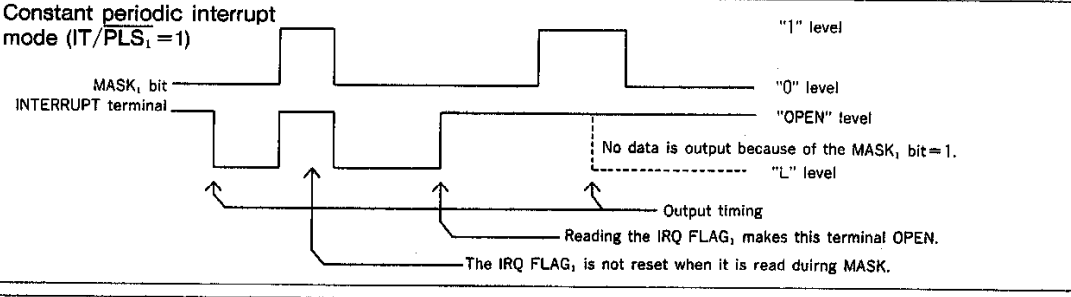
6. Timing of the constant periodic output and alarm output modes

For RTC-63421 or RTC-63421M, the INTERRUPT terminal sends alarm output and ORed data (see No.2 on page 12). For the simpler descriptions either of two output is show below:

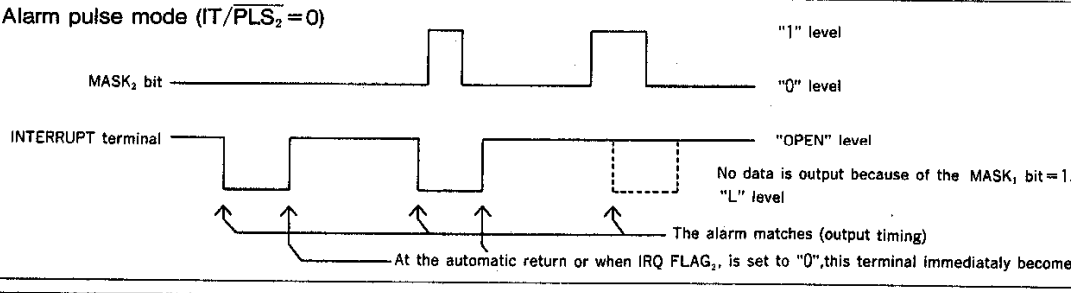
(1) Constant period pulse mode ($IT/\overline{PLS_1}=0$)



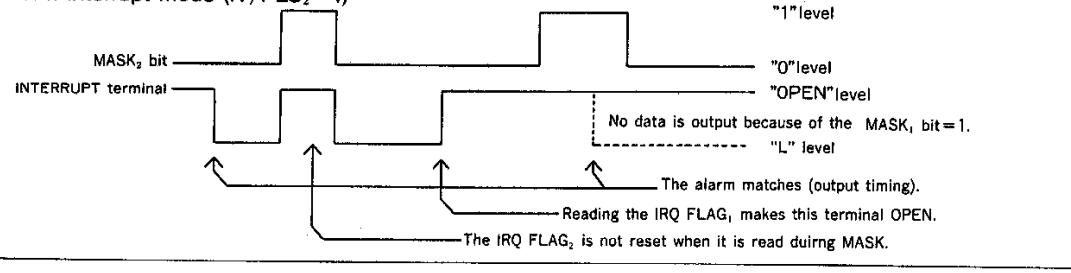
(2) Constant periodic interrupt mode ($IT/\overline{PLS_1}=1$)



(3) Alarm pulse mode ($IT/\overline{PLS_2}=0$)



(4) Alarm interrupt mode ($IT/\overline{PLS_2}=1$)



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7. Resetting the constant periodic output and alarm output modes

(1) Constant periodic output mode

Mode	D.P.	IRQ FLAG$_0$	IRQ FLAG$_1$	IRQ FLAG$_1$	INTERRUPT terminal
Constant periodic pulse mode ($MASK_1=0$, $IT/\overline{PLS_1}=0$)	0	Remains "0"	Set to "0"	Reset immediately after writing. ("1"→"0")	Reset immediately after writting IRQ FLAG. ("L"→"OPEN")
	1	Remains "0"	Write is disabled	Automatically returned by the set period	Automatically returned by the set period
	Don't Care	Remains "0"	Write is disabled	Automatically returned by the set period	Automatically returned by the set period
Constant periodic interrupt mode ($MASK_1=0$, $IT/\overline{PLS_1}=0$)	0	Remains "0"	Read	Reset immediately after reading ("1"→"0")	Reset immediately after reading IRQ FLAG$_1$ ("L"→"OPEN")
	1	Remais "1" for 122μs after an interrupt has occurred.	Read	Remains "1" for 122μs after the period timing.	Remains "L" for 122μs after the period timing.
	Don't Care	Remains "0", or remains "1" for 122μs.	No read	No next interrupt occurs because this bit has not been reset.	No next interrupt occurs because this terminal has not been reset.

(2) Alarm output mode

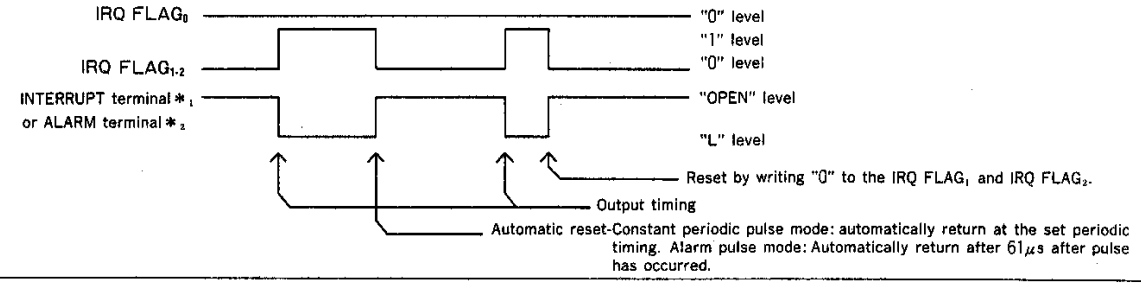
Mode	D.P.	IRQ FLAG$_0$	IRQ FLAG$_2$	IRQ FLAG$_2$	INTERRUPT terminal*$_1$ or ALARM terminal*$_2$
Alarm pulse mode ($MASK_2=0$, $IT/\overline{PLS_2}=0$)	0	Remains "0"	Set to "0"	Reset immediately after writing. ("1"→"0")	Reset immediately after writting IRQ FLAG. ("L"→"OPEN")
	1	Remains "0"	Write is disabled	Automatically reset in 61μs after the alarm timing	Automatically reset in 61μs after the alarm timing
	Don't Care	Remains "0"	Write is disabled	Automatically reset in 61μs after the alarm timing	Automatically reset in 61μs after the alarm timing
Alarm interrupt mode ($MASK_2=0$, $IT/\overline{PLS_2}=1$)	0	Remains "0"	Read	Reset immediately after reading ("1"→"0")	Reset immediately after reading IRQ FLAG$_1$ ("L"→"OPEN")
	1	Remains "1" for 122μs after the alarm timing.	Read	Remains "1" for 122μs after the alarm timing.	Remains "L" for 122μs after the alarm timing.
	Don't Care	Remains "0", or remains "1" for 122μs.	No read	No next interrupt occurs because this bit has not been reset.	No next interrupt occurs because this terminal has not been reset.

*$_1$…RTC-63421/63421M$_1$ *$_2$…RTC-63423

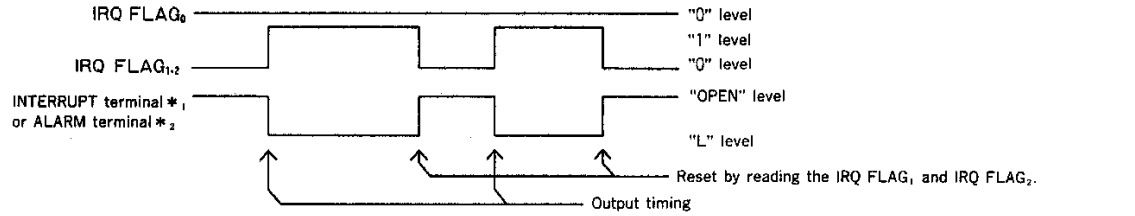
8. Reset timing of the constant periodic output and alarm output modes

(1) D.P. bit=0

① Constant periodic and alarm pulse modes ($IT/PLS_{1,2}=0$).



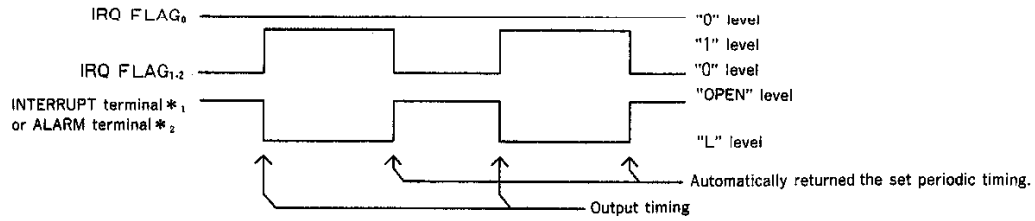
② Constant periodic and alarm interrupt modes.



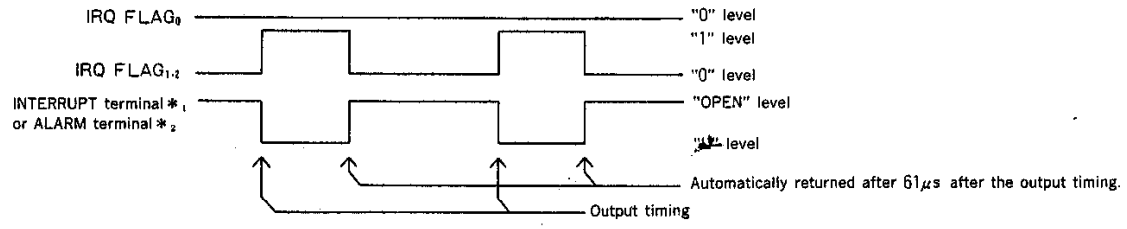
(2) D.P. bit=1

Since D.P.=1 (in the data protect mode), "0"cannot be written to the IRQ $FLAG_{1,2}$.

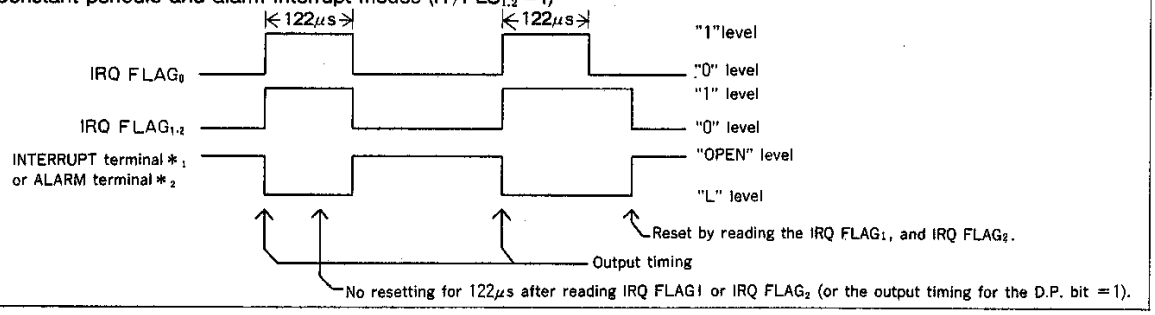
① Constant periodic pulse mode ($IT/\overline{PLS_1}=0$)



② Alarm pulse mode ($IT/\overline{PLS_2}=0$)

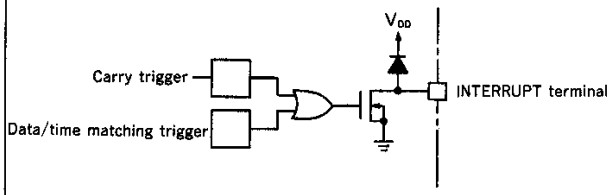


③ Constant periodic and alarm interrupt modes ($IT/\overline{PLS_{1,2}}=1$)



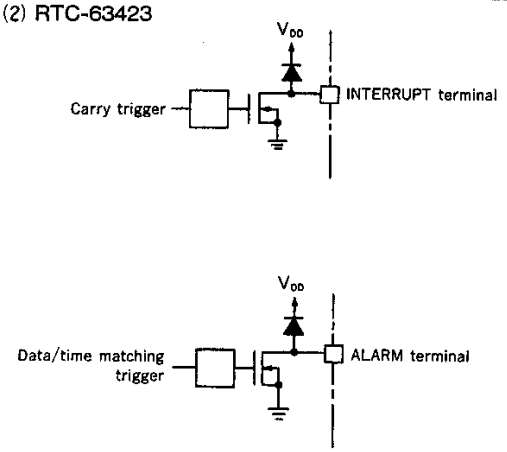
9. Internal block diagram of the INTERRUPT and ALARM terminals

(1) RTC-63421/63421M



INTERRUPT OUT and ALARM OUT are ORed and output.

(2) RTC-63423



■Register explanation

1. Time and calendar realtime registers

(1) Each of these registers is in the BCD code, and its logic is positive.

(2) R-W (Week registers)

Encode them for use.

Example:

Data	0	1	2	3	4	5	6
Day of the week	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

(3) R-H_1, R-H_{10}

Depending on the setting of the 24-hour system/12-hour system (C_E registers), a different time may exist. When the 12-hour system has been established, r-PM/$\overline{AM}$ must be set. When the 24-hour system is selected, the r-PM/$\overline{AM}$ bit automatically becomes "0".

24/$\overline{12}$ bit	Time which can exist
0 (12-hour system)	Time in 12:00am to 11:59am and 12:00pm to 11:59pm
1 (24-hour system)	00:00 to 23:59

(4) R-Y_1, R-Y_{10}

These registers use the Gregorian calendar. Leap years are automatically recognized. (A year whose lower two digits are a multiple of four is recognized as a leap year.)

Example: 92, 96, 00, 04, 08, 12

(5) CAL bit determines the counting-up rang of the alarms; CAL=0.

(6) Notice is for R-D_1 to R-Y_{10}. When registers marked with * are used as the RAM, read/write are enabled.

① Setting the time and calendar not contained in the registers used as the real-time registers may cause a counting error. Data out of range for the time and calendar must not be set.

② Bits marked with * used as real-time registers (CAL=1) are automatically set to "0" at read even when they have been set to "1".

2. C_D register (control register D)

(1) $MASK_1$ (D_0)

① This bit control the constant periodic output trigering the clock counter carry. The period can be set by CY_2, CY_1, or CY_0.

Relation between $MASK_1$ and constant periodic output.

$MASK_1$ bit	IT/$\overline{PLS_1}$ bit	INTERRUPT terminal	Remarks
0	1	Constant periodic interrupt mode	The period can be set by CY_2, CY_1, or CY_0.
	0	Constant periodic pulse output mode	
1	Don't Care	Open	

(2) $MASK_2$ (D_1)

① This bit control the alarm output trigerring the match between the specified alarm date/time and the clock counter. The alarm specification can be set by using the A.ENB register.

○ Relation between $MASK_2$ and alarm output

$MASK_2$ bit	IT/$\overline{PLS_2}$ bit	INTERRUPT or ALARM terminal	Remarks
0	1	Alarm interrupt mode	Alarm output of RTC-63421/63421M (18 pin type) is sent at the INTERRUPT terminal; alarm output of RTC-63423 (24 pins type) is sent at the ALARM terminal.
	0	Alarm pulse output mode	
1	Don't Care	Open	

(3) IT/$\overline{PLS_1}$ (INTERRUPT/$PULSE_1$) (D_2)

This bit determines the output mode for the constant periodic output. Setting this bit to "1" enables the interrupt mode; setting this bit to "0" enables the pulse mode.

(4) IT/$\overline{PLS_2}$ (INTERRUPT/$PULSE_2$) (D_3)

This bit determines the output mode for the alarm output. Setting this bit to "0" enables the interrupt mode; setting this mode to "0" enables the pulse mode.

3. C_E register (contorol register E)

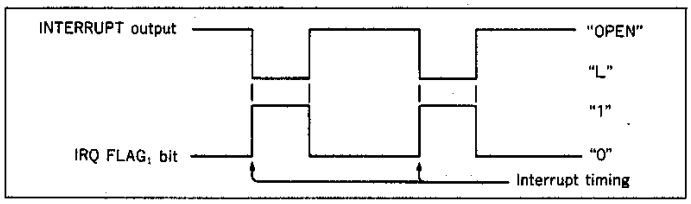
(1) IRQ $FLAG_1$ (INTERRUPT REQUEST $FLAG_1$) (D_0)

The IRQ $FLAG_1$ has two functions.

① This bit indicates the constant periodic interrupt request mainly for the microprocessor. The bit synchronizes with the INTERRUPT output.

○ Relation between INTERRUPT output and IRQ $FLAG_1$

INTERRUPT output	IRQ $FLAG_1$
L (Open→L)	1 (0→1)
OPEN (L→Open)	0 (1→0)



② Clearing this bit

I) Constant periodic interrupt mode

Reading this bit clears this bit (IRQ $FLAG_1$ = 0) and resets the INTERRUPT output (INTERRUPT output = Open). When the D.P. bit (D_0 of register C_E') is 1, reading this bit after an interrupt has occurred cannot immediatley clear the bit. It is only cleared after 122μs elapses after the interrupt has occurred.

II) Constant period pulse mode

Writing "0" to this bit clears this bit (IRQ $FLAG_1$ = 0) and resets the INTERRUPT output (INTERRUPT output = Open). Note that this bit is automatically return through the period timing set by $CY_{0\,to\,2}$ ($D_{0\,to\,2}$ of Register C_D) without writing "0" to this bit.

Clearing the IRQ FLAG bit

$IT/\overline{PLS}_1$ bit	The IRQ $FLAG_1$ bit setting	IRQ $FLAG_1$ bit output	Remarks
1	Reading IRQ $FLAG_1$	1→0 (cleared)	When D.P. = 1, this bit is not cleared 122μs after an iterrupt has occurred.
0	Writing "0" to IRQ $FLAG_1$		This bit may be automatically returned by the set period timing.

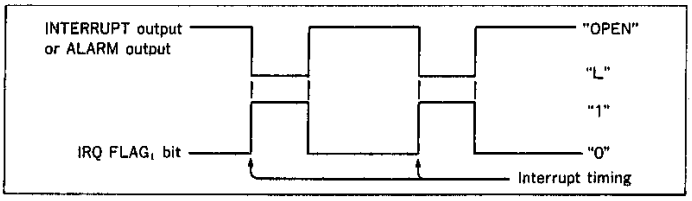
(2) IRQ $FLAG_2$ (INTERRUPT REQUEST $FLAG_2$) (D_1)

The IRQ $FLAG_2$ has two functions

① This bit indicates the alarm timer interrupt request mainly for the microprocessor. The bit synchoronizes with the INTERRUPT output for RTC-63421/63421M and the ALARM output for RTC-63423.

INTERRUPT output for or ALARM output *	IRQ $FLAG_2$
L (Open→L)	1 (0→1)
OPEN (L→Open)	0 (1→0)

* INTERRUPT output for RTC-63421/63421M
ALARM output for RTC-63423



② INTERRUPT output or ALARM output

Clearing this bit

I) Alarm interrupt mode

Reading this bit clears this bit (IRQ $FLAG_1$ = 0) and resets the INTERRUPT output (INTERRUPT output = Open or ALARM output = Open). When the D.P. bit (D_0 of register C_2) is 1, reading this bit after an interrupt has occurred cannot immediatley clear the bit. It is only cleared after 122μs elapses after the interrupt has occurred.

II) Alarm pulse mode ($IT/\overline{PLS_2}=0$)

Writing "0" to this bit clears this bit ($IRQ\ FLAG_2=0$) and sets the INTERRUPT output. (INTERRUPT output = Open). Note that this bit is automatically return after approximately 61μs after an interrupt has occured without writing "0" to this bit.

Clearing the IRQ FLAG bit

$IT/\overline{PLS}$ bit	$IRQ\ FLAG_2$ bit setting	$IRQ\ FLAG_2$ bit output	Remarks
1	Reading $IRQ\ FLAG_2$	1→0 (cleared)	When D.P. = 1, this bit is not cleared 122μs after an interrupt has occurred.
0	Writing "0" to $IRQ\ FLAG_2$		This bit may be automatically return after approximately 61μs after an interrupt has occurred.

(3) RESET (D_2)

① This bit resets the less than one second counter. The bit is kept reset during RESET=1. Reset is released by writing "0" to this bit. (When the CS_1 is set to "L", this bit is automatically released.)

(4) $IRQ\ FLAG_0$ (INTERRUPT REQUEST $FLAG_0$) (D_3)

This bit indicates whether the time is an extention (122μs) for the interrupt output in the D.P. bit=1.

This bit is not cleared by reading. This bit cannot be written.

$IT/\overline{PLS_1}$ or $IT/\overline{PLS_2}$	D.P.	$IRQ\ FLAG_0$ state
1	1	This bit is set to "1" for the time within 122μs (the extention zone) after an interrupt has occurred; the bit is automatically returned after 122μs has elapsed (set to "0").
Don't Care	0	0
0	Don't Care	0

4. C_F register (Control register F)

(1) READ FLAG (D_0)

This bit indicates the carry from the one-second digit and used to read the time data.

This bit is set to "1" when a carry occurs. Reading the bit releases the setting (sets this bit to "0").

This bit is setting set to "1" at a 30-seconds correction operation.

Condition	READ FLAG	Reading of $R\text{-}S_1$~R-W (see page 18)
Read of this bit	0	Read of enabled
Carry from the one-second digit and 30-seconds correction	1	Clear this bit (read this bit), then read $R\text{-}S_1$~R-W again.

(2) 30-seconds ADJ (30-seconds ADJUSTMENT) (D_1)

① This bit is used for 30-seconds correction writing "1" to this bit enables 30-seconds correction.

State of the second digit before correction	State of the second digit after correction
29 seconds or less	"0" second without a carry from the one-minute digit
30 seconds or more	"0" second with a carry from the one-minute digit

② For 250μs, the bit is automatically return before conducting read/write of the time registers. This does not apply when the time registers $R\text{-}D_1$ to $R\text{-}Y_{10}$ are used as the RAM. When 30-seconds correction is completed, the READ FLAG is also set to "1".

③ For only RTC-64323

This bit is also set to "1" when 30-seconds correction is conducted by the hardware.

(3) STOP (D_2)

① Writing "1" to this bit stops counting at 4096Hz or more; writing "0" to this bit restarts counting.

② For only RTC-62423

The $HD/\overline{SFT}$ (D_3 of the C_E') is also used to select STOP by hardware.

$HD/\overline{SFT}=0$	Software
$HD/\overline{SFT}=1$	Hardware

(4) $BANK_1/\overline{BANK_0}$ (D_3)

This bit selects resister BANK. When this bit is "0", $BANK_0$ is selected; when this bit is 1, $BANK_1$ is selected.

Write to this bit is executed even in the data protect mode.

5. Alarm registers

(1) The registers other than A-W (the day of week register) are in BCD code and the positive logic.

(2) The A-ENABLE register can determine the range of alarm settings (16 settings). (See the item of A-ENABLE.)

(3) $A\text{-}H_1$, $A\text{-}H_{10}$

To establish the 24-hour system, read/write to and from the a-PM/$\overline{AM}$ bit can still be conducted. The bit is assumed to match the r-PM/$\overline{AM}$ bit.

(4) The RAM area of the alarm registers

The registers outside the alarm setting area set by the A-ENABLE register can be used as the RAM areas. These RAM areas can read/write bits marked with *.

(5) Caution

Setting the time and calendar not contained in the registers used as the alarm registers does not generate the normal alarm. Data out of range for the actual time and calendar must not be set.

6. A-ENABLE registers

This register sets the range of collation the real-time counter against the alarm register. All bits of the alarm registers output the collation range can be used as the RAM.

Alarm collation range

	ae_8	ae_4	ae_2	ae_1	Alarm collation range
0	0	0	0	0	————
1	0	0	0	1	$A\text{-}S_1$
2	0	0	1	0	$A\text{-}S_1$ to $A\text{-}S_{10}$
3	0	0	1	1	$A\text{-}S_1$ to $A\text{-}MI_1$
4	0	1	0	0	$A\text{-}S_1$ to $A\text{-}MI_{10}$
5	0	1	0	1	$A\text{-}S_1$ to $A\text{-}H_1$
6	0	1	1	0	$A\text{-}S_1$ to $A\text{-}H_{10}$
7	0	1	1	1	$A\text{-}S_1$ to $A\text{-}D_1$
8	1	0	0	0	$A\text{-}S_1$ to $A\text{-}D_{10}$
9	1	0	0	1	$A\text{-}S_1$ to $A\text{-}MO_1$
A	1	0	1	0	$A\text{-}S_1$ to $A\text{-}MO_{10}$
B	1	0	1	1	$A\text{-}S_1$ to $A\text{-}H_{10}$, A-W
C	1	1	0	0	$A\text{-}S_1$ to $A\text{-}D_1$, A-W
D	1	1	0	1	$A\text{-}S_1$ to $A\text{-}D_1$, A-W
E	1	1	1	0	$A\text{-}S_1$ to $A\text{-}MO_1$, A-W
F	1	1	1	1	$A\text{-}S_1$ to $A\text{-}MO_{10}$, A-W

7. C_C' register (control C' register)

This register is used by Epson to test the system. The user must set both $TEST_1$ (D_0) and $TEST_2$ (D_1) to "0" to operate the system. The user function with the TEST bit=1 is not guranteed.

To clear this register, write "1" to the RESET bit (D_2 of the C_E) or, read once this register to set the register to "0".

The contents of the read value of this register are not determined.

8. C_D' register (control D' register)

This register sets the period of the constant periodic pulse (IT/$\overline{ST_1}$=0) and constant periodic interrupt (IT/$\overline{ST_1}$=1).

Relation between each bit and the period.

CY_2	CY_1	CY_0	Period	Time (duty) when INTERRUPT output in the automatic reset mode of IT/ST_1=0 is in the "L" level.
0	0	0	1/1024 second	Approximately 0.5msec (approx 1/2)
0	0	1	1/128 second	Approximately 3.9msec (approx 1/2)
0	1	0	1/64 second	Approximately 7.8msec (approx 1/2)
0	1	1	1/16 second	Approximately 31.3msec (approx 1/2)
1	0	0	1/2 second	Approximately 250.0msec (approx 1/2)
1	0	1	1 second	Approximately 61.0msec (approx 1/8,192)
1	1	0	1 minute	Approximately 61.0msec (approx 1/491,520)
1	1	1	10 minutes	Approximately 61.0msec (approx 1/4,915,200)

9. C_E' register (control E' register)

(1) HD/$\overline{SFT}$ (HARDWARE/SOFTWARE) (D_3). Valid only for RTC-63423.

① This bit determines whether the hardware (the STOP/$\overline{START}$ terminal) or the software (the STOP bit) is to be made effective, in the STOP/$\overline{START}$ and 30-seconds correction functions.

HD/$\overline{SFT}$ bit	Signification
1	Hardware (STOP/$\overline{START}$ terminal) is effective.
0	Software (STOP bit) is effective.

② Cautions

a) RTC-63421M cannot use both STOP/$\overline{START}$ function. Reading/writing this bit is available, but the bit is automatically assumed to be "0" by the system.

b) The STOP/$\overline{START}$ function cannot be used simultaneously for hardware and software.

(2) 24/$\overline{12}$ (24-hour system/12-hour system)

① This bit selects the 24-hour system or 12-hour system.

24/$\overline{12}$ bit	Signification
1	24-hour system (PM/$\overline{AM}$ automatically becomes "0".)
0	12-hour system (PM/$\overline{AM}$ must be set.)

② Cautions

Rewriting this bit may destroy data at R-H_1 or more.

After rewriting this bit, newly write data at R-H_1 or more.

(3) CAL (CALENDAR) (D_1)

① This bit specifies the range of counting up the real-time counters.

CAL bit	Counting up range
1	R-S_1~R-Y_{10} and R-W
0	R-S_1~R-H_{10} and R-W

② When this bit is 0, the R-D_1 to R-T_{10} may be used as a SRAM.

③ When this bit is 0, the alarm collation range for the R-D_1 to R-Y_{10} is assumed to be always matched.

(4) D.P. (DATA PROTECT) (D_0)

This bit has two functions.

① Disabling write to the register (to protect data)

* Setting this bit to "1" inhibits write to the register except to the BANK 1/0 (D_3 of the C_F register).
* This bit is intended to protect data against external noise, particularly incorrect write generated during shift to stand-by or exit from stand-by. To achive this, it is recommended to keep this bit at "1" when the read operation is not conducted.

② Inhibiting IRQ FLAG reset

* When this bit is 1, IRQ $FLAG_1$ or IRQ $FLAG_2$ is not cleared by reading it before 122μs, elapses from the interrupt occurrence timing. After 122μs, each of the IRQ FLAG is cleared. (See the timing for IRQ $FLAG_1$ and IRQ $FLAG_2$.)
* When the IRQ FLAG is read after approximately 122μs elapses from the interrupt occurrence timing, the IRQ FLAG is immediately cleared.

Supplement:

What 122μs is for: The setting is to prevent an interrupt from being cleared even when IRQ $FLAG_1$ or IRQ $FLAG_2$ is accidentally read by signal noise generated when using the interrupt signal to changing over to the stand-by voltage or system voltage.

③ Notes

a) Writing "1" to this bit is unsuccessful under the conditions:

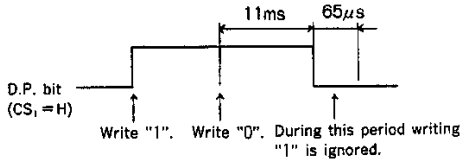
A. CS_1 = "L"

B. 65μs after rewriting this bit from "0" to "1".

b) Writing "0" to this bit is unsuccessful under the conditions:

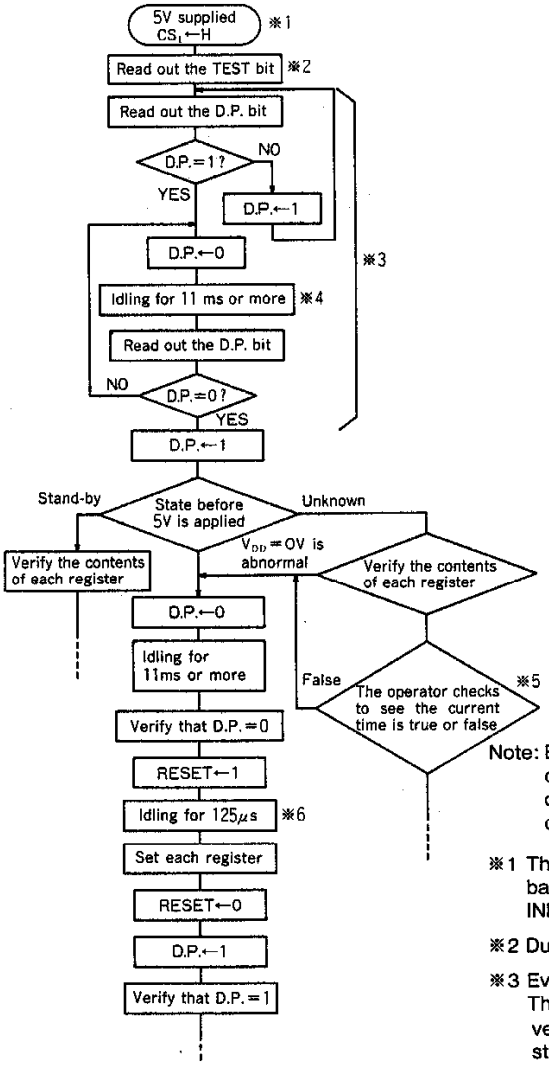
A. Within 2 ms after both CS_1 and CS_2 at "L" become "H".

B. Within 11 ms after writing "0" to this bit.

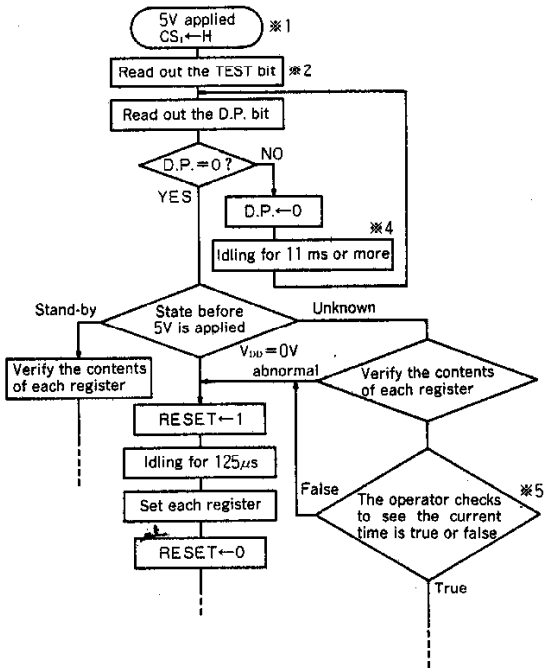


(1) Example of definition between the power on (initialization).

① When the D.P.=1 is used



② When the D.P.=0 is used



Note: Before the D.P. is set to "0", oscillation (count-up) has been done. When V_{DD} increases from 0V to 5V (at the initial power on), it takes 0.2 to 1 second until oscillation starts, depending on the time.

※1 The activities below are not needed when returning from the backup. When the power is turned on, all registers and the INRERRUPT and ALARM outputs are undefined.

※2 Dummy reading to reset the TEST bit.

※3 Even at D.P.=1, writing the BANK1/0 bit and D.P. bit is possible. Therefore, the complicated setting steps must be taken to prevent the D.P. bit from being set to "0" while the unstable power state of supplying 5V, and also to enable the D.P. bit to be set to "1" if write is conducted.

※4 It takes 9 to 11ms for D.P.=0 obtained in the RTC after writing "0" to the D.P. (oscillation must have started)

※5 To decided the state is the return from the backup or the initial power-on, as many register contents as possible should be checked. This decreases the probability of accident.
The chart omits D.P.=0 verification and the following D.P.=1 verfication loop.

※6 Wait time for a carry which has been generated to complete.

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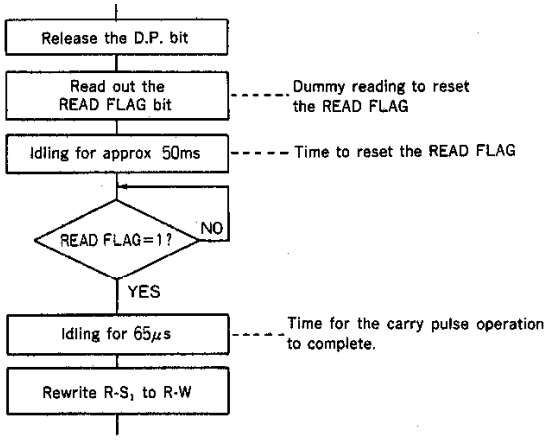
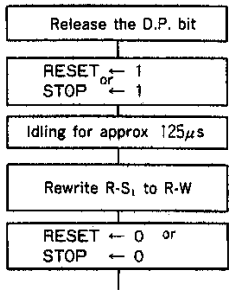
(2) Exmaple of rewriting the R-S_1 to R-W registers

① Example of rewriting the registers by using the READ FLAG



② Example of rewriting the register by the STOP or RESET bit.



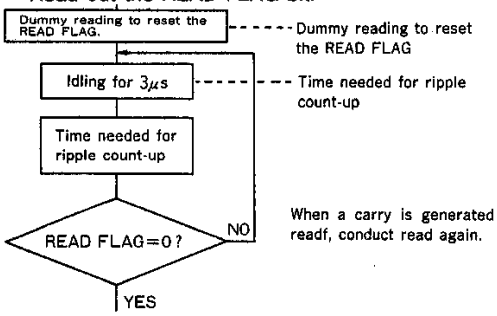
Wait time for a carry which may have been generated before setting the RESET or STOP bit to complete.

Note: In this writing, counting is delayed by reset of the less than one second counter and by counting stop.

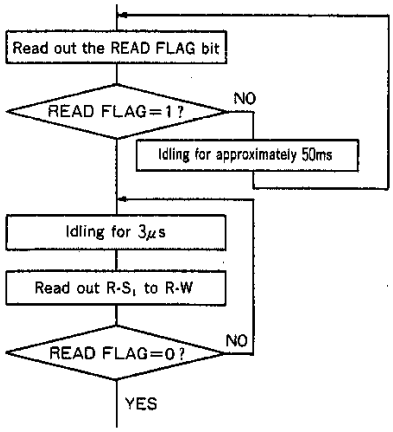
Note: This rewriting method is successful only when rewrite is completed before the next carry occurs.
(Time from the 50 ms idling to the R-S1 to R-W rewrite completed <1 second)

(3) Example of reading the R-S_1 to R-W registers

① Example of reading the registers at a desired time Read out the READ FLAG bit.

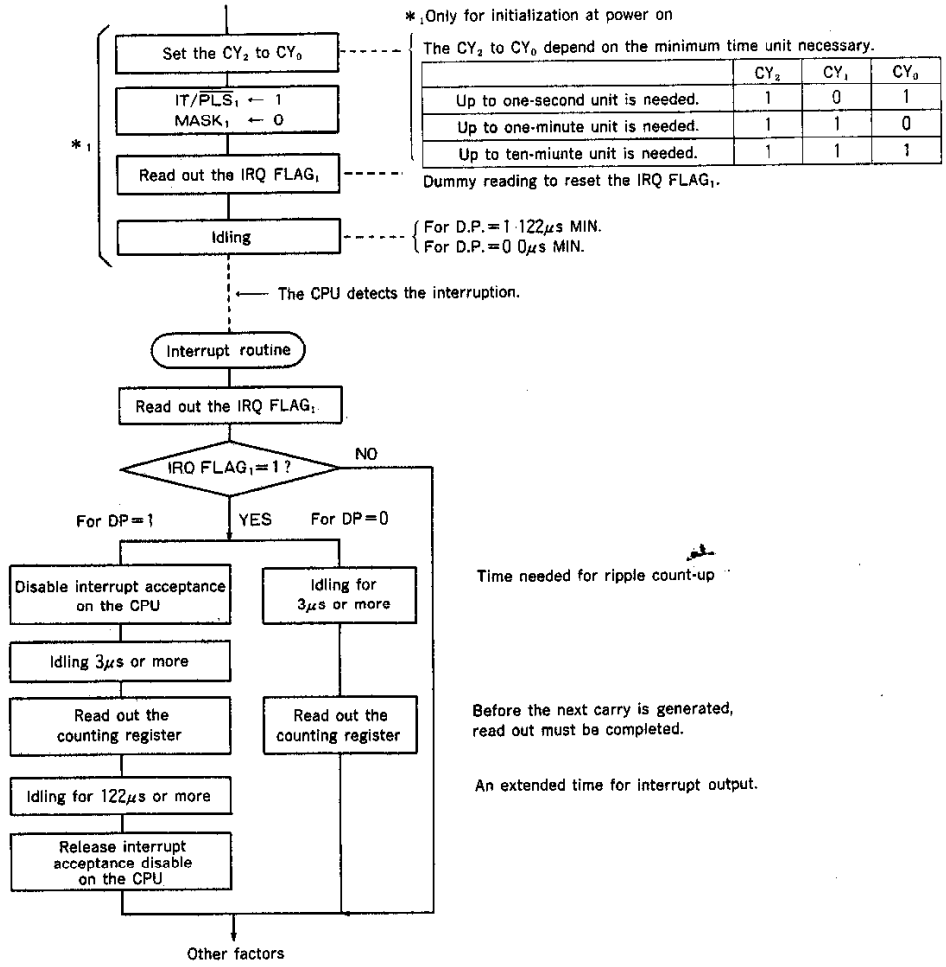


② Example of reading the registers by polling Read out READ FLAG bit.



Supplement: To avoid unnecessary frequent READ OUTs, we recommend it to use the method ② or ③.

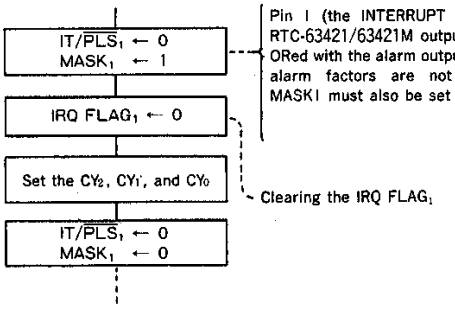
(4) Example of periodic reading



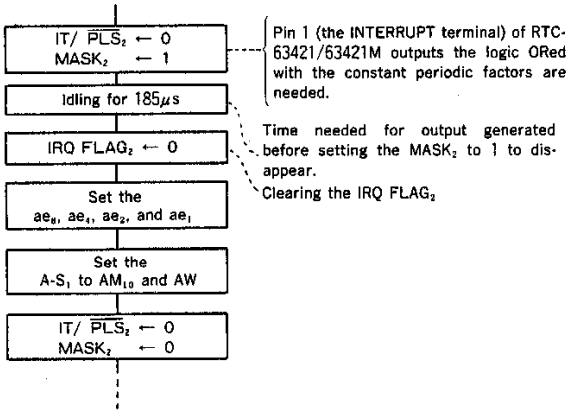
	CY2	CY1	CY0
Up to one-second unit is needed.	1	0	1
Up to one-minute unit is needed.	1	1	0
Up to ten-miunte unit is needed.	1	1	1

(5) Example of setting the periodic pulse output
(The chart omits the methods to release and set the D.P. bit.)

① Constant periodic pulse output



② Alarm pulse output



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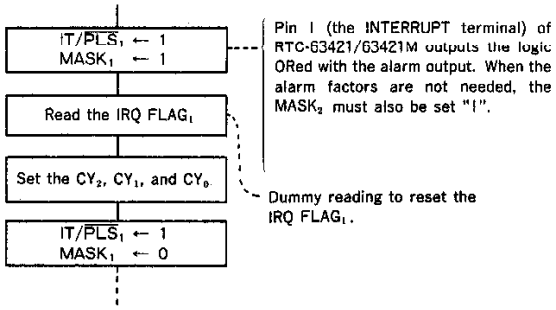
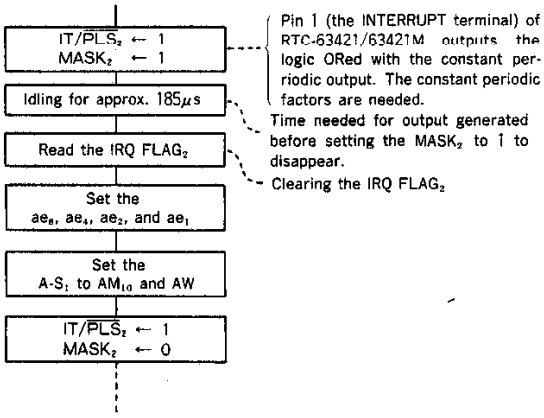
(6) Example of setting the interrupt output
(The chart omits the methods to releases and set the D.P. bit.)

① Constant periodic interrupt output

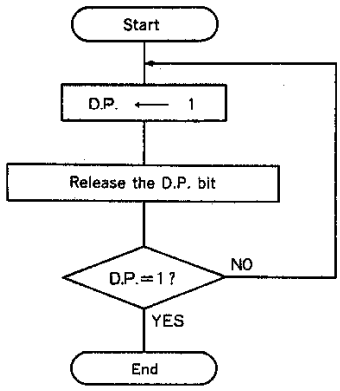


② Alarm interrupt output

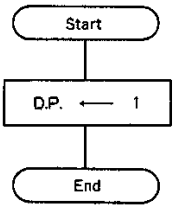


(7) Setting the data protect

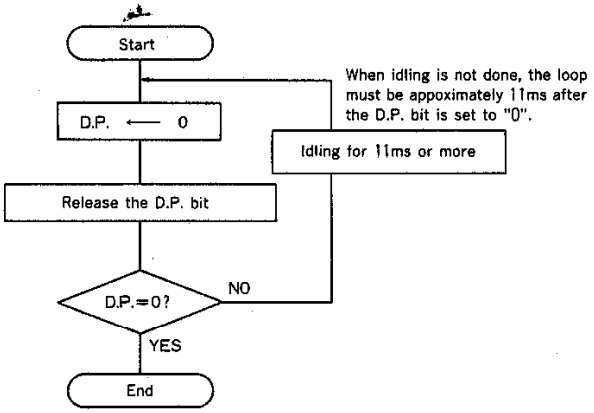
① Immediately after the D.P. bit is rewritten from "1" to "0" (within 65μs)



② More than 65μs after the D.P. bit is rewritten from "1" to "0"

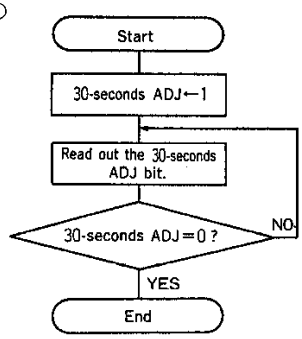


(8) Releasing the data protect

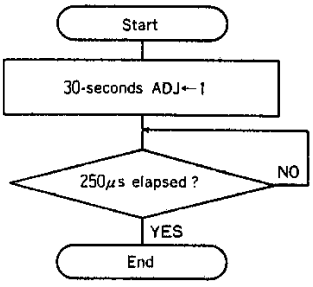


(9) Writing the 30-seconds ADJ bit

①



②



250μs is the maximum time needed for the 30-seconds ADJ bit, provided that oscillation has been started.

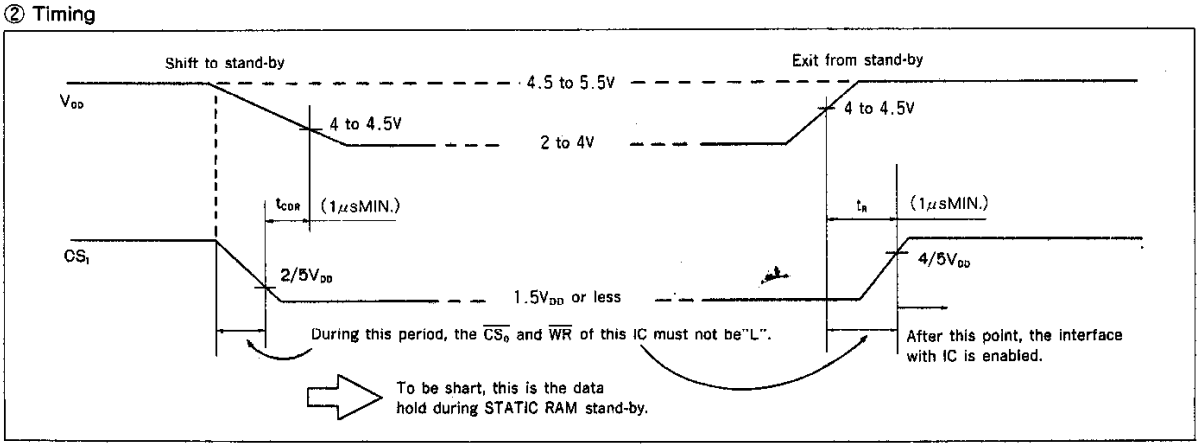
(10) Using the CS_1

① V_{IH} and V_{IL} of the CS_1 have three functions:

- Making the interface to the microprocessor effective when 5V is supplied.
- Saving current consumption during stand-by. (preventing through current specific to the C-MOS input)
- Protecting data during stand-by to execute these functions.
- Therefore you observe below necessary.
- Input $4/5V_{DD}$ or more for the interface to the microprocessor when 5V is supplied.
- Prevent through current by applying voltage as close to 0V as possible during stand-by.
- Observe the time chart below when shifting to or exiting from the stand-by state.

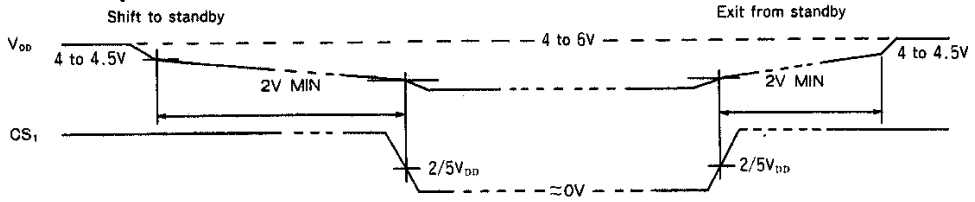
※The stand-by state means the supply voltage of 4.5-2V, the minimum value of the operating supply voltage. During this state, clocks are operating, but the interface to equipment outside the IC is not guaranteed.

② Timing



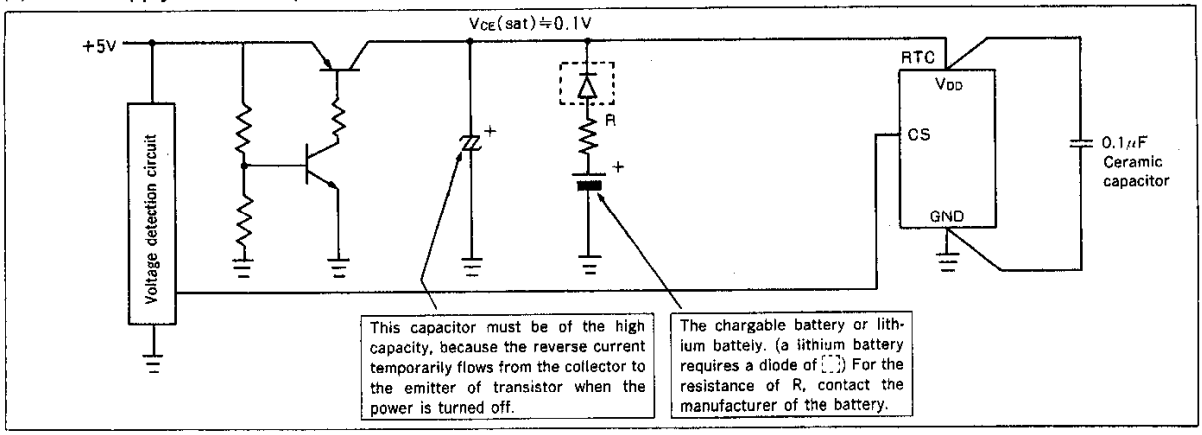
③To protect data against the incorrect write generated at shirt to stand-by or exit from stand-by, write "1" to the D.P. bit before starting the write operation. The timing above must be obeserved.

④ D.P.=1 has always been set



Note: As described in ③, incorrect data may be written at this timing when D.P.=0. Design your circuit to obtain the timing in ②, if possible.

(11) Power supply circuit sample



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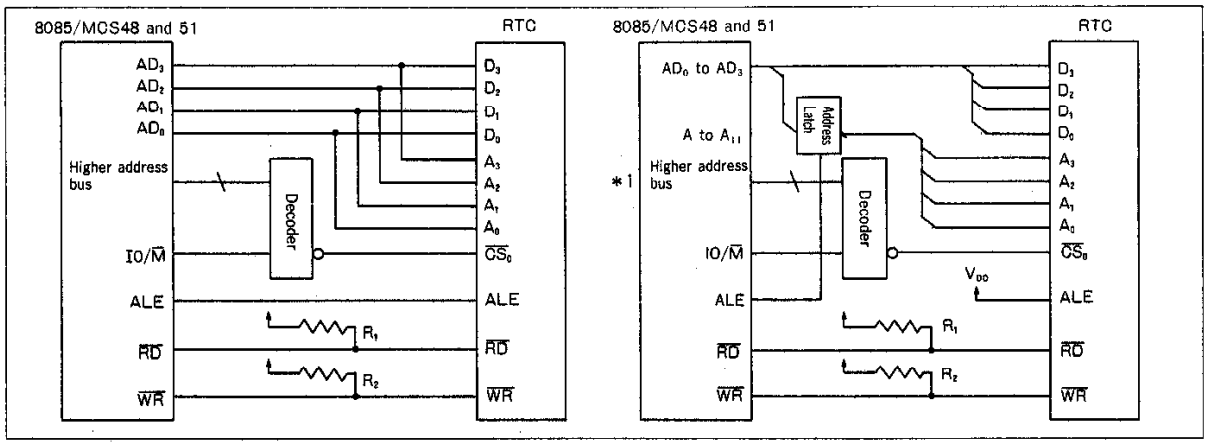
(12) Example of connecting the RTC to the microprocessor

① For the bus of multiplexers.



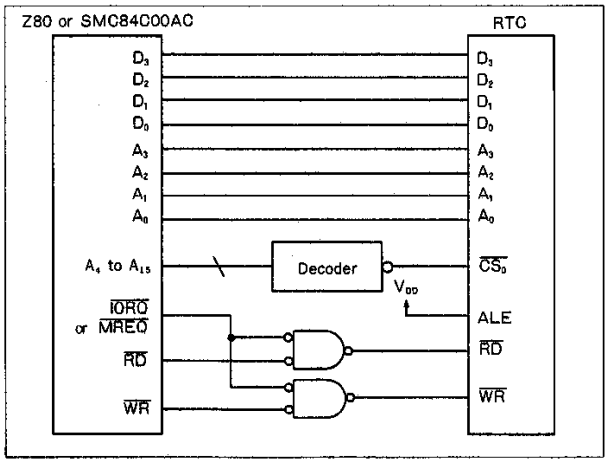
Note: 1. S_1 and S_2 of the decoder are not used unless the memory address of the program is overlapped with the address of RTC-6342 series.

2. IO/$\overline{M}$ of the decoder is not used unless the address of RTC-6342 series is overlapped with other addresses.

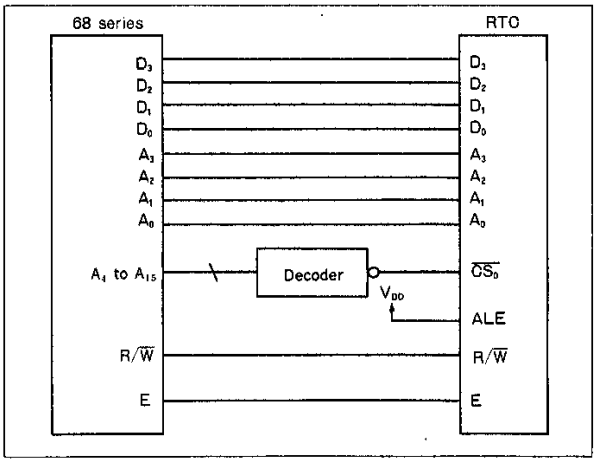
3. R_1 and R_2 are not used unless 8085 is in the HALT or HOLD state during CS_1 = "H" of RTC-6342 series.

*1 Address is not necessary when use I/$\overline{O}$ mapping system.

② For the bus of the Z80 series



③ For the bus of the 68 series



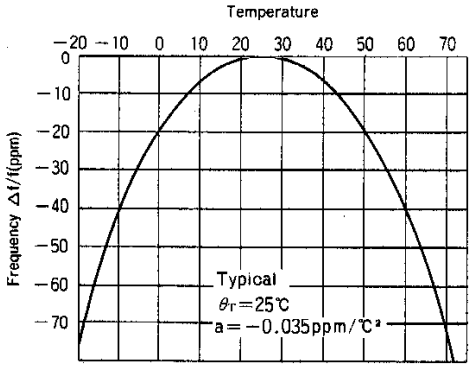
Note: Decide which is used, IORQ or MREQ, depending on what clock is used for Z80.

*The 8-bit microprocessor compatible with SMC84C00AC or Z80A.

RTC-63421/63421M/63423

■Reference data

(1) Example of frequency/temperature characteristics



How to determine frequency stability (clock error)

① The frequency temperature characteristics can be approximated by the expression below : $\Delta f_T(ppm) = a(\theta_T \times \theta_X)^2$

Δf_T(ppm)	: Frequency deviation at any temperature
a(ppm/℃²)	: Secondary temerature coefficient (−0.035±0.005ppm/℃²)
θ_T(℃)	: Peak temperature (25℃ ±5℃)
θ_X(℃)	: Any temperature

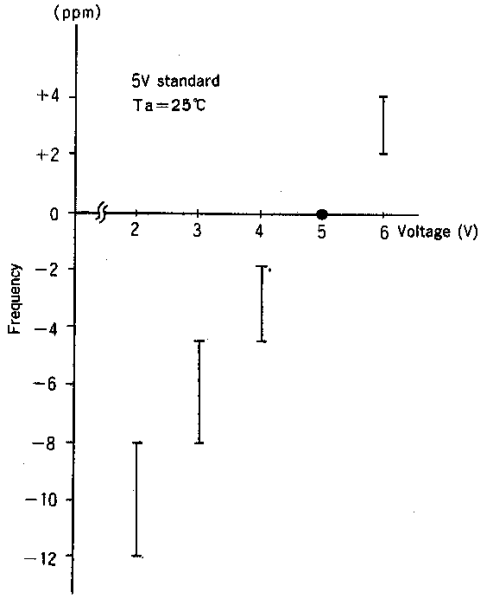
② To determine the clock error (accuracy), add the frequency tolerances and voltage characteristic to the below

$$\Delta f/f(ppm) = \Delta f/f_0 + \Delta f/f_T + \Delta fv$$

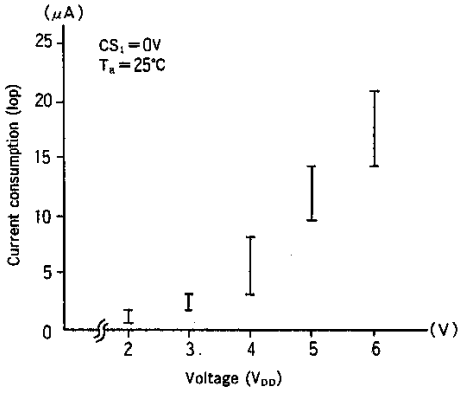
Δf/f(ppm)	: Clock accuracy (frequency stability) at any temperature and voltage
$\Delta f/f_0$(ppm)	: Frequency tolerances
Δf_T(ppm)	: Frequency deviation at any temperature
Δf_V(ppm)	: Frequency deviation at any voltage

③ How to determine the day difference (second/day)
Daily difference(second) = $\Delta f/f \times 10^{-6} \times 86{,}400$(seconds)
The day difference is approximately one second per day, at Δf/f is 11.574ppm.

(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/ voltage characteristics



Note: The data shows the standard values for a sample lot.
For the rated values, see the specifications.

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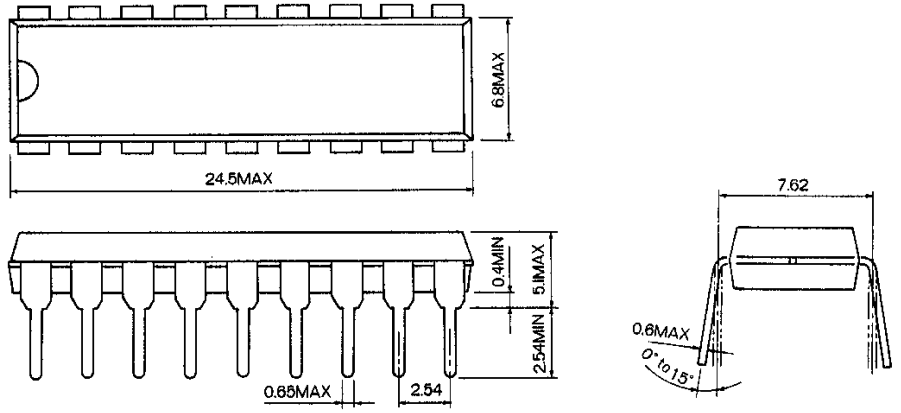
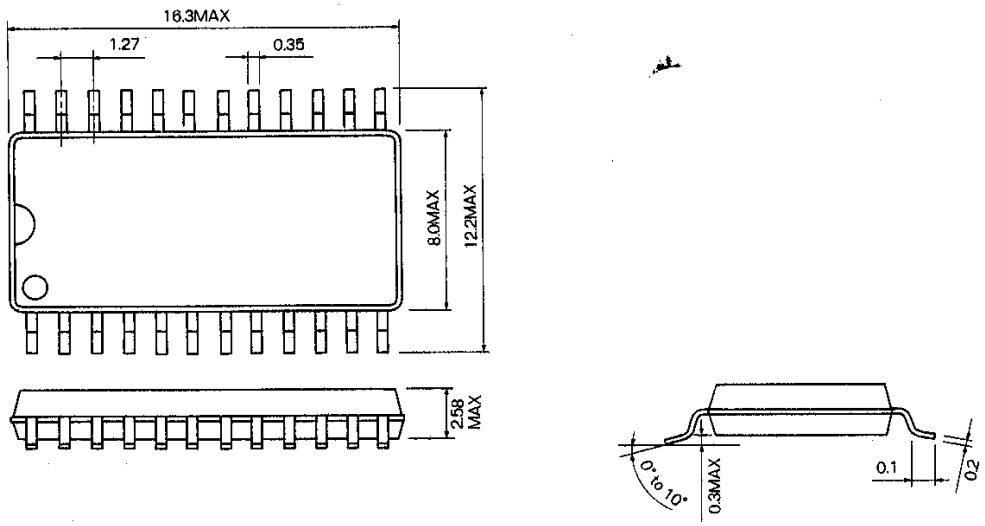
■Overview

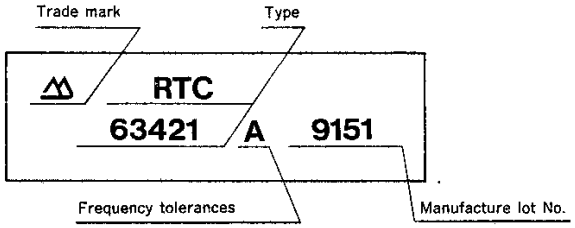
(1) RTC-63421, RTC-63421M



(2) RTC-63423



■Marking loyout



Type	Indication	Tolerances
RTC-63421- RTC-63421M	A	5±10ppm
	B	5±50ppm
RTC-63423	A	5±20ppm
	Not indicated	5±50ppm

Note: The indication above details the markings and outline their positions.
But does not specify the details of the type faces and sizes of characters and their positions.

■ Precautions

(1) This module uses a C-MOS IC for low power consumption. This following precautions shall be taken to ensure that it is not damaged.

① Static electricity

This unit have circuits to protect it from damage caused by static electricity, but exposure to excessive static electricity could damage the IC. Please use conductive packaging or shipping containers. Also, please use grounded soldering irons, measuring circuits, etc. that do not leak.

② Noise

Exposing the power source or input/output terminals to excessive noise could cause malfunctioning or a latch up phenomenon. To ensure stable operation, please attach a by pass capacitor (recommend ceramic type) of at least 0.1μF as close as possible to the module's power-source terminal (between V_{DD}-GND). Please do not place the module near anything that emits high noise.

③ Voltage level of input terminals

Please make the Voltage level settings of input terminals than CS_1 as close to the V_{DD}-GND level as possible, since a mid-level potential setting will cause an increase in current consumption, a decrease in the noise margin, and a deterioration of devices. The V_{IH} of CS_1 is $4/5V_{DD}$: V_{IL} is $1/5V_{DD}$.

Since a Voltage level setting between V_{IH}-V_{IL} of CS_1 will cause a marked increase in current consumption and operation cannot be guaranteed, please take ripple and noise into consideration before setting. (Interface is impossible with TTL.) We suggest driving with a the HC-MOS or Reset function IC.

④ Unused input terminals (with exception of (V_{DD}) terminal)

Because the input impedance of input terminals are extremely high, use in the open state may cause malfunctioning due to unset potential or noise. Therefore, unused input terminals should be either pulled up or down. Further, the NC terminal should be grounded in order to avoid noise. ALE connect to V_{DD} when unused it.

(2) Packaging precautions

① Soldering temperature conditions

I. RTC-63421/63421M

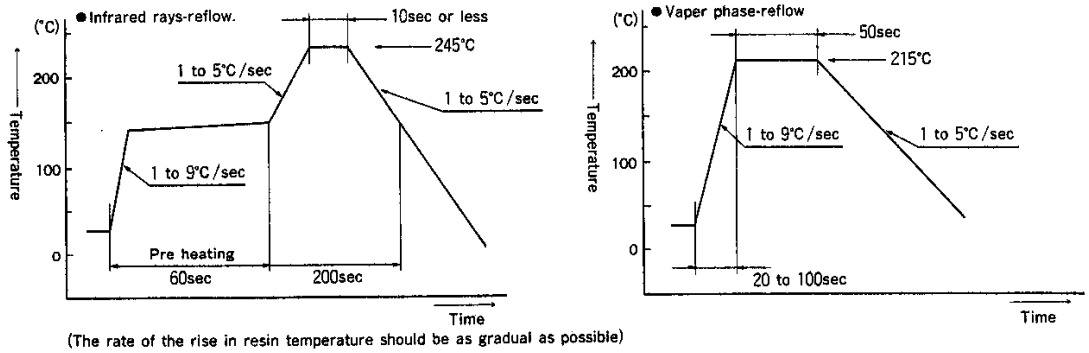
Since solder is used on the quartz crystal, if the temperature inside the package exceeds 150°C, the quartz could deteriorate or be damaged. (Solder conditions: 260°C or less × 10 seconds or less (on the leads only)). Either use a solder dip tank or solder by hand. Please refrain from using vaper, reflow, infrared, etc.

II. RTC-63423

Be certain to check the mounting temperature before mounting the unit, as the quartz crystal could deteriorate and be damaged if the temperature inside the package exceeds 260°C. Also, please check the packaging temperature before using RTC-63423 when conditions change.

(Solder conditions: 260°C or less × 10 seconds or less twice or fewer, or 230°C or less × 3 minutes or less)

Soldering conditions for SMD prnducts



(The rate of the rise in resin temperature should be as gradual as possible)

② Mounting machine

It is possible to use an all-purpose mounting machine's, but please be sure to check the machine's suitability at your company before using it, as physical shocks during mounting could lead to damage of the internal quartz crystal. When there is a change in conditions, please use the machine after making the above-mentioned check.

③ Ultrasonic cleaning

Depending on the conditions, ultrasonic cleaning could cause resonance damage to the quartz crystal.

Since we are unable to determine the usage conditions (type of cleaning unit, power, time, conditions inside the bath, etc.) at our company, we cannot guarantee the safety of this unit when it is cleaned in an ultrasonic cleaner.

④ Mounting direction

This module will be damaged if it is mounted backwards, so please make sure that it is packaged in the correct position.

⑤ Leak between terminals

Since turning on the unit when it is dirty or covered with condensation could lead to leaks between terminals, please clean and dry the module before turning it on.

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Application Manual for RTC-63421/63421M/63423

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SEIKO EPSON CORPORATION
QUARTZ DEVICE DIVISION QD Sales Dept.
8548 Nakaminowa, Minowa-machi,
Kamiina-gun, Nagano-ken, 399-46 JAPAN
Phone: (0265)79-9144 FAX: (0265)79-9492