EPSON

Application Manual

Real Time Clock Module
RTC-65271

SEIKO EPSON CORP.

CONTENTS

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REAL TIME CLOCK WITH S-RAM AND BATTERY HOLDER

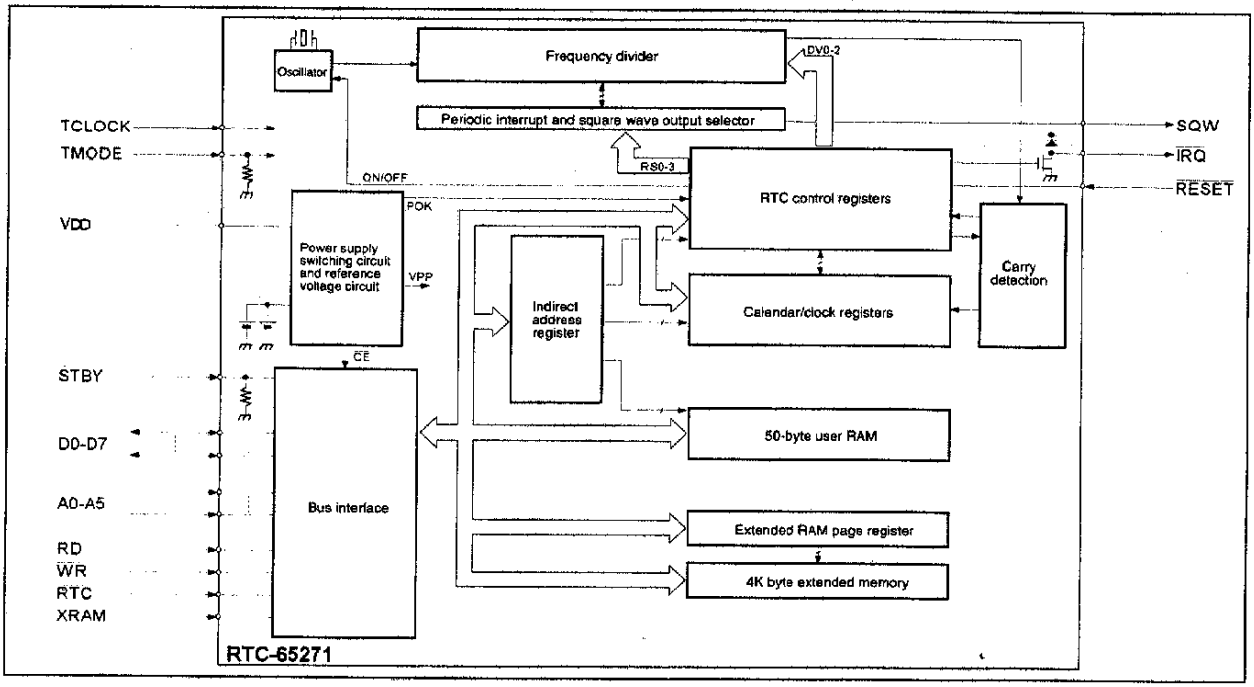
RTC-65271

- Built-in quartz crystal for adjustment-free operation and low mounting cost.
- Battery holder allows battery replacement. Also supports environmental restrictions.
- Ideal for PC/AT® compatible computers.
- Internal power supply switching circuit allows automatic backup of both RTC and S-RAM data.
- Real time clock is functionally compatible with MC146818A and DS1287.
  Indirect address register: 1 byte
  Clock, alarm and calendar registers: 10 bytes
  Control registers: 4 bytes
  User RAM: 50 bytes
- Extended RAM has 4k bytes of built-in S-RAM
  Page register: 1 byte
  RAM configuration:32 bytes x 128 pages = 4k bytes
- The adoption of a nonmultiplex bus allows direct connection to a CPU bus or the external bus of an i386™, i486™ or Pentium™ processor.
- Built-in battery protection resistor (UL-compliant).

Overview

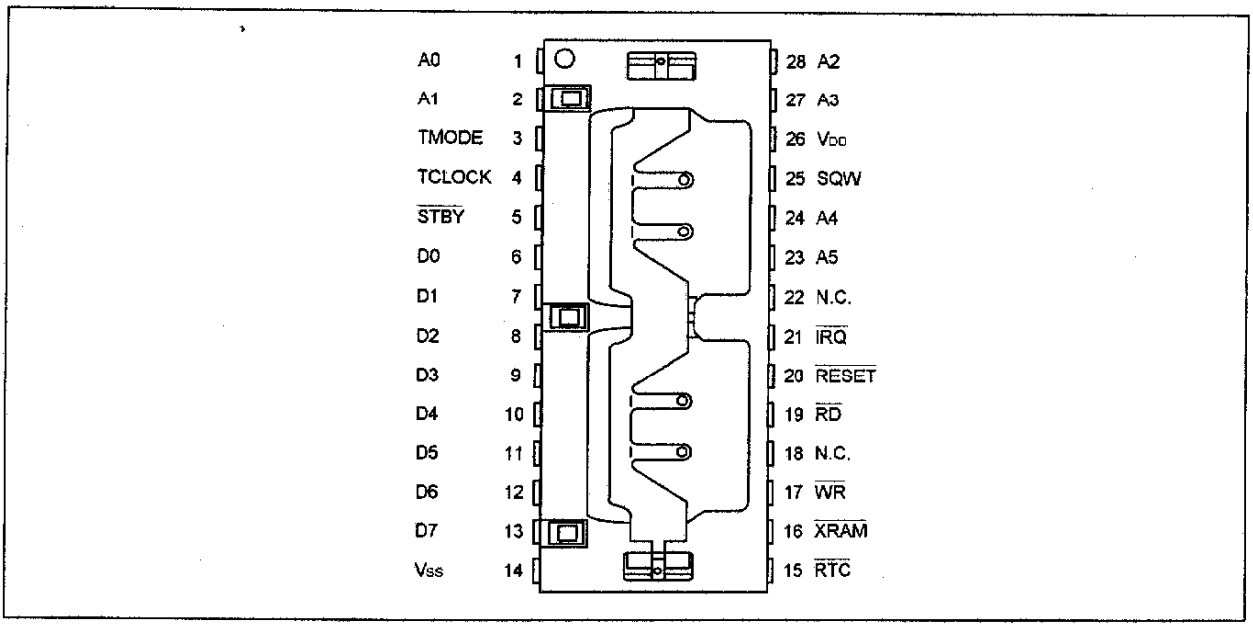
The RTC-65271 is a real time clock module with S-RAM, developed for use in PC/AT® compatible computers and workstations. The built-in quartz crystal provides high accuracy without adjustment, while the absence of any need for external components reduces the cost of incorporation into a system.
The module provides clock and calendar functions, with a daylight saving time function and various periodic reference signal outputs and interrupt functions, and also includes 4k bytes of S-RAM.
Being a C-MOS device, it has a very low power consumption, and the built-in battery holder, together with battery protection resistor and power supply switching function, gives the module an independent fully-automatic backup.

Block Diagram



RTC-65271

Pin Connections



Pin Functions

Pin names	Pin No.	Input/ output	Function
D0-D7 (Data bus)	6-13	Bi-directional	The bi-directional data bus can be connected to a CPU data bus, or PC/AT ISA or EISA bus. This bus is used for all data transfers from and to internal counters and registers. It accesses calendar and clock data when $\overline{RTC}$ is low, and extended RAM data when $\overline{XRAM}$ is low.
A0-A5 (Address bus)	1,2,23,24 27,28	Input	The address bus can be connected to a CPU address bus, or to a PC/AT ISA or EISA bus. When $\overline{RTC}$ is low, it accesses the RTC registers, using A0 to select the indirect address register or RTC data register. In this case A1 to A5 are ignored. When A0 is low (address 0), the indirect address register is selected. When A0 is high (address 1), the RTC data register is selected, and the register accessed is determined by the value in the indirect address register. When $\overline{XRAM}$ is low the extended RAM can be accessed, and A0 to A5 select the extended RAM address or extended RAM page register. When A5 is high (addresses 20 to 3F), the extended RAM page register is selected. When A5 is low (addresses 00 to 1F), the RAM page specified by the extended RAM page register is selected, and A0 to A4 specify the address within that page.
$\overline{WR}$ (WRite)	17	Input	The data value present on D0 to D7 is written to the address specified by either $\overline{RTC}$ or $\overline{XRAM}$ and A0 to A5 on a rising edge on $\overline{WR}$. $\overline{RD}$ and $\overline{WR}$ must not be low simultaneously.
$\overline{RD}$ (ReaD)	19	Input	The data value at the address specified by either $\overline{RTC}$ or $\overline{XRAM}$ and A0 to A5 is output on D0 to D7 while $\overline{RD}$ is low. $\overline{RD}$ and $\overline{WR}$ must not be low simultaneously.
$\overline{STBY}$ (STand BY)	5	Input	When this is low, the device enters the standby state. This inhibits all access, and all outputs are high impedance. Internal clock operation is maintained by the backup battery in the battery holder, and RAM data is also preserved. This pin has an internal pull-down resistor. If not using this pin function, connect to V_{DD}
$\overline{RTC}$ (RTC enable)	15	Input	When this is low the RTC registers can be accessed. If both $\overline{RTC}$ and $\overline{XRAM}$ are low simultaneously, $\overline{XRAM}$ takes precedence, and the RTC registers are not selected.
$\overline{XRAM}$ (eXtended RAM enable)	16	Input	When this is low the extended RAM can be accessed. If both $\overline{RTC}$ and $\overline{XRAM}$ are low simultaneously, $\overline{XRAM}$ takes precedence, and the RTC registers are not selected.
$\overline{IRQ}$ (Interrupt ReQuest)	21	Output	This is an n-channel open drain output, used to issue an interrupt request to the CPU or whatever. In the standby state, or on the backup state, this output is not issued, and the pin remains high impedance. According to the value in register B, this can be used to output an alarm, clock/calendar update completion interrupt, or periodic interrupt. The load voltage should not exceed V_{DD}. If the function is not used, leave this pin open-circuit.
SQW (SQuare Wave output)	25	Output	When output is enabled by the SQWE bit in register B, this pin outputs a square wave signal whose frequency is determined by the value in RS0 to RS3 in register A. In the standby state, or on the backup state, there is no output, and the pin remains high impedance.
$\overline{RESET}$ (RESET rtc)	20	Input	External reset function for RTC. When this pin is low, the RTC registers and signal states become as follows. • Register B bits SQWE, UIE, AIE and PIE, and register C bits UF, AF, PF, and IRQF are all cleared to zero. • The $\overline{IRQ}$ output goes high impedance. • The bus interface is disabled. After powering on the RTC, walt at least 300 ms before using this function. If this function is not used, connect to V_{DD}.
TCLOCK (Test CLOCK)	4	Input	This pin is for testing purposes only. If high, device behavior is not guaranteed. Always hold this pin low.
TMODE	3	Input	This pin is for testing purposes only. It has an internal pull-down resistor. If high, device behavior is not guaranteed. Always hold this pin low or leave open-circuit.
V_{DD}	26		Connect to power supply. For operation, supply between 4.75 V and 5.5 V. If this voltage falls below V_{ENABLE}, writes and reads to the RTC are inhibited. If it falls below V_{SWITCH} the power supply to the RTC is switched from this pin to the backup battery. Provided that a backup battery is fitted, timekeeping functions are maintained, and the RAM data is preserved regardless of the voltage on the V_{DD} pin. Connect a 0.01 to 0.1µF bypass capacitor between this pin and GND. To prevent noise problems, make the connection paths as short as possible, and the line impedance as low as possible.
GND	14		Connect to ground. Connect a 0.01 to 0.1µF bypass capacitor between this pin and V_{DD}. To prevent noise problems, make the connection paths as short as possible, and the line impedance as low as possible.
N.C. (No Connection)	18,22		These pins are not used. Connect to ground.

Battery holder	Use type BR-1225 lithium cells. Ensure that the batteries are fitted before powering on the device. (See pages 19, 26 and 27.)

Characteristics

1. Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply voltage	V_{DD}	V_{DD}-V_{SS}	-0.3	+7.0	V
Input voltages	V_{IN}	Input pins	Vss-0.3	V_{DD}+0.3	V
Storage temperature	T_{STG}	Temperature stored as separate item	-40	+85	°C
Soldering temperature	T_{SOL}	For leads	Maximum 260 °C for up to 10 seconds (package maximum 150 °C)		

2. Operating Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply	V_{DD}	V_{DD}-V_{SS}	4.75	5.0	5.5	V
Operating temperature	T_{OPR}		-10		+70	°C

Use two type BR1255 batteries for backup.

3. Frequency Characteristics

Item	Symbol	Conditions	Max.	Unit
Frequency accuracy	Δf/f0	Ta = 25°C; V_{DD} = 5.0 V	5±20	ppm
Temperature characteristics	tOP	Ta = -10 to 70 °C; V_{DD} = 5.0 V; 25 °C reference	+10 -120	ppm
Voltage characteristics	fv	Ta fixed, 5V reference	±5	ppm/V
Aging	fa	Ta = 25 °C; V_{DD} = 5.0 V	±5	ppm/Year

4. DC characteristics

(V_{DD} = 4.75 V to 5.5 V, Ta = -10 to 70°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltages	V_{IH}		2.2		V_{DD}+0.3	V
	V_{IL}		-0.3		0.8	V
Input leakage currents	I_L	$\overline{RESET}$, $\overline{RD}$, $\overline{WR}$, $\overline{RTC}$, $\overline{XRAM}$, D0 - D7, and A0 - A5			±1	µA
Output voltages	V_{OH}	V_{DD}=5.0V, I_{LOAD}=-4.0mA	2.4			V
	V_{OL}	V_{DD}=5.0V, I_{LOAD}=4.0mA			0.4	V
Power supply current consumption	I_{DD}	*1			15	mA
Current in battery backup state	I_{BAT}	Ta=25°C		0.5	1.0	µA
Current in standby state	I_{STBY}	$\overline{STBY}$ =Vss			2	µA

*1 With no load, SQW output 8.192 kHz, no access

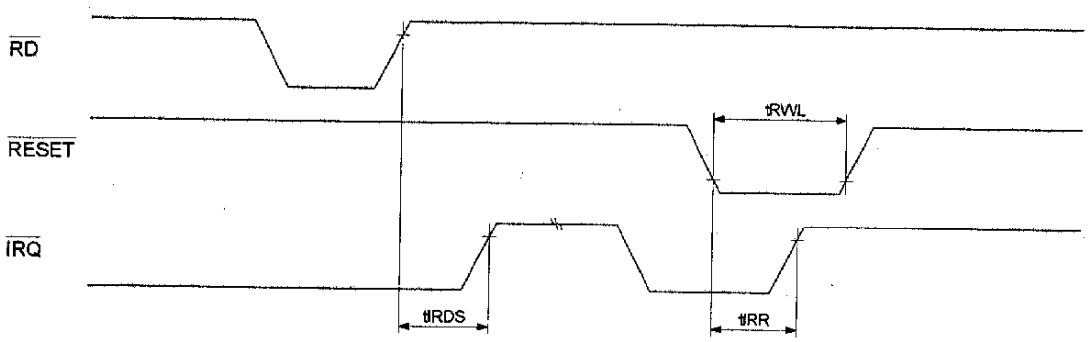
■ Switching Characteristics

1. Switching Characteristics

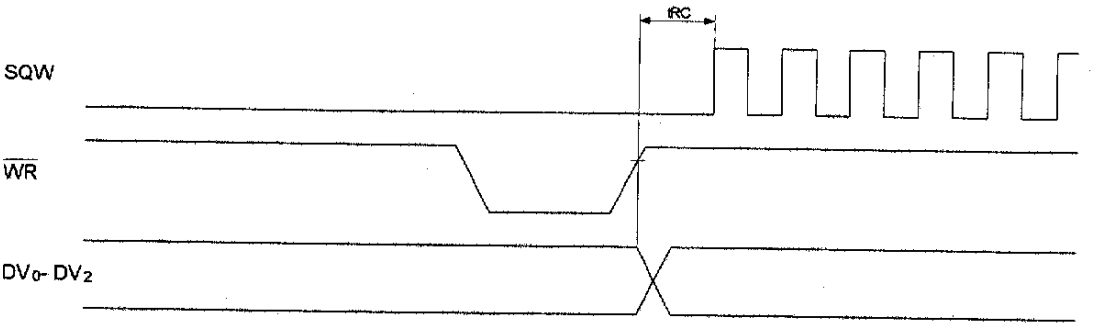
(VDD=4.75V to 5.5V, Ta=-10 to 70°C)

Item	Symbol	Conditions	Min.	Max.	Unit
Reset pulse width	tRWL		5		µs
Oscillation start time	tRC	See diagram below.		1	s
Release time from $\overline{RD}$ to $\overline{IRQ}$	tIRDS			2	µs
Release time from $\overline{RESET}$ to $\overline{IRQ}$	tIRR			2	µs

$\overline{IRQ}$ release delay time



Output start time



Conditions: With RS3 - RS0 set to 0011 (8.192 kHz)Writing 010 (start oscillation) to bit DV in the 000 state (oscillation stopped)

2. Power Supply On/Off Timing

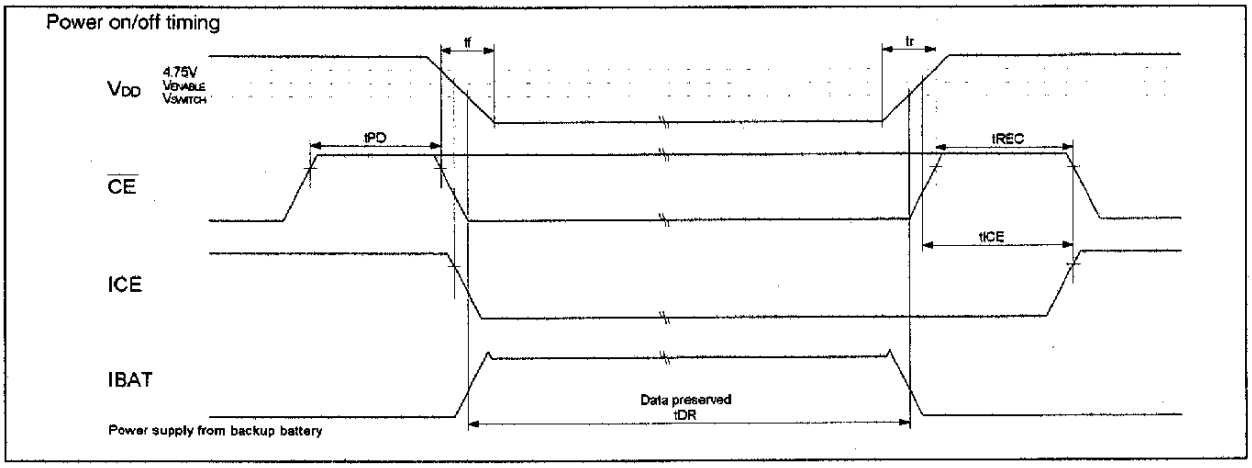
(Ta=-10 to 70°C)

Item	Symbol	Min.	Max.	Unit
Time for $\overline{CE}$ ≥VIH before power off (4.75 V)	tPD	0		µs
Vdd fall time (4.75 V → 0.0 V, $\overline{CE}$ ≤ VIH)	tf	300		µs/V
Vdd rise time (0.0 V → 4.75 V, $\overline{CE}$ ≤ VIH)	tr	100		µs/V
Invalid time for $\overline{CE}$ after power on (4.75 V)	tREC	300		ms
Power supply switching threshold voltage	VSWITCH	VBAT-0.1	VBAT+0.3	V
Chip enable threshold voltage	VENABLE	VBAT×1.25	VBAT×1.35	V
Battery check voltage	VCHECK	2.25	2.75	V
ICE rise time after power on	tICE	20	300	ms

$\overline{CE}$: External chip enable ($\overline{RTC}$ or $\overline{XRAM}$)

ICE: Internal chip enable

Power on/off timing



Power on

After the power supply is applied to VDD, and this voltage reaches the specified VENABLE level, there is then a delay of 300 ms (tICE) maximum before the device can be accessed. At this point, if bits DV0 to DV2 of register A are set to specify oscillation stopped, no clock operation takes place. To start the clock it is necessary to set bits DV0 to DV2, and activate the oscillation circuit. When the oscillation circuit is stopped it takes a maximum of one second before the oscillation of built-in quartz crystal stabilizes.

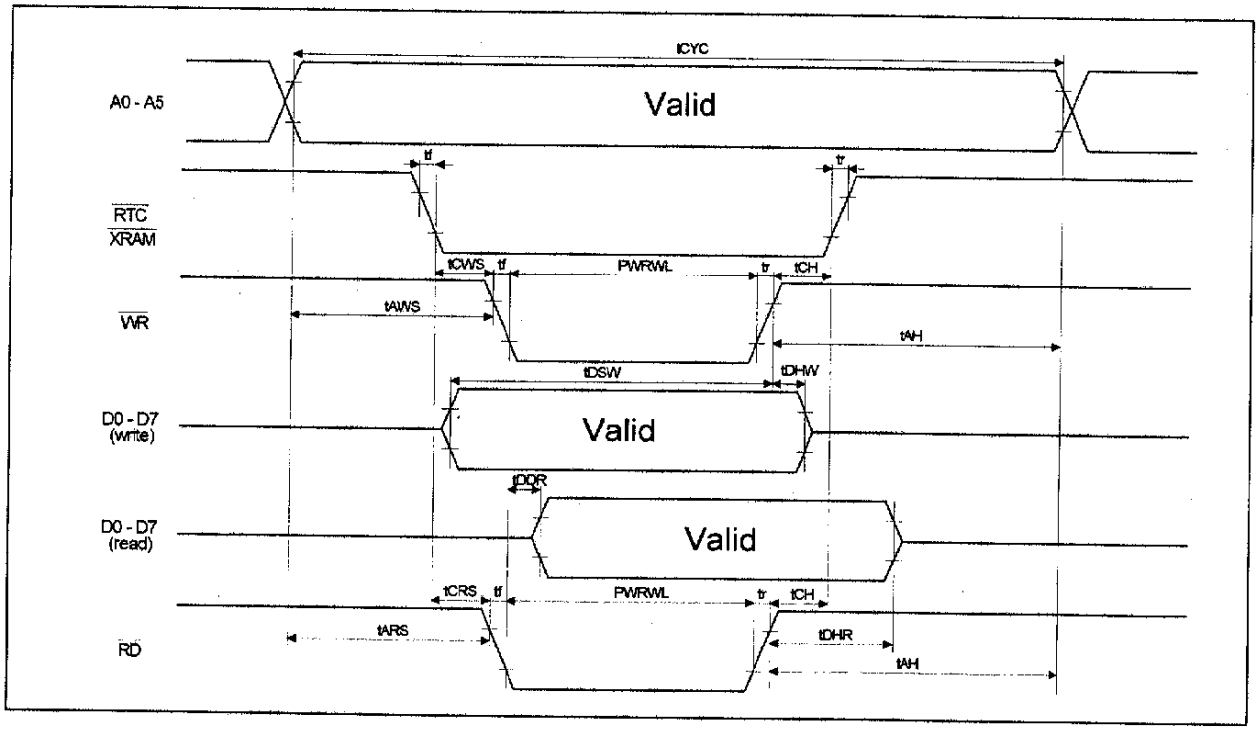
If the voltage supplied to VDD falls below VSWITCH, the power supply switches automatically to the backup battery, and even if VDD falls to zero the clock operations are maintained and the RAM data preserved.
Always ensure that the batteries are fitted before powering on the device.

3. AC Characteristics

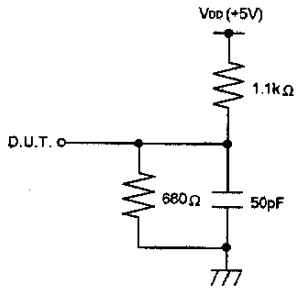
(VDD=4.75V to 5.5V, Ta=-10 to 70°C)

Item	Symbol	Min.	Max.	Unit
Cycle time	tCYC	395	DC	ns
$\overline{RD}$ and $\overline{WR}$ low interval pulse width	PWRWL	325		ns
$\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ signal rise and fall times	tr,tf		30	ns
Address hold time	tAH	20		ns
Address set-up time before $\overline{RD}$	tARS	50		ns
Address set-up time before $\overline{WR}$	tAWS	0		ns
Chip select set-up time before $\overline{RD}$	tCRS	50		ns
Chip select set-up time before $\overline{WR}$	tCWS	0		ns
Chip select hold time after $\overline{RD}$ and $\overline{WR}$	tCH	20		ns
Read data hold time	tDHR	10	100	ns
Write data hold time	tDHW	0		ns
Delay time from $\overline{RD}$ to data output	tDDR	20	240	ns
Write data set-up time	tDSW	200		ns

$\overline{CS}$ and chip select: external chip select ($\overline{RTC}$ or $\overline{XRAM}$)



Output load conditions



Registers

This device has two blocks of registers: one for the RTC functions, and one for the extended RAM functions. To access these it is necessary to make $\overline{RTC}$ low for RTC access and $\overline{XRAM}$ low for extended RAM access, and set the necessary register or memory address to pins A0 to A5. If both $\overline{RTC}$ and $\overline{XRAM}$ are low simultaneously, $\overline{XRAM}$ takes precedence, and the RTC registers are not selected.

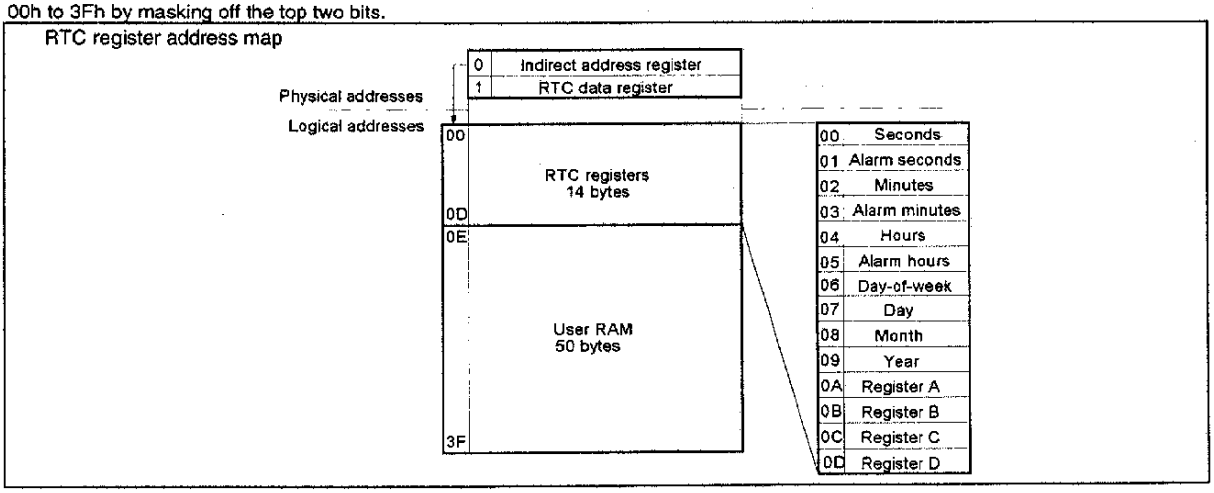
1. RTC Register Address Map

To access an RTC register externally, it is necessary to write the required logical register address in the indirect address register, then carry out the RTC register read or write. When accessing the RTC registers, only A0 of the physical address bits is used.

First, write the logical address of the register to be accessed in the indirect address register. The indirect address register is at physical address 0, so this write is carried out with A0 low. Next, to carry out the read or write to the register at the specified logical address, read to or write from the RTC data register. The RTC data register is at physical address 1, so this read or write is carried out with A0 high.

The internal RTC registers are the same as in the MC146818A and similar devices, with 10 bytes for the clock and calendar registers, 4 bytes of control registers, and 50 bytes of RAM, for a total of 64 logical addresses. Addresses 00h to 3Fh are assigned, but the top two bits are ignored so that these registers are always selected. In other words addresses 40h to FFh are mapped onto addresses 00h to 3Fh by masking off the top two bits.

RTC register address map



2. RTC Register Bit Structure

Address (hexadecimal)	Register name	Data bits D7	D6	D5	D4	D3	D2	D1	D0	Value (binary)	Value (BCD)	Notes
0	Seconds	×	s40	s20	s10	s8	s4	s2	s1	00-3B	0-59	
1	Alarm seconds	*	a-s40	a-s20	a-s10	a-s8	a-s4	a-s2	a-s1	00-3B	0-59	
2	Minutes	#	mi40	mi20	mi10	mi8	mi4	mi2	mi1	00-3B	0-59	
3	Alarm minutes	*	a-mi40	a-mi20	a-mi10	a-mi8	a-mi4	a-mi2	a-mi1	00-3B	0-59	
4	Hours	PM/AM	#	#	h10	h8	h4	h2	h1	01-0C(AM) 81-8C(PM)	01-12(AM) 81-92(PM)	12-hour mode
		#	#	h20	h10	h8	h4	h2	h1	00-17	00-23	24-hour mode
5	Alarm hours	a-PM/AM	*	#	a-h10	a-h8	a-h4	a-h2	a-h1	01-0C(AM) 81-8C(PM)	01-12(AM) 81-92(PM)	12-hour mode
		*	*	a-h20	a-h10	a-h8	a-h4	a-h2	a-h1	00-17	00-23	24-hour mode
6	Day-of-week	#	#	#	#	#	w4	w2	w1	01-07	01-07	
7	Day	#	#	d20	d10	d8	d4	d2	d1	01-1F	01-31	
8	Month	#	#	#	mo10	mo8	mo4	mo2	mo1	01-0C	01-12	
9	Year	y80	y40	y20	y10	y8	y4	y2	y1	00-63	0-99	
A	Register A	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	-	-	
B	Register B	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	-	-	
C	Register C	IRQF	PF	AF	UF	×	×	×	×	-	-	Read only
D	Register D	VRT	×	×	×	×	×	×	×	-	-	Read only
E : 3F	RAM	50 bytes RAM								-	-	

Notes: * This bit is used for alarm ignore settings. It may be read or written 0 and 1. (See page 11 "Alarm registers" and page 18 "Alarm interrupt".)

This bit can be read and written as 0 or 1, but 1 should not be written as it results in a non-existent date or time.

x Empty bit. Always reads as 0.

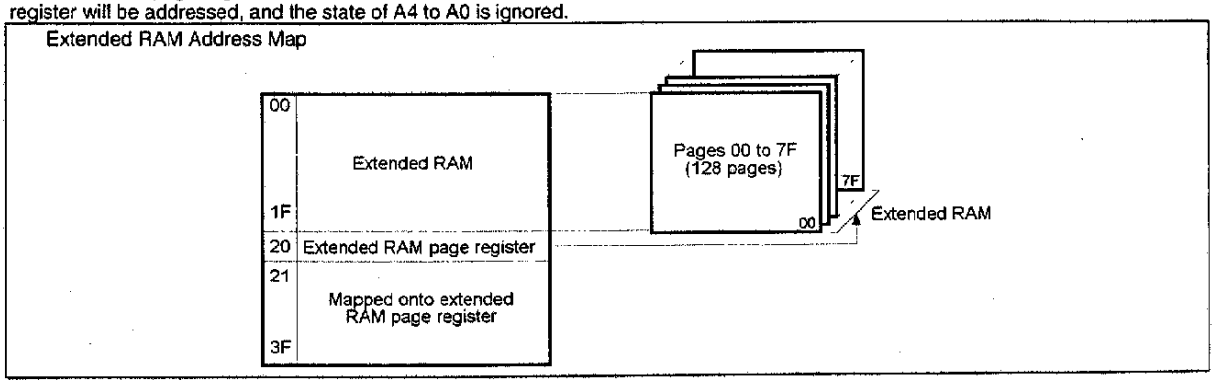
3. RTC Register Bit Functions (Summary)

Bit or register name	Function	See page
Clock and calendar registers	These hold the current date and time, in binary or BCD format as selected by the DM bit. The day-of-the-week is encoded as shown in the following table. Value: 1 Sunday; 2 Monday; 3 Tuesday; 4 Wednesday; 5 Thursday; 6 Friday; 7 Saturday	10
Alarm registers	These hold the alarm generation time: there are three registers for hours, minutes and seconds. To use the alarm function, write the alarm generation time to these registers; if any register has bits 6 and 7 set to 1, that is, a value of 11xxxxxx binary, that register is ignored in determining whether to issue the alarm. In other words, when the alarm register is set to this ignore code, whatever the value of the corresponding time register the alarm conditions may still hold. When the alarm conditions for all three values hold, the AF bit is set to 1. If the AIE enables an interrupt, an alarm interrupt will be issued.	11
RS0 to RS3	These bits set the frequency of the periodic square wave output from SQW.	12
DV0 to DV2	These bits are for control of the oscillator circuit and frequency divider.	12
UIP	This bit indicates the execution status of the RTC clock update cycle. If the value read from this bit is 1 the update cycle is in process of execution; if the value is 0 the update cycle is not being executed, and moreover no update will be carried out within the next 244µs. This bit is read-only. This bit can be cleared by setting the SET bit to 1.	12
DSE	This bit controls the daylight saving mode. Writing a 1 to DSE enables the daylight saving mode, and writing a 0 disables it.	13
24/12	This bit selects 12-hour or 24-hour clock mode. Writing a 1 to the 24/12 bit selects the 24-hour clock mode, and writing a 0 selects the 12-hour clock mode. When the 24/12 bit is set or changed, the clock registers and clock alarm registers must also be set again. If the settings of the clock registers are incompatible with the 12/24-hour mode selection the results are unpredictable.	13
DM	This bit selects the representation, binary or BCD, used for the values in the clock, calendar and alarm registers. Writing a 1 to the DM bit selects binary format, and writing a 0 selects BCD. After changing the setting of this bit, it is necessary to rewrite all of the clock, calendar and alarm registers in the new format. If the values in these registers are incompatible with the format specified by the DM bit the results are unpredictable.	13
SQWE	This bit controls the output of a square wave from the SQW pin. Writing a 1 to this bit enables the square wave output from SQW, and writing a 0 disables it, holding the SQW low. The frequency of the square wave output is determined by the settings of bits RS0 to RS3.	13
UIE	This bit controls the update-completed interrupt. Writing a 1 to this bit enables the update-completed interrupt, and writing a 0 disables it. The interrupt is issued when the clock update cycle is completed. This bit is cleared by setting the SET bit to 1.	14
AIE	This bit controls the alarm interrupt. Writing a 1 to this bit enables the alarm interrupt, and writing a 0 disables it. The interrupt is issued at the end of the clock update cycle when the clock registers are such that the conditions selected by the alarm registers are met.	14
PIE	This bit controls the periodic interrupt. Writing a 1 to this bit enables the periodic interrupt, and writing a 0 disables it. The periodic interrupt is issued at the frequency determined by the settings of bits RS0 to RS3.	14
SET	This bit controls RTC updating of registers. Writing a 1 to this bit stops the clock from updating registers, and simultaneously clears bits UIE and UIP to 0. Writing a 0 to the SET bit restarts clock updating of registers. This bit should be 0 during normal operation of the device, but writing a 1 to it before explicitly changing the values of the clock, calendar and alarm registers prevents those registers from being updated before the setting is completed. After completing the setting of the clock, calendar and alarm registers, write a 0 to the SET register to restart the normal clock/calendar operation. When the RTC is initially powered on, to ensure that internal registers are initialized correctly, always write a 1 to the SET register before proceeding.	14
UF	This bit indicates whether the update-completed interrupt timing has occurred since the UF bit was last read. When its value is 1, the update-completed interrupt timing has occurred, and when it is 0 the timing has not occurred. Reading this bit automatically clears it. This bit changes to 1 whenever the interrupt timing occurs, whether or not the interrupt is enabled by the UIE bit. This bit is read-only.	15
AF	This bit indicates whether the alarm interrupt timing has occurred since the AF bit was last read. When its value is 1, the alarm interrupt timing has occurred, and when it is 0 the timing has not occurred. Reading this bit automatically clears it. This bit changes to 1 whenever the interrupt timing occurs, whether or not the interrupt is enabled by the AIE bit. This bit is read-only.	15
PF	This bit indicates whether the periodic interrupt timing has occurred since the PF bit was last read. When its value is 1, the periodic interrupt timing has occurred, and when it is 0 the timing has not occurred. Reading this bit automatically clears it. This bit changes to 1 whenever the interrupt timing occurs, whether or not the interrupt is enabled by the PIE bit. This bit is read-only.	15
IRQF	This bit indicates whether an interrupt has been issued since the IRQF bit was last read. When its value is 1, an update-completed, alarm or periodic interrupt has been issued, and at that point the $\overline{IRQ}$ pin went low. When the IRQF bit is 0 no interrupt has been issued. Reading this bit automatically clears it. This bit is read-only.	15
VRT	This bit monitors the state of the backup battery voltage. When the value of the VRT bit is 1, the battery voltage is normal, and when it is 0, the battery voltage has fallen. This bit has an internal two-stage latch: the first time it is read the value reflects the battery voltage in the backup state, and, the second and subsequent times it reflects the battery voltage when V_{DD} power is supplied. This bit is read-only.	16

4. Extended RAM Address Map

The extended RAM has a 128-page configuration with 32 bytes in each page for a total of 4k bytes. The extended RAM page register specifies a page number within this configuration.

To access an address in the extended RAM, first write the required page number (0 to 127) to the extended RAM page register. The extended RAM page register is accessed at address 20h, but in fact as long as the A5 address line is high the extended RAM page register will be addressed, and the state of A4 to A0 is ignored.



5. RAM (RTC and extended RAM)

The RAM for the RTC and the extended RAM can be read and written freely a byte at a time. The RTC RAM is accessed in the same way as the RTC registers by specifying the address in the indirect address register, then accessing the RTC data register. For the extended RAM, any address can be accessed after specifying the page number in the extended RAM page register (32 bytes per page).

The contents of both areas of RAM are preserved by the backup battery.

During operation, these RAM areas can be accessed at any time, independently of the clock update cycle.

■ Register Functions

1. Indirect Address Register and RTC Data Register

The RTC functions of the device use only physical addresses 0 and 1. Access to the internal RTC registers is carried out using the indirect address register and RTC data register.

To access an internal RTC register, it is necessary first to write the required logical register address in the indirect address register at address 0, (for example, to access the years register, write 9.) The data in the specified address is accessed indirectly through the RTC data register: thus the write a value, write it into address 1, and to read a value read it from address 1.

2. Clock, Calendar and Alarm Registers

The values in the clock, calendar and alarm registers are read or written by accessing the corresponding registers. The representation of values in these registers is either binary or BCD, as specified by the value of the DM bit.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Seconds		s40	s20	s10	s8	s4	s2	s1
1	Alarm seconds		a-s40	a-s20	a-s10	a-s8	a-s4	a-s2	a-s1
2	Minutes		mi40	mi20	mi10	mi8	mi4	mi2	mi1
3	Alarm minutes		a-mi40	a-mi20	a-mi10	a-mi8	a-mi4	a-mi2	a-mi1
4	Hours	PM/AM		h20	h10	h8	h4	h2	h1
5	Alarm hours	a-PM/AM		a-h20	a-h10	a-h8	a-h4	a-h2	a-h1
6	Day-of-week						w4	w2	w1
7	Day			d20	d10	d8	d4	d2	d1
8	Month				mo10	mo8	mo4	mo2	mo1
9	Year	y80	y40	y20	y10	y8	y4	y2	y1

(1) Time and date registers

The hours register includes a combination of the hours value and the PM/AM bit. The sets of possible values of this register are therefore different in the 12-hour and 24-hour modes. The PM/AM bit is valid in 12-hour mode, and is then 1 to indicate PM and 0 to indicate AM. Thus, for example, if the BCD representation mode is selected, if the hours and minutes registers are read, and the hours value is (BCD) 88 (the PM/AM bit is set, so the more significant digit is an 8, and this is a PM time), and the minutes value is 00, then the time is 8:00 PM. Similarly, if the hours value is 11 (the PM/AM bit is zero, so this is an AM time), and the minutes value is 30, then the time is 11:30 AM.

In the 12-hour mode, the value of bit h20 is never 1, but it is possible to write a 1 to this bit. Since this leads to unpredictable results, be careful not to write erroneous values in this register. Again, in the 12-hour mode, if the PM/AM bit is incorrectly set, the time will be 12 hours out, and calendar updates will occur at noon. It is therefore always necessary to set the PM/AM bit correctly. Equally, when the 24-hour mode is selected, the PM/AM bit is always 0.

For the selection of 12-hour or 24-hour mode, see the description of the 24/12 bit (pages 13 and 17).

Time mode	Value range
12-hour clock	12:00:00 to 11:59:59am and pm *
24-hour clock	00:00:00 to 23:59:59

* Note: 12:00 AM represents 12:00 midnight (the first minute of the day), and 12:00 PM represents 12:00 noon.

(2) Day-of-the-week register

This holds the day-of-the-week as a 3-bit value, which cycles round from 1 to 7. It counts as the day register increments. The value is encoded as shown in the following table.

Value	1	2	3	4	5	6	7
Day	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

(3) Alarm registers

These hold the alarm generation time: there are three registers for hours, minutes and seconds. To use the alarm function, write the alarm generation time to these registers; if any register has bits 6 and 7 set to 1, that is, a value of 11xxxxxx binary, that register is ignored in determining whether to issue the alarm. In other words, when the alarm register is set to this ignore code, whatever the value of the corresponding time register the alarm conditions may still hold. When the alarm conditions for all three values hold, if the AIE enables an interrupt, an alarm interrupt will be issued.

The a-PM/AM bit is used in the 12-hour mode, and the a-h20 bit is used in the 24-hour mode.

The values in the alarm registers must be in the same format (specified in register B) as the clock and calendar registers. If the format is changed by rewriting register B, the alarm registers must be rewritten accordingly in the same way as the clock and calendar registers.

(4) Leap year calculation

Leap years are automatically identified, and this affects the handling of the month and day digits for February 29.

[Leap years]

In general, a year contains 365 days. However, the Earth takes slightly longer than exactly 365 days to rotate around the sun, so we need to set leap years in compensation. A leap year occurs once every four years, in years in the Gregorian calendar that are divisible by four. However, a further small correction is necessary in that years that are divisible by 100 are ordinary years, but years that are further divisible by 400 are leap years.

The main leap and ordinary years since 1900 and into the future are listed on the right.

[Leap years in the RTC-65271]

To identify leap years, the RTC-65271 checks whether or not the year digits are divisible by four. As implied above, 2000 will be a leap year, and so no further correction will be necessary in that case. This process identifies the following years as leap years:

(19)96, (20)00, (20)04, (20)08, (20)12,...

The turn-of-the-century years for which the RTC-65271 will require correction are shown shaded in the table on the right.

If year numbers from a different calendar are used, leap-year identification will only be correct if the year numbers in that calendar that are divisible by four are actually leap years.

Leap years and ordinary years		
Year	Leap year	Ordinary year
1900		○
⋮		
1993		○
1994		○
1995		○
1996	○	
1997		○
1998		○
1999		○
2000	○	
2001		○
2002		○
2003		○
2004	○	
2005		○
⋮		
2100		○
2200		○
2300		○
2400	○	
⋮		

3. Register A

Register A includes bits specifying the frequency of the SQW output signal and of the periodic interrupt, control bits for the oscillator-related circuits, and the update cycle execution status bit.

Register A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Effect of $\overline{\text{RESET}}$	No change	No change	No change	No change	No change	No change	No change	No change

(1) RS0, RS1, RS2 and RS3 bits (Rate Selection; read/write; D0 to D3)

The four bits RS0 to RS3 determine the frequency of the output from SQW and the periodic interrupt. This is done by dividing the original oscillation frequency of the internal crystal oscillator, which is 32.768 kHz into thirteen stages, down to 1 Hz. The relationship between the setting of these bits and the time interval between periodic interrupts and the frequency of the SQW output is as shown in the following table.

RS3	RS2	RS1	RS0	Interrupt period	SQW output frequency
0	0	0	0	-	-
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8192 Hz
0	1	0	0	244.141 µs	4096 Hz
0	1	0	1	488.281 µs	2024 Hz
0	1	1	0	976.5625 µs	1024 Hz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

The PIE and SQWE bits in register B control the periodic interrupt and the SQW output as follows.

PIE bit	SQWE bit	Periodic interrupt	SQW output
0	0	Disabled	Disabled
0	1	Disabled	Enabled
1	0	Enabled	Disabled
1	1	Enabled	Enabled

(2) DV0, DV1 and DV2 bits (DiVider selection; read/write; D4 to D6)

The three bits DV0 to DV2 control the oscillator and frequency divider. When all three bits are 0, the oscillator stops. Because the physical crystal oscillations are stopped, from this state there is a delay (t_{RC} = 1 s max.) until oscillation can be restarted. The relation between the settings of the bits and the control of the oscillator and frequency divider is as shown in the following table.

DV2	DV1	DV0	Oscillator	Frequency divider
0	0	0	Stopped	Stopped
0	1	0	Operating	Operating
1	1	X	Operating	Reset (8192 Hz and below)

This device is shipped from the factory without batteries. Therefore when the device is first powered on, and when batteries are first fitted, the settings of bits DV0 to DV2 are undefined. In these cases therefore, it is necessary to initialize bits DV0 to DV2 and start the oscillation circuit and frequency divider operating. For normal operation, the DV bits are set to 010. When, however, the RTC functions are not going to be used for a considerable period, setting all bits to 0 stops the crystal oscillator and frequency divider, and reduces battery consumption.

Writing 11x to bits DV0 to DV2 resets all the frequency stages below the oscillator frequency, from 8192 Hz down, providing more accurate time setting. However, from the time when the value is changed from 11x to 010, releasing the reset, to the time of the next clock update is approximately 0.5 seconds. In other words, this resets not to "x.0 seconds", but to "x.5 seconds".

The DV0 to DV2 bits are not affected by the state of the $\overline{\text{RESET}}$ pin.

(3) UIP bit (Update In Progress; read only; D7)

The UIP bit is read-only, and its status reflects the state of the RTC update cycle. The UIP bit becomes 1 once every second, then 244 µs later the clock is updated, and UIP goes back to 0. Therefore if this bit is read as 1 it indicates that the RTC is carrying out internal clock update processing. At this point reading or writing the clock, calendar and alarm registers should be avoided. If the UIP bit reads as 0, no update is being carried out, and moreover no update will be carried out for the next 244 µs. Therefore, when a value of 0 is read, for a period of 244 µs the clock, calendar and alarm registers can be safely written to.

The UIP bit is not affected by the state of the $\overline{\text{RESET}}$ pin. The UIP is, however, cleared to 0 when the SET bit is changed to 1.

4. Register B

Register B includes time mode bits, interrupt setting bits, and clock control bits.

Register B	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Effect of $\overline{\text{RESET}}$	No change	Set to 0	Set to 0	Set to 0	Set to 0	No change	No change	No change

(1) DSE bit (Daylight Saving Enable; read/write; D0)
The DSE bit controls the (North American) daylight saving time function.

DSE bit value	DSE bit function
0	Disable daylight saving time.
1	Enable daylight saving time.

Writing 1 to the DSE bit enables daylight saving time, and the time is shifted according to the rules embodied in the following table. Writing 0 to the DSE bit disables daylight saving time, and the time is constant throughout the year.

[Daylight saving time update rules]

Day	Update time	Note
First Sunday in April	1:59:59 AM → 3:00:00 AM	Summer time: advance one hour
Last Sunday in October	1:59:59 AM → 1:00:00 AM	Winter time: retard one hour

The DSE bit is not affected by the state of the $\overline{\text{RESET}}$ pin.

(2) 24/12 bit (24/12 control; read/write; D1)
The 24/12 bit selects the 12-hour or 24-hour operation mode.

24/12 bit value	24/12 bit function
0	Select 12-hour mode.
1	Select 24-hour mode.

Writing 1 to the 24/12 bit selects 24-hour mode. In 24-hour mode, the PM/AM bit is not used, and is always 0.
Writing 0 to the 24/12 bit selects 12-hour mode. In 24-hour mode, the PM/AM bit is used, and is 0 to indicate AM and 1 to indicate PM.
When the 24/12 bit is set or changed, it is necessary to reset the clock registers and alarm registers. If the values in these registers are incompatible with the mode specified by the 24/12 bit the results are unpredictable.
The 24/12 bit is not affected by the state of the $\overline{\text{RESET}}$ pin.

(3) DM bit (Data Mode; read/write; D2)
The DM bit selects whether the values in the clock, calendar and alarm registers are represented in binary or BCD.

DM bit value	DM bit function
0	Select BCD mode.
1	Select binary mode.

Writing 1 to the DM bit selects binary mode, and writing 0 to the DM bit selects BCD mode. When the DM bit is set or changed, it is necessary to load the values into the clock, calendar and alarm registers in the appropriate format (binary or BCD). If the values in these registers are incompatible with the mode specified by the DM bit the results are unpredictable.
The DM bit is not affected by the state of the $\overline{\text{RESET}}$ pin.

(4) SQWE bit (SQuare Wave Enable; read/write; D3)
The SQWE bit controls the output of a square wave signal on the SQW pin.

SQWE bit value	SQWE bit function
0	Fix at low level.
1	Enable the square wave output at frequency determined by RS0 to RS3.

Writing 1 to the SQWE bit enables the output of a square wave signal on the SQW pin. Writing 0 disables the square wave output, and holds the SQW pin at low level.
The frequency of the square wave output from pin SQW is determined by the value in RS0 to RS3. (See page 12.)
The SQWE bit is cleared by a $\overline{\text{RESET}}$ pin going low.

(5) UIE bit (Update-completed Interrupt Enable; read/write; D4)
The UIE bit controls the issuing of the update-completed interrupt.

UIE bit value	UIE bit function
0	Disable update-completed interrupt.
1	Enable update-completed interrupt.

Writing 1 to the UIE bit enables the update-completed interrupt, and writing 0 disables the update-completed interrupt. When the UIE bit is 1, an interrupt event occurs at the end of the update cycle, and an interrupt is issued. The interrupt brings the $\overline{IRQ}$ pin low, and sets the update flag, bit UF, to 1.
The UIE bit is cleared by a $\overline{RESET}$ pin going low or by the SET bit going to 1.

(6) AIE bit (Alarm Interrupt Enable; read/write; D5)
The AIE bit controls the issuing of the alarm interrupt.

AIE bit value	AIE bit function
0	Disable alarm interrupt.
1	Enable alarm interrupt.

Writing 1 to the AIE bit enables the alarm interrupt, and writing 0 disables the alarm interrupt. When the AIE bit is 1, an interrupt event occurs at the end of the update cycle if a comparison of the alarm and clock registers produces a match, and an interrupt is issued. (In this case, if any of the alarm registers are set to the ignore code, they always match.) The interrupt brings the $\overline{IRQ}$ pin low, and sets the alarm flag, bit AF, to 1.
The AIE bit is cleared by a $\overline{RESET}$ pin going low.

(7) PIE bit (Periodic Interrupt Enable; read/write; D6)
The PIE bit controls the issuing of the periodic interrupt.

PIE bit value	PIE bit function
0	Disable periodic interrupt.
1	Enable periodic interrupt.

Writing 1 to the PIE bit enables the periodic interrupt, and writing 0 disables the periodic interrupt. When the PIE bit is 1, an interrupt event occurs at the periodic interval whose frequency is specified by bits RS0 to RS3, and an interrupt is issued. The interrupt brings the $\overline{IRQ}$ pin low, and sets the periodic interrupt flag, bit PF, to 1.

The PIE bit is cleared by a $\overline{RESET}$ pin going low.

(8) SET bit (SET; read/write; D7)
The SET bit controls RTC updating of registers.

SET bit value	SET bit function
0	Carry out RTC updating of registers. (Normal state.)
1	Disable RTC updating of registers.

Writing 1 to the SET bit disables RTC updating of registers, and writing 0 restarts the normal operation of updating. While this bit is 1, the contents of the clock, calendar and alarm registers are preserved. There is no effect on the square wave output from pin SQW nor on the periodic interrupt. This bit should be 0 during normal operation of the device, but writing a 1 to it before explicitly changing the values of the clock, calendar and alarm registers prevents those registers from being updated before the setting is completed. After completing the setting of the clock, calendar and alarm registers, write a 0 to the SET register to restart the normal clock/calendar operation.
When the RTC is initially powered on, to ensure that internal registers are initialized correctly, always write a 1 to the SET register before proceeding.
Writing 1 to the SET bit clears bits UIP and UIE.
The SET bit is not affected by the state of the $\overline{RESET}$ pin.

5. Register C

Register C includes flag bits which indicate interrupt states. Bits 0 to 3 are spare, and always read as 0. Reading the register has the effect of clearing all the bits to 0, and therefore if more than one interrupt is being used, it is necessary to check all bits of this register each time it is read.

Register C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	IRQF	PF	AF	UF	-	-	-	-
Read/write	Read only	Read only	Read only	Read only	-	-	-	-
Effect of $\overline{\text{RESET}}$	Set to 0	Set to 0	Set to 0	Set to 0	-	-	-	-

(1) UF bit (Update-completed interrupt Flag; read only; D4)
The UF bit is set to 1 at the end of the clock update cycle, and is automatically cleared to 0 when read.

UF bit value	UF bit significance
0	No clock update cycle has been completed since this register was last read.
1	A clock update cycle has been completed since this register was last read.

The UF bit is always set by the completion of an update cycle, regardless of the setting of the UIE bit. If the UIE bit is 1, enabling the update-completed interrupt, then at the end of the update cycle, the UF bit is set and simultaneously $\overline{\text{IRQ}}$ goes low, and the IRQF bit is set to 1.
The UF bit is cleared to 0 by the $\overline{\text{RESET}}$ pin going low, and also by register C being read.

(2) AF bit (Alarm interrupt Flag; read only; D5)
The AF bit is set to 1 when at the end of a clock update cycle the current time registers match the values of the alarm time registers, with ignore codes treated as "don't care" values which always match. It is automatically cleared to 0 when read.

AF bit value	AF bit significance
0	No alarm time match has occurred since this register was last read.
1	An alarm time match has occurred since this register was last read.

The AF bit is always set by an alarm match, regardless of the setting of the AIE bit. If the AIE bit is 1, enabling the alarm interrupt, then when there is an alarm match, the AF bit is set and simultaneously $\overline{\text{IRQ}}$ goes low, and the IRQF bit is set to 1.
The AF bit is cleared to 0 by the $\overline{\text{RESET}}$ pin going low, and also by register C being read.

(3) PF bit (Periodic interrupt Flag; read only; D6)
The PF bit is set to 1 at intervals corresponding to the frequency specified by bits RS0 to RS3, and is automatically cleared to 0 when read.

PF bit value	PF bit significance
0	The specified period has not elapsed since this register was last read.
1	The specified period has elapsed since this register was last read.

The PF bit is always set by the periodic signal, regardless of the setting of the PIE bit. If the PIE bit is 1, enabling the periodic interrupt, then when the specified period has elapsed, the PF bit is set and simultaneously $\overline{\text{IRQ}}$ goes low, and the IRQF bit is set to 1.
The PF bit is cleared to 0 by the $\overline{\text{RESET}}$ pin going low, and also by register C being read.

(4) IRQF bit (Interrupt ReQuest Flag; read only; D7)
The IRQF bit indicates that an enabled interrupt condition has occurred, and is set to 1 when an update-completed interrupt, alarm interrupt or periodic interrupt is issued. At the same time the $\overline{\text{IRQ}}$ output goes low. This bit is automatically cleared to 0 when read.

IRQF bit value	IRQF bit significance
0	No interrupt has been issued.
1	An interrupt has been issued.

The IRQF bit is set when any of the following conditions holds:
i. The UIE bit is 1 and the UF bit has been set to 1 (update-completed interrupt).
ii. The AIE bit is 1 and the AF bit has been set to 1 (alarm interrupt).
iii. The PIE bit is 1 and the PF bit has been set to 1 (periodic interrupt).

In other words, represented as a logical expression, with multiplication representing logical and addition representing logical OR:

$$IRQF = UIE \cdot UF + AIE \cdot AF + PIE \cdot PF$$

The IRQF bit is cleared to 0 by the $\overline{\text{RESET}}$ pin going low, and also by register C being read.

6. Register D

Register D includes the backup battery voltage monitoring bit. Bits 0 to 6 are spare, and always read as 0.

Register D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit name	VRT	-	-	-	-	-	-	-
Read/write	Read only	-	-	-	-	-	-	-
Effect of $\overline{\text{RESET}}$	No change	-	-	-	-	-	-	-

(1) VRT bit (Valid RAM and Time; read only; D7)

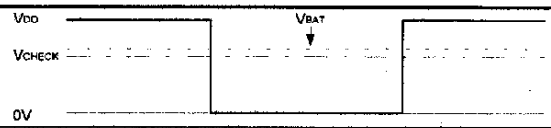
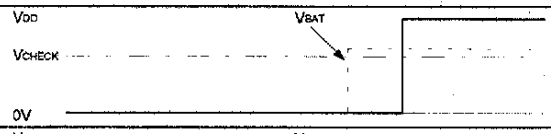
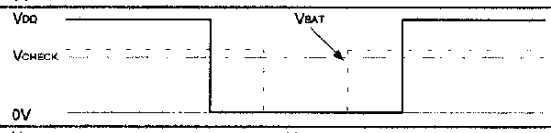
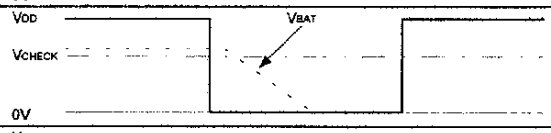
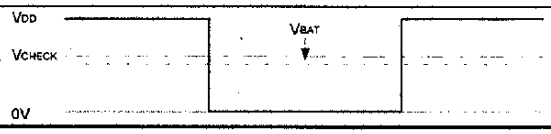
The VRT bit is monitors the state of the backup battery voltage, and indicates the battery voltage state during the backup state and when the device was last powered on. The first time it is read after installing the batteries, the value is always 0. This bit is subject to a power on reset, and there are therefore no problems of indeterminate settings or incorrect results caused by the power on (even without the battery backup).

VRT bit value	VRT bit significance
0	The battery voltage is low, or the battery voltage has been low at some point because for example during backup the batteries were replaced. The RTC clock data and RAM data is not guaranteed.
1	The battery voltage is normal, and preservation of backed-up data is guaranteed.

The VRT bit has an internal two-stage latch, and the values read have different meanings on the first and second readings, as shown in the following table.

Time of reading	VRT bit significance
First	The state of the battery voltage V_{BAT} during the backup period (returns 0 if at any point $V_{BAT} < V_{CHECK}$ held).
Second and subsequent	The state of the battery voltage V_{BAT} at power on.

Another way of expressing the meaning of these values is shown in the following table.

Condition	VRT bit values		Timing diagram
	First reading	Second and subsequent readings	
Normal	1	1	
Initial power on	0	1	
Battery changed during backup	0	1	
Battery voltage fell below Vcheck during backup	0	0	
Device was powered on (i.e. Vdd supplied) with the battery voltage low	0	0	

At power on, in the interval while V_{DD} goes from 0 to V_{SWITCH}, power is supplied from the battery. When V_{DD} exceeds V_{SWITCH} the power supply switches to V_{DD}, but the circuit still draws a forced current of 1 µA from the battery. This forced current flows until V_{DD} reaches V_{ENABLE}. At this point a comparison is made of the battery voltage and V_{CHECK}, and the comparison result is stored in the VRT bit. The forced current is stopped after the voltage comparison result has been stored in the VRT bit.

When the device is powered on, ensure that there is always the batteries present. The unconnected battery terminals have a high impedance, and if left open-circuit are likely to lead to noise problems.

7. Extended RAM Page Register

As has been mentioned above, the extended RAM has a 128-page configuration with 32 bytes in each page for a total of 4K bytes. To access an address in the extended RAM, first write the required page number to the extended RAM page register. The page number is encoded in binary. The range of values of the page number is from 00H to 7FH, but the top bit is ignored for the purposes of page selection. Therefore pages 80H to FFH are mapped onto pages 00H to 7FH. The extended RAM page register is accessed when the A5 address line is high and the extended RAM enable signal $\overline{\text{XRAM}}$ is low. Therefore when extended RAM access is enabled, addresses 20H to 3FH all map onto the extended RAM page register. The selected page of extended RAM is then accessed at addresses 00H to 1FH.

Operation Procedure

1. Clock, Calendar and Alarm Registers

Note the following points when setting or changing the contents of the clock, calendar and alarm registers. When writing to these registers, it is first necessary to set the SET bit of register B to 1 (see pages 14 and 21). This prevents the values from being corrupted if an update produced a carry. After writing to the registers set the SET bit back to 0, to restart the clock.

(1) Data formats

The values in the clock, calendar and alarm registers are read and written by directly accessing the registers. The format of the data values is determined by the DM bit in register B, and can be binary or BCD.

When the DM bit setting is changed, it is necessary to load the values into the clock, calendar and alarm registers in the appropriate format (binary or BCD). If the values in these registers are incompatible with the mode specified by the DM bit the results are unpredictable.

(2) 24/12-hour modes

Either the 24-hour clock or 12-hour clock can be selected. The setting is determined by the 24/12 bit in register B. When the 24/12 bit is set or changed, it is necessary to reset the hours registers and alarm-hours registers. If the values in these registers are incompatible with the mode specified by the 24/12 bit the results are unpredictable.

2. Interrupts

The RTC provides three independent interrupt functions, which may be used to send an interrupt to a CPU or other device.

Alarm interrupt:	Can be issued at a specified time from once per second to once per day.
Periodic interrupt:	Can be issued at fixed intervals, ranging from 122µs to 500ms.
Update-completed interrupt:	Can be issued every second at the end of the clock update cycle. This enables an external circuit to determine the timing of the update cycle of the RTC.

(1) Interrupt enable bits

The three interrupt enable bits, AIE, PIE and UIE in register B enable or disable the three interrupts.

When an interrupt enable bit is 1, the corresponding interrupt is enabled, and when the corresponding interrupt event occurs, an interrupt signal is output. When the interrupt occurs, $\overline{IRQ}$ goes low, and in register C, bit IRQF is set to 1, and the interrupt flag bit for the corresponding interrupt is set to 1.

When an interrupt enable bit is 0, if the corresponding interrupt event occurs, the interrupt signal output and the setting of the IRQF are inhibited. On the other hand, even when the interrupt enable bit is 0, the interrupt flag bit for the corresponding interrupt is set to 1 when the interrupt event occurs.

(2) Interrupt status

Register C is an interrupt status register, and includes the three flag bits AF, PF and UF. When an interrupt event occurs, the corresponding flag bit is set to 1. These bits are set, as has already been stated, when the interrupt event occurs, regardless of the setting of the corresponding interrupt enable bit. These bits thus allow the functions to be used by software polling, without using an interrupt mechanism.

Reading register C automatically clears these bits to 0. In order to prevent dropped interrupts, it is therefore necessary always to check all the bits when this register is read. Register C has a 2 stage latch function so that if an interrupt event occurs during the reading cycle, it is held pending internally until the end of the cycle.

When an interrupt enable bit in register B is set to enable the interrupt, if the corresponding interrupt event occurs, and the corresponding flag is set in register C, then the IRQF bit in register C is also set, and at the same time the $\overline{IRQ}$ pin goes low to output an interrupt request.

(3) Periodic interrupt

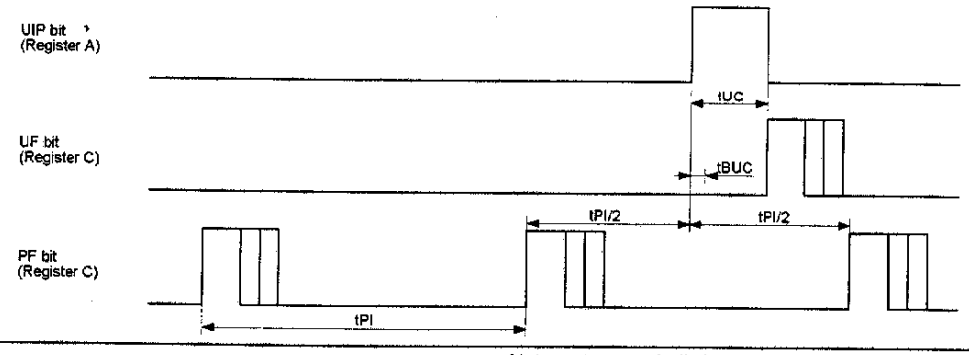
The periodic interrupt can be issued at fixed intervals, ranging from 122µs to 500ms, as determined by the settings of bits RS0 to RS3 in register A. If the periodic interrupt enable bit PIE in register B is 1, this enables the interrupt. When the interrupt event occurs, the $\overline{IRQ}$ output goes low. Furthermore, by reading the periodic interrupt flag PF in register C, it is possible to determine that the periodic interrupt event has occurred.

(4) Update-completed interrupt

The UIP bit in register A, the update-in-progress status bit, is set to 1 every second during the clock update cycle. The UF bit in register C, the update-completed flag bit, is set to 1 at the completion of the update cycle (on the falling edge of the UIP bit).

If the update-completed interrupt enable bit UIE in register B is 1, this enables the interrupt. When the interrupt event occurs, the $\overline{IRQ}$ output goes low. Furthermore, by reading the update-completed interrupt flag UF in register C, it is possible to determine that the update-completed interrupt event has occurred.

Timing of the periodic interrupt and update-completed interrupt



Notes: tPI = periodic interrupt time interval (see page 12)
tUC = update cycle time (1987µs)
tBUC=delay before update cycle time (244µs)

(5) Alarm interrupt

The alarm interrupt uses an alarm time written in the alarm registers, and is issued when the values in the clock registers match those in the alarm registers. There are two principal ways in which this function can be used.

i. Alarm time interrupt

This is the basic method of use, in which an alarm time is written in the alarm registers, and the alarm interrupt is issued when the values in the clock registers match those in the alarm registers.
By setting the AIE alarm interrupt enable bit in register B to 1, the alarm interrupt is enabled. When the interrupt event occurs, $\overline{IRQ}$ output goes low. By reading the alarm interrupt flag AF in register C, it is possible to check that the alarm interrupt has occurred.

ii. Repeated alarm interrupt

For each alarm register, an ignore code (or "don't care") can be set, so that whatever the value of the corresponding clock register, this register matches. Using these ignore codes, it is possible to generate an alarm every hour, every minute or every second, for example. For each one of the three registers, the ignore code has bits 6 and 7 set to 1, and any values in the other bits (binary 11xxxxxx). In different words, all hexadecimal values from C0H to FFH are ignore codes. The following table gives examples.

Alarm hours register	Alarm minutes register	Alarm seconds register	Alarm generation conditions
Ignore code	Ignore code	Ignore code	Every second
Ignore code	15	30	15 minutes 30 seconds past every hour
8	Ignore code	00	Every minute (on 00 seconds) from 8:00 to 8:59

(6) Update cycle

The RTC has an update cycle which occurs every second, to allow for carry propagation through the clock and calendar registers. In the update cycle the clock is advanced by one second, carries are propagated as necessary. At the same time the values of the clock registers are compared with the values in the alarm registers. If the values of the clock registers and the values in the alarm registers match, at the end of the update cycle the AF alarm flag bit in register C is set to 1. If the AIE alarm interrupt enable bit in register B is 1, the alarm interrupt is generated, the IRQF flag bit is set to 1 and the $\overline{IRQ}$ output goes low.
The UF update flag bit in register C is set to 1 at the end of the update cycle. If the UIE update-completed interrupt enable bit in register B is 1, the update-completed interrupt is generated, the IRQF flag bit is set to 1 and the $\overline{IRQ}$ output goes low.
During the update cycle, reading the clock and calendar registers can give erroneous results. To ensure that only correct values are read, use one of the following procedures. Note the RTC RAM and the extended RAM can be read or written reliably regardless of the state of the update cycle.

Procedure 1: Using the update-completed interrupt (see page 23)

When the update-completed interrupt enable bit UIE in register B is set to 1, an interrupt is issued immediately after the completion of the update cycle. If the values are read out within 998 ms of this interrupt, they are guaranteed free of corruption. The interrupt handler must read register C in order to clear the update-completed flag UF.

Procedure 2: Monitoring the update-in-progress status bit UIP (see page 23)

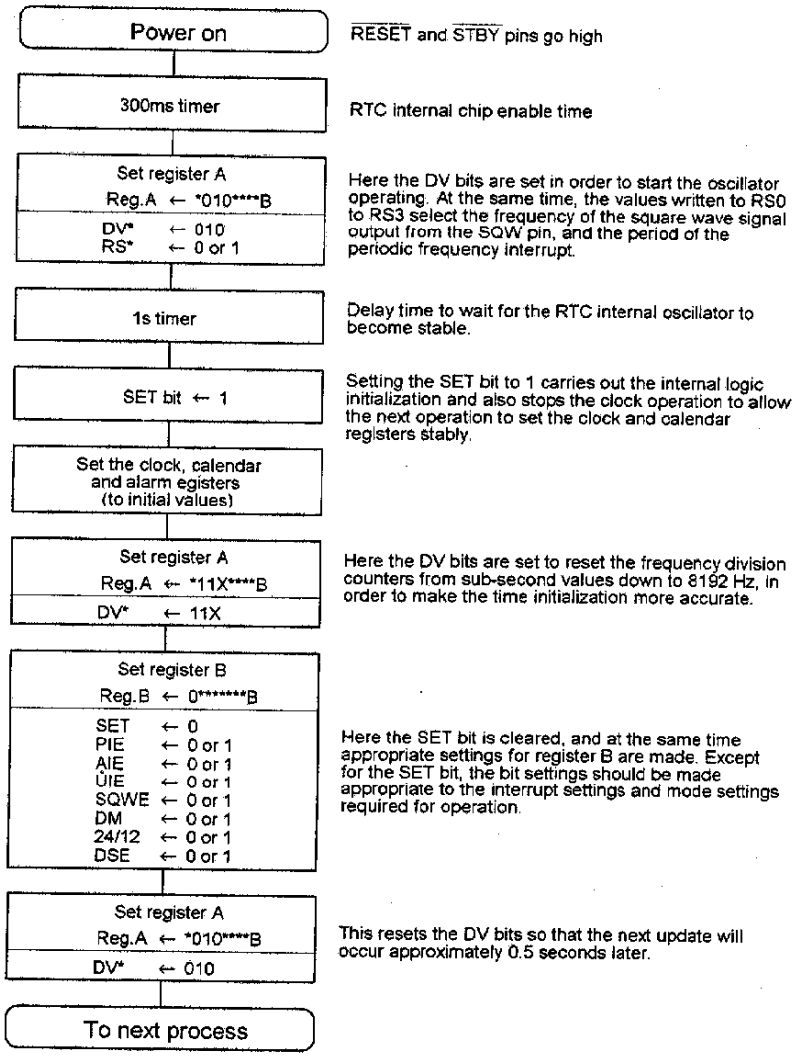
The updating of the clock and calendar registers is carried out 244µs after the time when the update-in-progress status bit UIP changes to 1. In other words, if reading the UIP bit produces 0, there will be no update cycle for at least 244µs.
Therefore, in other words, a satisfactory method is to read the UIP bit, and when it is 0, carry out the clock/calendar register access within 244µs.

Procedure 3: Using the periodic interrupt (see page 23)

The UIP bit in register A is set to 1 exactly half-way through the cycle from one rising edge of the PF bit in register C to the next (see the timing chart at the top of the page). If the periodic interrup period tPI is set to at least 7.8125ms (128 Hz or less) using bits RS0 to RS3, then the rising edge of the PF bit is guaranteed to come after the update cycle has completed, and it is therefore possible to read out the clock and calendar registers once per cycle of the periodic interrupt. The reading must also be completed within a time of tPI/2 + tBUC, to avoid interference from the update cycle.
Before the interrupt routine ends it must read register C in order to clear the PF bit.

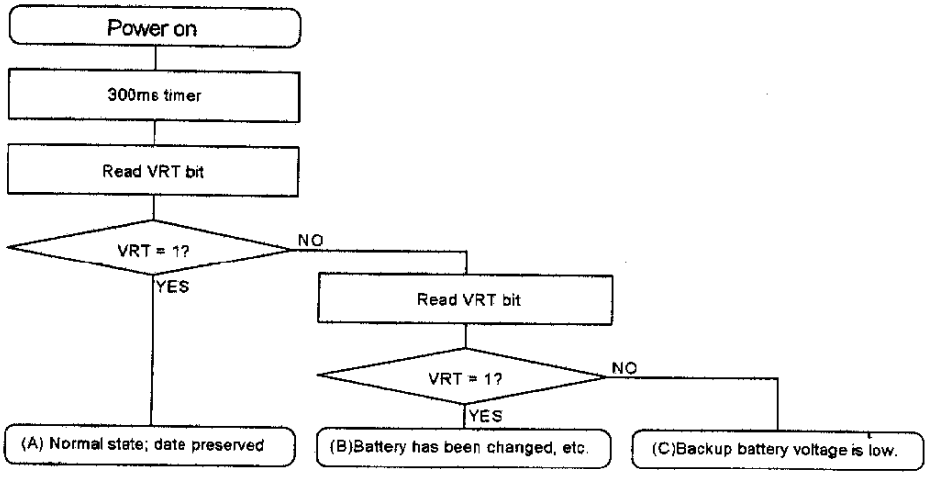
3. Procedure at Power On

(1) Settings at initial power on (initialization)



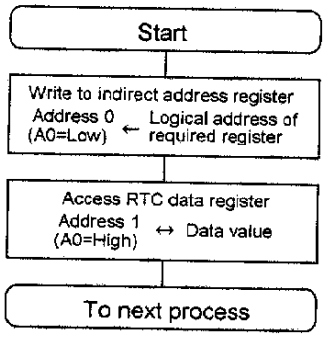
When the device is powered on, ensure that there is always a backup battery present.

(2) Data preservation decision on powering on from backup state



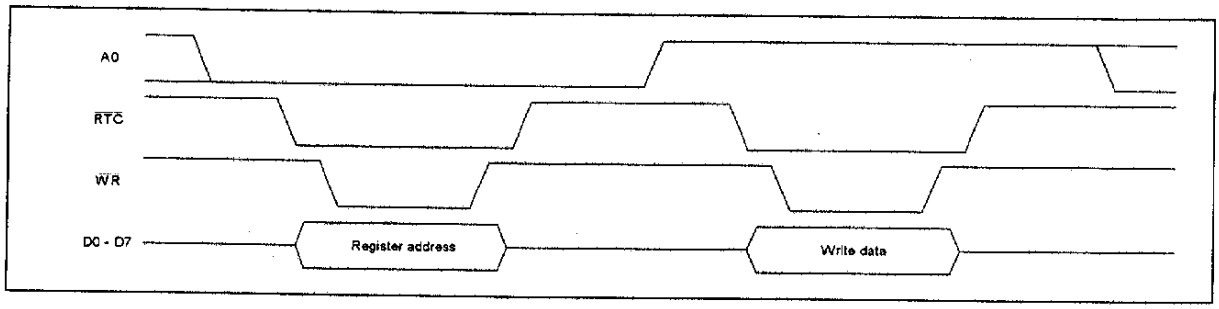
(A) "Normal state" means that the backup battery voltage is adequate, and that clock data and RAM data has been preserved normally.
(B) "Battery has been changed" means that although the backup battery voltage was normal at the power on, at some point since the previous power on the battery voltage had fallen below the threshold, for example when the batteries were changed.
(C) "Backup battery voltage is low" means that at the time of power on the backup battery voltage was inadequate to have maintained the backup function, or that possibly the backup batteries have been removed.
In both of cases (B) and (C) there is a possibility that the clock setting and RAM data have not been preserved correctly, and therefore these values are not guaranteed.
(VRT bit: see page 16.)

4. RTC Access

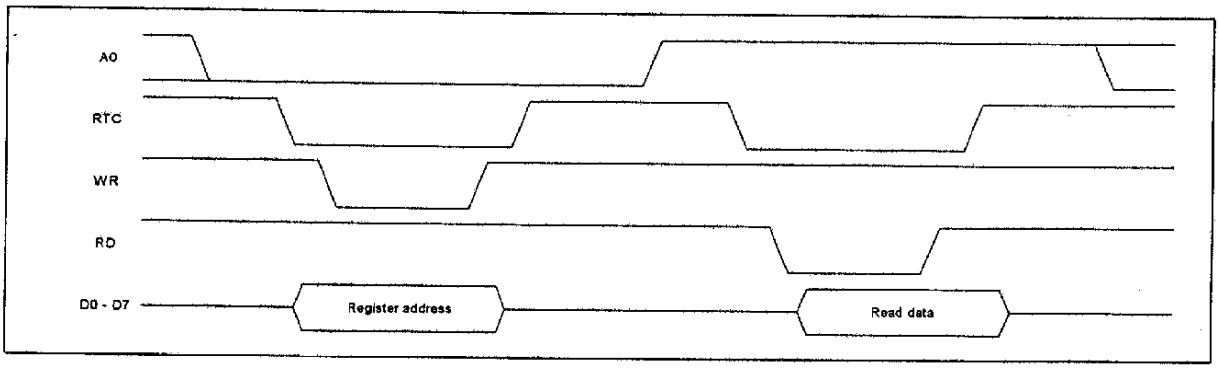


Once the indirect address register is set, to access the same internal register twice in succession it is not necessary to set the indirect address register more than once. However, when the $\overline{\text{RESET}}$ pin goes low, the contents of the indirect address register become indeterminate, and it is then necessary to set the indirect address register again. The indirect address register is not affected by changes in the state of the $\overline{\text{STBY}}$ pin, and its value is preserved through a standby state.

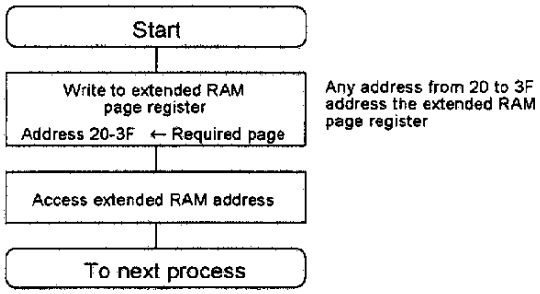
5. Writing to the RTC



6. Reading from the RTC

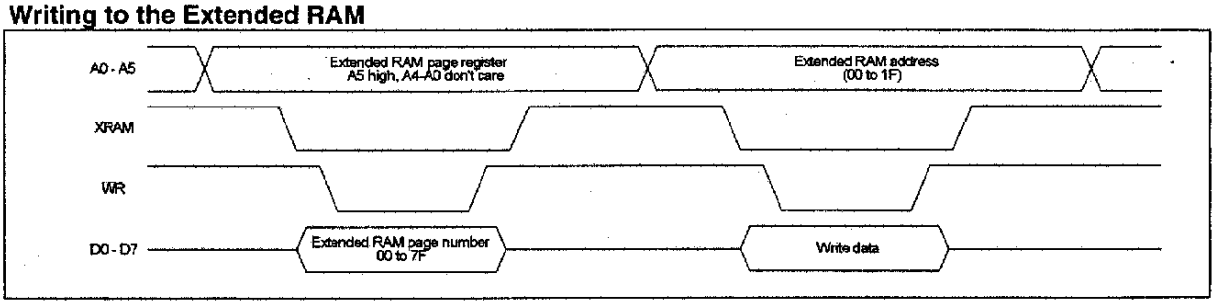


7. Extended RAM Access

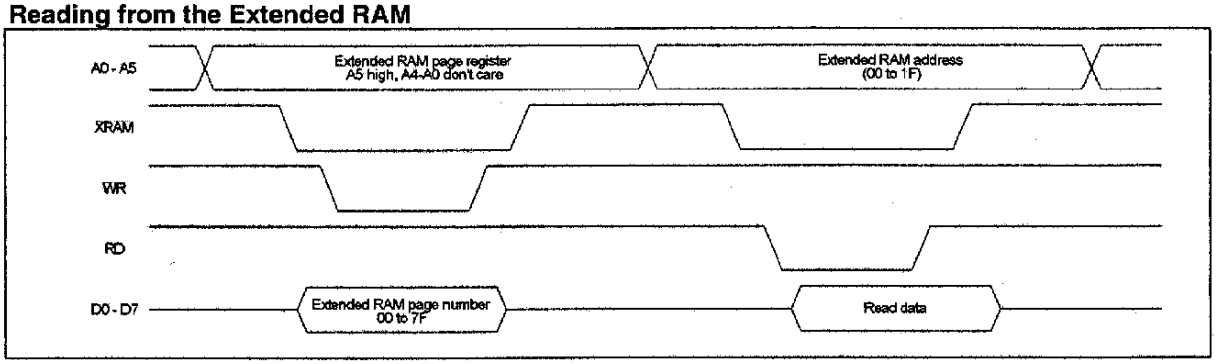


Once the extended RAM page register is set, to access the same page twice in succession it is not necessary to set the extended RAM page register more than once. However, when the $\overline{\text{RESET}}$ pin goes low, the contents of the extended RAM page register become indeterminate, and it is then necessary to set the extended RAM page register again. The extended RAM page register is not affected by changes in the state of the $\overline{\text{STBY}}$ pin, and its value is preserved through a standby state.

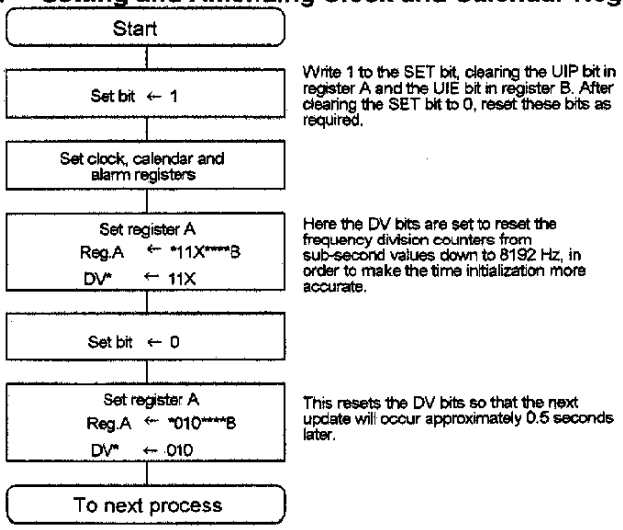
8. Writing to the Extended RAM



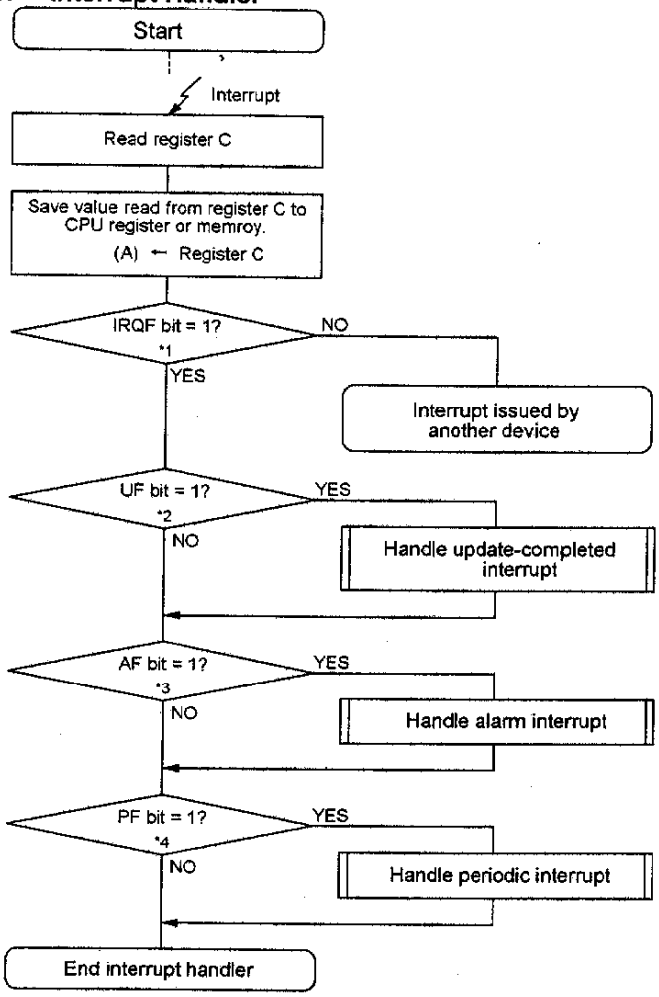
9. Reading from the Extended RAM



10. Setting and Amending Clock and Calendar Registers



11. Interrupt Handler

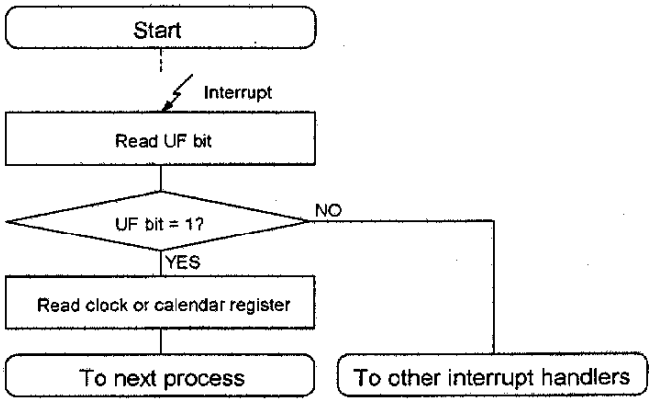


Note	Flag mask expression	Notes
*1	(A) & 80H	This decision branch is not necessary unless there is another device connected to the CPU at the same interrupt level.
*2	(A) & 10H	This decision branch is not necessary if the update-completed interrupt is not being used.
*3	(A) & 20H	This decision branch is not necessary if the alarm interrupt is not being used.
*4	(A) & 40H	This decision branch is not necessary if the periodic interrupt is not being used.

Reading register C clears all the bits in it. Therefore each call to the interrupt handler must check all the bits, to avoid dropped interrupts, as shown for reference in the flowchart above.

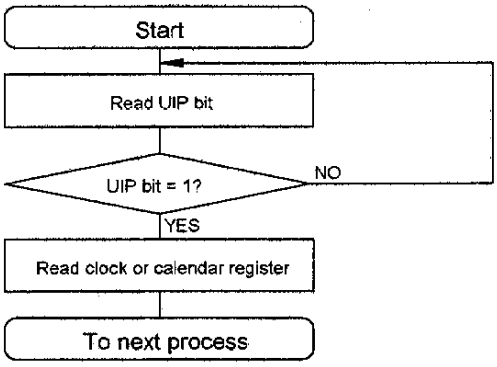
12. Reading the Clock and Calendar Registers

(1) Procedure 1: Using the update-completed interrupt



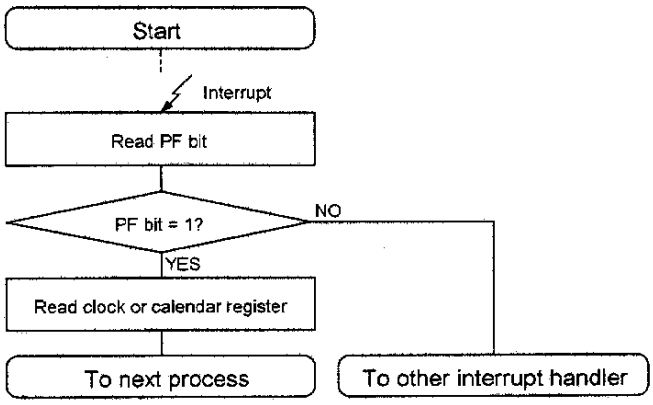
To enable the update-completed interrupt set bit UIE in register B to 1 in an initialization routine. Remember that the UIE bit is cleared to 0 by setting the SET bit of register B to 1.

(2) Procedure 2: Monitoring the update-in-progress status bit UIP



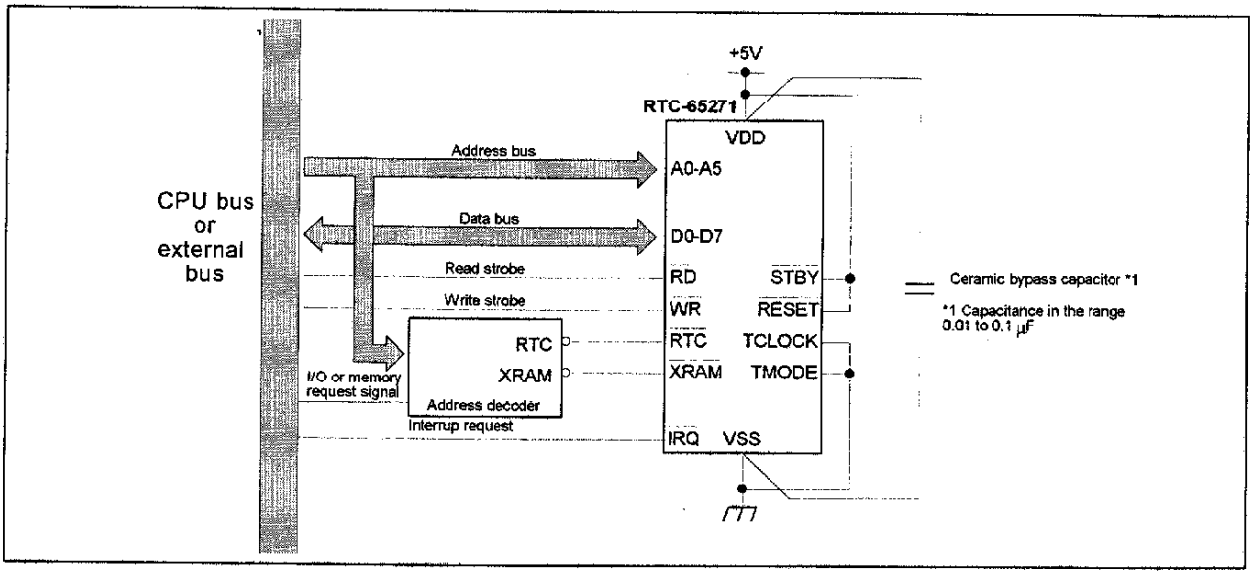
If reading the UIP bit produces 0, there will be no update cycle for at least 244µs. Therefore, complete the reading of the clock and calendar registers within 244µs.

(3) Procedure 3: Using the periodic interrupt



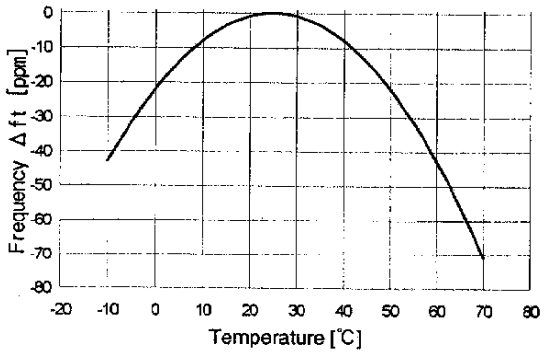
To enable the periodic interrupt set bit PIE in register B to 1 in an initialization routine.

Example Application



Reference Data

1. Frequency temperature characteristics

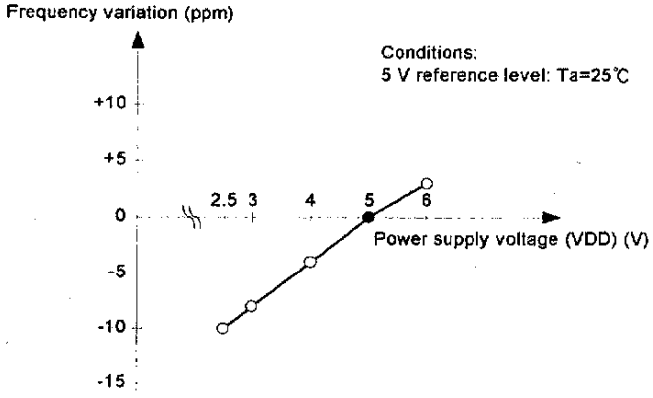


θT = 25°C TYP.
α = -0.035ppm/°C² TYP.

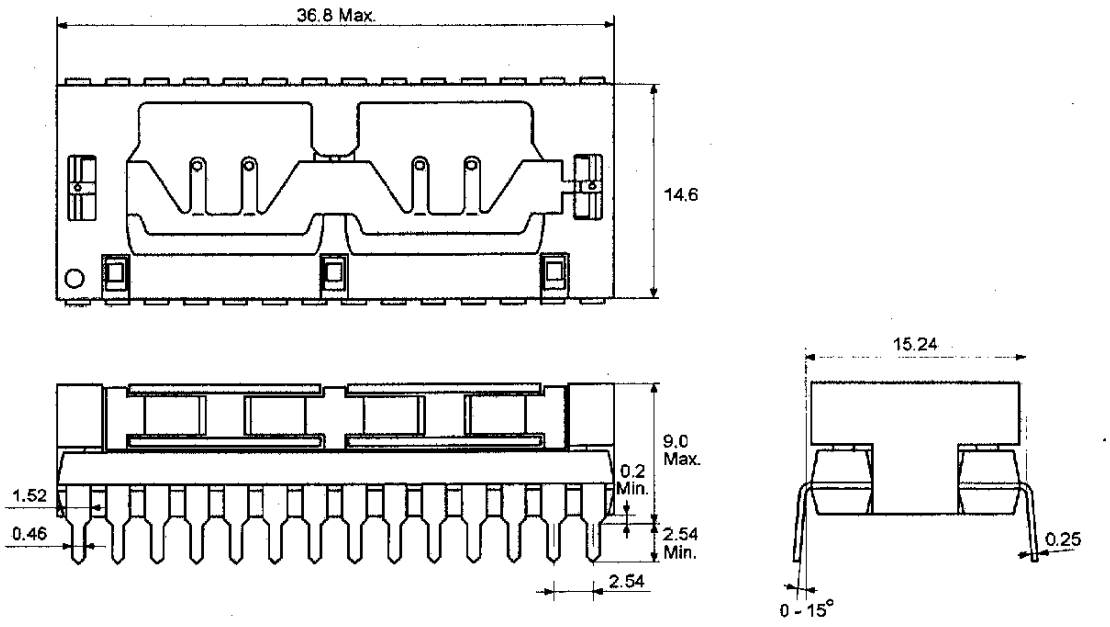
Finding the frequency stability (clock error)

1. The frequency temperature characteristics can be approximated by using the following expression:
   $\Delta f_T(ppm)=\alpha(\theta_T-\theta_X)^2$
   - Δf_T(ppm) : Frequency deviation at target temperature
   - α(ppm/℃²) : Secondary temperature coefficient (-0.035±0.005ppm/℃²)
   - θ_T(℃) : Peak temperature (25℃±5℃)
   - θ_X(℃) : Target temperature
2. To determine the overall clock accuracy, add the frequency tolerance and the voltage characteristics:
   $\Delta f/f(ppm) = \Delta f/f_0 + \Delta f_T + \Delta f_V$
   - Δf/f (ppm) : Clock accuracy at a given temperature and voltage (frequency stability)
   - $\Delta f/f_0$(ppm) : Frequency tolerance
   - Δf_T (ppm) : Temperature dependent frequency deviation
   - Δf_V (ppm) : Voltage dependent frequency deviation
3. Finding the daily deviation
   Daily deviation (seconds)=Δf/f X 10^{-6} X 86400
   The clock error is one second per day at 11.574 ppm.

2. Frequency voltage characteristics

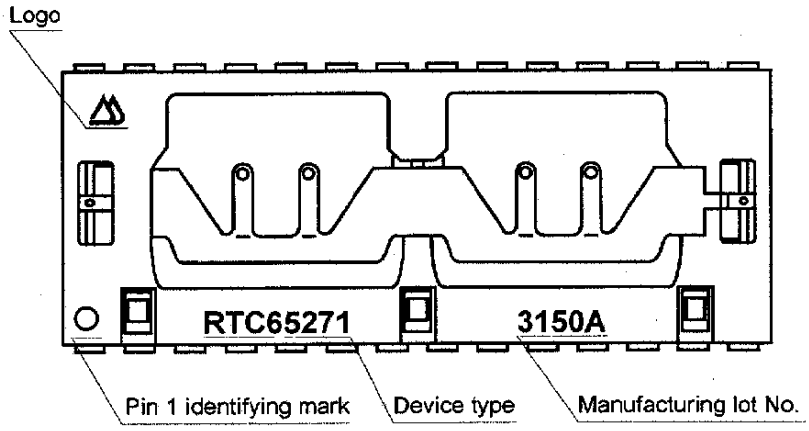


External Dimensions



All dimensions are in millimeters.

Marking Layout



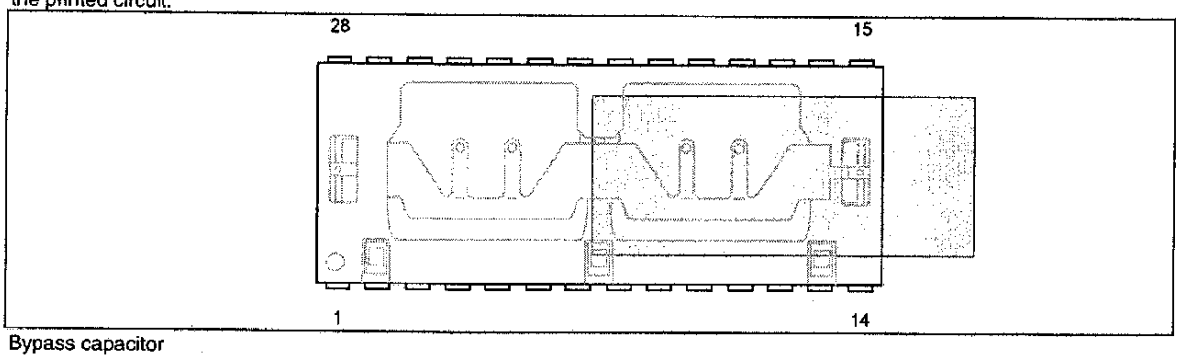
Note: The illustration is a general representation of the markings on the device, but not a detailed specification of the typeface, size, or positioning of printing used.

■ Application Notes

1. Notes on Handling

(1) Avoiding interference from signal lines

The oscillation circuit of this device has a high impedance, and is susceptible to inductance noise effects from nearby conductors. In particular the shaded portion in the figure below should be kept clear of signal lines, and if possible be within a ground land of the printed circuit.



(2) Bypass capacitor

If excessive external noise is present on the power supply, the device may malfunction or "latch up." To ensure stable operation against power supply transients and noise, connect a bypass capacitor of from 0.01µF to 0.1µF (ceramic recommended) between the VDD and GND pins. To obtain the maximum effect of noise reduction, make the circuit connection as short as possible, and the line impedance as low as possible.

(3) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such equipments which do not leak high voltages should be used with this module, which should also be grounded when such equipments are being used.

(4) Voltage levels of input pins

Intermediate voltage levels applied to the signal pins will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, ensure that all voltage levels connected to the pins are at the VDD and VSS levels.

(5) Unused signal pins

Since the input impedance of the signal pins is extremely high, operating the device with these pins open circuit can lead to malfunctions due to noise. Connect all unused signal pins to VDD or ground, or connect pull-up or pull-down resistors of not more than a few kilohms. Pins with no internal connection (N.C.) should also be connected to ground to prevent noise problems.

(6) Condensation

Operation of the device cannot be guaranteed if condensation is present. Dry the device, then power on again.

(7) Storage conditions

When storing the device in its packaging, maintain it at normal temperature and humidity to prevent packaging deterioration.

(8) Battery state during operation

If the device is powered on with no backup batteries, the battery terminals are likely to lead to noise problems, and correct operation cannot be guaranteed. Ensure that the batteries are always fitted.

2. Notes on Mounting

(1) Soldering temperature conditions

Apply solder to the lead portions only, and strictly follow the condition below. Ensure that the package temperature is kept below 150 °C

Soldering conditions: 260°C maximum x 10 seconds maximum

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, you should confirm that the module will survive the mounting process that will be used before actually using this module in full-scale production. In addition, if the mounting conditions are later changed, the survivability of the module should be reconfirmed under the new conditions.

(3) Ultrasonic cleaning

There is a possibility that the quartz crystal may be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

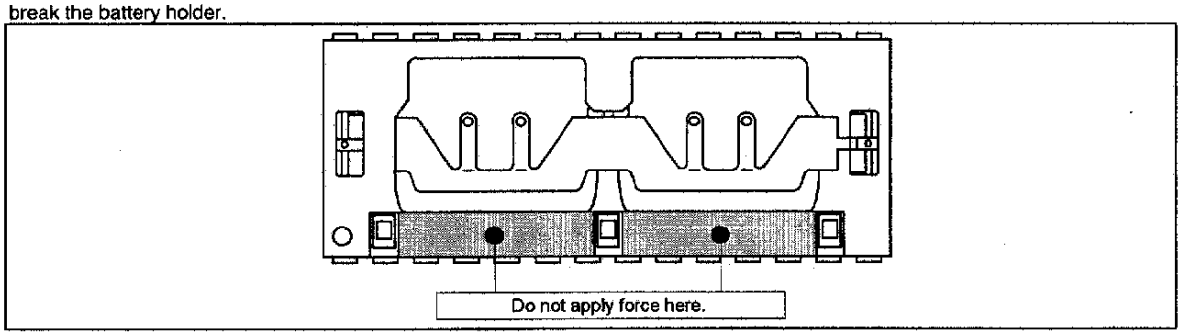
(5) Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

3. Notes on Battery Holder and Battery Handling

(1) Batteries used
Use the following type of lithium cells.
Type BR-1225 (12.5 mm diameter, 2.5 mm thickness, 3.0 V)
Do not mix old and new batteries. Do not leave exhausted batteries in place, as this can lead to electrolyte leakage, and damage to the module.

(2) Battery mounting orientation
Check that the batteries are installed with the polarity correct.

(3) Battery holder
Do not remove or modify the battery holder.
Do not apply an external power supply directly to the battery terminals.
When the batteries are not installed, be careful not to apply force to the portions indicated in the following figure. Doing so can break the battery holder.



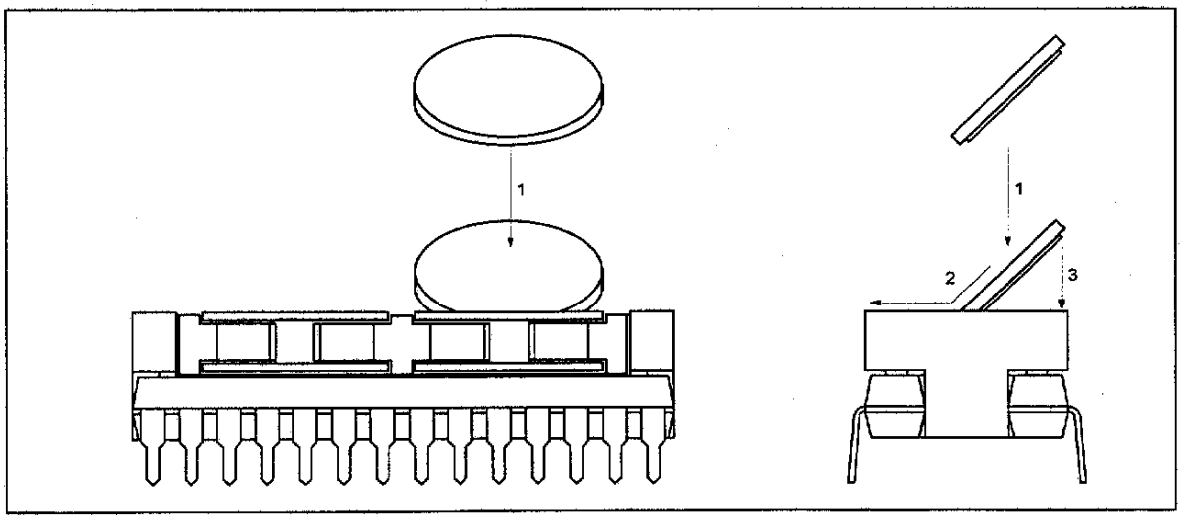
(4) Handling the batteries
Do not pick up the batteries with bare fingers or with metallic implements such as tweezers.

(5) Disposal of used batteries
This device has no internal batteries. The implementer is responsible for all matters relating to used battery disposal, including any local regulations which may apply.
End-user documentation for equipment using this device should include instructions on the use of batteries, and appropriate warnings.

4. Fitting and Removing Batteries

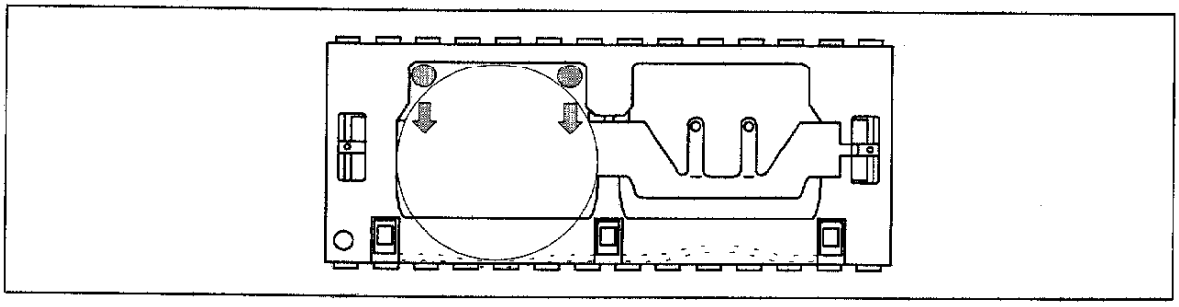
(1) Fitting
Use the procedure shown in the figure below.

1 Insert the batteries diagonally from the pin 28 side into the holder.
2 Push the batteries firmly in to the pin 1 side.
3 Press the batteries into place from above.



(2) Removal

To remove a battery, insert an insulating pointed object at the positions marked with ● in the figure below to lever out the battery. Hold your finger over the battery as you do this, as otherwise the battery will jump out.



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RTC-65271 Application Manual

New Edition
Revision 1.0: 1 April, 1994

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Cylinder type for high-frequency range, high-accuracy	**CA-303H**
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Quartz Temperature Sensor

Cylinder type	**HTS-206**

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