REAL TIME CLOCK MODULE
RTC 65 SERIES
APPLICATION MANUAL

EPSON

Contents

NOTES

- This manual is based on material as of NOVEMBER 1992.
  The contents are subject to change without notice. Please contact us separately for information regarding the product's warranty.
- In this manual, the component and circuit examples other than RTC are designed solely to describe the product and we are not responsible for any problems that may occur as a result of these examples. All behaviors must be verified by you.
- This manual neither guarantees any rights to the buyer, nor is it a commercial title or license.
- We have prepared this manual as carefully as possible. If you find it incomplete or unsatisfactory in any respect, we would welcome your comments.

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Overview

The RTC-65 series is a real-time clock that was developed as a peripheral IC for PC/AT*-compatible computers, work station or other computer systems.
The RTC-65 series has a built-in 32.768kHz crystal. Other functions include a calendar (year, month, day and day of the week), clock (hours, minutes, seconds), selection of 12-hour or 24-hour timekeeping, automatic leap year adjustment, and programmable square wave output.
Because this product is a CMOS device, it consumes little current. In addition, a special battery holder provides a backup power supply, making the RTC-6581/RTC-6591 ideal for backing up CPU data.

Product	Package Type	Extended Alarm	Battery Holder
RTC6581	DIP	Not available	Integral
RTC6583	SOP	Not available	None
RTC6587	PLCC	Not available	None
RTC6591	DIP	Available	Integral
RTC6593	SOP	Available	None
RTC6597	PLCC	Available	None

Features

1. Scope

This real time clock module is suitable for application to computer systems such as PC/AT* compatibles and work stations.

* PC/AT is a trademark of IBM Corporation in U.S.A.

2. Features

Standard features

- Available in 24-pin DIP, 24-pin SOP or 28-pin PLCC packages.
- Upward compatible with MC146818A (in 32.768 kHz mode).
- Provides 114 bytes of backed-up general purpose RAM.
- Includes a V_{DD} - V_{BAT} power switching circuit.
- Built-in 32.768 kHz crystal resonator
- Low current consumption 0.5 μA (TYP.) under back up mode. (V_{BAT} = 3.0 V, Ta = 25°C)

RTC-659X series only

- Extended alarm function is available that supports second to year. It works both the operation mode and the back up mode.

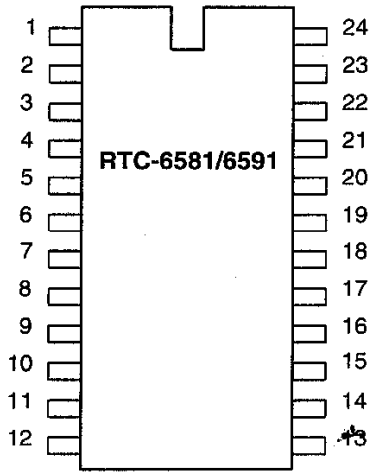
RTC-6581/6591 (DIP) only

- Built-in lithium battery holder and protection resistor (in accordance with UL).
- Batteries can be replaced.

Pinout

1. Pinout

(1) RTC-6581/6591



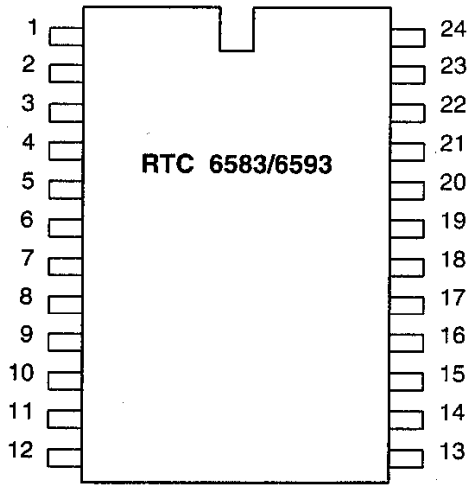
NC: Pin is not connected internally.

Pin No.	6581	6591
1	MOT	MOT
2	NC	NC
3	NC	NC
4	AD 0	AD 0
5	AD 1	AD 1
6	AD 2	AD 2
7	AD 3	AD 3
8	AD 4	AD 4
9	AD 5	AD 5
10	AD 6	AD 6
11	AD 7	AD 7
12	V_{SS}	V_{SS}

Pin No.	6581	6591
13	$\overline{CS}$	$\overline{RTC}$
14	AS	AS
15	R/$\overline{W}$	R/$\overline{W}$
16	NC	NC
17	DS	DS
18	$\overline{RESET}$	$\overline{RESET}$
19	$\overline{IRQ}$	$\overline{IRQ}$
20	NC	NC
21	NC	$\overline{XIRQ}$
22	NC	$\overline{XALM}$
23	SQW	SQW
24	V_{DD}	V_{DD}

* A bypass capacitor of 0.01μF or greater must be connected between V_{DD} and V_{SS}.

(2) RTC-6583/6593



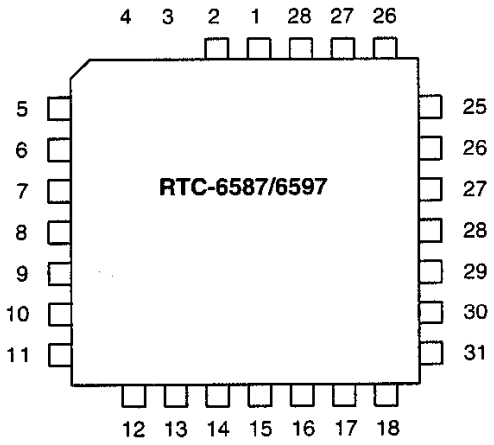
NC: Pin is not connected internally.

Pin No.	6583	6593
1	MOT	MOT
2	NC	NC
3	NC	NC
4	AD_0	AD_0
5	AD_1	AD_1
6	AD_2	AD_2
7	AD_3	AD_3
8	AD_4	AD_4
9	AD_5	AD_5
10	AD_6	AD_6
11	AD_7	AD_7
12	V_{SS}	V_{SS}

Pin No.	6583	6593
13	$\overline{CS}$	$\overline{RTC}$
14	AS	AS
15	R/$\overline{W}$	R/$\overline{W}$
16	NC	NC
17	DS	DS
18	$\overline{RESET}$	$\overline{RESET}$
19	$\overline{IRQ}$	$\overline{IRQ}$
20	V_{BAT}	V_{BAT}
21	NC	$\overline{XIRQ}$
22	NC	$\overline{XALM}$
23	SQW	SQW
24	V_{DD}	V_{DD}

* A bypass capacitor of 0.01μF or greater must be connected between V_{DD} and V_{SS}.

(3) RTC-6587/6597



NC: Pin is not connected internally.
NP: No physical pin

Pin No.	6587	6597
1	NC	NC
2	MOT	MOT
3	NP	NP
4	NP	NP
5	AD 0	AD 0
6	AD 1	AD 1
7	AD 2	AD 2
8	AD 3	AD 3
9	AD 4	AD 4
10	AD 5	AD 5
11	NC	NC
12	AD 6	AD 6
13	NC	NC
14	AD 7	AD 7

Pin No.	6587	6597
15	VSS	VSS
16	$\overline{CS}$	$\overline{RTC}$
17	AS	AS
18	NC	NC
19	R/$\overline{W}$	R/W
20	NC	NC
21	DS	DS
22	$\overline{RESET}$	$\overline{RESET}$
23	$\overline{IRQ}$	$\overline{IRQ}$
24	VBAT	VBAT
25	NC	$\overline{XIRQ}$
26	NC	$\overline{XALM}$
27	SQW	SQW
28	VDD	VDD

* A bypass capacitor of 0.01µF or greater must be connected between VDD and VSS.

2. Signal Descriptions

(1) V_{DD},V_{SS} -- Power Supply

D.C.power is provided to the device on these pins. V_{DD} is the +5V input. When V_{DD} is applied within normal limits, the device is fully accessible and data can be written and read. When V_{DD} is below V_{ENABLE}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{DD} falls below V_{SWITCH}, the RAM and Real Time Clock are switched over to the power supply from the V_{BAT} pin. The timekeeping function maintains an accuracy of approximately 1 minute per month at 25°C regardless of the voltage input on the V_{DD} pin.

(2) MOT -- Mode Select (input)

The MOT pin offers the flexibility to choose between two bus types. When connected to V_{DD}, the Motorola bus timing is selected. When connected to V_{SS} or disconnected, the Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20kΩ.

(3) AD_0-AD_7 -- (Multiplexed Bi-Directional Address/Data Buses)

Multiplexed buses save pins because address information and data information time share the same signal paths. The address are presented during the first portion of the bus cycle and the same pins and signal paths are used for data in the second portion of the cycle. Address/data multiplexing does not slow the access time of the Real Time Clock since the bus change from address to data occurs during the internal RAM access time.Address must be valid prior to the falling edge of AS or ALE, at which time the Real Time Clock latches the address from AD_0 to AD_6.Valid write data must be present and held stable during the latter portion of the DS or WR pulses.In a read cycle the Real Time Clock outputs of 8 bits data during the latter portion of the RD or DS pulses. The read cycle is terminated and the bus return to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

(4) AS -- Address Strobe (input)

A positive going address strobe pulse serves to demultiplex the bus.The falling edge of AS/ALE cause the address to be latched within the Real Time Clock.

(5) DS -- Data Strobe or Read Strobe (input)

The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{DD},Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the module is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the module to latch the written data.
When the MOT pin is connected to V_{SS},Intel bus timing is selected. In this mode the DS pin is called Read(RD). RD identifies the time period when the module drives the bus with read data.The RD signal is the same definition as the Output Enable(OE)signal on a typical memory device.

(6) R/$\overline{W}$ -- Read/Write(input)

The R/$\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{DD} for Motorola timing, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated by a high level on R/$\overline{W}$ while DS is high. For write cycles, R/$\overline{W}$ is low while DS is high.
When the MOT pin is connected to V_{SS} for Intel bus timing, the R/$\overline{W}$ signal is an active low signal called $\overline{WR}$. In this mode the R/$\overline{W}$ pin has the same meaning as the Write Enable signal (WE) on a generic RAM.

(7) $\overline{RTC}$ ($\overline{CS}$)-- Real Time Clock Select (input)

The Real Time Clock Select signal must be asserted low for a bus cycle in which the Real Time Clock and RAM module are to be accessed. $\overline{RTC}$ must be kept in the active state ("L") during DS and AS is High for Motorola timing and during RD and WR is Low for Intel timing. Bus cycles which take place without asserting $\overline{RTC}$ will latch addresses but no access will occur. When V_{DD} is below V_{ENABLE}, the module internally inhibits access cycles by internally disabling the RTC input. This action protects both the Real Time Clock data and RAM data during power failures.

(8) $\overline{XALM}$ -- Extended Alarm Select (For RTC-6591/6593/6597 only.)

The Extended Alarm Select signal must be asserted low for a bus cycle in which the extended alarm registers of the module are to be accessed. $\overline{XALM}$ must be kept in the active state during DS and AS is High for Motorola timing and during RD and WR is Low for Intel timing. Bus cycles which take place without asserting $\overline{XALM}$ will latch addresses but no access will occur. When V_{DD} is below V_{ENABLE} ,the module internally inhibits access cycles by internally disabling the $\overline{XALM}$ input. This action protects the extended alarm data during power outages.
This pin is provided with an internal pull-up resistor.

(9) $\overline{IRQ}$ -- Interrupt Request (output)

The IRQ signal is an active low, open drain output that is used as a processor interrupt request. The $\overline{IRQ}$ output follows the state of the interrupt pending bit (bit 7) in status register C. $\overline{IRQ}$ may be asserted by the alarm, update ended or periodic interrupt functions depending on the configuration of register B.

(10) $\overline{XIRQ}$ -- Extended alarm interrupt request (For RTC-6591/6593/6597 only.)

The $\overline{XIRQ}$ signal is an active low, open drain output that is used as a processor interrupt request. $\overline{XIRQ}$ may be asserted by the extended alarm functions depending on the configuration of extended alarm register 6 and 7.
This pin is active even during backup by a battery .

(11) $\overline{RESET}$ -- Reset (input):

The reset signal is used to initialize certain registers to allow proper operation of the module. When $\overline{RESET}$ is low, the following occurs:

① The following register bits are cleared:
   a. Periodic interrupt enable (PIE).
   b. Alarm interrupt enable (AIE).
   c. Update ended interrupt (UF).
   d. Interrupt request flag (IRQF).
   e. Periodic interrupt flag (PF).
   f. Alarm interrupt flag (AF).
   g. Square wave output enable (SQWE).
   h. Update ended interrupt enable (UIE).
② The $\overline{IRQ}$ pin is in the high impedance state.
③ The module is not processor accessible.

(12) V_{BAT} -- Back-up power supply (RTC-6583/6593, RTC-6587/6597 only. Input)

The V_{BAT} pin supplies the device with power while the system is powered off or in stand-by mode. This input is designed for a 3.0V lithium battery.

V_{ENABLE} (Internal chip enable voltage) = $V_{BAT} \times$ 1.3[V] (TYP.)
V_{CHECK} (VRT bit threshold voltage) = 2.50V (TYP.)
V_{BAT} operation current = 1000 nA(MAX.),500 nA (TYP.)

This device is optimized for a lithium battery. If an another power source is used the application must not allow the charging voltage at V_{BAT} pin to exceed $V_{BAT} \times 1.3$(TYP.).
If the voltage on the V_{BAT} pin is too great, the device's internal chip enable circuit disallows access to the device.

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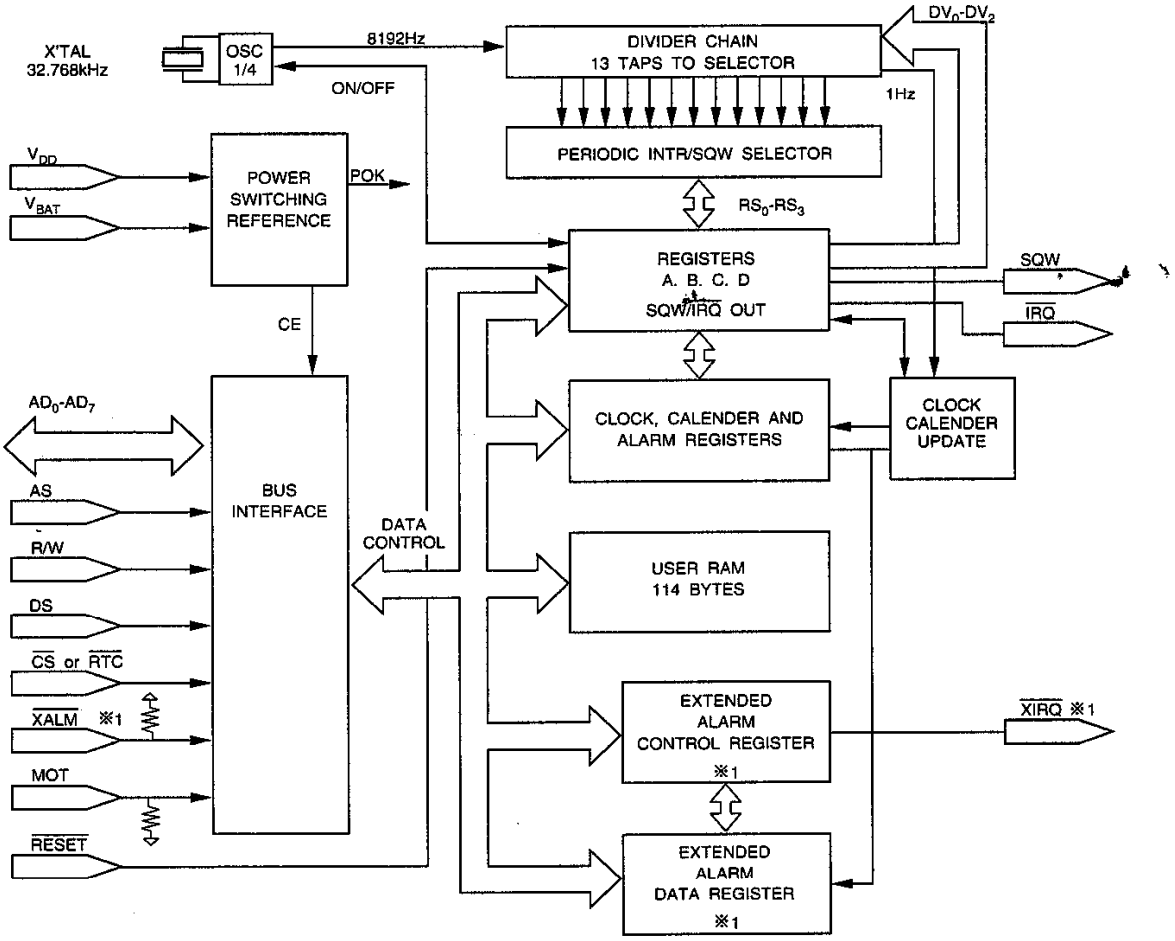
Block Diagram



※ 1 For RTC-6591/6593/6597 only.

Absolute Maximum Ratings

Item	Symbol	Conditions (Pins)	Specifications	Unit
Supply voltage	V_{DD}	V_{DD}-V_{SS}	−0.3 to +7.0	V
Input voltage	V_{IN}	Input Pin	Vss−0.3 to VDD +0.3	
Storage temperature	T_{STG}	Note 1	(RTC-6581/6591) −40 to +85 (RTC-6583/6587/6597) −55 to 125	°C
Soldering conditions	T_{SOL}	RTC-6681/6591	260°C or less, for within 10 seconds. Package temperature should be 150°C or less	
		RTC-6583/6593 RTC-6587/6597	Twice under 260°C for within 10 sec. or under 230ÉC within 3 min.	

Note 1: Storage temperature as a discrete component.

Operating Conditions

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.0	5.5	V	Between V_{DD} and V_{SS}
Battery voltage	V_{BAT}	Note 2	3.0	Note 2	V	Between V_{BAT} and V_{SS}
Operating temperature	T_{OPR}	−10	—	+70	°C	

Note 2: Please refer to V_{ENABLE} and V_{CHECK} voltage (p. 14).

Electrical Characteristics

1. Frequency Characteristics

Item	Symbol	Conditions	MAX.	Unit
Frequency tolerance	Δf/f0	Ta = 25° C V_{DD} = 5.0V	5 ± 20	ppm
Aging	fa	Ta = 25° C, V_{DD} = 5.0V, first year	± 5	ppm/y
Temperature characteristics	top	V_{DD} = 5.0V, Ta = −10 to 70°C Note 3	+ 10 −120	ppm
Voltage characteristics	fv	Ta = stable Note 3	± 6	ppm/V

Note 3: The frequency deviation (0ppm) at Ta = 25°C for "top" or at V_{DD} = 5V for "fv" is used as the reference value.

Remarks: Clock accuracy at 25°C is from −1.6 seconds/day to +2.4 seconds/day (5 ± 20ppm). (Clock accuracy will differ in environments where the temperature is not 25°C.)

2. DC Characteristics

V_{DD} = 5.0V ± 10%, Ta = −10 to 70°C

Characteristic	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input High Voltage	V_{IH}		2.2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		−0.3		0.8	V
Input Leakage	I_I	A_0 to A_7, D_0 to D_7, AS, DS, R/$\overline{W}$, $\overline{CS}$ or $\overline{RTC}$			±1	μA
Output Low Voltage	V_{OH}	V_{DD} = 5.0V I_{LOAD} = − 4.0mA	2.4			V
Output Low Voltage	V_{OL}	V_{DD} = 5.0V I_{LOAD} = 4.0mA			0.4	V
Power Supply Current	I_{DD}	Output Unloaded, 8.192kHz, non access time		3	10	mA
Input Current	* I_{XALM}	$\overline{XALM}$ = V_{SS}			−500	μA
Input Current	* I_{XALM}	$\overline{XALM}$ = V_{DD}			2	μA
Input Current	I_{MOT}	MOT = V_{SS}			−2	μA
Input Current	I_{MOT}	MOT = V_{DD}			500	μA
Battery Supply Current	I_{BAT}	V_{BAT} = 3V, V_{DD} = 0V, Ta = 25°C			1	μA

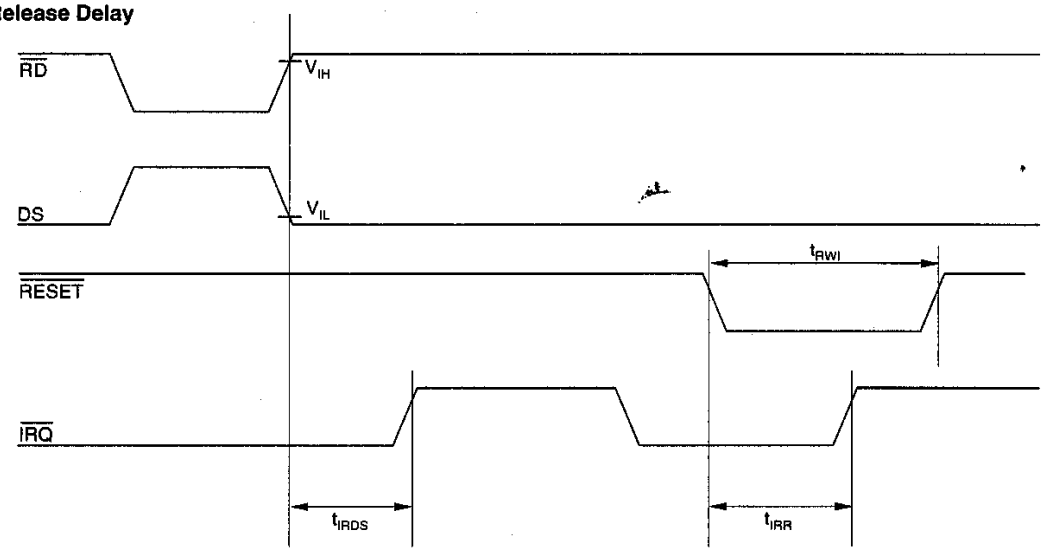
* RTC-6591/6593/6597 only.

3. Switching Characteristics

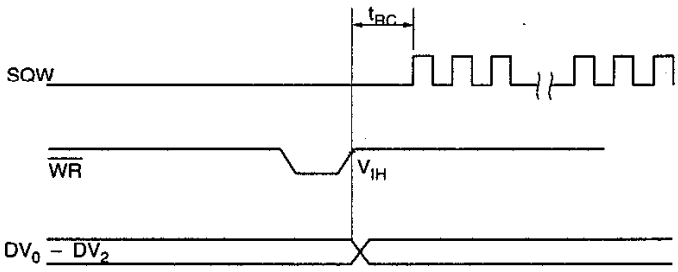
−10 to 70°C, V_{DD} = 4.5V to 5.5V

Characteristic	Symbol	Test Condition	MIN.	MAX.	Unit
Reset Pulse Width	tRWL	—	5		µs
Oscillator Startup	tRC	After DV bits have been enabled by software.		1	sec.
IRQ Release from DS Low	tIRDS	—		2	µs
IRQ Release from Reset Low	tIRR	—		2	µs
VRT Bit Delay	tVRTD	VDD > VENABLE		1	µs

$\overline{IRQ}$ Release Delay



Oscillator Start Up



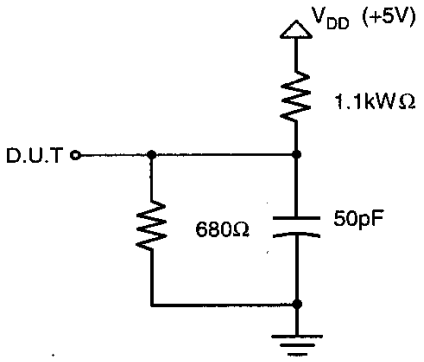
Note: V_{DD} = 4.5V to 5.5V
V_{IH} = 2.2V V_{IL} = 0.8V V_{OH} = 2.4V V_{OL} = 0.4V
Timing assumes RS_3 – RS_0 Bits = 0011.
Writing patterns of 000 to 010 to DV bits.

4. Bus Timing

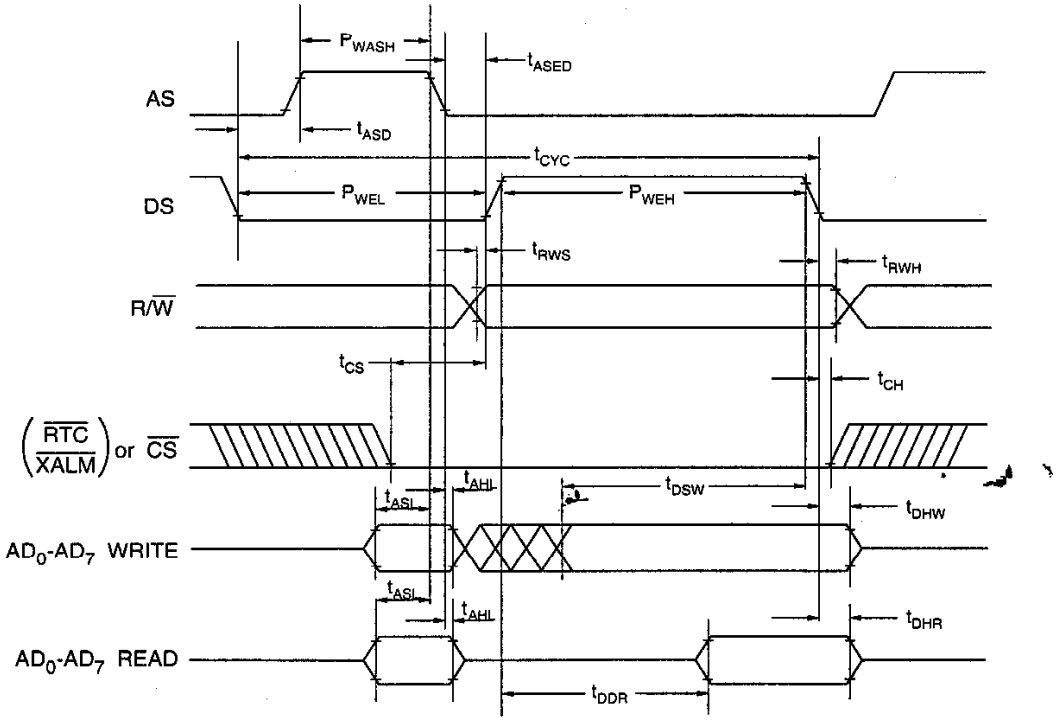
Ta=–10°C to 70°C, V_{DD} = 4.5V to 5.5V

Parameter	Symbol	MIN.	MAX.	Unit
Cycle time	tCYC	953	DC	ns
Pulse width DS/E low or $\overline{RD}$/$\overline{WR}$ high	PWEL	300	—	ns
Pusle width DS/E high or $\overline{RD}$/$\overline{WR}$ low	PWEH	325	—	ns
Input RISE/FALL time	tR, tF	—	30	ns
R/$\overline{W}$ hold time	tRWH	10	—	ns
R/$\overline{W}$ setup time before DS/E	tRWS	80	—	ns
Chip select setup time before DS, $\overline{WR}$ or $\overline{RD}$	tCS	25	—	ns
Chip select hold time	tCH	0	—	ns
Read data hold time	tDHR	10	100	ns
Write data hold time	tDHW	0	—	ns
Multiplexed address valid time to AS/ALE fall	tASL	50	—	ns
Multiplexed address hold time	tAHL	20	—	ns
Delay time DS/E to AS/ALE rise	tASD	50	—	ns
Pulse width AS/ALE high	PWASH	135	—	ns
Delay time AS/ALE to DS/E rise	tASED	60	—	ns
Output data delay time from DS/E or $\overline{RD}$	tDDR	20	240	ns
Write Data setup time	tDSW	200	—	ns

Output Load



For Motorola Timing

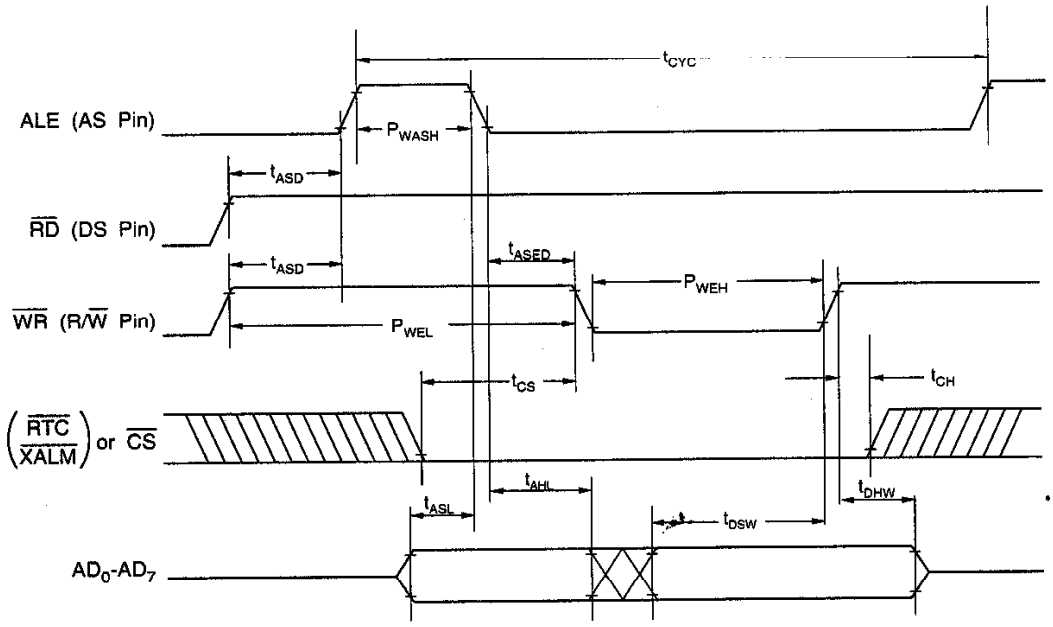


Notes: V_{DD} = 4.5V to 5.5V

V_{IH} = 2.2V V_{OH} = 2.4V

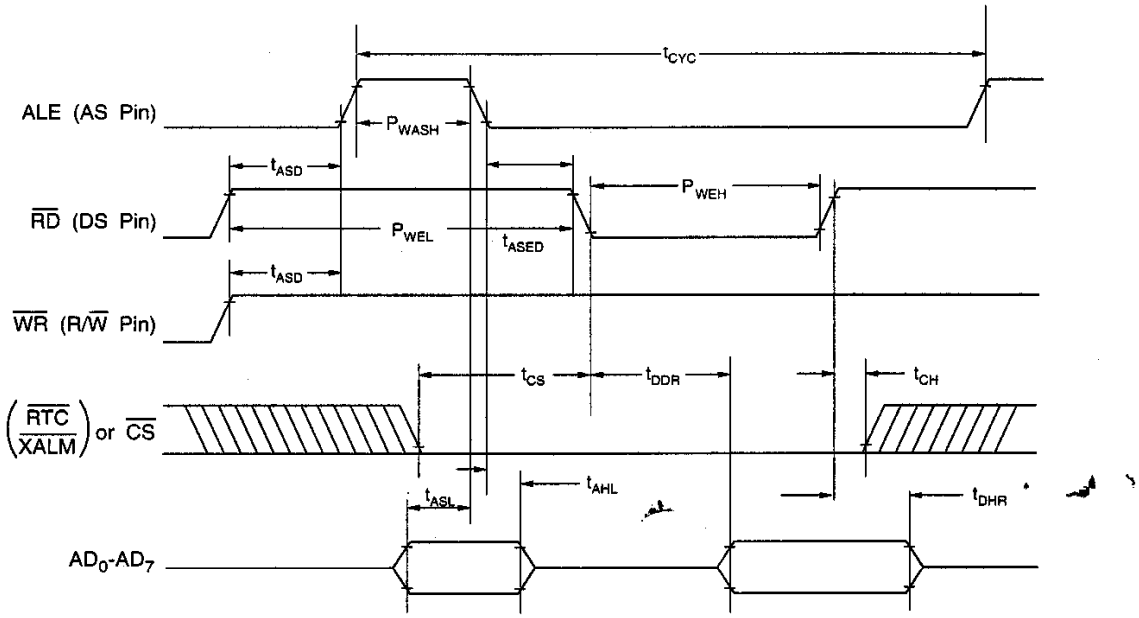
V_{IL} = 0.8V V_{OL} = 0.4V

For Intel Write Timing



Notes: V_{DD} = 4.5V to 5.5V
V_{IH} = 2.2V V_{OH} = 2.4V
V_{IL} = 0.8V V_{OL} = 0.4V

For Intel Read Timing

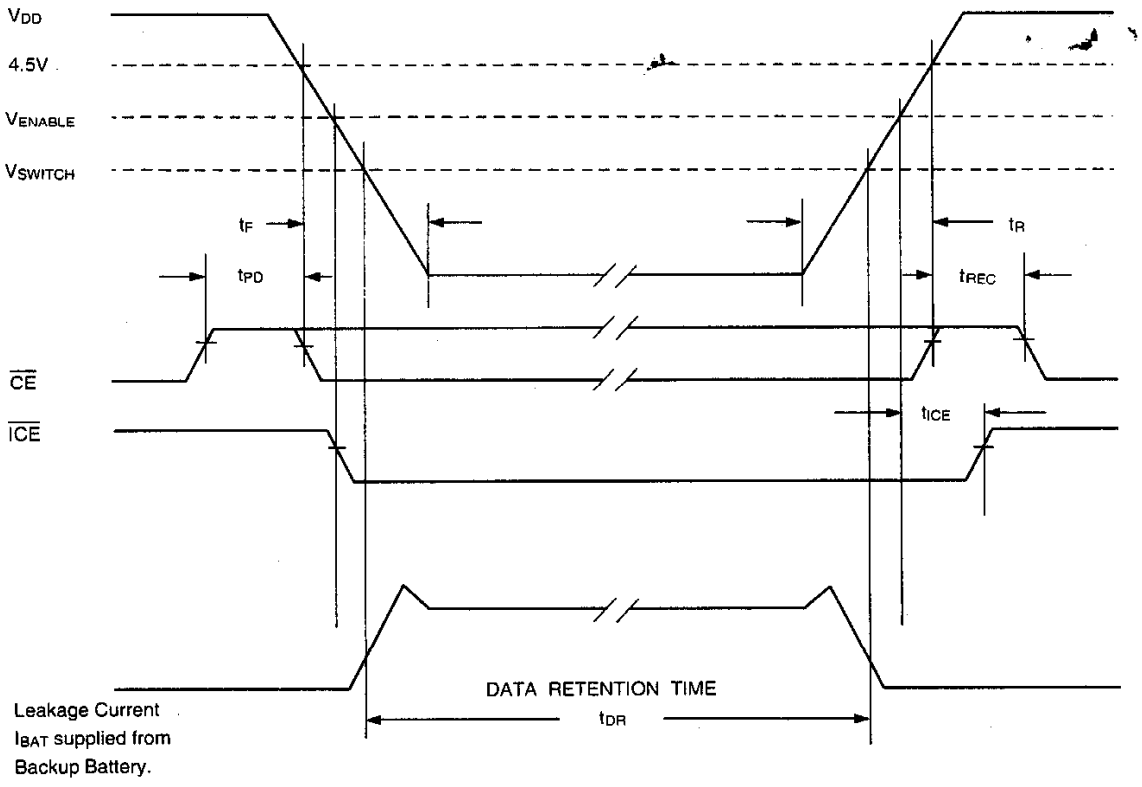


Notes: V_{DD} = 4.5V to 5.5V
V_{IH} = 2.2V V_{OH} = 2.4V
V_{IL} = 0.8V V_{OL} = 0.4V

5. Power Down/Power Up Timing

Parameter		Symbol	MIN.	MAX.	Unit
Time for $\overline{CE}$ = VIH before power (4.5V) down		tPD	0	—	µs
Time for VDD to drop from 4.5V to 0.0V ($\overline{CE}$ = VIH)		tF	66	—	µs
Time for VDD to rise from 0.0V to 4.5V ($\overline{CE}$ = VIH)		tR	22	—	µs
Time for $\overline{CE}$ = VIH after power (4.5V) on.		tREC	200	—	ms
Power switching threshold value.		VSWITCH	VBAT-0.1	VBAT+0.3	V
Chip enable threshold value.	1.3 (TYP) × VBAT >VR	VENABLE	VBAT × 1.25± 0.05	VBAT × 1.35± 0.05	V
	VR, 1.3 (TYP) × VBAT	VENABLE	1.5	3.1	V
Battery check voltage		VCHECK	2.25	2.75	V
$\overline{ICE}$ rise time after power on		tICE	20	200	ms
Power on reset threshold voltage		VR	1.5	3.1	V

Power Down/Power Up Relationships



$\overline{CE}$ = External Chip Enabled for access, i.e., { ($\overline{RD}$ or $\overline{WR}$) and ($\overline{CS}$) for RTC-658 series, ($\overline{RD}$ or $\overline{WR}$) and ($\overline{XALM}$ or $\overline{RTC}$) for RTC-659 series.

$\overline{ICE}$ = Internal Chip Enable

Functions

1. Power-down/Power-up Considerations

When a suitable back-up voltage is supplied to the V_{BAT} pin, the Real Time Clock module will continue to operate and all of the RAM, time, calendar, alarm, and extended alarm memory locations will remain non-volatile regardless of the voltage level of V_{DD}. When the voltage level applied to the V_{DD} input is greater than V_{ENABLE}, the module becomes accessible within 200 ms provided that the oscillator and countdown chain have been programmed to be running. This time period allows the module to stabilize after power is applied. When V_{DD} falls below V_{ENABLE}, the chip select inputs, $\overline{RTC}(\overline{CS})$ or $\overline{XALM}$, are forced to an inactive state regardless of the state of the pin signals. This puts the module into a write protected mode in which all inputs are ignored and all outputs are in a high impedance state. Furthermore, when V_{DD} falls below V_{SWITCH}, the module is switched over to a battery power source or V_{BAT} so that power is not interrupted to time keeping and non-volatile RAM functions.

2. Address Map

The registers of the device appear in two distinct address ranges. One set of registers is active when $\overline{RTC}(\overline{CS})$ is asserted low and represents the real time clock. The second set of registers is active when $\overline{XALM}$ is asserted low and represents the extended alarm. (RTC-6591/6593/6597 only)

(1) RTC Address Map: The address map of the RTC module is shown in the following.
The address consists of 114 bytes of general purpose RAM, 10 bytes of RTC/calendar information, and 4 bytes of status and control information.
① Registers C and D are Read Only (Status information)
② Bit 7 of Register A is Read Only
③ Bit 7 of the "Seconds" byte (00) is Read Only

(2) Extended alarm Address Map: (RTC-6591/6593/6597 only)

The address map of the extended alarm is shown in the following. The address consists of six bytes of full alarm information and two bytes of control and status information.

Address Map Real-time-clock

00	14 bytes	00H	0	Seconds
			1	Seconds Alarm
			2	Minutes
13		0DH	3	Minutes Alarm
		0EH	4	Hours
14			5	Hours Alarm
			6	Day of the Week
			7	Day of Month
			8	Month
	114 bytes		9	Year
			10	Register A
			11	Register B
			12	Register C
			13	Register D
			14	General purpose RAM
127		7FH	127	

Address Map Extended Alarm (RTC-6591/6593/6597 only)

00	8 bytes	00H	0	Extended Seconds Alarm
			1	Extended Minutes Alarm
			2	Extended Hours Alarm
			3	Extended Day of the Week Alarm
			4	Extended Day of Month Alarm
			5	Extended Month Alarm
			6	Register 6
07		07H	7	Register 7

3. Time, Calendar, Alarm,and Extended alarms Locations (659X series only)

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, alarm, and extended alarm are set or initialized by writing to the appropriate RAM bytes. The contents of the sixteen time, calendar, alarm, and extended alarm bytes may be either binary or binary coded decimal (BCD) format. Before writing to the internal time, calendar, alarm, and extended alarm registers, the SET access bit in register B should be set to one. This prevents updates from occurring while the access is being attempted. In addition to writing to the sixteen time, calendar, alarm, and extended alarm registers in a selected format (binary or BCD), the Data Mode (DM) bit of register B must be set to the appropriate logic level. All sixteen time, calendar, alarm, and extended alarm registers must use the same data mode. The SET bit in register B should be cleared after the DM bit has been written to allow the Real Time Clock (RTC) to update the time and calendar bytes.

Once initialized, the RTC makes all the updates in the selected mode. The data mode cannot be changed without reinitializing all sixteen data bytes. The following table shows the binary and BCD formats of the sixteen time, calendar, alarm, and extended alarm locations. The 24/$\overline{12}$ bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents p.m. when it is one. Once per second, the time and calendar bytes are advanced and a check for alarm and extended alarm conditions are made. If a read of the time and calendar information is made during an update cycle, it is possible that the seconds, minutes, hours etc. data may not correlate. The probability of reading the incorrect time is low, but this possibility should be considered. See also Section 9.

The calendar compensates for leap years and advances the date of the month through 29 in February of a leap year. The calendar does not compensate for leap centuries and will always make the 00 year a leap year. The year 2000 will be correctly compensated by providing 29 days in February, but 2100 will be erroneous and require manual intervention.

Time Calendar And Alarm Data Modes

$\overline{CS}$	ADRS	Function	DEC	Range	Range
				Binary Data Mode	BCD Data Mode
$\overline{RTC}$ or $\overline{CS}$ ="L"	0	Seconds	0-59	00-3B	00-59
	1	Seconds Alarm	0-59	00-3B	00-59
	2	Minutes	0-59	00-3B	00-59
	3	Minutes Alarm	0-59	00-3B	00-59
	4	Hours-12 Hour Mode	1-12	01-0C am, 81-8C pm	01-12 am, 81-92 pm
		Hours-24 Hour Mode	0-23	00-17	00-23
	5	Hours Alarm-12 Hour Mode	1-12	01-0C am, 81-8C pm	01-12 am, 81-92 pm
		Hours Alarm-24 Hour Mode	0-23	00-17	00-23
	6	Day of Week (Sunday=1)	1-07	01-07	01-07
	7	Day of Month	1-31	01-1F	01-31
	8	Month	1-12	01-0C	01-12
	9	Year	0-99	00-63	00-99
* $\overline{XALM}$ ="L"	0	Extended Seconds Alarm	0-59	00-3B	00-59
	1	Extended Minutes Alarm	0-59	00-3B	00-59
	2	Extended Hours-12 Hour Mode	1-12	01-0C am, 81-8C pm	01-12 am, 81-92 pm
		Extended Hours-24 Hour Mode	0-23	00-17	00-23
	3	Extended Day of Week (Sunday=1)	1-07	01-07	01-07
	4	Extended Day of Month	1-31	01-1F	01-31
	5	Extended Month Alarm	1-12	01-0C	01-12

* For RTC-6591/6593/6597 only.

4. Non-volatile RAM

The 114 bytes general purpose non-volatile RAM are not dedicated to any specific function. They may be accessed by the processor as non-volatile memory at any time, even during an update cycle.

5. $\overline{IRQ}$ Interrupts

The module includes three separate, fully automatic sources of $\overline{IRQ}$ interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates of 500 ms to 122 µs. The update-ended interrupt may be used to indicate to the processor that an update cycle is complete. Each of these interrupt conditions is described in greater detail in the following sections.

(1) Enabling Interrupts

Three bits in Register B are used to select which source or sources of interrupt will be enabled. Setting the appropriate interrupt-enable bit to 1 permits the interrupt to be initiated when the interrupt event occurs. A 0 interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, the $\overline{IRQ}$ pin is asserted immediately even though the event causing the interrupt may have occurred much earlier. As a result, there are cases where the program should clear any pending interrupt conditions before enabling new interrupts.

(2) Interrupt Status

Register C is used as an interrupt status register. Three flag bits correspond to the three interrupt sources. These three bits are set respectively when the appropriate interrupt condition is satisfied regardless of the setting of interrupt enable bits in register B. These flag bits can be used in a polling mode without enabling the corresponding interrupt enable bits. When a flag bit is set in register C, this is an indication to the program that an interrupt event has occurred since the register C has last been read. The act of reading register C clears all flag bits. Therefore all flag bits should be examined by software upon each read of register C to insure that no interrupts are lost. Interrupt flags are double buffered so that new interrupt events are held pending.

If an interrupt enable bit in register B is set and its corresponding interrupt flag in register C is also set, the $\overline{IRQ}$ bit is asserted low. The $\overline{IRQ}$ bit is asserted low as long as at least one of the three interrupt sources has both its flag bit (in register C) and its enable bit(in register B) set. The IRQF bit in register C will read logic as the $\overline{IRQ}$ pin is being driven low. The microprocessor can determine if the real time clock module has initiated the interrupt by reading register C. A logic one in the bit 7 position of register C indicates that one or more interrupts have been initiated by the real time clock module. The act of reading register C clears all active flag bits and the IRQF bit.

(3) Periodic Interrupt

The periodic interrupt will cause the RTC module to generate an interrupt at time intervals ranging from 122 µs to 500 ms. This function is separate from the alarm function which may generate interrupts at intervals of once per second to once per day. The periodic interrupt rate is selected using the RS_0 - RS_3 bits in register A. Changing the RS bits affect both the periodic interrupt rate and the square wave output rate.

(4) Update (Cycle) Ended Interrupt

The Update-In-Progress (UIP) bit in register A pulses once per second whenever an update cycle occurs. The Update ended interrupt Flag (UF) will be set at conclusion of the update cycle or when the UIP bit in register A toggles from logic 1 to logic 0. If the Update-ended Interrupt Enable (UIE) bit in Register B is also set, the $\overline{IRQ}$ pin will be asserted low.

(5) Alarm Interrupt

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is set to logic 1.
Second, it is used to insert a "don't care code" into one or more of the three alarm bytes. The "don't care code" is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when they are set to logic 1. An alarm each hour occurs when "don't care codes" are written in the hours alarm locations.

6. XIRQ Interrupt: (For RTC-6591/6593/6597 only)

The extended alarm functions provide the additional interrupt signal $\overline{XIRQ}$. This is independent of the alarm functions using the $\overline{IRQ}$ interrupt. The extended alarm interrupt may be programmed to occur at rates from once per second to once per year. This interrupt may be used as a wake-up system for a main CPU.
This interrupt condition is described in greater detail in the following sections.
This interrupt is active even during battery backup.

(1) Enabling the extended alarm interrupt: (For RTC-6591/6593/6597 only)

The XAIE bit in register 6 of Extended alarm area indicates whether the interrupt is enabled. Writing 1 to the XAIE bit permits the interrupt to occur when the extended alarm interrupt event occurs. A 0 in the XAIE bit prohibits the $\overline{XIRQ}$ pin from being asserted from that interrupt condition. If an extended alarm interrupt flag is already set when an interrupt is enabled, the $\overline{XIRQ}$ pin is asserted immediately even though the event causing the interrupt may have occurred much earlier.

(2) Extended alarm interrupt Status: (For RTC-6591/6593/6597 only)

The XAF bit of register 7 of extended alarm area is used as an interrupt status register. This bit is set respectively when the appropriate interrupt condition is satisfied regardless of the setting of XAIE bit in register 6. This flag bit can be used in a polling mode without enabling the corresponding XAIE bit. When the XAF bit is set in register 7,this is an indication to the program that an extended alarm interrupt event has occurred since the register 6 was last read. Interrupt flags are double buffered so that new interrupt events are held pending.

If the XAIE bit in register 6 is set and its corresponding interrupt flag in register 7 is also set, the $\overline{XIRQ}$ pin is asserted low.The $\overline{XIRQ}$ pin is asserted low as long as at the extended alarm interrupt source has both its XAF bit and its XAIE bit set. The microprocessor can determine if the RTC module has initiated the extended alarm interrupt by reading the XAF bit in register 6. A one in the XAF bit indicates that the extended alarm interrupt has been initiated by the RTC module. The act of reading register 7 clear the XAF bit.

(3) Extended alarm Interrupt: (For RTC-6591/6593/6597 only)

The six alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate locations, the alarm interrupt is initiated at the specified time each year if the XAIE bit is set to one. Second, it is used to insert a "don't care code" into one or more of the six alarm bytes. The "don't care code" is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when they are set to logic one. An alarm each hour occurs when "don't care codes" are written in the hours, day-of-week, day and month alarm locations.

7. Oscillator Control Bits

When power is first supplied, the status of these bits is indeterminate. After the batteries are installed, a pattern of 000 should be written to the module to turn off the oscillator to prevent the battery power source from being used.

A pattern of 010 in bits 4 through 6 of register A will turn on the oscillator and enable the countdown chain . A pattern of 11X will turn on the oscillator but will leave the countdown chain reset. Please refer Register A-(2) about DV_0 to DV_2 bits as details.

8. Square Wave Output Selection

Thirteen of the fifteen divider taps are made available to a 1 of 15 selector. The divider taps may be used for two purposes: first, to generate a fixed frequency square wave output signal on the SQW pin; second, to generate interrupts at a selected frequency. The RS_0-RS_3 bits in register A establish the square wave output frequency and/or interrupt rate. These frequencies are listed in Register A-(3). Once the frequency is selected, the SQW pin signal may be enabled or disabled under program control using the Square Wave Enable (SQWE) bit in Register B.

9. Update Cycle

The RTC module executes an update cycle once per second. The primary purpose of the update cycle is to increment the clock/calendar by one second and to compare the updated time to the two alarm times.

If the time matches the Real-Time-Clock alarm at the end of the update cycle, then the Alarm Flag (bit 5 of Register C) is set. If Alarm Interrupt Enable (bit 5 of Register B)is set, an Interrupt Request is generated on the $\overline{IRQ}$ pin and the IRQF (bit 7 of Register C) is also set.

If the time matches the extended alarm at the end of the update cycle, then the XAF bit is also set. If XAIE is set, an extended alarm interrupt request is generated on the $\overline{XIRQ}$ pin. (For RTC-6591/6593/6597 only.)

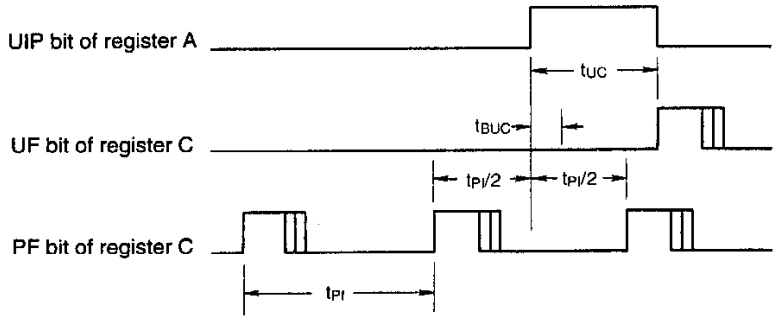
At the end of every update cycle, the Update Flag (bit 4 of Register C) is set. If the Update ended Interrupt Enable (bit 4 of Register B) is set then an Interrupt Request is generated and the IRQF is set.

There are three methods which can be employed to accurately access time, date and calendar data from the real time clock module. The first uses the update-ended interrupt. If this interrupt is enabled, an interrupt occurs after every update cycle. Immediately following this interrupt, the processor has 998 ms in which to read time and date information before the next update cycle. If the processor reads the time and date within this interval, no possibility exists for reading inconsistent time and calendar data. As with all interrupts, the IRQF bit in Register C should be cleared before leaving the interrupt service routine.

Using the second method for reading time and date, the processor polls the Update-In-Progress (UIP) bit in Register A to determine if the update cycle is in progress. The UIP bit will pulse once each second. After the UIP bit goes to one, the update transfer occurs 244 µs later. If the UIP bit is 0, the processor has at least 244 µs before the time/date data will be updated. Therefore the system should insure that interrupts and DMA activity do not preclude reading the time and date information within 244 µs.

The third method uses the periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is pulsed high half way between two PF bit pulses in Register C. The processor should read time and date information within the time interval of $(Tpi/2)+T_{BUC}$

Periodic Interrupt And Update Ended Interrupt Relationship



Notes:

t_{PI} = time interval for periodic interrupt according to Table 3
t_{UC} = update cycle time = 1984µs
t_{BUC} = delay before update cycle = 244µs

Registers

The Real Time Clock module has six control registers which are accessible at all times, even during update cycles.

1. Register A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV_2	DV_1	DV_0	RS_3	RS_2	RS_1	RS_0

(1) UIP:
The Update-In-Progress (UIP) bit is a status flag that can be monitored by the processor. When the UIP bit reads logic 1, a single update transfer will occur. When the UIP reads 0, the update transfer will not occur for at least 244 µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read only and is not affected by a reset. Setting the SET bit in register B to one aborts any update transfer and clears the UIP status bit.

(2) DV_0, DV_1, DV_2:
These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn on the oscillator and allow the RTC to keep time. A pattern of 11X enables the oscillator but holds the count down chain in reset. The oscillator becomes active after t_{RC}, when the DV bits are changed from 000. If the timing chain is held in reset with the oscillator running by writing a pattern of 11X, the first update transfer occurs 500 ms after writing a pattern of 010 to bits DV_0, DV_1, and DV_2 respectively.

Oscillator control bits

DV2	DV1	DV0	Effect on Divider
0	0	0	Oscillator off
1	1	X	Reset divider chain. Oscillator enabled.
0	1	0	Normal operation. Oscillator on

(3) RS_3, RS_2, RS_1,RS_0:
These four bits are used to select 1 of 13 frequencies on the 15 stage divider and to disable the divider output pin signal. See table below. The selected frequencies may be used to generate an output square wave (on the SQW pin) and/or a periodic interrupt. The user may do one of the following:

1 : Enable the interrupt with the PIE bit="1", SQWE bit="0"
2 : Enable the SQW output pin with the SQWE bit="1", PIE bit ="0"
3 : Enable both PIE and SQWE bit with the PIE=SQWE="1"
4 : Not use both PIE and SQWE bit with the PIE=SQWE="0"

Periodic Interrupt Rate And Square Wave Output Frequency

Register A Select Bits				Periodic	SQW Output
RS_3	RS2	RS_1	RS_0	Interrupt Rate	Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.282 µs	2.048 kHz
0	1	1	0	976.5625 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125.0 ms	8 Hz
1	1	1	0	250.0 ms	4 Hz
1	1	1	1	500.0 ms	2 Hz

2. Register B:

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/$\overline{12}$	DSE

(1) SET (Set: Read / Write)

When the SET bit is logic zero, the update transfer functions normally by advancing the real time clock value once each second. When the SET bit is logic one, all update transfers are suspended and the program may initialize the time and calendar bytes without an update occurring during the initialization.

For initialization of the RTC module, first set the SET bit to 1, then carry out the initialization. The UIP bit is held low and the UIE bit is reset. Data read from the time and calendar bytes will be static as long as the SET bit is one. The SET bit is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the RTC module. When the SET bit is cleared to zero the clock will begin keeping the time again. This bit has no effect on the square wave output nor the periodic interrupt.

(2) PIE (Periodic Interrupt Enable: Read / Write)

The Periodic Interrupt Enable (PIE) bit is a read/write bit which allows the Periodic interrupt Flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at the periodic interrupt rate specified by the RS_3 through RS_0 bits of Register A. A 0 in the PIE bit inhibits the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt. PF is always set at the periodic interrupt rate regardless of the state of the PIE bit. The PIE bit is not modified by any internal RTC module functions but is cleared by the hardware RESET signal.

(3) AIE (Alarm Interrupt Enable: Read / Write)

The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to one, permits the Alarm Flag (AF) bit in Register C to assert the IRQ signal. An alarm interrupt occurs for each second that the three alarm bytes (including the don't care alarm codes) equal the three time bytes. When the AIE bit is set to zero, the AF bit does not assert the IRQ signal. The AIE bit is not modified by any internal RTC module functions but is cleared by the hardware $\overline{\text{RESET}}$ signal.

(4) UIE (Update Ended Interrupt Enable: Read / Write)

The Update ended Interrupt Enable (UIE) bit is a read/write bit, which when set to one, enables the Update end Flag (UF) in Register C to assert the $\overline{\text{IRQ}}$ pin low. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

(5) SQWE (Square Wave Enable: Read / Write)

When the Square Wave Enable (SQWE) bit is set to one, a square wave signal at the rate selected by the rate selection bits is output to the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. The SQWE bit is cleared by the RESET pin. The SQWE bit is a read/write bit.

(6) DM (Data Mode: Read / Write)

The Date Mode (DM) bit indicates whether the time, calendar and extended alarm information is in binary or BCD format. The DM bit is set by only the program to the appropriate format and can be read as required. This bit is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the RTC module. Setting the DM bit to one selects the binary date format while setting it to 0 selects the BCD format.

(7) 24/$\overline{12}$ (24/$\overline{12}$ Control: Read / Write)

The 24/$\overline{12}$ control bit selects the format of the hours byte and also the hours byte of the extended alarm register. A logic one selects the 24 hour mode and a logic 0 selects the 12 hour mode. This bit is a read/write bit which is not affected by $\overline{\text{RESET}}$ or internal functions of the RTC module.

(8) DSE (Daylight Saving Enable: Read / Write)

The Daylight Saving Enable (DSE) bit is a read/write bit which enables two special updates when the DSE bit is set to 1. On the first Sunday in April, the time increments from 1:59:59 am to 3:00:00 am. On the last Sunday in October when the time first reaches 1:59:59 am, it changes to 1:00:00 am. These special updates do not occur when the DSE bit is 0. This bit is a read/write bit which is not modified by $\overline{\text{RESET}}$ or internal functions of the RTC module.

3. Register C

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

(1) IRQF (Interrupt Request Flag: Read only)

The Interrupt Request Flag (IRQF) bit is set to one when 1 or more of the following conditions holds:

PF = PIE = 1
AF = AIE = 1 → IRQF=1
UF = UIE = 1

That is, IRQF = PF•PIE + AF•AIE + UF•UIE
The IRQF bit is cleared by a hardware RESET. All flag bits and IRQF bit are cleared to 0 after reading Register C.

(2) PF (Periodic Interrupt Flag: Read Only)

The Periodic interrupt Flag (PF) is a read only bit which is set to one when an edge occurs on the selected tap of the dividers. The RS_3 through RS_0 bits establish the periodic divide rate. The PF bit is set to one independent of the state of the PIE bit. When both the PF and PIE bits are set to 1, the $\overline{\text{IRQ}}$ signal is asserted and the IRQF bit is set to 1. The PF bit is cleared by a hardware $\overline{\text{RESET}}$ or by a read of Register C.

(3) AF (Alarm Interrupt Flag: Read Only)

The Alarm interrupt Flag (AF) is set when the current time matches the alarm register time. If the AIE bit is also set to 1, the $\overline{\text{IRQ}}$ pin is driven low and the IRQF bit is set to 1. The AF bit is cleared by a hardware RESET or by a read of Register C.

(4) UF (Update Ended Interrupt Flag: Read Only)

The Update ended interrupt Flag (UF) is set after each update cycle. If the UIE bit is also set to 1, the $\overline{\text{IRQ}}$ pin is driven low and the IRQF bit is set to 1. The UF bit is cleared by a hardware $\overline{\text{RESET}}$ or by a read of Register C.

(5) Bits 3 through 0 (Read Only)

The remaining bits in Register C are read only and will always read as 0.

4. Register D

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

(1) VRT (Valid RAM and Time: Read Only)

The VRT bit provides a check function to determine if the back-up power supply was maintained. After a return from battery backup mode, the first value read reflects the state of the V_{BAT} voltage during the back-up interval. When this first value read is 1, the back-up has functioned correctly, and the RAM contents are guaranteed. If this bit first reads as 0, the back-up power was not maintained throughout the back-up period, and therefore the contents of memory in the device are not guaranteed. It will be necessary to re-initialize. At power up when V_{DD} pin voltage is between 0 to V_{SWITCH}, the module will be powered from the battery. When the V_{DD} voltage exceeds V_{SWITCH}, the module is switched from backup power to V_{DD} power. At the same time, an artificial load of 1 μA (TYP.) is switched to the backup power.

The artificial load remains applied until the V_{DD} voltage reaches V_{ENABLE} voltage. At this time the backup power voltage is compared with a V_{CHECK} reference value. The voltage comparator output is clocked into the VRT bit latch. The artificial load is removed after the comparator output state has been latched. This bit is not affected by the $\overline{RESET}$ pin.

This bit will always read as "0"on the first read after a battery is installed and V_{DD} is supplied. All subsequent reads will indicate the state of the battery on the most recent V_{DD} power on .

(2) Bits 6 through 0 (Read Only)

The remaining bits in Register D are read only and will always read as 0.

5. Register 6 in Extended Alarm locations (For RTC-6591/6593/6597 only)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	XAIE

(1) XAIE (Extended Alarm Interrupt Enable: Read / Write)

The Extended Alarm Interrupt Enable (XAIE) bit is a read/write bit, which when set to 1, permits the Extended Alarm Flag (XAF) bit in same Register to assert the XIRQ signal. An extended alarm interrupt occurs for each second that the six extended alarm bytes (including the don't care alarm codes) equal the six time and calendar bytes. When the XAIE bit is set to 0, the XAF bit does not assert the XIRQ signal. The XAIE bit is not modified by any internal RTC module functions or hardware RESET signal.

(2) Bits 7 through 1 (Read Only)

The remaining bits in extended alarm register 6 are read only and will always read as 0.

6. Register 7 in Extended Alarm locations (RTC-659X series only)

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	XAF

(1) XAF (Extended Alarm Interrupt Flag: Read only)

The Extended Alarm interrupt Flag (XAF) is set when the current time matches the extended alarm register time. If the XAIE bit is also set to logic one, the $\overline{\text{XIRQ}}$ pin is driven low . The XAF bit is cleared by a read of register C.

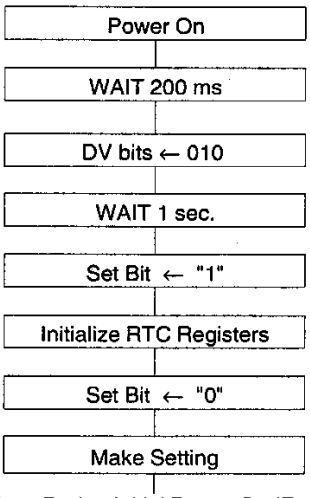
(2) Bits 7 through 1 (Read only)

The remaining bits in Extended alarm register 7 are read only and will always read as 0.

■ Operation Procedure

1. Initial Settings During Power On ($\overline{\text{RTC}}$ pin = "L")

(1) Settings During Initial Power On (For RTC-6581/6583/6587 only.)

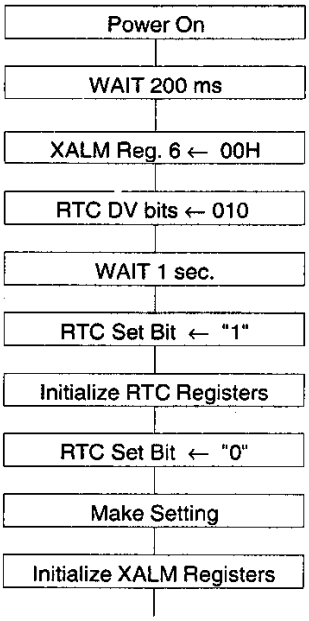


Chip enable delay by interval function of IC.

Oscillator on.

Allows oscillation to stabilize.

(2) Settings During Initial Power On (For RTC-6591/6593/6597 only.)

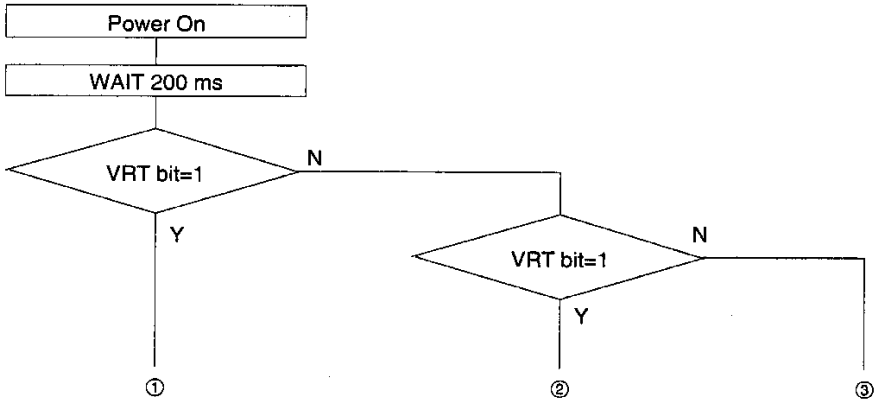


(Disable XIRQ) *1

*1 Since the XIRQ signal is indeterminate at initial power on, disable is necessary.

(3) Settings During Power On from Backup State

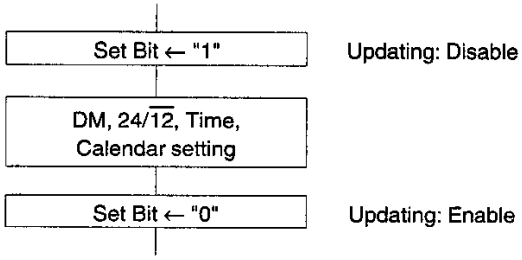
① The battery voltage is normal.
Data that was backed up is guaranteed.



② While in the backup state, the battery voltage dropped temporarily (because the battery was removed, for example). Data that was backed up is not guaranteed.

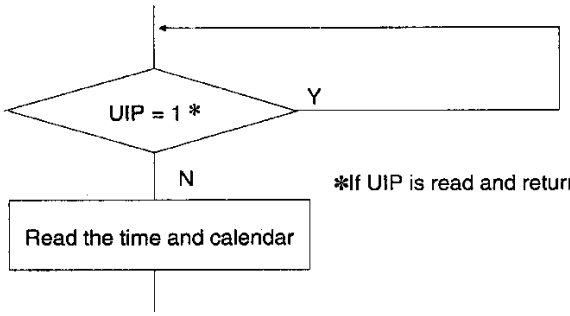
③ The battery voltage is low, please change the battery.
Data that was backed up is not guaranteed.

2. Setting and Correcting the Time and Calendar ($\overline{RTC}$ pin = "L")



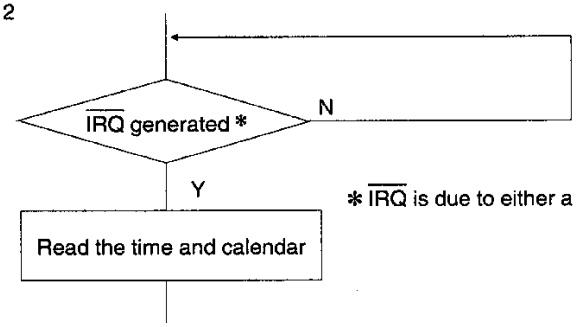
3. Reading the Time and Calendar ($\overline{RTC}$ pin = "L")

Method 1



*If UIP is read and returns "0", then no update will occur for at least 244µs.

Method 2



* $\overline{IRQ}$ is due to either a periodic interrupt or an update ended interrupt.

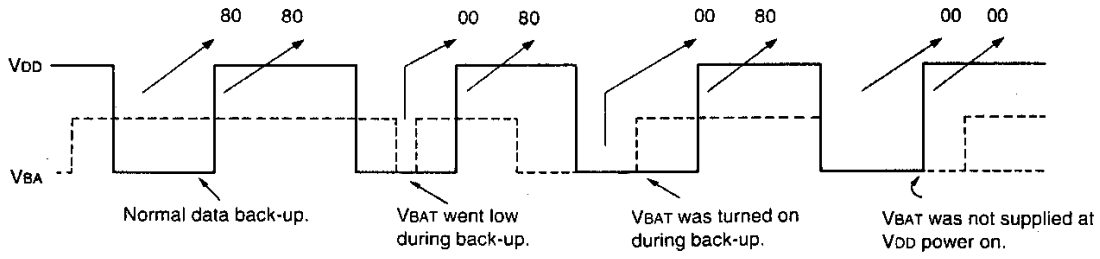
4. VRT bit

The VRT bit provides a check function to determine if the back-up power supply was maintained. (RTC register D)

After the V_{DD} power on, the first value read reflects the state of the V_{BAT} voltage during the back-up interval.

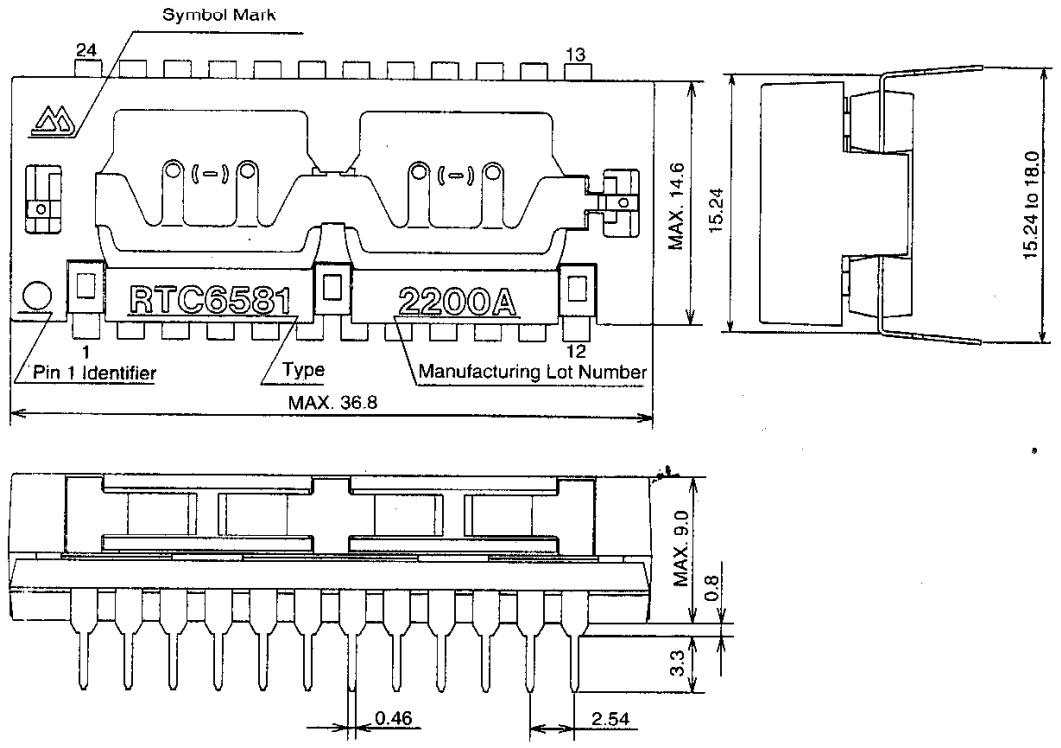
The second and subsequent values read reflect the V_{BAT} state at the time of V_{DD} power on. Only the first value read, therefore, can be used as a back-up check to determine the integrity of the chip data.

Value of register D.



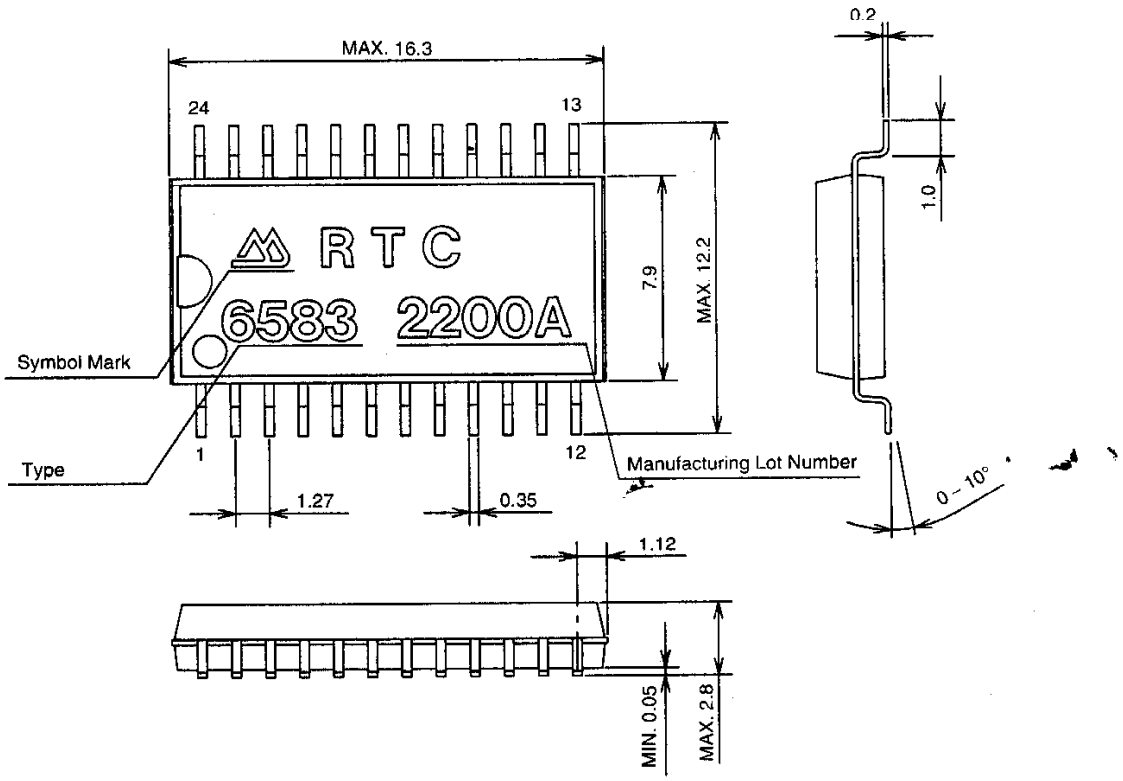
External Dimensions And Markings

RTC-6581/6591



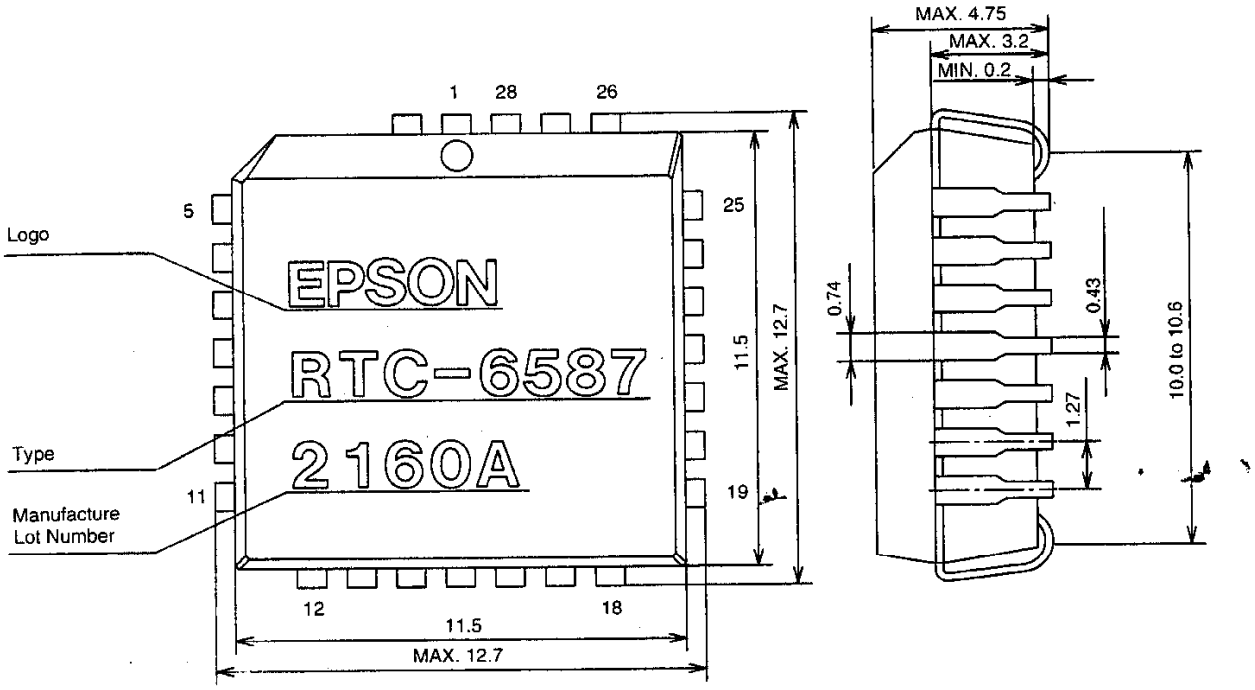
*The above diagram is merely a rough depiction of the contents and the positioning of the external markings; these diagrams are not intended as specifications for the size, shape or positioning of these markings.

RTC-6583/6593



*The above diagram is merely a rough depiction of the contents and the positioning of the external markings; these diagrams are not intended as specifications for the size, shape or positioning of these markings.

RTC-6587/6597



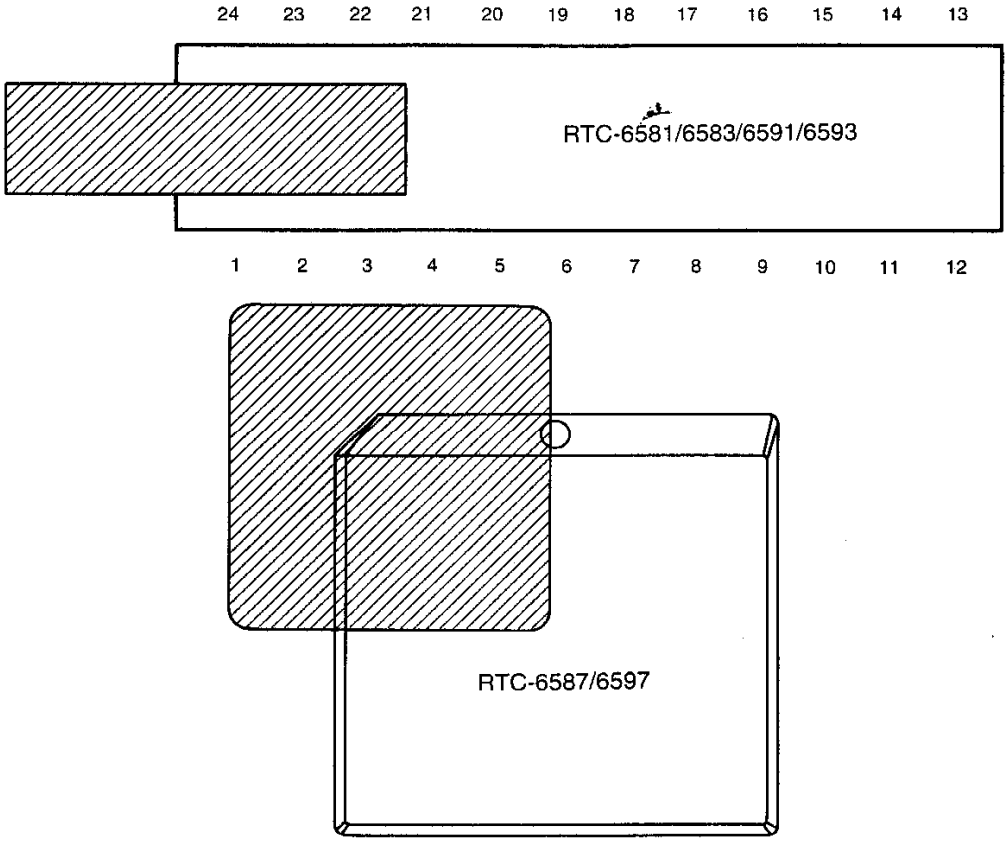
*The above diagram is merely a rough depiction of the contents and the positioning of the external markings; these diagrams are not intended as specifications for the size, shape or positioning of these markings.

Precautions Concerning Use

(1) Notes on the $\overline{\text{XALM}}$ function

① When not maintained by the back-up power supply, at initial power on the $\overline{\text{XIRQ}}$ state is indeterminate.
② XIRQ is not affected by $\overline{\text{RESET}}$ or other signals, nor by any of the $\overline{\text{RTC}}$ functions.
③ XIRQ goes active immediately the alarm conditions are met, even if in the back-up power state.
④ The extended alarm data mode must be set the same as the $\overline{\text{RTC}}$ data mode. (24/$\overline{12}$ hour setting, and BCD/binary data format)
⑤ The $\overline{\text{XALM}}$ pin has an internal pull-up resistor, so if $\overline{\text{XALM}}$ and $\overline{\text{XIRQ}}$ are left open-circuit, the extended alarm functions will be completely ignored.

(2) In order to achieve low power consumption in the oscillator section of the RTC-65 series, high impedance is used. Since the shaded portion of the diagram is highly inductive, do not put signal wires into close proximity of the shaded portion.



(3) Bypass capacitor:
In order to provide for stable operation (i.e., to prevent interruptions and noise), install a 0.01µF or more bypass capacitor close to the RTC.

(4) Although the device is resistant to impact up to the point of being dropped on a hard wooden board from 75cm, there is a chance that the resonator may be damaged during assembly by inserter equipment, etc., depending on the machine and other conditions. Therefore, please confirm that the equipment to be used is safe for this device before putting it into service.
In addition, be sure to reconfirm the safety of the equipment if any of the mounting conditions are changed at a later point in time.

(5) During ultrasonic cleaning, the crystal resonator may begin to resonate and be damaged. Since we are unable to specify the conditions (type of cleaning equipment, power, time, positioning within container, etc.) under which ultrasonic cleaning may be used, we do not guarantee this device under ultrasonic cleaning.

(6) Since this RTC utilizes a CMOS IC, the same handling precautions concerning static electricity that apply to typical CMOS ICs also apply to this device.

(7) Since a floating for the input pins may result in increased current consumption and damage to the device, be sure that the input pin voltage has a potential setting near that of V_{DD} and V_{SS}.

(8) Concerning input impedance: since the CMOS inputs that are used result in a high level of noise induction, either unused pins should be connected directly to V_{DD} or GND, or pull-up or pull-down resistance of several kilohms should be provided.
Pins indicated as NC have no internal connections. Inputting a signal to any of them has no effect.

(9) Condensation can cause errors, so the same precautions concerning condensation that apply to typical CMOS ICs should also be used with this device.

(10) Keep this device at room temperature and normal humidity when storing this device in a packaged state.

(11) (12) and belows are only for DIP type.

(12) Do not remove or modify the battery holder.

(13) Do not connect an external power supply, etc., to the battery contacts.

(14) Do not use old and new batteries together.

(15) Use the specified lithium batteries.

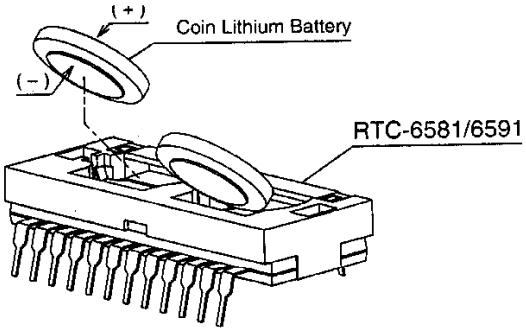
- BR1225 (Size: diameter - 12.5mm; Thickness - 2.5mm; Nominal voltage - 3.0V)

(16) Be sure to insert the batteries correctly in terms of polarity (+, –).

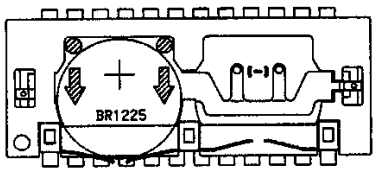
(17) If the batteries should leakage, wipe off the leakage and replace the new batteries.

(18) Battery insertion and removal:

Battery Insertion



Battery Removal

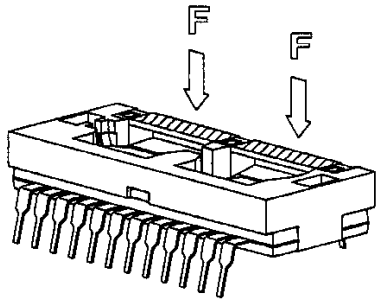


To remove battery, apply pressure at points marked ⊘ with a stick.

❶ The batteries have a tendency to pop out during removal. Place your finger over the top of the battery (the + side) during removal to prevent it from popping out.

❷ Position a stick (a diameter of 1 to 1.3 mm is best) against the side of the battery and press it in the direction indicated in the illustration.

(19) When installing batteries or installing the device in a socket on a board, do not apply force to the parts marked with an "F" in the diagram below if no batteries are installed in the holder. Pressing down on these parts can damage the battery holder.



(20) If the device is operated without batteries installed, the battery terminals will collect noise, making normal operation impossible. Always operate the device with batteries installed.

(21) Back-up power supply:
This device is designed to operate with a 3V lithium battery as the back-up power supply. If using a different back-up power supply, note that the device cannot be accessed if the condition below is met:

$$V_{DD} < V_{BAT} \times 1.3 \text{ (TYP.)}$$

Moreover, if V_{BAT} is always lower than V_{CHECK} (2.75 to 2.25V), the VRT bit is always set to 0. Using a back-up power supply of less than 2.75V is not recommended.

(22) This device has no built-in batteries; it is the responsibility of the user to observe any restrictions and cautions applying to use and disposal of lithium batteries. In particular, end-user documentation should include appropriate indications on battery use, including instructions on disposal.