I²C-Bus interface Real-Time-Clock module.

# RTC-8563

**Preliminary**

- Built in 32.768KHz quartz crystal.
- I²C-Bus Interface Compatible.( fscl=400KHz )
- Alarm and Timer functions are Available.
- Available 32.768KHz frequency output immediately at initial power-on.
- Century-Bit is available to 2000years countermeasures.
- Wide operating voltage range : 1.8V to 5.5V
- Wide data hold voltage range : 1.0V to 5.5V
- Low backup current : 0.3μA/3.0V ( TYP. )
- Small package ( SA : SOP-14pin )
- Low profile package ( JE : VSOJ-20pin )

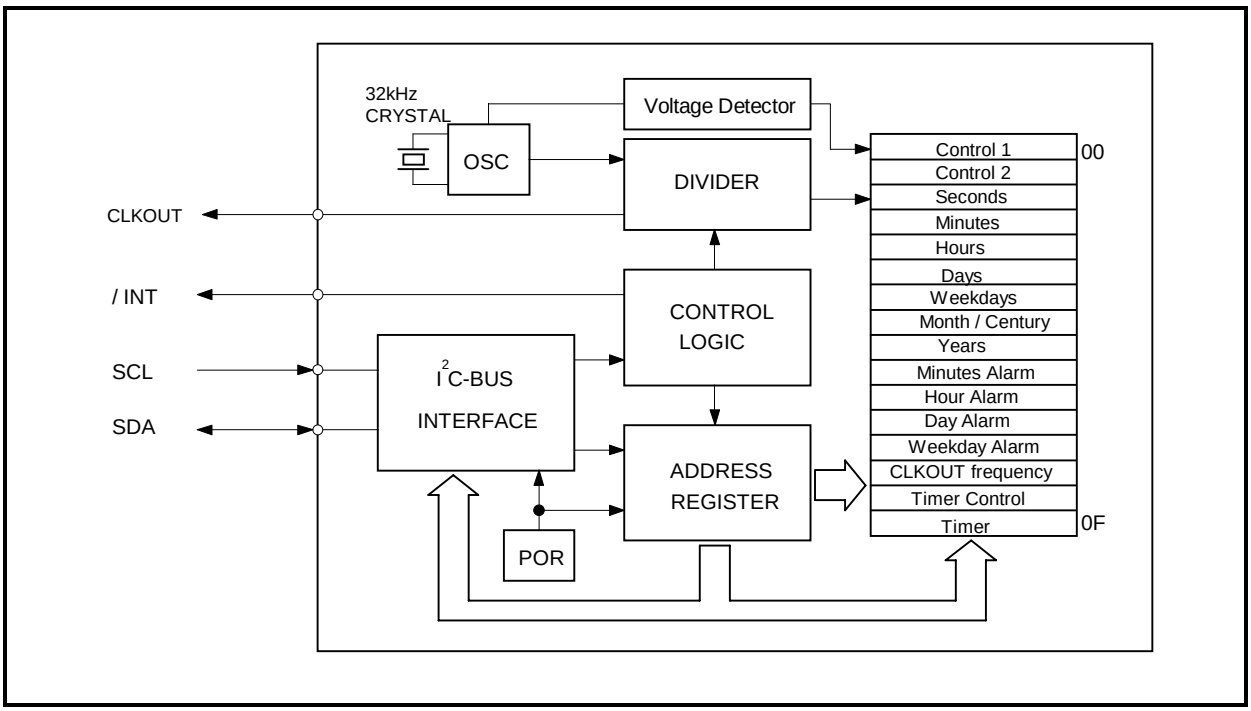


## ■ GENERAL

The RTC8563 is a CMOS real-time clock/calendar optimized for low power consumption.
A programmable clock output, interrupt output and voltage low detector are also provided.
All address and data are transferred serially via a two-line bi-directional I ² C bus.
Maximum bus speed is400kbit/sec.
The built-in word address register is incremented automatically after each written or read databyte.

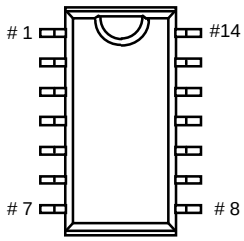
APPLICATIONS
Mobile telephones
Portable instruments
Fax machines
Battery powered products

## ■ Block Diagram



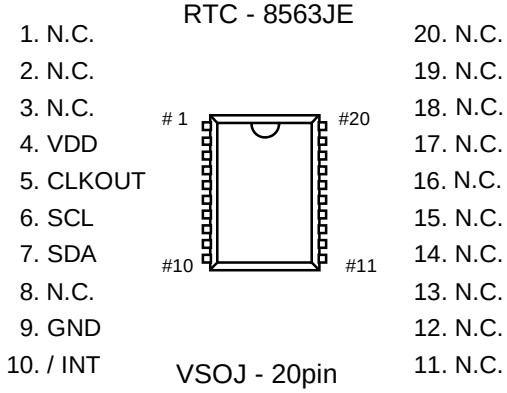
■ Terminal descriptions

RTC - 8563SA




SOP - 14pin

RTC - 8563JE




VSOJ - 20pin

| Signal name | Pin No. SOP(VSOJ) | I / O | DESCRIPTION |
|---|---|---|---|
| SCL | 2 ( 6 ) | IN | Serial clock input. |
| SDA | 3 ( 7 ) | I/O | Serial data I/O. Bi-directional pin. |
| GND | 5 ( 9 ) | - | Ground. |
| / INT | 7 (10) | OUT | Open drain interrupt output (active LOW). |
| VDD | 11 ( 4 ) | - | Positive supply. |
| CLKOUT | 14 ( 5 ) | OUT | Open drain clock output.<br>If disabled it becomes logic 0 ( Low level ). |
| N.C. | 1,4,6,8-10, 12,13 (1-3,8,11-20) | - | Don't connect. |

*A bypass capacitor of 0.01$\mu$F or greater must be connected between VDD and GND.

## ■ Characteristics

### 1.Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ - GND | -0.5 | +6.5 | V |
| Supply current | $I_{DD}$ | $V_{DD}$ | -50 | 50 | mA |
| Input voltage | $V_I$ | Input Pin | GND-0.5 | $V_{DD}$+0.5 | V |
| Output voltage | $V_O$ | CLKOUT, /INT | GND-0.5 | $V_{DD}$+0.5 | V |
| DC input current | $I_I$ | | -10 | 10 | mA |
| DC output current | $I_O$ | | -10 | 10 | mA |
| Storage temperature | $T_{STG}$ | as a discrete component. | -55 | +125 | °C |

### 2.Operating Conditions

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Supply voltage(note1) | $V_{DD}$ | 400KHz $I^2C$ -BUS activity | 1.8 | 5.5 | V |
| clock data integrity | $V_{DD}$ | 25°C | $V_{LOW}$ | 5.5 | V |
| Operating temperature | $T_{OPR}$ | | -40 | +85 | °C |

### 3.Frequency characteristics

| Parameter | Symbol | Conditions | MAX. | Unit |
|---|---|---|---|---|
| Clock tolerance | $\Delta f/fo$ | Ta=+25°C, $V_{DD}$=3.0V | 5 ± 23 | ppm |
| Temperature characteristics | top | Ta=+25°C, -10 to +70°C, $V_{DD}$=3.0V | +10<br>-120 | ppm |
| Voltage characteristics | f/V | Ta=+25°C,$V_{DD}$=1.0 to 5.5V, | ± 2 | ppm/V |
| Startup time | $t_{STA}$ | Ta=+25°C,$V_{DD}$=1.8V | 3 | sec |
| Aging | fa | Ta=+25°C,$V_{DD}$=3.0V | ± 5 | ppm/y |

### 4. DC characteristics

$V_{DD}$=1.8 to 5.5V , Ta=-40 to +85°C

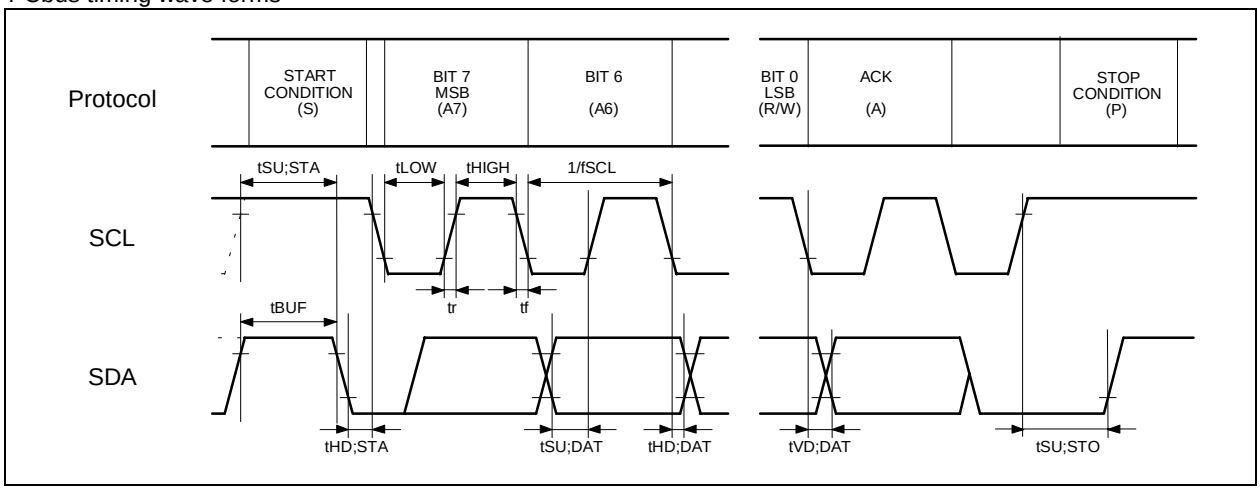
| Parameter | Pin | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply current<br>( BUS activity ) | | $I_{DDO}$ | $f_{SCL}$=400KHz<br>$f_{SCL}$=100KHz | | | 800<br>200 | μA<br>μA |
| Supply current<br>( BUS inactivity )<br>( CLKOUT=0Hz ) | | $I_{DD}$ | $f_{SCL}$=0Hz, $V_{DD}$=5.0V<br>$f_{SCL}$=0Hz, $V_{DD}$=3.0V<br>$f_{SCL}$=0Hz, $V_{DD}$=2.0V | | 0.35<br>0.30<br>0.25 | 0.75<br>0.65<br>0.60 | μA<br>μA<br>μA |
| Supply current<br>( CLKOUT=32KHz ) | | $I_{DD32K}$ | $f_{SCL}$=0Hz, $V_{DD}$=5.0V<br>$f_{SCL}$=0Hz, $V_{DD}$=3.0V<br>$f_{SCL}$=0Hz, $V_{DD}$=2.0V | | 0.85<br>0.55<br>0.45 | 1.70<br>1.10<br>0.90 | μA<br>μA<br>μA |
| LOW input voltage | | $V_{IL}$ | | GND | | 0.3 x $V_{DD}$ | V |
| HIGH input voltage | | $V_{IH}$ | | 0.7 x $V_{DD}$ | | $V_{DD}$ | V |
| LOW output current | SDA | $I_{OL(SDA)}$ | $V_{OL}$=0.4V, $V_{DD}$=5V | -3 | | | mA |
| LOW output current | / INT | $I_{OL(/INT)}$ | $V_{OL}$=0.4V, $V_{DD}$=5V | -1 | | | mA |
| LOW output current | CLKOUT | $I_{OL}$ (CLKOUT) | $V_{OL}$=0.4V, $V_{DD}$=5V | -1 | | | mA |
| output leakage | | $I_{LO}$ | $V_O$=$V_{DD}$ or GND | -1 | | 1 | μA |
| Low voltage detection | | $V_{LOW}$ | | | 1.0 | 1.2 | V |

5. AC Characteristics

VDD=1.8 to 5.5V , Ta=-40 to 85°C

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | | | | 400 | KHz |
| tolerable spike width on bus | $t_{SW}$ | | | | 50 | ns |
| set-up time for a repeated START condition | $t_{SU, STA}$ | | 0.6 | | | μs |
| START condition hold time | $t_{HD, STA}$ | | 0.6 | | | μs |
| SCL LOW time | $t_{LOW}$ | | 1.3 | | | μs |
| SCL HIGH time | $t_{HIGH}$ | | 0.6 | | | μs |
| SCL,SDA rise time | tr | | | | 0.3 | μs |
| SCL,SDA fall time | tf | | | | 0.3 | μs |
| data set-up time | $t_{SU;DAT}$ | | 100 | | | ns |
| data hold time | $t_{HD;DAT}$ | | 0 | | | ns |
| set-up time for STOP condition | $t_{SU;STO}$ | | 4.0 | | | μs |

$I^2C$bus timing wave forms



## ■ Registers

### 1. Registers Table

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Control 1 | TEST | 0 | STOP | 0 | TEST | 0 | 0 | 0 |
| 01 | Control 2 | 0 | 0 | 0 | TI / TP | AF | TF | AIE | TIE |
| 02 | Seconds | VL | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 03 | Minutes | x | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 04 | Hours | x | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 05 | Days | x | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 06 | Weekdays | x | x | x | x | x | 4 | 2 | 1 |
| 07 | Months / Century | C | x | x | 1 | 8 | 4 | 2 | 1 |
| 08 | Years | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 09 | Minute Alarm | AE | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 0A | Hour Alarm | AE | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 0B | Day Alarm | AE | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 0C | Weekday Alarm | AE | x | x | x | x | 4 | 2 | 1 |
| 0D | CLKOUT frequency | FE | x | x | x | x | x | FD1 | FD0 |
| 0E | Timer control | TE | x | x | x | x | x | TD1 | TD0 |
| 0F | Timer | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

### 2. Notes

① Bit positions labeled as ‘x’ are not implemented. This bit are write impossibility and Readout value isn't fixed.
② Therefore,need to mask it with software when began to read it.
③ As for data 0 of register 0 and 1, a write is possible, but 0 thing use it.
④ Count data of address more than 02 to 05, 08 to 0B is BCD type approval entirely.
⑤ This device can't renew data on a day justly when sets the time and date data which isn't existed in.
⑥ There is a bit setting up test mode in register 0. Test mode is a special mode for device check. Don't set test bit in 1 absolutely. Test mode may let all data change. Operate register 0 carefully.

### 3. Functions

#### 3-1.CONTROL/STATUS 1

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00 | Control 1 | TEST | 0 | STOP | 0 | TEST | 0 | 0 | 0 |

TEST : These bits are presented for use test. Test mode is a special mode for device check.
Don't set these bits in 1 absolutely. Test mode may let all data change.

STOP : If this bit is "0", a clock works. When I set it in 1.While this bit sets it in 1, all frequency divider for less than 1 second of clockwise rotation road becomes 0 clearing state. Reset this bit in "0" at time tone and same time when adjust time of day precisely until less than 1 second. Frequency output from CLKOUT terminal may not stop by a limit, logical state of this bit when selects 32.768KHz.

#### 3-2.CONTROL/STATUS 2

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01 | Control 2 | 0 | 0 | 0 | TI / TP | AF | TF | AIE | TIE |

AF, TF: Alarm Flag, Timer Flag
When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software.
If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits.
To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.
Write ‘1’ to AF or TF: No change to flag
Write ‘0’ to AF or TF: Respective flag is cleared

AIE,TIE: Alarm Interrupt Enable, Timer Interrupt Enable.
These bits activate or deactivate the generation ofan interrupt when AF or TF is asserted , respectively.
The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

TI/TP: Timer Interrupt/ Timer Periodic INT mode.
TI/TP = 0: INT is active when TF is active. (subject to the status of TIE).
TI/TP = 1:INT pulses active according to the below table. (subject to the status of TIE).

INT OPERATION (TI/TP=1)

| | /INT PERIOD | |
|---|---|---|
| SOURCE CLOCK | n>1 | n=1 |
| 4096Hz | 1/4096 seconds | 1/8192 seconds |
| 64Hz | 1/64 seconds | 1/128 seconds |
| 1Hz | 1/64 seconds | 1/64 seconds |
| 1/60Hz | 1/64 seconds | 1/64 seconds |

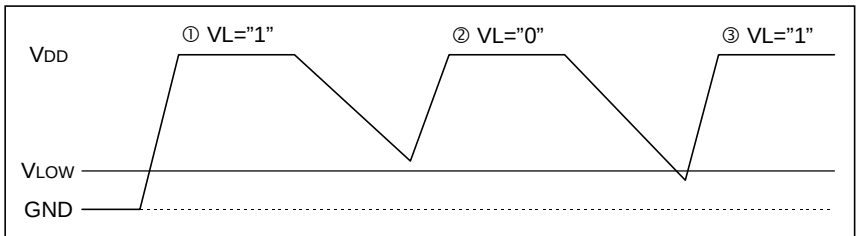
**Note**
1. n = Loaded countdown value. Timer stopped when n=0.
2. TF and INT become active simultaneously.

## 3-3.CLOCK and CALENDAR REGISTERS.

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 02 | Seconds | VL | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 03 | Minutes | x | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 04 | Hours | x | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 05 | Days | x | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 06 | Weekdays | x | x | x | x | x | 4 | 2 | 1 |
| 07 | Months / Century | C | x | x | 1 | 8 | 4 | 2 | 1 |
| 08 | Years | 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 |

These registers contain the respective time and date values coded in BCD format.
Example: seconds register contains ‘x1011001’ = 59 seconds. The PCF8563A stores the time of day in 24-hour format.

VL: Bit 7 of the seconds register is used to detect lowering of power supply voltage.
This bit is set 1 when initial power on occurred. But it means that there was degradation of power supply voltage during back up when device returned from back up state if this bit was 1. In this case, initialize of all data is necessary.This bit can't clear it besides software.




①:Because initial power on occurred, VL is 1.
②:Because the voltage doesn't fall to VLOW voltage, VL keeps "0".
③:VL is with "1" so that power supply is less than VLOW voltage.
Refer DC characteristics table.

C:This bit is a bit showing century updating.
When data of year renewed it from 99 to 00, this bit is set.
This bit is set in 1 when set up this bit in 0 during the 20th century when it became it in 2000.
2001year is the right opening year of 21st century but.

**WEEKDAYS**

The weekday register has a bit assignment as shown in the table below. Only the 3 LSBs are utilized.

| DAY | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|
| Sunday | X | X | X | X | X | 0 | 0 | 0 |
| Monday | X | X | X | X | X | 0 | 0 | 1 |
| Tuesday | X | X | X | X | X | 0 | 1 | 0 |
| Wednesday | X | X | X | X | X | 0 | 1 | 1 |
| Thursday | X | X | X | X | X | 1 | 0 | 0 |
| Friday | X | X | X | X | X | 1 | 0 | 1 |
| Saturday | X | X | X | X | X | 1 | 1 | 0 |

**MONTHS / CENTURY.**

The months/century register utilizes the 5 LSBs to encode the month of the year as shown in the table below. Bit 7 of the months/century register also contains the century indicator. When C=0, the century is 20xx, when C=1 the century is 19xx. This bit is toggled when the years register overflows from 99 to 00.

| MONTH | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|
| January | C | x | x | 0 | 0 | 0 | 0 | 1 |
| February | C | x | x | 0 | 0 | 0 | 1 | 0 |
| March | C | x | x | 0 | 0 | 0 | 1 | 1 |
| April | C | x | x | 0 | 0 | 1 | 0 | 0 |
| May | C | x | x | 0 | 0 | 1 | 0 | 1 |
| June | C | x | x | 0 | 0 | 1 | 1 | 0 |
| July | C | x | x | 0 | 0 | 1 | 1 | 1 |
| August | C | x | x | 0 | 1 | 0 | 0 | 0 |
| September | C | x | x | 0 | 1 | 0 | 0 | 1 |
| October | C | x | x | 1 | 0 | 0 | 0 | 0 |
| November | C | x | x | 1 | 0 | 0 | 0 | 1 |
| December | C | x | x | 1 | 0 | 0 | 1 | 0 |

**YEARS.**

The years register encodes the two lower year digits in BCD format according to the table below. When the years register overflows from 99 to 00, the century bit C in the months/century register is toggled.

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| 8 | 4 | 2 | 1 | 8 | 4 | 2 | 1 |

**LEAP YEAR COMPENSATION.**

The PCF8563A compensates for leap years by adding a 29th day to February if the year counter contains a value which is divisible by 4, including the year 00.

## 3-4.ALARM REGISTER

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 09 | Minute Alarm | AE | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 0A | Hour Alarm | AE | 4 | 2 | 1 | 8 | 4 | 2 | 1 |
| 0B | Day Alarm | AE | x | 2 | 1 | 8 | 4 | 2 | 1 |
| 0C | Weekday Alarm | AE | x | x | x | x | 4 | 2 | 1 |

**MINUTE ALARM, HOUR ALARM, DAY ALARM,WEEKDAY ALARM.**
The registers at addresses 09h through 0Ch contain alarm information.
When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding 'Alarm Enable' (AE, bit 7) is '0', then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the 'Alarm Flag' (AF, bit 3 in control/status 2 register) is set. AF will remain set until cleared by software.
Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more.
Alarm registers which have their 'Alarm Enable' bit at '1' par will be ignored.
AE = 0:Compare Alarm register with current time.
AE = 1: Ignore Alarm register.

## 3-5.CLKOUT TIMER

### CLKOUT FREQUENCY

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0D | CLKOUT frequency | FE | x | x | x | x | x | FD1 | FD0 |

FE : Frequency output enable.
FE = 0 : The CLKOUT output is inhibited and CLKOUT output is set to logic0.
FE = 1 : The CLKOUT output is activated.

Frequency selector

| Output frequency | FD1 | FD0 |
|---|---|---|
| 32768Hz | 0 | 0 |
| 1024Hz | 0 | 1 |
| 32Hz | 1 | 0 |
| 1Hz | 1 | 1 |

### TIMER CONTROL

| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0E | Timer control | TE | x | x | x | x | x | TD1 | TD0 |

TE : Timer Enable bit.
TE = 0 : Timer is disabled.
TE = 1 : Timer is enabled (i.e. timer counts down)
TD1, TD0 : Timer source clock frequency select.
These bits determine the source clock for the countdown timer (address 0Fh).
When not in use, TD1 & TD0 should be set to 1/60Hz for power saving.

| SOURCE CLOCK FREQUENCY | TD1 | TD0 |
|---|---|---|
| 4096Hz | 0 | 0 |
| 64Hz | 0 | 1 |
| 1Hz | 1 | 0 |
| 1/60Hz | 1 | 1 |

TIMER

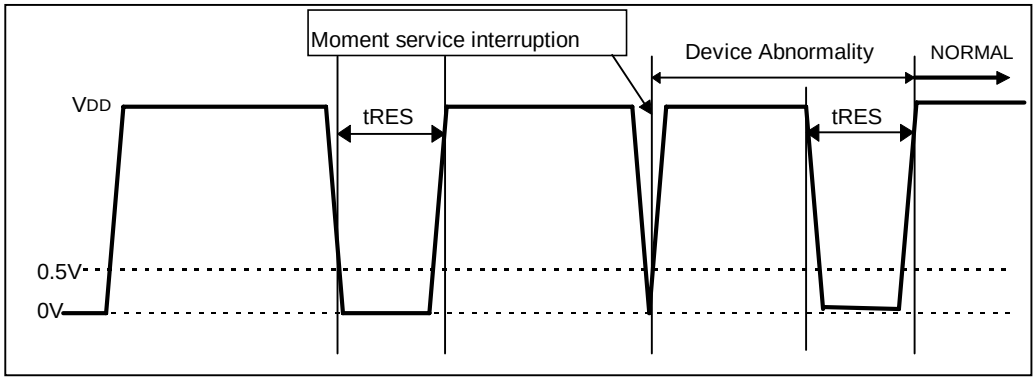
| Address | Function | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0F | Timer | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

The timer register is an 8-bit binary countdown timer.
It is enabled/disabled via the timer control register.
The source clock for the timer is also selected by the timer control register. Other timer properties such as single or periodic interrupt generation are controlled via the control/status 2 register (address 01h).
For accurate read back of the count down value, the $I^2C$ clock (SDA) must be operating at a frequency of at least twice the selected timer clock.

Countdown Period = n / Clock Frequency.

## ■ About cutoff and reclosing of power supply.

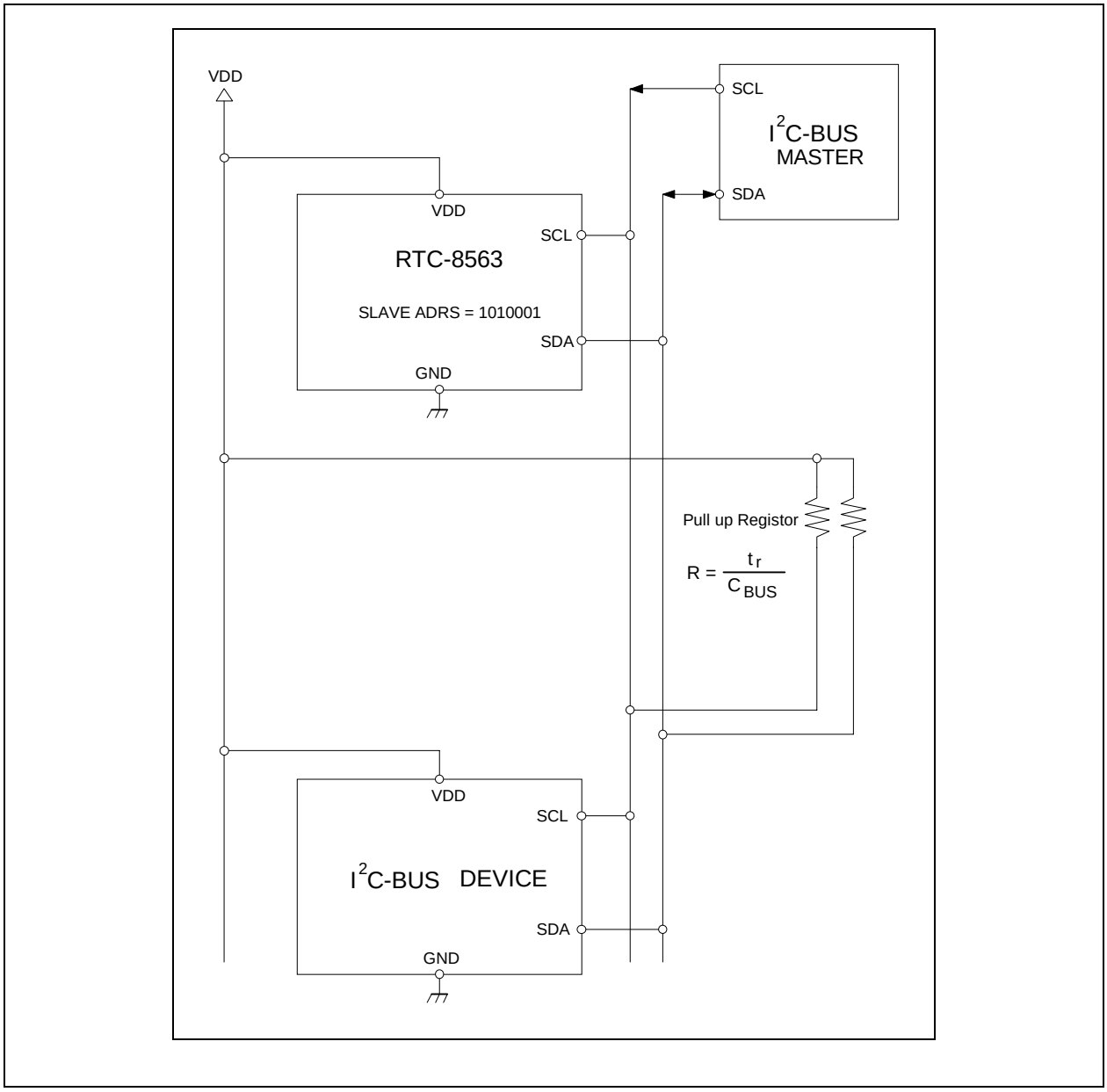
This device has power-on reset circuitry built-in.
Power-on reset isn't completed when doesn't do appropriate power activation.
Built-in quartz crystal is necessity for approximately 2 seconds till I start the vibration that powered on again, and became stable after oscillation stopped.
Therefore device inside goes initialize from power activation during 2 seconds.
When there is reclosing of power supply during this 2 seconds, power-on reset operation doesn't function in normal.
As concrete appearance, clock output of 32.768KHz stops, and access to device isn't completed, and it is thought.
As for power activation, there is the necessity that the following assumption is kept so that device resets it surely.
Time interval from power supply OFF to ON is necessary for more than 2 seconds.
tRES =2 sec (MIN)
Above power supply OFF is the state that VDD deteriorated than 0.5 V.
When device doesn't work in normal with incidence of moment service interruption, do reclosing of power supply.




If VDD voltage rises from 0 V, Device works in normal.

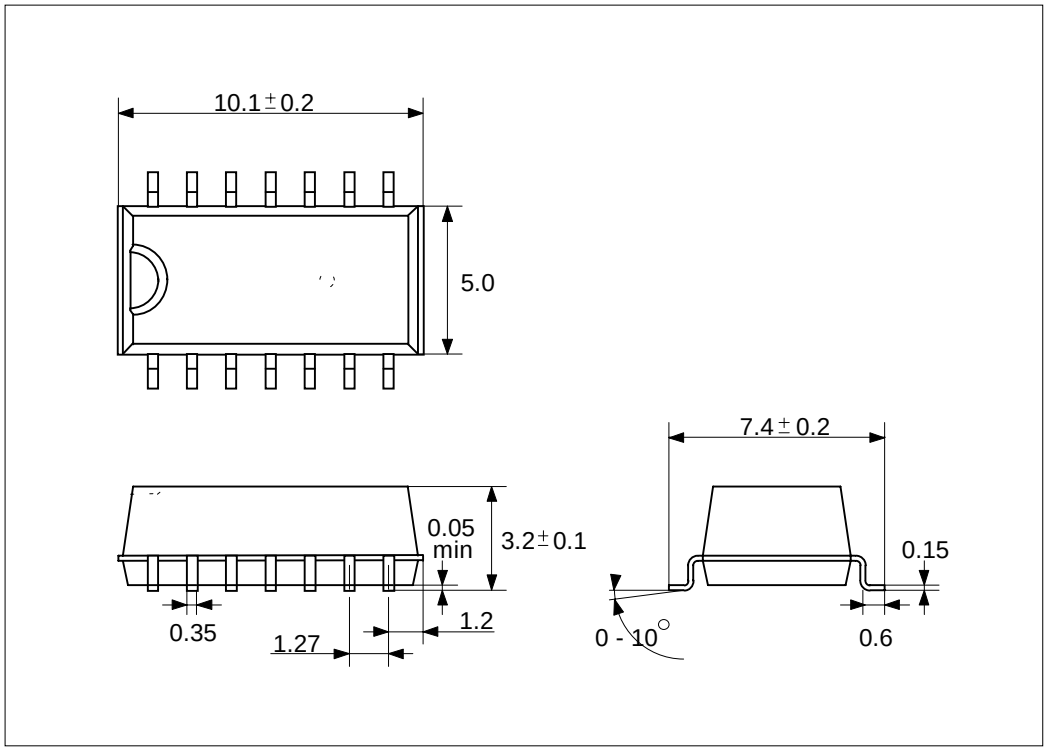
Device works in normal when returned to normal voltage from back up voltage.

■ Typical applications

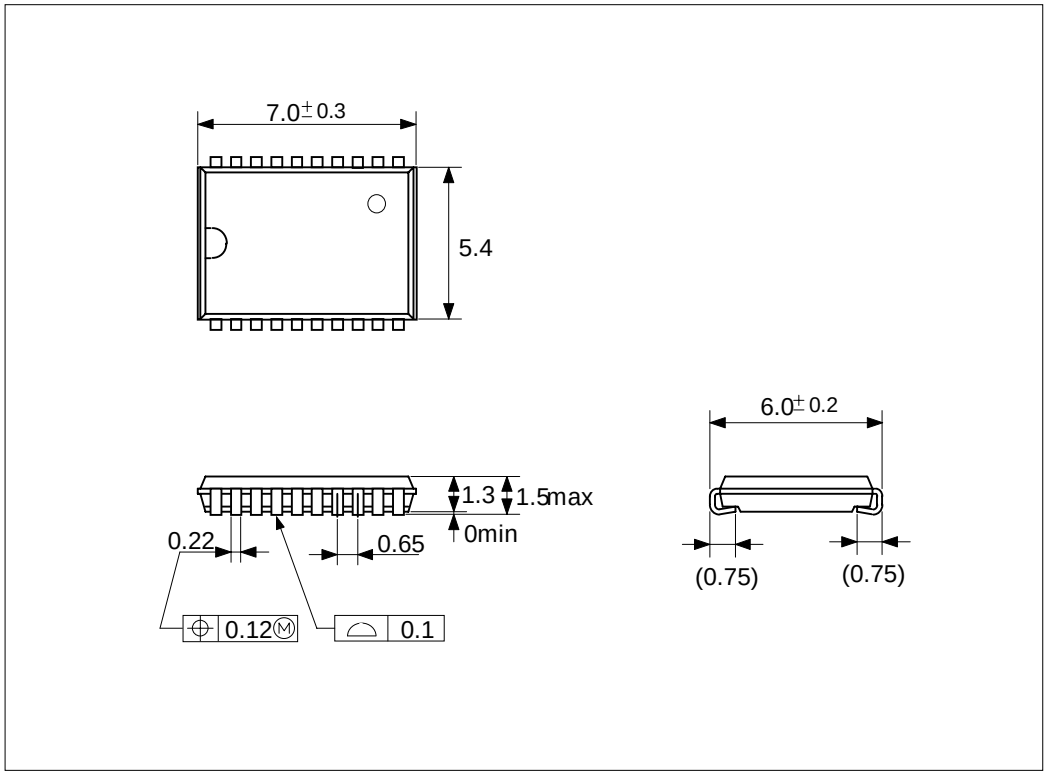


■ External dimension

● RTC-8563SA ( SOP 14-pin )

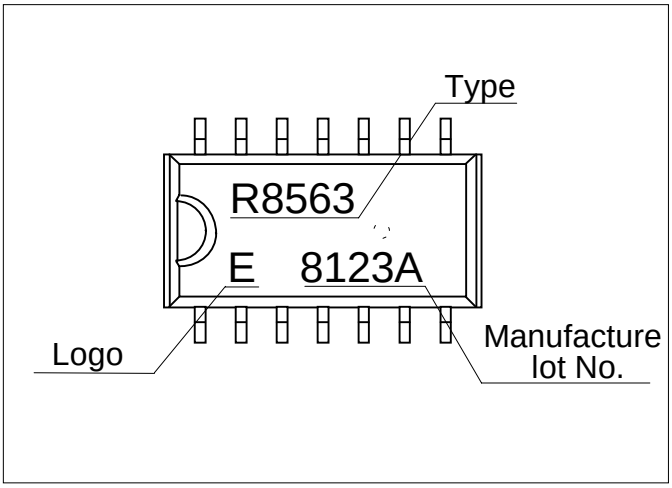



● RTC-8563JE ( VSOJ 20-pin )

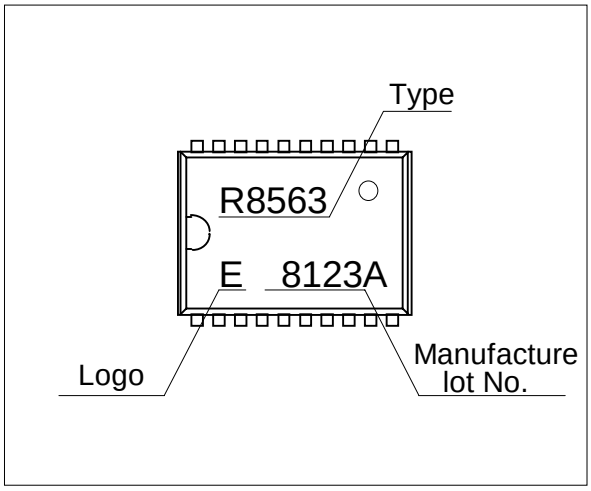


## ■ Marking layout

● RTC-8563SA ( SOP 14-pin )




● RTC-8563JE ( VSOJ 20-pin )




The indication above details the markings and outline their positions. But it does not specify the details of the type faces, sizes of characters and their positions.

## ■ Notes on Use

### ( 1 ) Notes on handling

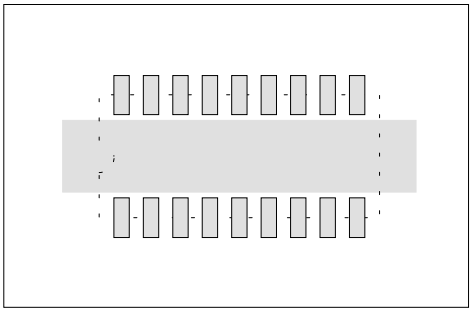
In order to attain low power consumption, this module incorporates a CMOS IC. Therefore, the following points should be kept in mind when using this module.

### 1. Static electricity

While this module does have built-in circuitry designed to protect it against damage from electrostatic discharge, the module could still be damaged by an extremely large electrostatic discharge. Therefore, packing materials and shipping containers should be made of conductive materials. Furthermore, use soldering equipment, test circuits, etc., that do not have high-voltage leakage, and ground such equipment when working with it.

### 2. Electronic noise

If excessive external noise is applied to the power supply and I/O pins, the module may operate incorrectly or may even be damaged as a result of the latch-up phenomenon. In order to assure stable operation, connect a pass through capacitor (ceramic is recommended) of at least 0.1$\mu$F located as closely as possible to the power supply pins on this module (between $V_{DD}$ and GND). Furthermore, do not place a device that generates high noise levels near this module. Keep signal lines away from the shaded areas shown in the figure at right, and fill the area with a GND pattern, if possible.



### 3. Electric potential of I/O pins

Because having the electric potential of the input pins at an intermediate level contributes to increased power consumption, reduced noise margin, and degradation of the device, keep the electric potential as close as possible to the electric potential of $V_{DD}$ or GND.

### 4. Treatment of unused input pins

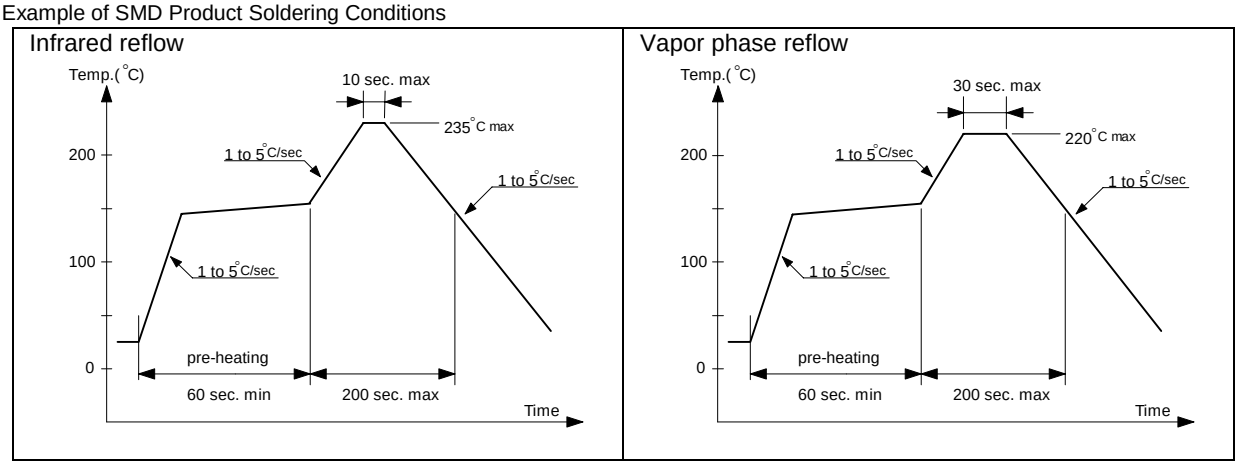
Because the input impedance of the input pins is extremely high and using the module with these pins open can result in unstable electric potential and miss operation due to noise, unused input pins must always be connected to a pull-up or pull-down resistor.

## ( 2 ) Notes on mounting

### 1. Soldering temperature conditions

If the internal temperature of the package exceeds 260°C, the characteristics of the crystal resonator may deteriorate and the package may be damaged. Therefore, before using this module, be sure to confirm what temperatures it will be exposed to during the mounting process. If the mounting temperature conditions are ever changed, the suitability of those temperature conditions for this package must be confirmed again.
Soldering conditions: Up to 260°C for up to 10 seconds, twice, or up to 230°C for up to 3 minutes.

Example of SMD Product Soldering Conditions




### 2. Mounters

While this module can be used with general-purpose mounters, be sure to confirm the force of impact that the module will be subjected to during mounting, since certain machines or conditions can result in damage to the internal crystal resonator. If the mounting conditions are ever changed, the suitability of those conditions for this package must be confirmed again.

### 3. Ultrasonic cleaning

Under certain conditions, ultrasonic cleaning can damage the crystal resonator. Because we cannot specify the conditions under which you perform ultrasonic cleaning (including the type of cleaner, the power level, the duration, the condition of the inside of the chamber, etc.), Seiko-Epson does not warrant this product against ultrasonic cleaning.

### 4. Mounting orientation

If this module is mounted backwards, it may be damaged. Always confirm the orientation of the module before mounting it.

### 5. Leakage between pins

If power is supplied to this module while it is dirty or while condensation is present, leakage between pins may result. Be sure that the module is clean and dry before supplying power to it.